HIGH PERFORMANCE FUEL CELL POWER GENERATION SYSTEM FOR STAND-ALONE APPLICATIONS

MARTIN ORDONEZ


CENTRE FOR NFLD. STUDIES
MEMORIAL UNIVERSITY
OF NEWFOUNDLAND

High Performance Fuel Cell Power Generation System for Stand-alone Applications

by

©Martin Ordonez, Ing., MEng.

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To Erika and Mom

Abstract

Fuel Cell (FC) power generation for stand-alone applications such as residential power supply, building power generation (for hospitals, office buildings, schools, and airports), and portable power supply have the potential to meet high energy standards comprising high conversion efficiency, low emissions, and quiet operation. The strong interaction between the load, power conditioning stage, and FC system makes the design and coordinated operation a remarkable challenge in stand-alone applications. In this thesis, a detailed description of a high-performance FC power conversion system is presented. Key aspects such as power extraction, efficiency, dynamic response, monitoring, and power quality are addressed as part of this work.

An advanced isolated dc-dc power converter topology and control scheme is proposed to address minimization of power losses and switching stress in the entire range of operation of the system. Architectural and control aspects (dynamic behavior) of the generation system are investigated at the system level with the objective of reducing the effect of low frequency ripple current in the FC. The concept of swinging bus is introduced and characterized to absorb the inverter ripple current. A novel control strategy based on curved switching surfaces is investigated to control the inverter stage, producing high quality output power while rejecting the fluctuations in the swinging bus. In addition, an innovative feature is incorporated to perform on-line monitoring and diagnosis of the FC stack. This critical component based on frequency response analysis is required to realize a fully functional system and has not been addressed in previous FC power conversion systems.

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List of Abbreviations

ADC	Analog to Digital Converters
ACOA	Atlantic Canada Opportunities Agency
AFC	Alkaline Fuel Cell
AIF	Atlantic Innovation Fund
AM	Amplitude Modulation
CF	Crest Factor
CFRA	Commercial Frequency Response Analyzer
CMC	Current Mode Control
DFT	Discrete Fourier Transform
DMFC	Direct Methanol Fuel Cell
DSP	Digital Signal Processor
EFRA	Embedded Frequency Response Analyzer
ESR	Equivalent Series Resistance
FB-M	Full-bridge Modified Topology

FB-ZVS	Full-bridge Zero Voltage Switching
FC	Fuel Cell
FCC	Federal Communications Commission
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
FRA	Frequency Response Analysis
IIR	Infinite Impulse Response
LIA	Lock-in Amplification
LPF	Low-pass Filter
MAF	Moving Averaging Filter
MCFC	Molten Carbonate Fuel Cell
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
NSERC	National Science and Engineering Research Council of Canada
OP	Operation Point
PAFC	Phosphoric Acid Fuel Cell
PCB	Printed Circuit Board
PEMFC	Proton Exchange Membrane Fuel Cell
PLECS	Piece-wise Linear Electrical Circuit Simulation
RCD	Resistor Capacitor Diode

SNR	Signal-to-Noise Ratio
SOFC	Solid Oxide Fuel Cell
SS	Switching Surfaces
THD	Total Harmonic Distortion
UTN	National Tecnological University
ZVS	Zero Voltage Switching
ZVT	Zero Voltage Transition

List of Symbols

a	Semiminor axis
A_1	Control loop compensator
A_c	Effective cross section of the core
b	Semimajor axis
B_{ac}	Alternating current flux density
β	Control loop feedback
°C	Degrees Celsius
C	Capacitance
C_{bus}	Bus capacitance
C_d	Double layer capacitor
C_{oss}	MOSFET output capacitance
C_{out}	Output capacitor bank
C_w	Interwinding capacitance
ΔV_{Act}	Voltage drop due to the activation of the anode and cathode

ΔV_{Ohmic}	Voltage drop due to the electrodes and membrane resistance
ΔV_{Trans}	Voltage drop due to decrease in the concentrations of the reactants
di/dt	Current rate of change
dv/dt	Voltage rate of change
D_x	Diode
E	Nerds voltage
E_o	Standard reference potential
f	Frequency
F_E	Non-linear potential
f_L	Inverter output frequency
F_{Ln}	Normalized inverter output frequency
f_{max}	Maximum frequency
f_{min}	Minimum frequency
F_o	Natural frequency
F_S	Sampling frequency
F_{sw}	Switching frequency
F_{swn}	Normalized switching frequency
$i(t)$	Lock-in amplifier input signal
I_X	In-phase component of the measured current

I_Y	In-quadrature component of the measured current
i_{cap}	Bus capacitor current
i_{Cn}	Normalized filter capactior current
i_{Crn}	Normalized filter capacitor reference current
I_{dc}	Direct current
i_{Dx}	Diode current
I_F	Diode forward current
i_{fc}	Fuel cell output current
i_L	Filter inductor current
i'_L	Filter inductor current reflected to the primary
i_{Ln}	Normalized inductor current
i_{mos}	MOSFET current
i_{Mx}	MOSFET drain to source current
i_o	Output current
i_p	Transformer primary current
i_{Qx}	MOSFETs N-channel current
i_s	Transformer secondary current
J	Current density
k	Number of cycles per frequency

K_f	Waveform coefficient
K_u	Window utilization factor
L'	Filter inductor reflected to the primary
L_a	Modified topology auxiliary inductor
L'_a	Modified topology auxiliary inductor reflected to the primary
λ_0	Target operating trajectory
λ_x	Inverter natural trajectories
L_b	Modified topology auxiliary inductor
L_d	Leakage inductance from the leakage magnetic flux
L_{lk}	Transformer leakage inductance
L''_{lk}	Transformer leakage inductance reflected to the secondary
L_s	Load series inductance
L_{zvt}	Auxiliar zero voltage switching inductor
M	Kernel length
M_x	MOSFET (transistor and body diode)
n	Normalized subscript
N	Number of frequency points
$n(t)$	Noise and harmonic distorsion
N^2	Transformer ratio squared

ω_{sw}	Angular switching frequency
ω_L	Inverter fundamental frequency in radians
ω_o	Inverter filter natural frequency in radians
P_{fc}	Fuel cell output power
P_{in}	Input power
$P_{lossCON}$	Conduction losses
P_o	Output power
P_{oNOM}	Nominal output power
P_t	Apparent power
Q_{rr}	Reverse recovery charge
Q_x	MOSFET N-Channel
R_a	Combined activation and mass transport losses
R_c	dc and skin effect copper losses equivalent resistance
R_{Conc}	Concentration Voltage
R_{dsON}	MOSFET on resistance
R_l	Load resistance
R_{ln}	Normalized load resistance
R_m	Core losses equivalent resistance
R_{Ohmic}	Resistance of the electrodes (electrons) and membrane (protons)

r_p	In-phase reference
r_q	In-quadrature reference
σ	Phase shift
σ_x	Natural switching surface control law
t_i	Sampling instant
T_{line}	Line frequency period
T_{max}	Maximum time per frequency
T_{min}	Minimun time per frequency
t_n	Normalized time
T_o	Natural frequency period
T_{wait}	Wait time before each measurement
t_x	Time instant
$t_x - t_y$	Time interval
u	Switch position
V_X	In-phase component of the measured voltage
V_Y	In-quadrature component of the measured voltage
V_{Act}	Activation voltage
R_{Act}	Activation equivalent resistance
v_{bus}	Bus capacitor voltage

v_{cc}	Inverter input voltage
v_{ccn}	Normalized inverter input voltage
v_{ds}	Drain to source voltage
v_{fc}	Fuel cell output voltage
v_g	Gate to source voltage
V_H	Secondary voltage referred to the primary side
V_i	Input voltage
V_i''	Input voltage reflected to the secondary
V_L	Primary voltage
v_{M_r}	MOSFET drain to source voltage
v_{nom}	Nominal voltage
V_o'	Output voltage reflected to the primary
v_{on}	Normalized output voltage
v_{op}	Output voltage peak value
v_p	Transformer primary voltage
V_R	Reverse applied voltage
v_r	Reference voltage
v_{rn}	Normalized reference voltage
v_s	Transformer secondary voltage

W_a	Window area
Z_o	Characteristic impedance

Chapter 1

Introduction and Literature Review

Fuel Cells (FC) are power sources that convert electrochemical energy into electrical and thermal energy in a clean and efficient manner. Fuel cells have the potential to meet a new generation of energy standards comprising low cost, high efficiency, low emission, quiet operation, as well as ensure energy availability for the future. A basic FC arrangement is like a battery consisting of anode and cathode electrodes linked by electrolyte. However, unlike batteries, FCs can operate continuously while they are externally fed with fuel. As a result of a chemical reaction at the anode, electrons are generated. The electrons circulate externally through the desired electrical load towards the cathode, producing work. The maximum theoretical potential generated by a single FC is 1.23V (Nerds voltage). However, due to several parasitic effects, the practical output voltage of a single FC lies below 1V. As most applications require a greater voltage, several single FCs can be connected in series to form a FC stack.

FC stacks provide unregulated DC output voltage at their output terminals that change with the loading conditions. In order to integrate a FC system and the

application, a power management or power conditioning system is required. A power electronics converter is used to adjust the unregulated output voltage of the FC to meet the requirements of the specific application.

1.1 Fuel Cell Systems

Different types of FCs are currently under development and can be classified into three groups by their operating temperature: Solid Oxide Fuel Cell (SOFC) and Molten Carbonate Fuel Cell (MCFC) belong to the high temperature category (1000°C and 650°C respectively) and can be fuelled by methane, propane, butane, natural gas, and gases from coal in the case of MCFC; Phosphoric Acid Fuel Cell (PAFC) operate in a range of medium temperatures (150-200°C) and are tolerant to carbon monoxide impurities in the hydrogen fuel; and Direct Methanol Fuel Cell (DMFC) operated with methanol and water, Proton Exchange Membrane Fuel Cell (PEMFC) fuelled by high-purity hydrogen, and recent developments in Alkaline Fuel Cell (AFC, also operated with hydrogen) belong to the low temperature group, with operating temperatures of 80°C, 50-100°C, and 25-70°C respectively [1, 2].

FCs can be used in a wide range of transportation, stationary power generation, and portable power applications [2, 3]. Application of FC in automotive power trains has been receiving more attention in recent years [4]. Even though commercial vehicles powered by FCs are not yet available, the major automotive companies in partnership with FC producers are developing and testing FC cars. Moreover, some existing FC pilot projects in public transportation have proven the advantages of this concept [5]. Recent substantial improvements in PEMFC put this technology ahead of the other types of FCs for transportation as well as small power generation applications. The main advantages of PEMFC are high power density, no moving

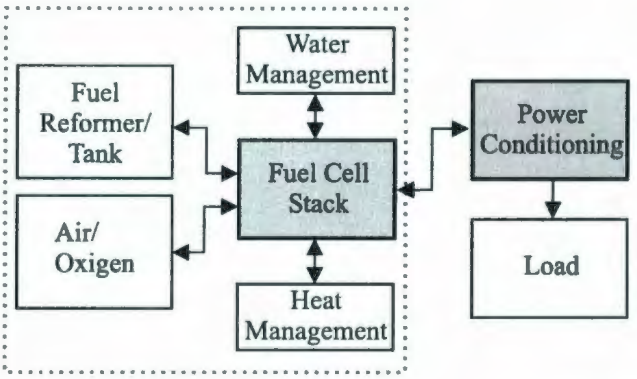


Figure 1.1: Conceptual block diagram of a fuel cell system.

parts, and water as a by-product. PEMFCs are also being tested in golf carts, scooters, underwater vehicles, and light airplanes [6–8]. The stationary power generation segment includes utility power plants, building power generation (for hospitals, office buildings, schools, and airports), and low power residential applications [9, 10]. The FC systems described above require auxiliary equipment in order to operate in addition to the FC stack: fuel management, air management, thermal management, and water management [1, 2] as indicated in Fig. 1.1. These subsystems are designed to meet specific requirements for each FC technology and application. Hydrogen FCs primarily fuelled with hydrocarbons also require a fuel processor/reformer conversion stage. The fuel management subsystem includes pipes, tank, and pressure regulators to control fuel at the anode inlet. The air subsystem provides air/oxygen supply management in the cathode. An air blower can be used for low pressure supply. However, since high pressure air supply improves the overall performance of FCs, an air compressor is desirable. A liquid coolant or water circuit that interconnects the FC stack to the heat exchanger (or radiator) provides thermal management to control the temperature of the FC stack. The water management system involves water removal from exhaust gas, storage, and reutilization for humidification of the reactant. In addition, if a reformer is used, water is also supplied to this stage.

Since FC stacks provide unregulated dc output voltage, a power conditioning stage is required between the FC and the load. A power electronics converter is connected to the output terminals of the FC to adjust the unregulated dc output voltage to meet the requirements of the specific application [11]. The interaction between the load, power converter, and FC system presents a number of technical problems which must be addressed during the design stages. In fact, as discussed in this work, integrated control strategies for the FC system and power converter are required to ensure good performance in the FC system while complying with the load demands. This is one of the key challenges addressed in this work.

1.1.1 The Fuel Cell in Steady State Operation

The previous section provided a brief description of the existing FC technologies and the subsystems of a FC generation system. This section introduces the static and dynamic behavior of PEMFC and DMFC (both polymer-electrolyte FC) under different operating conditions, providing the basis for successful design of the FC control and power conditioning stages. Each subsystem shown in Fig. 1.1 controls the factors that govern the behavior of the FC system. For example, in a PEMFC, four input flows are basically manipulated: hydrogen supply to the anode, air/oxygen supply to the cathode, water/air to the coolant channels, and water supply to the humidifier [12]. As well, the electrical load connected to the FC determines its output current, which is also an important parameter. Finally, the FC temperature, which is significant parameter, is controlled by a simple on/off air blower or more sophisticated coolant variable flow.

The factors that mainly contribute to the PEMFC output voltage behavior are hydrogen partial pressure (supplied to the anode), air/oxygen partial pressure (sup-

plied to the cathode), and operating temperature (coolant channels), [1, 12, 13]. In addition, the output current of the PEMFC greatly affects the output voltage and hence its output power. Interaction between parameters exist, that is, a change in one parameter on the output voltage may be dependent on the setting of the other parameters, revealing that FC systems are in nature non-linear multivariate systems [14].

PEMFCs can be operated in different power regions. The low power region provides excellent efficiency in the FC and low efficiency in the subsystems [15]. As the output power increases the efficiency of the FC is reduced and the efficiency of the additional equipment shows improvement. From a utilization point of view, the PEMFC should be operated in the medium power region, where the combined efficiency of the FC and additional equipment is still acceptable. However, the high power region provides a better cost per kW and power density figure, which is a key consideration for applications where space is limited.

In a DMFC, the factors that mainly contribute to its output voltage behavior are fuel (methanol concentration), fuel flow rate (supplied to the anode), air/oxygen flow rate (supplied to the cathode), and operating temperature [1]. As well, the system output current is a significant factor that affects the output voltage and hence its output power. To better illustrate this behavior, a set of experiments were performed using a laboratory single DMFC [16]. Figure 1.2 shows a family of polarization curves (voltage versus current) of a $5.3cm^2$ electrode area DMFC under different operating conditions. The figure shows how the output voltage and power availability of the FC is modified by the operating conditions (e.g., operating temperature, oxygen flow rate, and output current using a fixed methanol concentration). When the voltage and power curves presented in Fig. 1.2 are plotted as a function of the electrode current density, the results can be extended to bigger electrode area and cells in

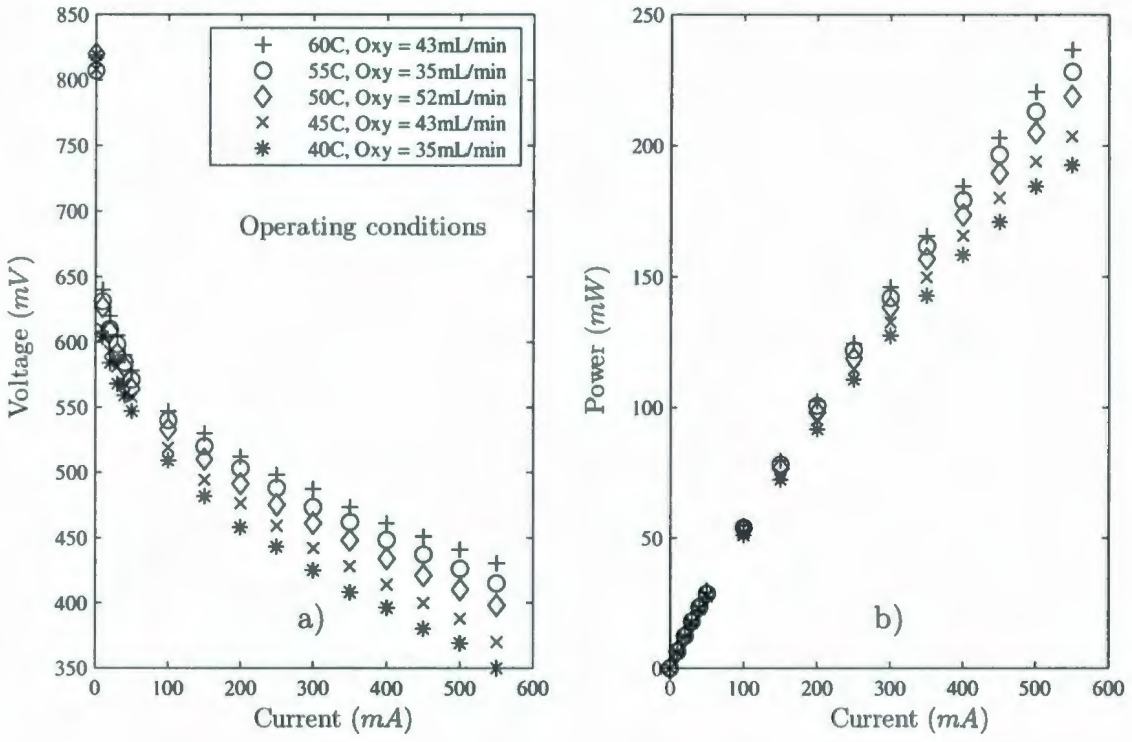


Figure 1.2: Steady state characteristic of a Direct Methanol Fuel Cell. a) Polarization curve and b) Output power characteristic.

series (stacks).

It is interesting to note how the output voltage of this typical DMFC is greatly affected by its operating temperature and output current (fuel and oxygen flow rates are close to optimal in this case). This results in a significant change of the available output power as depicted in Fig. 1.2(b). The following can be concluded from these steady state figures: In order to obtain a desired output power, it is first necessary to modify the operating conditions. For example, to extract 200mW the operating temperature must be at least 45°C as shown in Fig. 1.2(b). It should be pointed out that the transition from a given polarization curve to another through variation in operating conditions is very slow. The main reasons for this behavior are the high heat capacity of the cell, and the slow mass transport processes in the flow fields

and electrodes (fuel distribution in the flow channels and electrodes assembly)[17, 18]. Hence, a fast dynamic response of this power source should not be expected. However, a dynamic behavior of the FC exists when the output current changes for fixed operating condition.

1.1.2 Electric Circuit Model of the Fuel Cell

A comprehensive review of the many models developed for FCs has been presented in the literature [19]. The electrical behavior of polymer-electrolytes FCs can be modelled in terms of the equivalent circuit shown in Fig. 1.3 [18]. What follows is a description of the basic features needed to understand the electrical characteristics of the FC.

In Fig. 1.3, the electrochemical and thermal behavior of the FC is modeled using the following components: E is the equivalent internal potential or open circuit output voltage. For a DMFC, the theoretical voltage (E) in Fig. 1.4 is given as a function of the methanol and oxygen feed concentrations by the Nernst equation [1]. The theoretically predicted value lies around 1.2V for a single cell. However, typically, the practical open circuit output voltage remains below 0.8V, and the voltage drops further as current is drawn from the cell. E_o is standard reference potential at 1 ATM and 25°. f_E is a non-linear potential associated to chemical reactant variations and fuel/oxidant delay and is a function of the cell internal temperature and the output current. In this model, the activation voltage drop $V_{Act}(T)$ corresponds to the activation of the anode and cathode, which depends primarily on the cell temperature, the catalyst effectiveness, and the active areas of the electrodes. The effect of the output current associated with the activation voltage drop is modelled by R_{Act}. R_{Ohmic} represents the voltage drop due to the resistance of the electrodes (electrons)

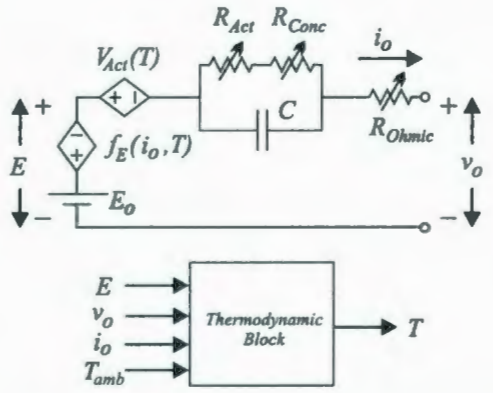


Figure 1.3: Fuel cell equivalent circuit.

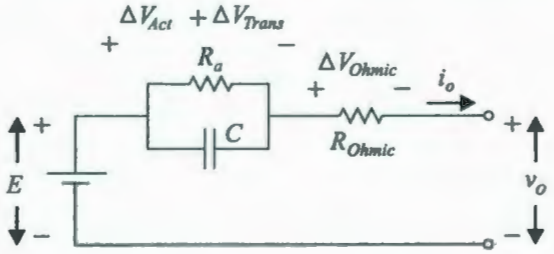


Figure 1.4: Simplified equivalent model of the Fuel Cell.

and membrane (protons). The concentration voltage drop reflects the decreases in the concentrations of the reactants within the electrodes, for example, methanol at the anode and oxygen at the cathode in a DMFC. This is included in the model as R_{Conc}. Finally, the thermodynamic block represents the slow thermal dynamic behavior of the FC as a function of ambient temperature, output current, output voltage, and internal potential.

As can be seen in Fig. 1.3, the model shows an intricate non-linear dependence on temperature and reactants behavior. Nevertheless, when the FC is operated with fixed operating conditions (i.e., fixed temperature, fuel concentration and air flow), the model of Fig. 1.3 can be significantly simplified using the circuit in Fig. 1.4.

The several factors that cause voltage drop or irreversibility, namely activation losses (Tafel equation), fuel crossover and corrosion, internal currents, ohmic losses,

and mass transport are conceptually represented in a simple general equation (1.1) [1]. The influence of these factors results in the FC polarization (voltage vs. current).

$$V_o = E - \Delta V_{Ohmic} - \Delta V_{Act} - \Delta V_{Trans} \tag{1.1}$$

The second term in (1.1), ΔV_{Ohmic}, represents the voltage drop due to the electrodes and membrane resistance. The third term of the equation, ΔV_{Act}, corresponds to the activation of the anode and cathode. Finally, ΔV_{Trans} is due to decreases in the concentrations of the reactants.

In the equivalent circuit shown in Fig. 1.4, the ohmic loss is represented by R_{Ohmic}, while the activation and mass transport losses are combined as R_a. Although R_a exhibits a complex dependence on the current drawn from the cell, it can be considered as approximately constant under medium and high loading conditions. The electrodes capacitance C, known as the double layer capacitance, acts in parallel with R_a. The double layer capacitance is a characteristic of any interface between an electron conducting phase and an ion conducting phase. It arises from the fact that (in the absence of a Faradaic process) charge cannot cross the interface when the potential across it is changed [20]. As will be seen, the key component for its dynamic behavior is the large capacitance (C) of the cell.

The action of the cell capacitance in conjunction with ΔV_{Act} and ΔV_{Trans} is described using Kirchhoff's current law as follows:

$$\frac{d(\Delta V_{Act} + \Delta V_{Trans})}{dt} = i_o \frac{1}{C} - \frac{\Delta V_{Act} + \Delta V_{Trans}}{R_a C} \tag{1.2}$$

where i_o is the FC output current, and R_a is a non-linear resistor that produces both ΔV_{Act} and ΔV_{Trans} drops during steady state operation.

For a given set of operating conditions (i.e., specified temperature, fuel concentration and air flow), the parameters in the model will remain approximately constant, except for R_a at low current densities. A change in the operating conditions produces a change in the values of the model parameters.

1.1.3 The Dynamic Behavior of the Fuel Cell

This section describes the dynamic behavior of a polymer-electrolyte FC, focusing on the aspects that are relevant to stationary power conditioning. Two main characteristic behaviors are discussed, namely power availability and power reduction due to ripple current for fixed operating conditions.

It has been shown in Section 1.1.1 that the steady state behavior of a polymer-electrolyte FC with fixed operating conditions can be represented with a non-linear polarization curve (v-i characteristic). If the operating conditions are modified, a new polarization curve is obtained. As indicated in Section 1.1.1, this change in the polarization curve occurs very slowly due to the high heat capacity of the cell and slow mass transport processes in the flow fields and electrodes. A fast dynamic behavior, however, takes place when the operating conditions are fixed and the output current changes. The objective of this section is to explain the transient behavior of the FC system under different loading conditions. The following analysis provides the foundation for successful coordination between the FC system and power conditioning stage, an important consideration that forms the basis for the development of innovative techniques in this work. Two experiments, namely power steps and ripple current were specifically performed to explain the unusual behavior of the FC. The experiments described in this section address a subject that is of interest to the power electronics community [17].

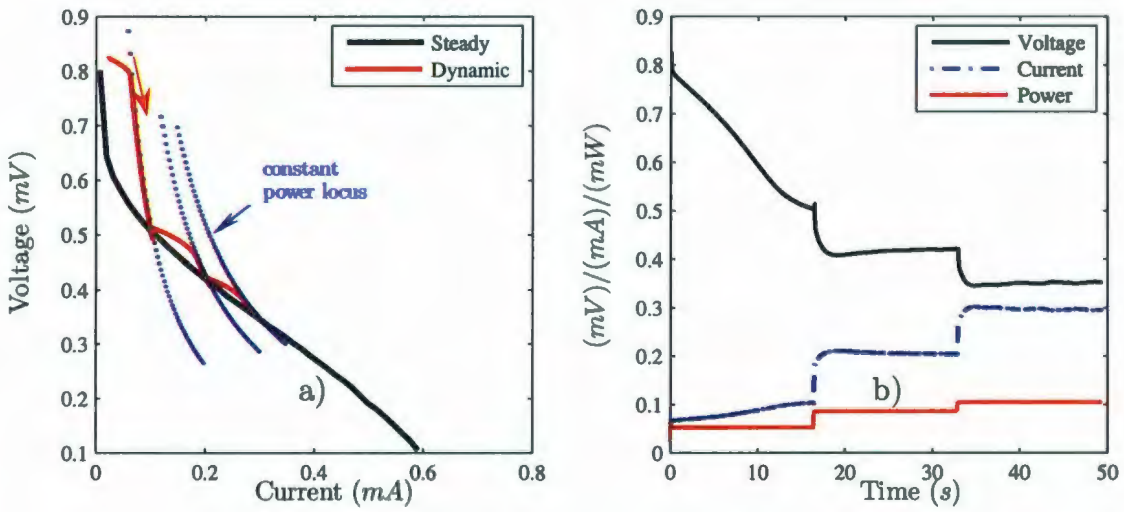


Figure 1.5: The dynamic response of the DMFC to a series of power steps: a) v-i plot and b) time domain plot.

A test of constant power steps was performed with the objective of demonstrating that polymer-electrolyte FC can cope with sudden power demands within its power limits. Figure 1.5 shows the experimental results obtained for this series of power steps in v-i and time domain plots respectively. The bold line of the v-i plot of Fig. 1.5 represents the steady state polarization curve. The dashed curves on the v-i plot correspond to the operating point trajectories or dynamic paths for the series of power steps ($52.4mW$, $86.0mW$, and $104.5mW$).

Two important points can be highlighted from this experiment: 1) The FC is able to adjust its output current instantaneously to match the power demand, and 2) the operation point (OP) can depart significantly from the steady state polarization curve during transients. Considering the equivalent circuit shown in Fig. 1.4, it can be seen that the output voltage transient of the FC is influenced by the charging and discharging of the cell's double layer capacitance, C.

Ripple current on the dc power source, in this case the FC power system, is inherent to single-phase and three-phase inverters. For single-phase inverters, the

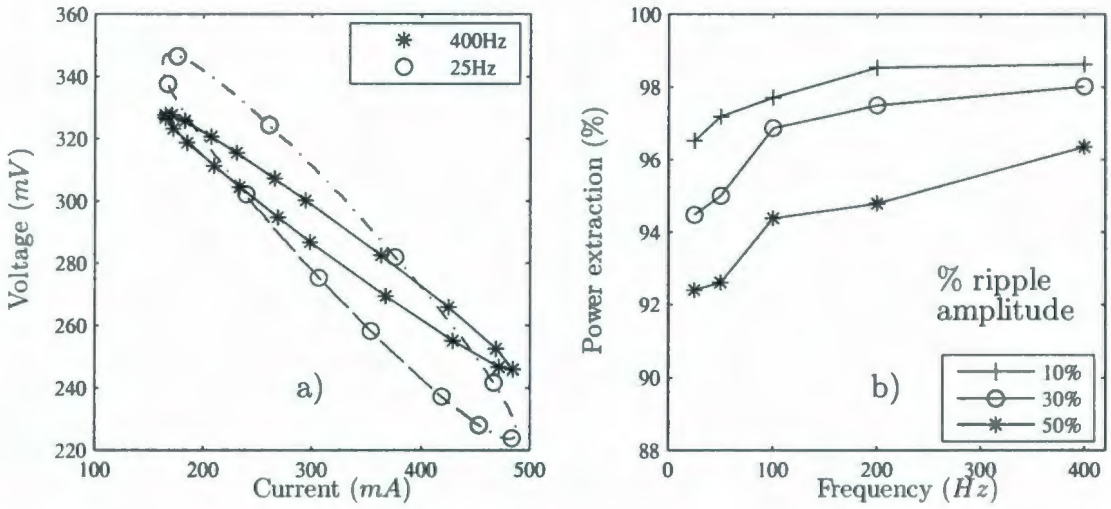


Figure 1.6: dc+ac current test of the DMFC for 25Hz and 400Hz: a) Zoom of the v-i plot and b) FC power extraction with ripple current as a percentage of the power extraction without ripple.

fundamental frequency of the ripple is double the line frequency. The behavior of commercial FC under 120Hz current ripple has been evaluated and its impact on the FC is a topic under investigation [21–23]. Experimental results demonstrating the current ripple effect are presented in Fig. 1.6(a), which shows that the extracted current has a dc operating point of $325mA$ superimposed with 25Hz and 400Hz ripple current. As can be seen in this v-i plot, the trajectory of the operating point has a hysteresis behavior. The hysteresis behavior, which denotes a phase difference between the voltage and current, is associated with the double layer capacitor. As the frequency increases (i.e., $400Hz$), the hysteresis is reduced and the power extraction increases.

The power extraction for different current ripple amplitudes and frequencies as a percentage of the power without ripple is presented in Fig. 1.6(b). The test was performed for amplitudes of 10%, 30% and 50% of the dc operating point ($325mA$). The curves show the decrease in power extraction when the amplitude of the ripple

increases. An increase in the frequency of the current ripple helps to increase the power extraction. Similar effects have been reported for hydrogen fuelled FCs [21].

For simplicity and accuracy, these experimental tests were performed using a small laboratory polymer-electrolyte FC setup with methanol as fuel. These results and conclusions are valid for larger electrode areas and stacks where the current levels and voltages are expected to increase. Having demonstrated the power availability nature of polymer-electrolyte FC systems and how it is affected by ripple current, this work develops a control scheme that eliminates or minimizes the ripple current generated by the power conditioning stage.

1.2 Fuel cell power conditioning

Fuel cell stacks are low-voltage high-current power systems that provide unregulated dc output voltage. Typical loads in the segment of stationary low power generation are home appliances, lights, electronics apparatus, and heating/cooling systems, which normally require 120/220V at 60/50Hz. In order to comply with this requirement, the low dc voltage produced by the FC needs to be increased and then converted into alternate current using an inverter. A conceptual block diagram of a FC power conditioning system is depicted in Fig. 1.7, illustrating some of the possible configurations. Galvanic isolation from the main power source is generally recommended for enhanced safety and can be obtained by either using a high frequency transformer in the dc-dc converter or a line frequency transformer in the inverter stage [11].

A high frequency transformer provides a significant core size reduction at the expense of a more complex dc-dc power stage (i.e. full-bridge). On the other hand, a line frequency transformer substantially increases the magnetic core size and weight of the inverter stage. Systems based on line frequency transformers, including fer-

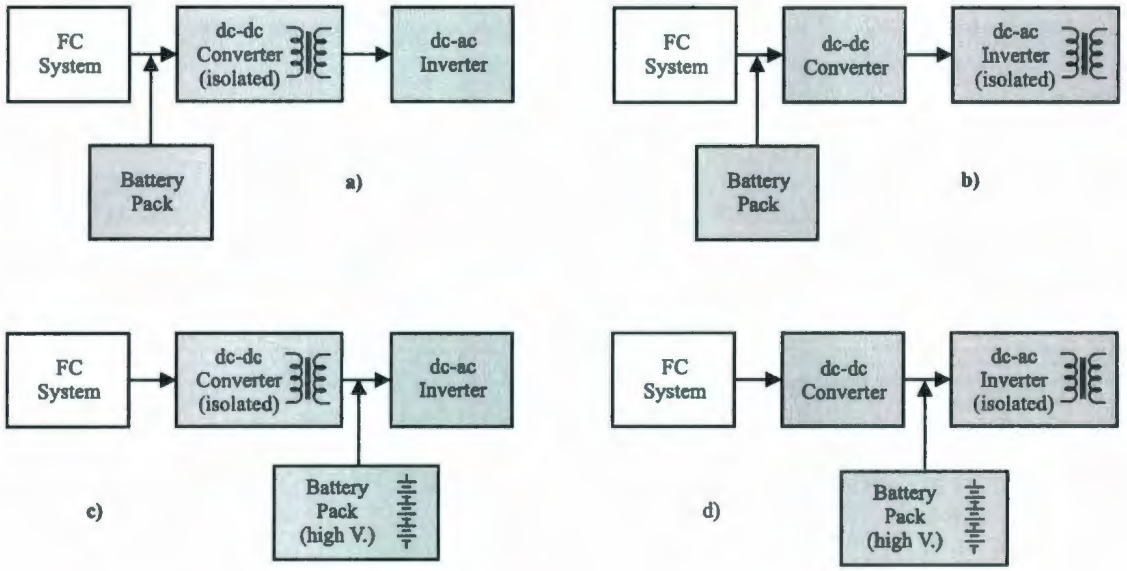


Figure 1.7: Some possible configurations for FC power conditioning systems.

roresonant inverters, are extremely rugged and reliable due to the low components count. Nevertheless, their excessive weight makes them unsuitable for residential and commercial stationary applications. The battery pack shown in Fig. 1.7 is employed to supply peak load demands (i.e. motors during start up) or higher than average power consumption during peak hours. As can be noted in Fig. 1.7(a) and Fig. 1.7(b), the battery pack can be included in the low voltage side (dc-dc input side). For this scheme, the excess peak power is supplied by the battery pack and circulates through the dc-dc converter. Hence, the dc-dc converter has to be designed to support full peak load capacity. When several batteries are connected in series to the high voltage side (inverter dc link), the dc-dc converter only handles the power coming from the FC (Fig. 1.7(c) and Fig. 1.7(d)). During normal operation, the FC provides energy to supply both the inverter output and charge the battery pack.

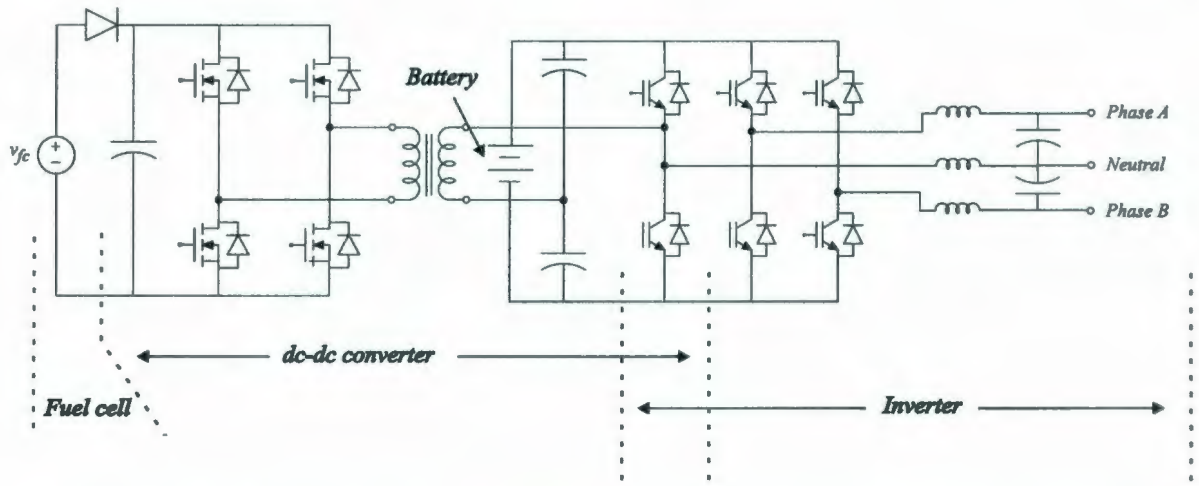


Figure 1.8: Fuel cell power converter based on a controlled voltage doubler [24].

1.2.1 State-of-the-art Power Converter Topologies

This section describes the relevant power converter topologies reported in the literature that may be employed for FC stationary applications. The key features and drawback of the proposed topologies are discussed with a view to identify the main challenges in the area of FC power conversion.

A fuel cell power converter based on a controlled voltage doubler is introduced in [24]. This converter uses phase shift to control the power flow through the dc-dc stage which supplies 400V to split-phase inverter as shown in Fig. 1.8 The main advantage of this design is that filtering is eliminated in the dc-dc converter side. Instead, the transformer leakage inductance is used as a key parameter to control power flow through the transformer. A battery pack is attached to the high voltage dc link as an energy storage system. The main drawbacks of this interesting topology with low component count are low efficiency [25], undesired low current ripple reflection on the FC, and reduced battery lifetime (due to low frequency ripple current on the high voltage dc link). Since a battery pack is connected to the high voltage dc link, line frequency ripple current constantly circulates through the battery, affecting its life

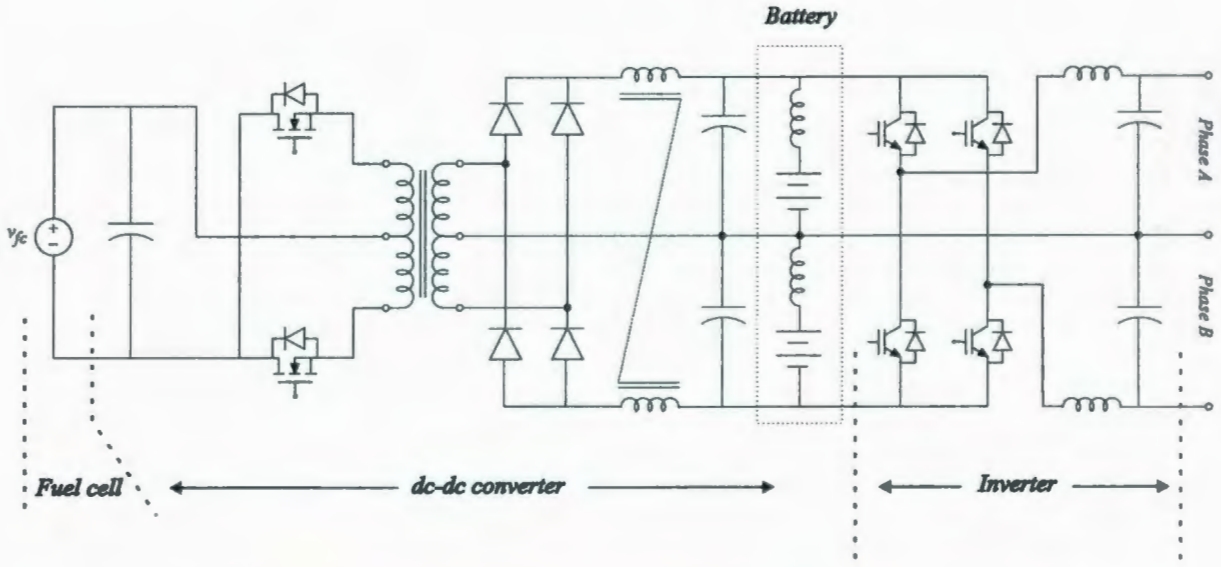


Figure 1.9: Fuel cell power converter based on push-pull topology [26].

time. Charging the battery pack using constant current, constant voltage cycle does not seem to be an option with the proposed scheme. Finally, the inverter stage is constructed with three legs in which one leg is shared with the doubler while working as neutral phase.

A fuel cell inverter with DSP control based on a push-pull dc-dc converter is shown in Fig. 1.9 [26]. This system features low cost, low components count, and state of the art DSP control. Like the previous description, a battery bank is also included on the inverter dc link with inductors in series to limit the effect of ripple current on the batteries. Again, the batteries are exposed to degrading low frequency ripple current. In addition, as the power rating increases, the push-pull topology may easily saturate the transformer due to the asymmetry in the windings and slight imbalance in the excitation.

A current-fed push-pull power converter with grid connection capability has recently been reported and is shown in Fig. 1.10 [27]. This award wining system (Future Energy Challenge 2005) includes an innovative current-fed concept based on an in-

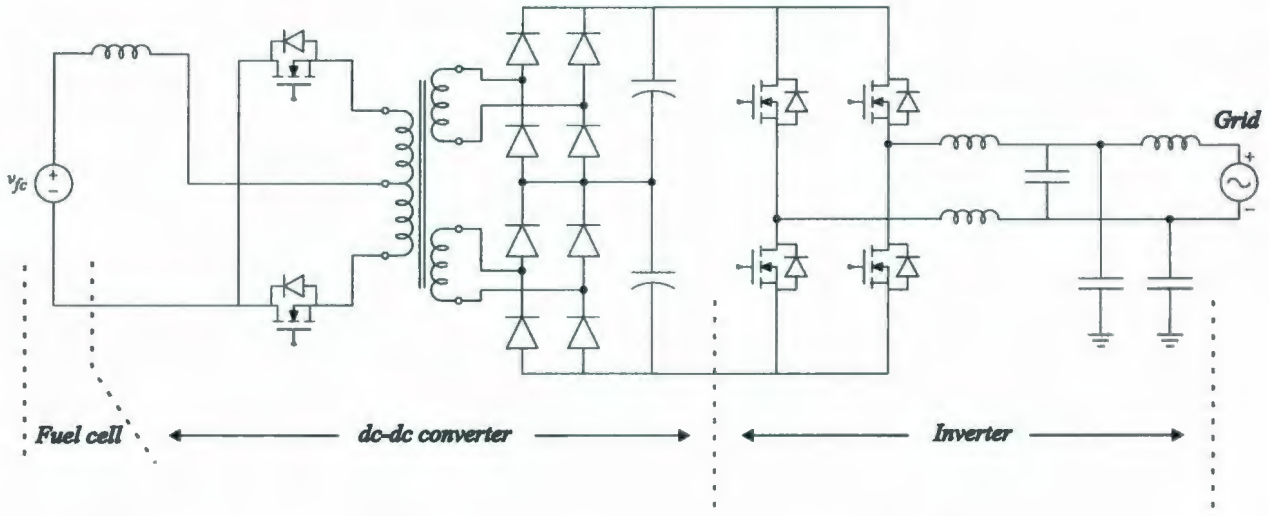


Figure 1.10: Fuel cell power converter based on current-fed push-pull topology [27].

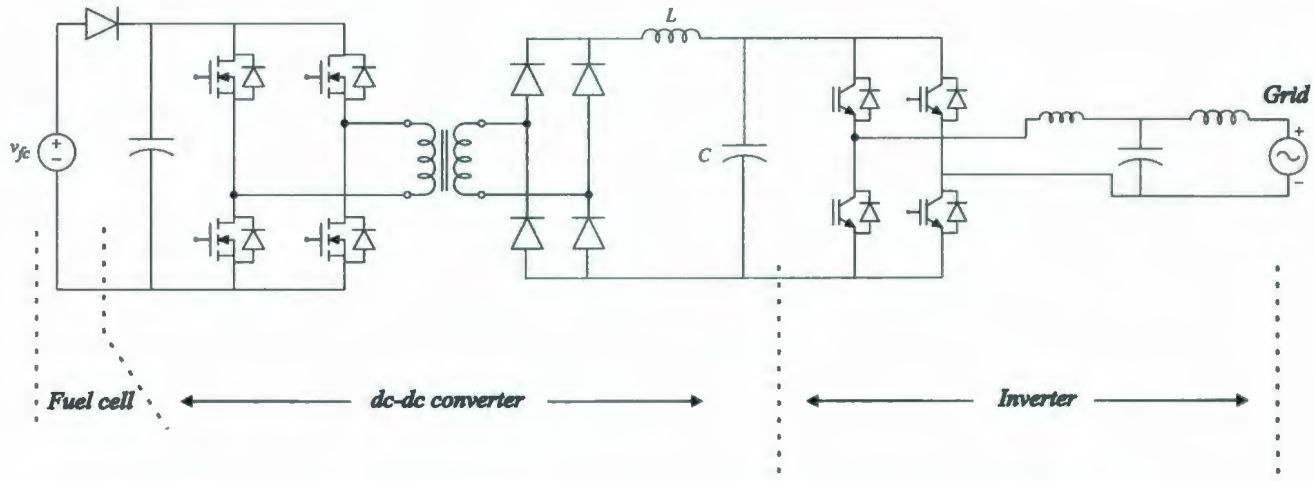


Figure 1.11: Fuel cell power converter based on full-bridge forward topology [28]

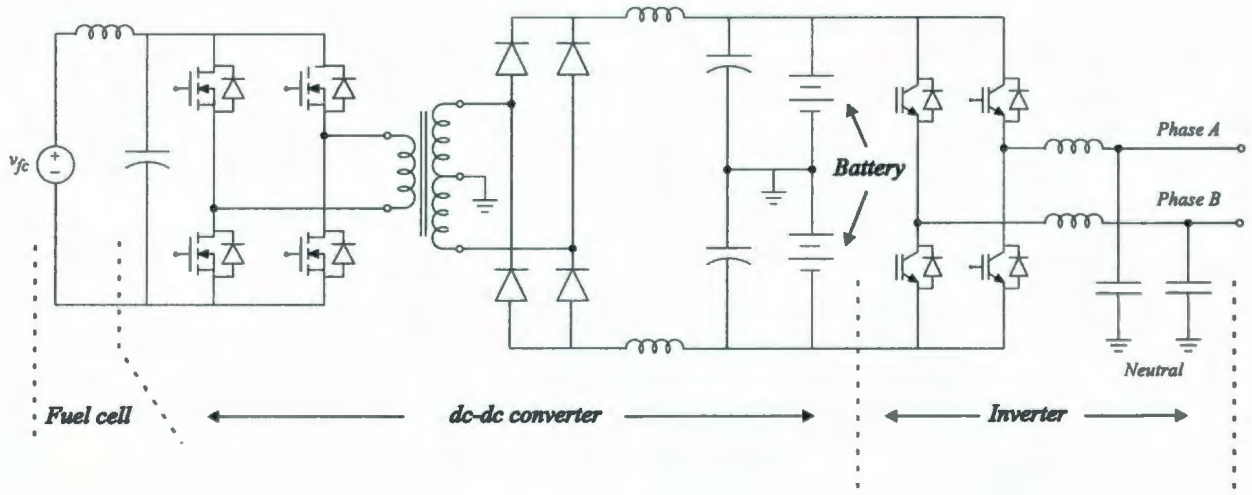


Figure 1.12: Fuel cell power converter based on full-bridge topology [29].

ductor connected in series with the input voltage source. Hence, the primary source behaves like a current source. One of the main issues for this design is the leakage inductance of the transformer and the voltage rating of the switches. The energy accumulated cycle by cycle in the leakage inductance is mostly dissipated in the switches with a controlled turn off strategy, which affects the efficiency of the system. As well, push-push topology reduces transformer utilization and compromises magnetization balance as the power rating increases.

The second prize winner of Future Energy Challenge 2005 is based on a full-bridge forward converter with full-bridge rectifier dc-dc power stage (Fig. 1.11), combined with a full bridge inverter [28]. As discussed in detailed in Chapter 2, this is a very robust topology when operated with hard switching technique and represents a probable industry standard. Yet, the topology poses many technical challenges such as efficiency, devices stress and power density that need to be addressed to improve the overall performance when employed in FC applications.

Another system with similar characteristics was reported by University of Wisconsin for the Future Energy Challenge 2001 competition [29], which is shown in Fig.

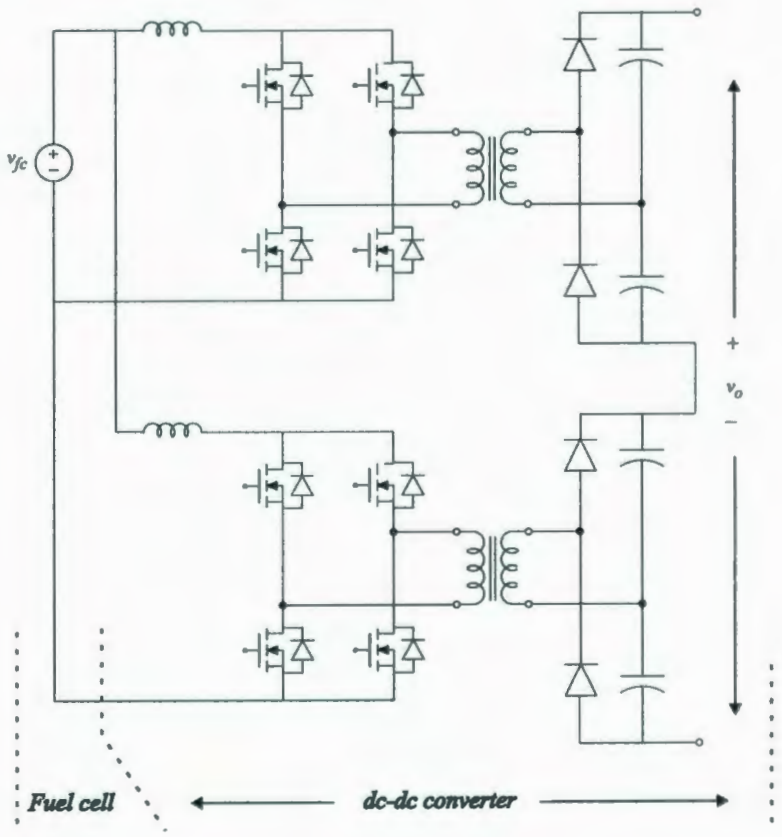


Figure 1.13: Interleaved current-fed full bridge dc-dc converter [30].

1.12. A battery pack was included as part of the inverter dc link presenting the same rapid degrading problems as discussed for the preceding two topologies [26] and [24].

An interleaved current-fed full bridge dc-dc converter was proposed featuring low input current ripple and reduced stress in the input side semiconductors, which is shown in Fig. 1.13 [30]. The main drawbacks in this topology are: a) Excessive high frequency ripple current in the output capacitors is experienced during each operating state. Recall that ripple current defines the lifetime of the filter capacitors; b) Like in other current-fed topologies, the leakage inductances combined with the interwinding capacitances play a key role in defining undesirable current oscillation during power transfer; c) The number of drivers and transformers is doubled. The topology employs 2 transformers and 8 MOSFET drivers; d) Two large input induc-

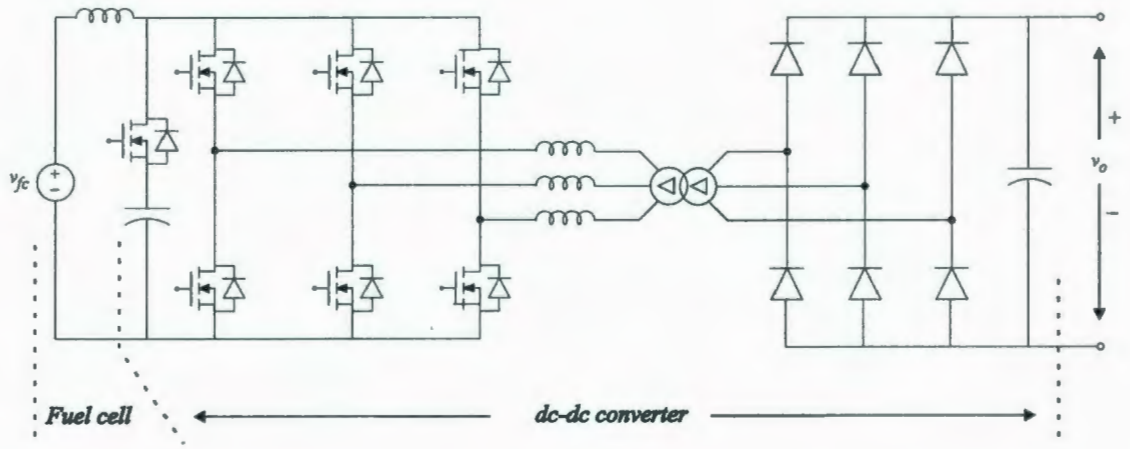


Figure 1.14: Three-phase current-fed dc-dc converter with active clamp [31].

tors are needed, which should be rated at very high current. Note that it is always desirable to place the inductor in the high-voltage side of the converter where the current rating is reduced, thus simplifying its construction.

A three-phase current-fed dc-dc converter with active clamp has been proposed, which is shown in Fig. 1.14 [31]. The active clamp consists of an auxiliary MOSFET in series with a capacitor, as shown in Fig. 1.14. The transformer leakage inductance is used to achieve Zero Voltage Switching ZVS in the primary switches and the three-phase arrangement increases the transformer utilization. This converter transfers power in a pulsating fashion with reduced RMS. However, the utilization of the switches is low and the overall power transfer is inherently limited by the transformer leakage inductance. The ripple current in the output capacitor is large and the component count is large as well. Like in other configurations with the rectifier connected directly to the output capacitors, the possibility of current sharing between power converters becomes an issue.

A variation of the previously discussed current-fed topologies has been proposed in [32]. An active clamping circuit based on an auxiliary buck converter is incorporated as part of the topology to return the energy of the snubber capacitor to the input

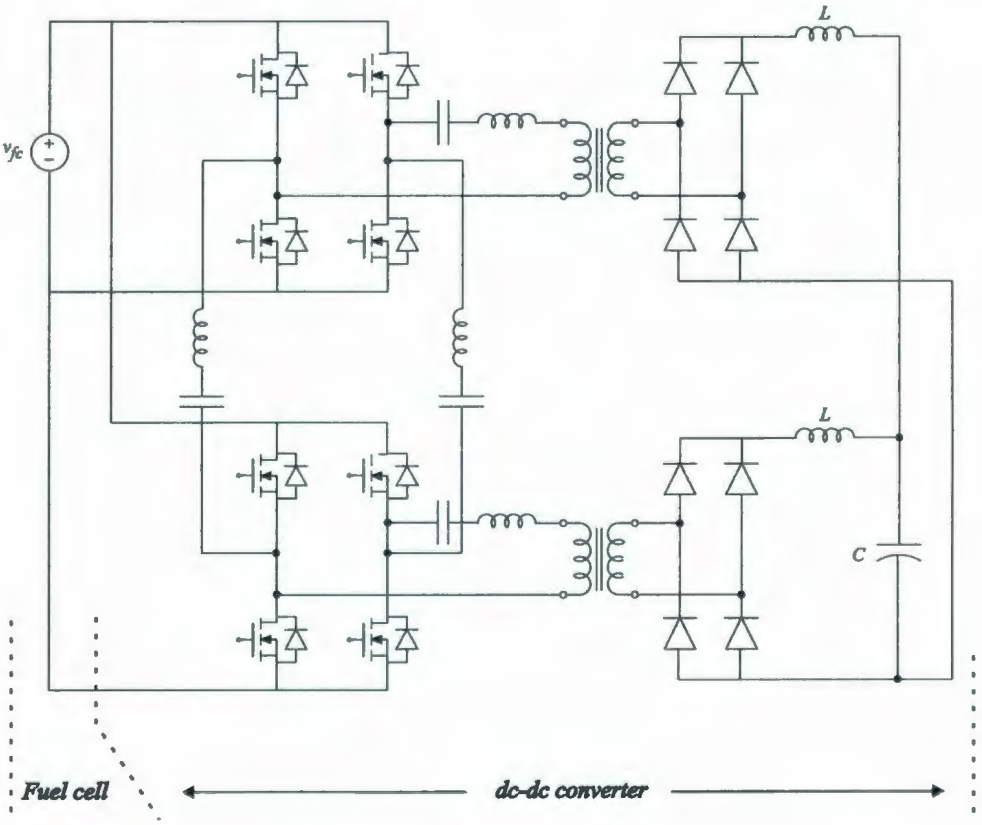


Figure 1.15: A phase-shift ZVS with adaptive energy storage [33].

capacitor bank. Similar characteristics and disadvantages are found in this power converter.

A new family of phase-shift ZVS with adaptive energy storage was proposed to increase the efficiency using auxiliary circuits, which is shown in Fig. 1.15 [33]. The objective of this interesting topology is to minimize auxiliary circulating currents under different input voltage and loading conditions. Low-voltage high-current input applications makes the inclusion of series capacitors (dc blocking) in the primary a practical challenge due to the very high ripple current flowing through it (accelerated lifetime reduction). As well, the primary leakage inductance required to achieve ZVS is either hard to integrate in the transformer or costly to include externally in the primary considering its high current rating. Unlike applications with high input volt-

age, achieving ZVS with low voltage does not lead to subtancial efficiency gains given the small energy storaged in the MOSFETs output capacitance (Coss), being the square of the input voltage the main factor that defines turn-on power losses. The power dissipated in the MOSFET output capacitance is given by $\frac{1}{2}\ F_{sw}\ C_{oss}\ {v_{fc}}^2$, where F_{sw} is the switching frequency and v_{fc} the FC output voltage. Finally, while modularity is one of the key advantages of the proposed scheme, a large number of components is required to built a basic cell (i.e., 8 MOSFETS and drivers, 8 diodes and 2 transformers).

Finally, in addition to the various power converters described above for stationary power generation, other power converters for applications such as transportation have been proposed for high voltage FC systems (200-400V) and multiple output voltages [34, 35], which is not the aim of this work.

1.2.2 Advanced Control Schemes

In the previous section, a number of interesting topological arrangements for FC power converters were described highlighting their main advantages and drawbacks. This section outlines aspects related to control and operation of the mentioned topologies.

The power converter based on a controlled voltage doubler shown in Fig. 1.8 employs a strategy based on transformer power flow control [24]. The key element for this topology is the transformer leakage inductance. Both the full bridge and the voltage doubler are operated in square-wave mode with a given phase shift. The phase shift between the full bridge and the doubler determines the power flow through the transformer as indicated by,

$$P = \frac{V_H V_L \delta(\pi - \delta)}{\omega L_{lk} \pi}, \tag{1.3}$$

where,

V_H : secondary voltage referred to the primary side

V_L : primary voltage

δ : phase shift

ω : angular switching frequency

L_{lk} : transformer leakage inductance on primary side

Equation (1.3) denotes the power transfer between two square waveforms with a given phase shift that are connected using an inductor. The primary of the power converter in Fig. 1.8 applies a square waveform to the primary while the controlled voltage doubler rectifier also applies a square waveform to the secondary of the transformer. The phase shift between the square waveforms in combination with the transformer leakage inductance results in a net power flow from the primary to the secondary. As can be seen in (1.3), the power transfer capability is limited by the transformer leakage inductance L_{lk}. The control system of the power converter monitors the inverter output power and calculates the power required to discharge or charge the battery pack depending on the loading condition. Therefore, the phase shift angle is controlled to satisfy the power balance equation. Since the FC may restrict the instantaneous power availability, the batteries provide compensation during peak power demands. Conventional pulse-width modulation technique is employed to control the inverter.

The topology presented in Fig. 1.9 represents a more traditional approach for low power conversion for FC systems [26]. A push-pull dc-dc stage is used to boost the FC output voltage to 400V using a commercial current control integrated circuit (UC3825B). This chip employs an inner current loop subordinated to an outer voltage loop. An error in the output voltage increases the current reference level and hence the pulse width (duty cycle). The inverter stage is operated using a low-cost DSP with no particular control scheme. As described in the previous case, similar problems

are identified for the batteries in this converter. As well, transformer magnetization balance presents a problem as the power rating of the converter increases.

The dc-dc current-fed push-pull converter presented in Fig. 1.10 introduces some innovative concepts over the traditional push-pull converter described above [27]. An inductor is included in series with the primary power source to obtain current-fed effect. The control scheme of the dc-dc converter is also based on an inner current and outer voltage loop concept. Since the converter behaves like a current source, constant current can be extracted from the FC to reduce low frequency ripple, resulting in an improvement over existing strategies. However, experimental results show that the current injected into the inverter dc link has a 120Hz ripple current denoting that low frequency ripple is inevitably reflected to the FC stack. This undesired behavior is not due to a topological limitation but rather to the selected inner current, outer voltage loop control scheme. In stand-alone mode, the inverter stage is simply operated in open loop to meet a minimum of 5% regulation with 30% load to comply with Future Energy Challenge 2005 basic requirement. Since the converter is mainly focused on grid connected operation, a controller for stand-alone operation is not discussed.

The full-bridge forward converter with full-bridge rectifier shown in Fig. 1.11 is operated with phase shift PWM to boost dc from a varying 30-60V dc power source [28]. This technique can achieve zero-voltage switching to reduce turn on losses. Higher conduction losses are characteristic of this soft switching converter, which can be a disadvantage at light loading conditions [36]. The control strategy is based on a PI voltage regulator with an inner current loop to improve the dynamic response and limit current levels during transient. The inverter is also controlled with a small-signal PI regulator for both stand-alone and grid connected operations.

A similar topological arrangement shown in Fig.1.12 with a different control strat-

egy is presented in a report for the Future Energy Challenge 2001 by the University of Wisconsin [29]. This system includes a control scheme for the dc-dc converter that draws stiff output current from the FC avoiding undesirable ripple current. The control scheme is implemented by using Current Mode Control (CMC) to directly regulate the input current level [36]. On the inverter side, and in order to compensate for the bus voltage ripple, the modulation index M is controlled with an inverse relation of the bus voltage. This technique is used to decouple the effect of the bus voltage variations over the output filter. In addition, a state observer for the capacitor current combined with output voltage feedback are employed to control the inverter [37].

The remaining power converters shown in Fig. 1.13, Fig.1.14, and Fig.1.15 only tackle the dc-dc power conversion stage and do not include the inverter component [30, 31, 33]. The interleaved current-fed full bridge dc-dc converter (Fig. 1.13) is a boost derived topology that operates with a phase-shift between modules. The control scheme is based on traditional small signal analysis. The three-phase current-fed dc-dc converter (Fig.1.14) has a special PWM strategy for its operation and no details are available in the literature in terms of the control scheme. Finally, the phase-shift ZVS with adaptive energy storage (Fig. 1.15) has analytical steady state equations and a control method to ensure ZVS, which can be implemented with digital or analog circuits.

1.3 Technical Challenges and Proposed Research

Power conditioning for FC systems is an active area of research that has recently gained special attention. As alternative energy sources, FC systems are characterized by a high level of interaction between the power source (FC), the power conditioning

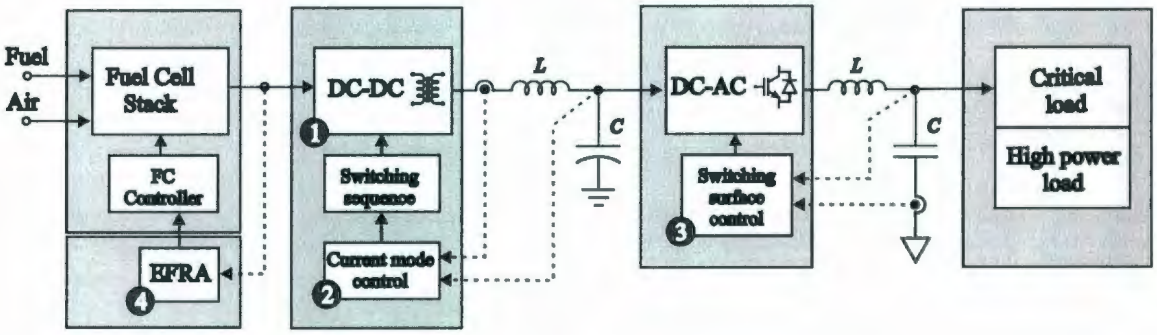


Figure 1.16: Conceptual block diagram of the proposed system.

stage, and the load. For this reason it is extremely challenging to produce an effective design and coordinated operation of the entire system while minimizing power losses and cost. In this section, a number of challenging research subjects are identified and discussed, and the proposed research is outlined.

A conceptual block diagram of the proposed FC power generation system is shown in Fig. 1.16, where the four critical sub-systems are identified to be investigated in this work. In this arrangement, the FC controller adjusts the operating point to match the power required by the load. The isolated dc-dc converter elevates the non-regulated dc output voltage of the FC and the output of the dc-dc converter feeds the inverter. The controller of the inverter generates the modulation pulses to drive the inverter power stage producing high quality output power. Finally, during the operation of the system, the Embedded Frequency Response Analyzer (EFRA) monitors the FC internal processes (impedance measurement) within the FC stack, to provide information on the operating conditions that can be used to control the FC stack.

The objective of this research is to make significant contributions in the critical components of the FC power generation system, while developing a complete and fully operational prototype. The technical challenges and proposed research focus on the four decisive areas identified in 1.16 and are described below.

1.3.1 Isolated dc-dc Power Converter Topology

Commercial FC power sources provide unregulated dc output voltage with high-current capability. As the output current increases the output voltage experiences a significant drop due to the output impedance of the cells. In order to obtain standard 120V 60Hz (or 220V 50Hz) output voltage, the FC dc voltage must be first increased (i.e., 210Vdc for a full-bridge 120Vac inverter) and then modulated using an inverter. Galvanic isolation is among the important features required for the dc-dc power converter stage as outlined in IEEE Standards 519 and 1547 [38, 39]. Therefore, the dc-dc power converter should not only boost the voltage but also provide galvanic isolation to enhance safety.

Several isolated topologies have been proposed and employed in a wide variety of power conversion systems. These can be classified or derived from five basic topologies: flyback, forward, push-pull, half bridge, and full bridge. As well, these topologies can also be categorized as unidirectional and bidirectional depending on the transformer core excitation method [40]. In this work, all the possibilities are carefully explored to find a topology suitable for FC power conditioning. Once the topology is selected, the output rectification method and the transformer configuration are chosen. Two fundamental criteria are followed to select the final topology: efficiency and low device stresses within the entire range of operation of the converter.

As discussed in the introductory chapter and unlike other power sources, FC systems present a wide output voltage range as a function of the loading condition. In addition, the expected loading level in stationary applications can range from 0 to 100% within short periods. These broad operating ranges present additional challenges for the dc-dc converter and further adaptations or modifications to the

selected basic topology are explored.

A comprehensive procedure to evaluate power losses mechanisms in power converters is carried out. The method consists of evaluating conduction and switching losses for each device that is part of the converter (MOSFETs and diodes). The detailed analysis includes turn-on, turn-off, and reverse recovery among switching losses and conduction losses associated with the drain-to-source on-resistance in the MOSFETs and forward bias voltage across the diodes (body and rectifiers). The possibility of employing soft switching techniques is also explored with a view to increasing the overall efficiency of the power converter. Furthermore, other serious problems such as transformer ringing is carefully considered to reduce snubber losses, EMI, maximum reverse voltage and stress on the rectifiers, and overvoltage between transformer windings.

Finally, the modulation or switching sequence that drives the converter is investigated to generate soft switching states and reduce unnecessary conduction losses which are characteristic of some modulation techniques (i.e., current circulating in the primary of the transformer during off states). The details of the investigation and the development of various approaches are presented in Chapter 2.

1.3.2 Control Strategy for Low Frequency Ripple Current Elimination: System Level Study

In addition to the abovementioned constraints in the selection of an isolated dc-dc converter, low frequency ripple current extraction on the FC is also a subject of great concern. This is directly related to the interaction between the dc-dc power conditioning stage and the inverter, which is reflected to the FC. As discussed in the

FC introductory section, the effect of low frequency ripple current is considerable reduction of power availability in the FC and associated power losses [16, 21]. Therefore, low frequency ripple current should be avoided by means of operating the isolated dc-dc power converter as a constant current source.

All the stages in the system, their respective specifications, and interactions between them are key for a successful operation. It becomes, therefore, essential to study the behavior of the power generation scheme at the system level. A system behavioral model is developed as part of this work and analyzed under steady and dynamic operating conditions. The effect of low frequency ripple current generated by the inverter in the swinging bus scheme is studied. Since the inverter extracts low frequency ripple current from the filter capacitor of the dc-dc converter, any attempt to control a fixed voltage on this capacitor results in a reflection of the ripple to the input of the dc-dc converter (FC system). In this work, the concept of swinging bus is studied with the objective of reducing or eliminating the reflected ripple current.

A control scheme is proposed which effectively regulates the current injection in the filter capacitor. In order to do so, an investigation of the relationship between constant current injection under linear, non-linear, and pulsating loading conditions is undertaken as part of the system level study. The details of the investigation and the development of the control schemes are presented in Chapter 3.

1.3.3 Swinging Bus Inverter Control Strategy

The swinging bus concept described above is employed to absorb the 120Hz pulsating current from the inverter. As a result, low frequency ripple current reflection in the FC is eliminated at the expense of the voltage swing at the input terminals of

the inverter. Since inverters are traditionally operated with stiff dc input voltages, the swinging bus presents an unprecedented challenge for the control scheme of the inverter. In order to comply with stringent standards for transient and steady state performance, a control scheme based on curved switching surfaces is proposed. The use of curved switching surfaces to control power converter is an emerging method for fast transient response that has been gaining attention recently [41–43].

A normalization technique to analyze the inverter is proposed as a tool to evaluate curved switching surfaces and simplify the design of the buck-derived inverter in general. The normalization method aims to reduce the number of variables involved in the analysis leading to generality and providing insight into the transient behavior of the converter.

The curved switching surface is constructed by employing three key variables in the circuit; input voltage, output voltage and filter capacitor current. The final selection of the curved switching surface is based on the results from the evaluation of the trajectories of the selected normalized variables under different load transient conditions. The objective of the proposed control scheme is to produce high quality output power under any operating condition, while rejecting the swinging voltage on the dc link. As a result of a rigorous evaluation, a control law for inverters defined as natural SS is proposed and thoroughly characterized for operation under fixed and swinging bus. Throughout this work, novel operating characteristics such as fixed switching frequency, monopolar, bipolar, and mixed operating modes are analytically investigated using the natural SS and validated through experimentation. The development of the concepts is presented in Chapter 4.

1.3.4 Monitoring and Diagnosis of FC systems

In the preceding section, a complete description and analysis of the components required to control and operate the FC and the power conditioning stages have been presented. Still, a critical component that is mandatory to realize a fully functional system has not been addressed by any of the proposed FC power generation systems: Embedded monitoring and diagnosis for FC stacks.

So far, measurement instruments for impedance spectroscopy and voltammetry have been used in research laboratories to characterize and diagnose FC systems [44, 45]. These precision instruments are costly and bulky, as they are meant to test a wide variety of electrochemical based systems. By measuring the cell output impedance, techniques to evaluate effects such as drying and flooding have been developed [46], which are derived from Frequency Response Analysis (FRA) methodology. By using FRA technique the impedance of a system can be measured at different frequency values within a given spectrum of interest [47]. FRA technique allows the characterization of different electrochemical processes that are produced at different timescales. For example, in a PEMFC, the high-frequency response depends mainly on the electrode kinetic response, while the low-frequency response can be attributed to water management [48]. An equivalent electrical circuit of the system can be identified by computing the real and imaginary components of the impedance [21]. In addition, since the AC perturbation signal has small amplitude, it can be superimposed on a DC signal allowing the measurement of the system at different operating points.

The proposed measurement system is based on a technique known as lock-in amplification (LIA), which allows very accurate and precise ac measurements, even in the presence of high noise levels. This is a fundamental requirement since the FC

output voltage contains ripple due to the effect of the converter switching frequency and the auxiliary equipment that are also supplied by the FC. The objective of this work is to implement this indispensable instrument with a simple hardware architecture and low power consumption, so that it can be easily integrated as part of the FC control system or embedded in the FC power conditioning stage. By doing so, advanced features such as real-time monitoring and diagnosis will be available as part of the FC power generation system. The complete development of the EFRA is described in Chapter 5.

In Chapter 6, a summary of the research, including innovative theoretical analysis, advanced simulations, and state-of-the-art experimental prototyping, as well as the major contributions of the research are presented.

Successful development of the proposed system requires mastery of the following sub-disciplines: FC technologies - steady and dynamic behavior, control, modeling, and experimental operation of the system; Advanced power electronics - converter topologies (dc-dc and dc-ac conversion), advanced modulation techniques, linear and non-linear control (variable structure); Digital signal processing - fixed point DSP programming, frequency and impedance analysis, digital filtering; Design of power devices and components - design of high frequency transformers, inductors, isolated drivers, high-current high frequency PCB, and snubbering techniques; Analog and digital electronics - low-voltage high-current electronic loads, lock-in amplification techniques and industrial communication protocols; As well, it is crucial to understand the type of loads involved in stationary applications (i.e., non-linear with high crest factor), the usage profile of those loads, and Simulation platforms (S-functions and Simulink-PLECS).

Chapter 2

High-Efficiency Low Switching Stress Isolated dc-dc Converter

Fuel Cells stacks are low-voltage high-current power systems that provide unregulated dc output voltage. A power converter that transforms this low voltage into standard 120V 60Hz or 220V 50Hz is required to supply any commercial electrical apparatus (i.e. appliances). There is a general consensus about the importance of galvanic isolation from the main power source (FCC Class A), especially for grid connected systems FEC05. Hence, the power converter should not only boost the voltage but also provide galvanic isolation to enhance safety.

This chapter begins with the study of isolated dc-dc power converters to elevate the FC voltage with a view to select a suitable topology. As will be seen, the full-bridge forward converter is the preferred option, which can be operated in soft switching and makes better utilization of the transformer core. The power loss mechanisms namely, conduction losses, switching losses, and reverse recovery losses are investigated for the selected topology in traditional hard switching and Zero Voltage Switching (ZVS) operation, including undesired effects such as transformer ring-

ing. The analysis is carried out using Piecewise Linear Electrical Circuit Simulation (PLECS) in Matlab and Simulink environments. In order to improve the efficiency of the power converter, a modified soft switching topology is proposed to achieve maximum performance and high efficiency, taking into consideration the voltage regulation nature of the polymer-electrolyte FCs. As a result, reduction in conduction losses in the MOSFETs and reverse recovery in the output rectifiers are achieved while minimizing transformer ringing. A special right aligned modulation is developed as part of the converter switching sequence. A detailed analysis of the behavior of the proposed converter is presented including all the switching instants and effects involved in efficiency gains. Two state-of-the-art prototypes were developed and employed to provide experimental validation of the proposed modified topology. As well, comparative efficiency measurements were performed to highlight the efficiency gains under different loading conditions.

2.1 Input Side Topology Selection

Five basic hard switching topologies that provide both dc-dc boost and isolation are discussed in this section: flyback, forward, push-pull, half bridge, and full bridge. Isolated dc-dc converters can be categorized as unidirectional and bidirectional transformer core excitation. The unidirectional converters are flyback (derived from the basic buck-boost basic topology) and forward (derived from the basic buck topology). On the other hand, push-pull, half bridge, and full bridge topologies belong to the bidirectional category (all derived from the basic buck topology) [40]. Since the flyback converter is only suitable for very low power applications, it is not considered for residential power applications. The forward topology, also suitable for low power conversion, is also discarded due to its low switch utilization and the need for a mag-

netization reset circuit (with its associated power loss). Converters with bidirectional core excitation make better use of the transformer magnetic properties at the expense of additional switches. Fig. 2.1 shows a simplified circuit schematic for these converters. From the viewpoint of driver requirements, push pull topology (Fig. 2.1(a)) is undoubtedly an excellent option since both MOSFET source terminals are grounded. However, in high power applications, the push-pull topology suffers from transformer saturation due to windings asymmetry and slight imbalance in the excitation. This makes the push-pull topology an impractical option. At a glance, the attractive simplicity of the half-bridge topology (Fig. 2.1(b)) seems to be the next logical option. Nevertheless, in-depth evaluation indicates that the switches must handle twice the current due to the split capacitor bank, a true challenge for a printed circuit layout, transformer design, and dc link snubbers, with the additional disadvantage of higher turns ratio and significant ringing due to parasitics in the transformer. The full-bridge topology (Fig. 2.1(c)) is perhaps the most suitable solution, even though 4 switches are required [49]. In full-bridge topology, the equivalent on resistance of the MOSFETs ($R_{ds_{ON}}$) must be taken in to consideration to keep conduction power losses within acceptable levels, specially since the FC voltage is low and current levels high. As well, full-bridge topology presents the additional advantage of soft switching transition capabilities.

2.1.1 Rectification Method Analysis

The galvanic isolation of the dc-dc power converter is obtained by means of a high frequency transformer. As a general rule, transformer design is constrained by the output power requirement within a given specified regulation. Transformer efficiency, limited by losses in the magnetic core and the windings, is an important requirement

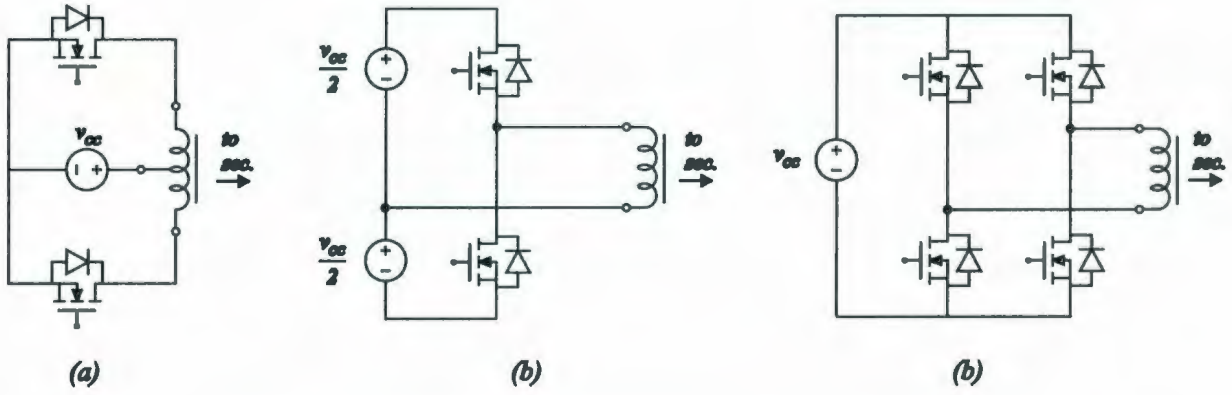


Figure 2.1: Simplified circuit schematic for input topologies.

in FC power systems. As well, the allowable increase in temperature due to power losses must be addressed once the operating environment is defined. Physical constraints such as volume, weight, and shape make transformer design trade-off even more intricate. Finally, a cost-effective transformer is of primarily importance in FC power systems. Equation (2.1) provides an excellent illustration of the points mentioned above [50] as a function of the apparent power, which is defined as $P_t = P_o + P_{in}$, where P_o =output power and P_{in} = input power.

$$W_a \; A_c = \frac{P_t \; 10^4}{B_{ac} f \; J \; K_f \; K_u} \tag{2.1}$$

where,

W_a = window area, cm^2

A_c = effective cross section of the core, cm^2

P_t = apparent power, watts

B_{ac} = alternating current flux density, tesla

f = frequency, Hz

J = current density, amps per cm^2

K_f = waveform coefficient

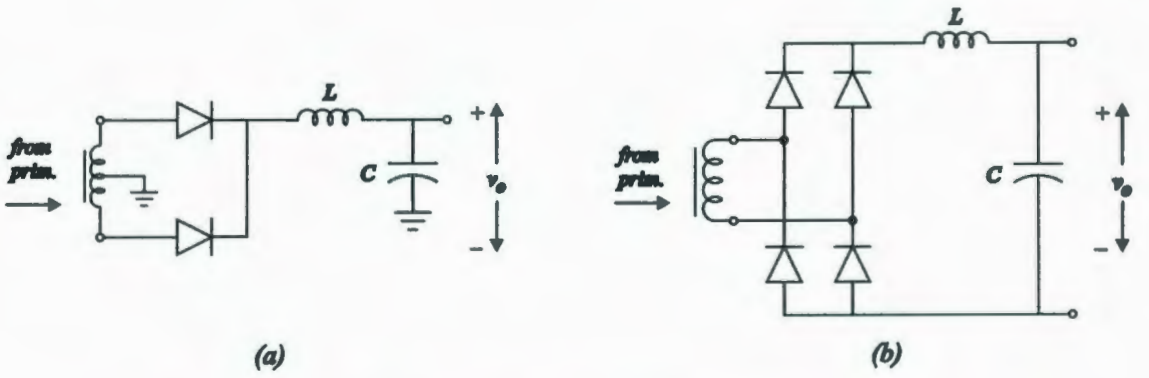


Figure 2.2: Simplified circuit schematic for output topologies.

K_u = window utilization factor

For the studied isolated dc-dc converter, the transformer secondary can be arranged in two basic ways depending on the rectification method as shown in Fig. 2.2. As described in (2.1) the core and windings are capable of handling a certain apparent power P_t which is affected by the rectifier selection as follows: The full wave rectifier presented in Fig. 2.2(a) requires a center tap, which creates a current interruption in one of the windings during positive and negative half cycles. This effect increases P_t by 20.7% [50] and hence the area product $W_a \times A_c$, leading to a bigger transformer core compared to a full bridge rectifier. Another way of looking into this effect is by using the window utilization factor criteria. As can be seen in (2.1) a window full of copper ($K_u = 1$) not only helps to increase current density but also reduces the area product (smaller transformer core). In a center tapped transformer, the secondary windings are used one at a time. Thus, the window is always occupied by a winding which is not used, resulting in a low effective window occupation factor K_u. Finally, the use of center tap not only reduces the transformer utilization but also doubles the voltage rating of the diodes and hence reverse recovery losses.

In general, center tap transformers are preferred for low voltage applications where the additional drop introduced with a full-bridge rectifier is unacceptable (e.g., con-

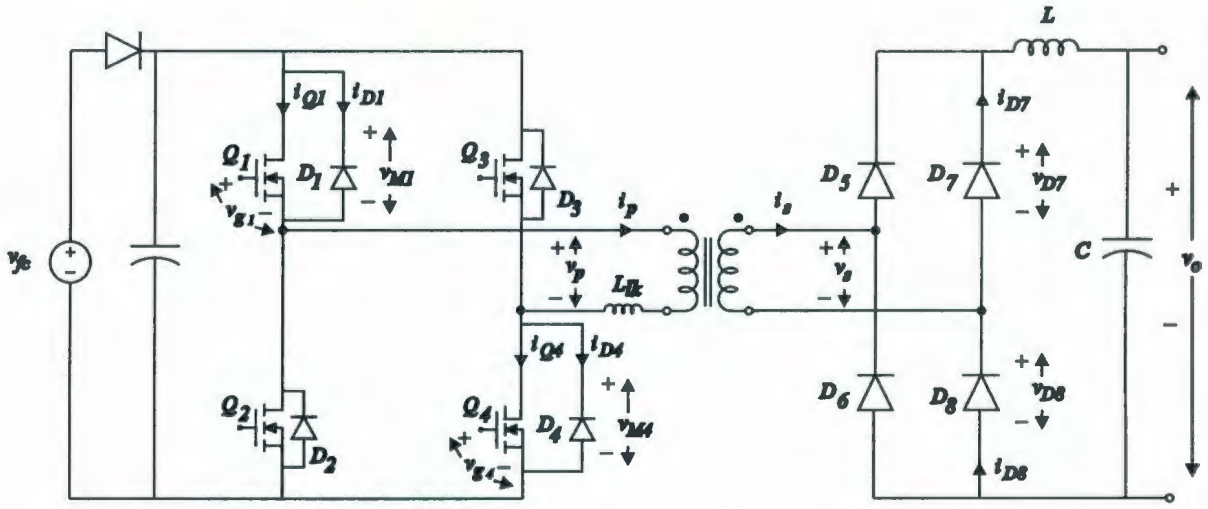


Figure 2.3: Simplified circuit schematic for the full-bridge dc-c topology with phase shift PWM.

sumer electronics power supply). In the studied FC power converter for residential application, the output voltage of the isolated dc-dc converter ranges between 210-250Vdc for 120Vac utility and 380-450Vdc for 220Vac utility. The high voltage requirement can be achieved using a full bridge rectifier while taking full advantage of the transformer magnetic properties and construction simplicity. In this case, the efficiency of the system is affected by the conduction losses of two extra diodes. From the above discussion, a combination of full-bridge topology and full-bridge rectifier is selected to provide voltage boost and galvanic isolation. Figure 2.3 shows a simplified circuit schematic of a basic dc-dc power converter topology for stationary applications.

2.2 The Full-Bridge Forward Converter with Phase-Shift PWM

The selected topology shown in Fig. 2.3 is not without technical complications. The following discussion presents the most important technical challenges related to the

topology. The analysis includes the origin of power losses in both the full-bridge and the rectifier stage under phase-shift PWM operation.

The analysis starts with MOSFET M_1 with its respective body diode D_1 when the converter is operated with phase shift PWM under heavy loading conditions. Figure 2.4 shows conceptual switching waveforms for Q_1 and D_1 during a full cycle period including gate signals, drain-to-source voltages, and currents for the MOSFETs N-channel and the body diode. The aim of this figure is to highlight both switching and conduction losses, as well as the effect of dead time insertion between each complementary pair of switches. Turn on and turn off switching losses for Q_1 are related to rise and fall times, which are associated with the input and output capacitances of the MOSFET. The instantaneous power loss can be calculated as the product of v_{ds} and i_{mos} during the switching transition. A reduction in the rise and fall time is required to decrease losses. This is achieved by means of rapid filling and removal of total gate charge of the MOSFET. This, of course, increases the current rating of the drivers. As the on time is reduced to the minimum possible, a negative effect appears in the form of ringing produced by the PCB stray inductances and inter-winding capacitance of the transformer [51], which is discussed later in this section. As well, shoot through due to high dv/dt is another undesirable effect when transition times are reduced. Figure 2.4 shows turn-on and turn-off voltage (v_{M_1}) across MOSFET M_1 and current transitions (i_{M_1}) at t_2 and t_4 instants. As can be seen, the turn-on transition occurs under zero current switching (ZCS) and turn-off transition is hard switching for the analyzed case. Dead time insertion between the upper and lower side MOSFETs is illustrated in the intervals $t_1 - t_2$ and $t_4 - t_5$.

Conduction losses depend on the MOSFETs ON-resistance $R_{ds_{ON}}$ and the RMS current flowing through the switches. As can be noted in Fig. 2.4, Q_1 has conduction losses during the entire on time period, $t_3 - t_4$ interval, which is almost 50% for phase

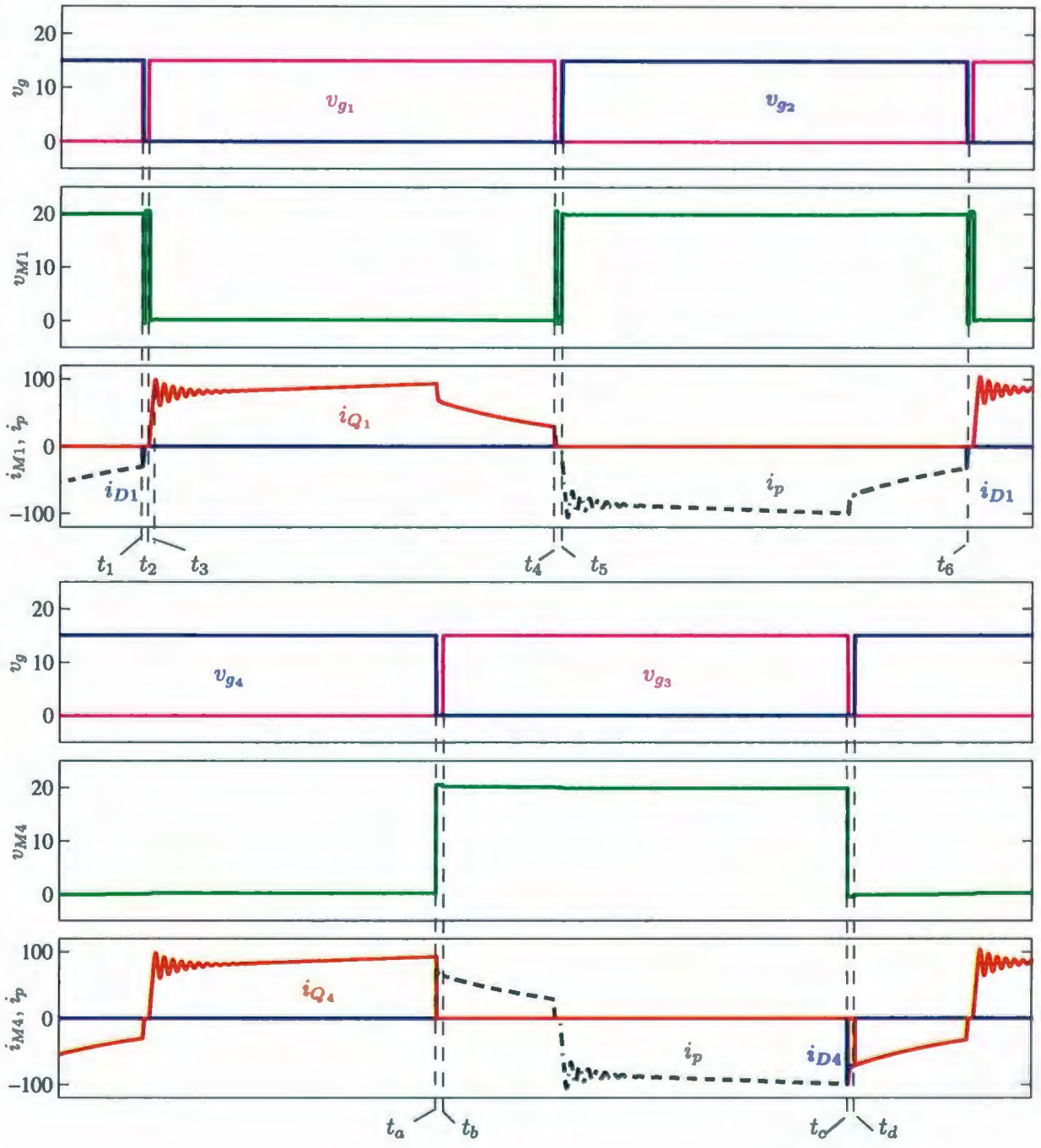


Figure 2.4: Full-bridge forward converter in hard switching operation: voltage and current waveforms for upper M_1 and lower M_4 MOSFETs .

shift PWM).

In addition to the switching and conduction losses in the MOSFETs, reverse recovery and conduction losses in the body diode D_1 must be considered. In order to illustrate the power losses, Fig. 2.4 presents the behavior of diode D_1 acting as voltage clamp within the dead time interval at $t_1 - t_2$. Diode turn-on or forward bias losses are neglected due to the intrinsic fast response of the devices. The conduction losses can be calculated by multiplying the forward conduction voltage by the forward current starting at t_1 until the current reaches zero. As can be seen in Fig. 2.4, the current decreases linearly and sharply during the clamping process (between $t_1 - t_2$ interval). The current slope (di/dt) depends on the transformer leakage inductance L_{lk}. When the current reaches zero, the voltage across the diode is reversed but an inverse current takes place due to the reverse recovery charge Q_{rr} as shown conceptually in Fig. 2.5(a). The reverse recovery charge Q_{rr} indicated in this graphics is directly related to the power losses as follows,

$$P_{loss} = Q_{rr}\ V_R\ F_{sw} \tag{2.2}$$

where,

V_R = reverse applied voltage

F_{sw} = switching frequency

Figure 2.5(b) shows the reverse recovery charge Q_{rr} as a function of di/dt for a low-voltage high-current MOSFET body diode (IRFB4310) [52]. The figure shows the depedence of the reverse recovery charge and hence the total reverse recovery losses on di/dt and operating temperature. The exact analysis applies for M_2 that combines Q_2 and D_2.

While switch Q_1 and diode D_1 present hard switching behavior, switch Q_4 and

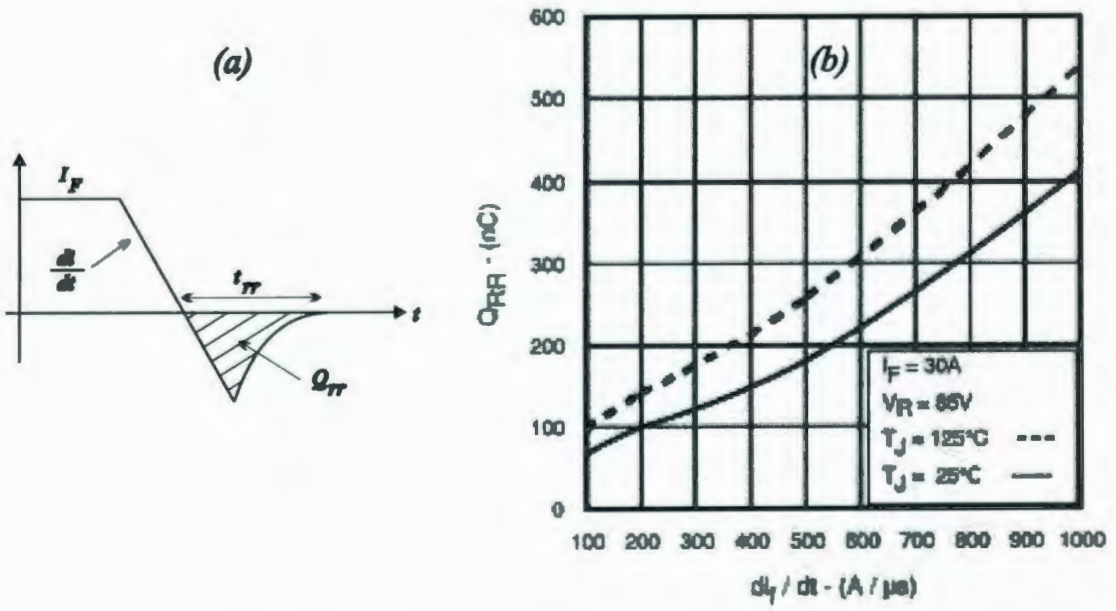


Figure 2.5: Reverse recovery charges.

diode D_4 show reduced switching stress when operated with phase shift PWM as explained below. The phase difference between the leg composed by Q_1 and Q_2, and Q_3 and Q_4 produce a current flow through the transformer that lags the voltage across the primary of the transformer. This results in Zero Votage Transition (ZVT) in the switching waveforms of Q_2 and Q_4 during turn-on as shown in Fig. 2.5 for M_4. In this case, D_4 clamps the voltage during the dead time interval $t_c - t_d$ creating a zero voltage condition across Q_4 at turn-on instant t_d. The same effect occurs with D_3 and Q_3, which can be inferred from the interval $t_a - t_b$ in Fig. 2.5. Hence, Q_3 and Q_4 are able to turn-on in a soft switching fashion at t_b and t_d respectively . As well, reverse recovery losses are avoided in D_3 and D_4 since no reverse voltage is applied across them during the periods of forward conduction. Conduction losses in D_4 (and D_3) are function of the forward conduction voltage and forward current i_{D_4} during the dead time intervals.

Another important component of power losses occurs at the output of the dc-dc

power converter. The output stage comprises D_5, D_6, D_7, and D_8 which are arranged as a full bridge rectifier connected to the converter LC output filter. Since the pairs of upper diodes D_5 and D_7, and lower diodes D_5 and D_7 present the same behavior, only D_7 and D_8 are examined. The current and voltage waveforms are presented in Fig. 2.6 where both conduction and reverse recovery losses can be identified. The conduction interval for D_7 is $t_3' - t_7$ and the reverse recovery instants are t_3 and t_7. The current rate of change in the rectifier recovery process in the interval $t_1 - t_3$ is high. The rate is determined by the transformer leakage inductance L_{lk} and the input voltage, which results in hig reverse recovery charges Q_{rr}. As well, the blocking voltage is also large and aggravated by ringing, so significant power losses are produced determined from (2.2). Finally, diode D_8 conduction interval begins at t_c and finishes at t_b' of the following cycle and the reverse recovery instant is t_b'.

To complete the analysis of the full-bridge topology, other important aspects related to the transformer parasitic effect must be considered. When the transformer leakage inductance and winding capacitance are included as part of the transformer model, severe transient effects appear in the form of high frequency oscillations in both the secondary and primary of the transformer. Ringing has several negative impacts in the power converter. First, the maximum reverse voltage rating of the rectifier diodes must be increase to ensure that the peak of the ringing voltage does not exceed the breakdown voltage. In general, a snubber circuit is included (RCD type) to limit the peak voltage of the ringing creating additional losses and circuit elements in the converter. As well, other undesirable effects like EMI and over voltage between transformer windings are experienced. Ringing is propagated throughout the converter including the drivers (coupled through the drain to gate or source to gate capacitance). Excessive ringing may produce false triggering with irreparable consequences to the power devices.

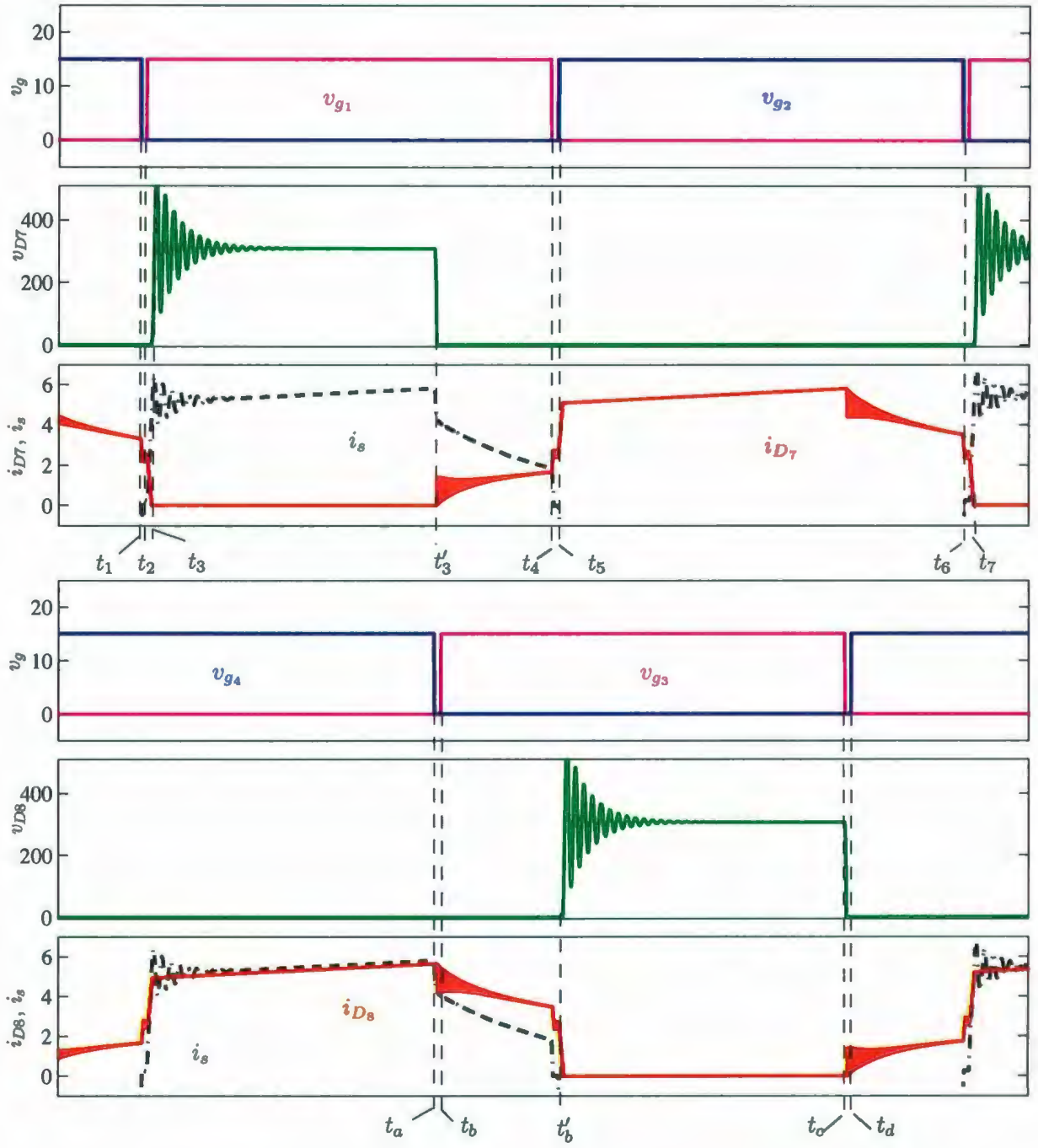


Figure 2.6: Full-bridge forward converter in hard switching operation: voltage and current waveforms for upper D_7 and lower D_8 diodes .

In order to clarify the origin of ringing, the current and voltage waveforms on the primary and secondary of the transformer must be examined. Figure 2.7 shows the resulting primary and secondary waveforms when the converter is operated using phase shift PWM under the same operating conditions presented in Fig. 2.4 and Fig. 2.6. It can be noted in this figure that the primary voltage v_p waveform in Fig. 2.7(a) is not necessarily reflected on the secondary voltage v_s (Fig. 2.7(b)). When the primary voltage is applied at t_0, the rectifier in combination with the filter inductor forces a zero voltage state across the secondary of the transformer until the secondary current reaches the current level of the filter inductor at t_1. The leakage inductance experiences a rapid current charge while the zero voltage state at the output of the transformer is present. When the primary current reflected to the secondary matches the filter inductor current, the secondary zero voltage state is cleared producing a high dv/dt edge which violently excites the transformer parasitics resulting in the oscillations.

The actual resulting effect of the oscillations can be investigated by replacing the transformer with the equivalent model shown in Fig. 2.8. This lump parameter model includes dc and skin effect copper losses (R_c), leakage inductance resulting from the leakage magnetic flux (L_d), capacitance between windings C_w, and core losses represented by R_m. In this work, the parameters are estimated from a high frequency transformer constructed using a 3F3-E55/28/25 ferrite, copper shim for a two turns primary (foil winding), and 26 turns using stranded wires. The voltage ringing on the transformer secondary is illustrated in Fig. 2.9 along with the main waveforms in the converter and occurs when the primary current reflected to the secondary matches the current level of the inductor. The peak level of the oscillations and damping effect depend on the characteristics of the transformer and generally require a snubber circuit to dissipate the oscillation energy as mentioned earlier. For a high efficiency

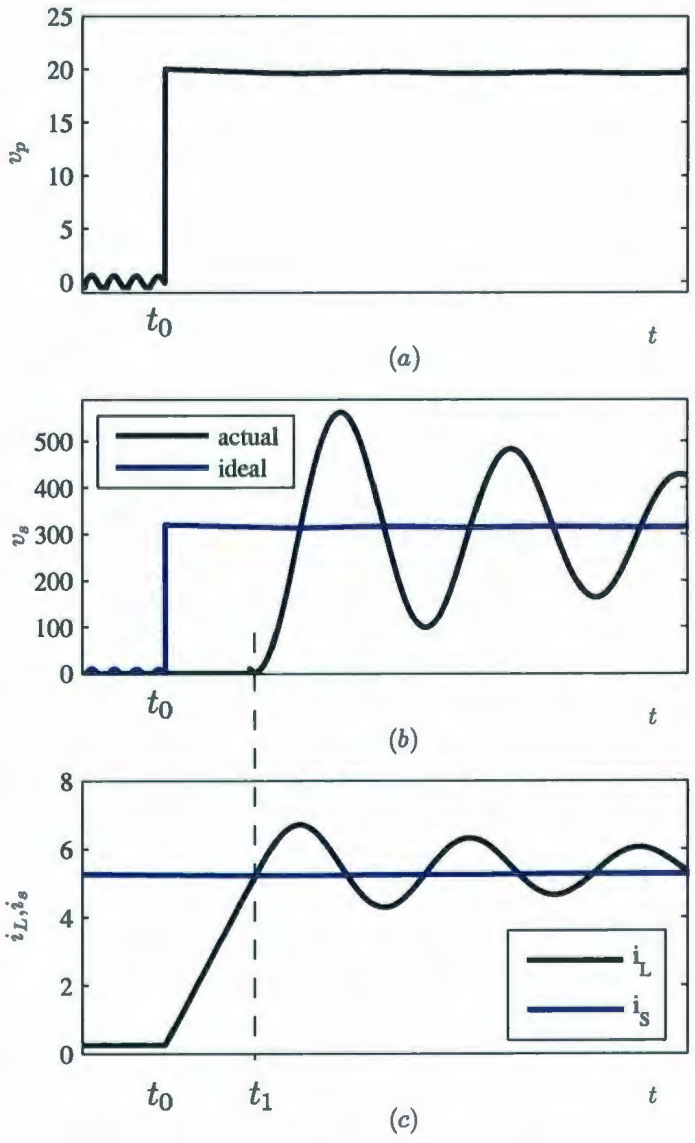


Figure 2.7: Full-bridge forward converter ringing effect: a) transformer primary voltage, b) transformer secondary voltage (ideal and actual), and c) transformer secondary and inductor current.

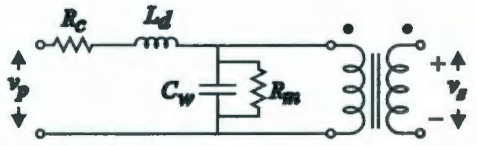


Figure 2.8: High frequency transformer lump model.

transformer (low current density, no skin effect, and low core magnetization) the peak of the oscillation may double the actual output voltage.

When the power converter is operated in discontinuous conduction mode, the ringing is still present but the oscillations are a result of the voltage step directly applied by the action of the MOSFETs. In this case, the turn-on time plays an important role in defining the severity of the ringing which affect the system efficiency (higher switching losses). In other words, increasing the turn-on time will only reduce the ringing with light loading conditions (discontinuous conduction mode) but dramatically increase the switching power losses under medium to heavy loading conditions.

From the discussion above, the mechanisms to reduce ringing are identified as follows:

- avoid a zero voltage state on the transformer secondary during on-state intervals;
- reduce the matching current level between the leakage and output inductor;
- increase the turn-on time in discontinuous conduction mode.

It can be therefore concluded that in order to improve the efficiency of the converter and reduce stresses in the switches, a more advanced topology is required. In Section 2.4, the above mechanisms are considered in the development of a topological modification to overcome ringing problems and reduce reverse recovery losses.

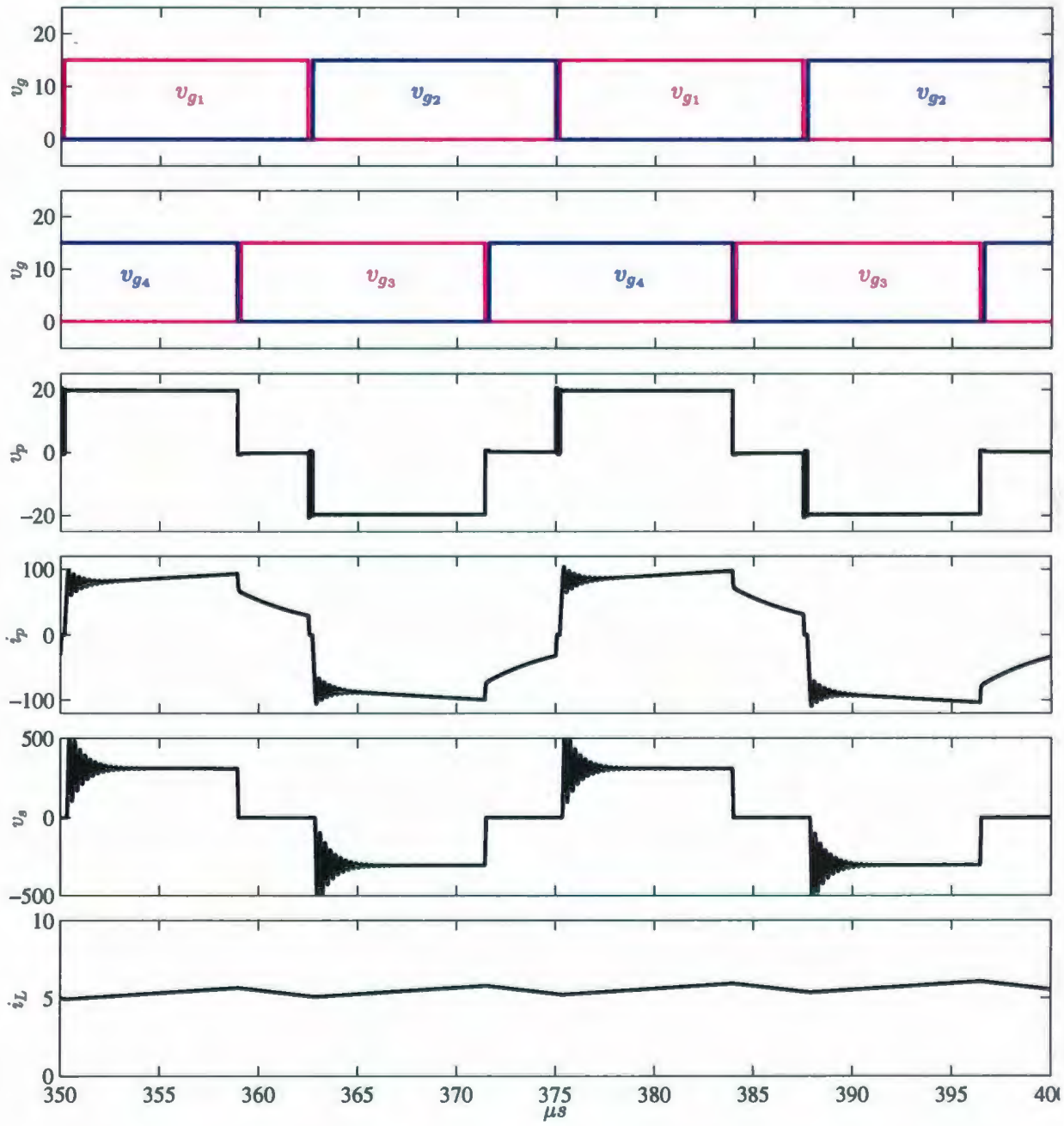


Figure 2.9: Full-bridge forward converter in hard switching operation: main primary and secondary voltage and current waveforms.

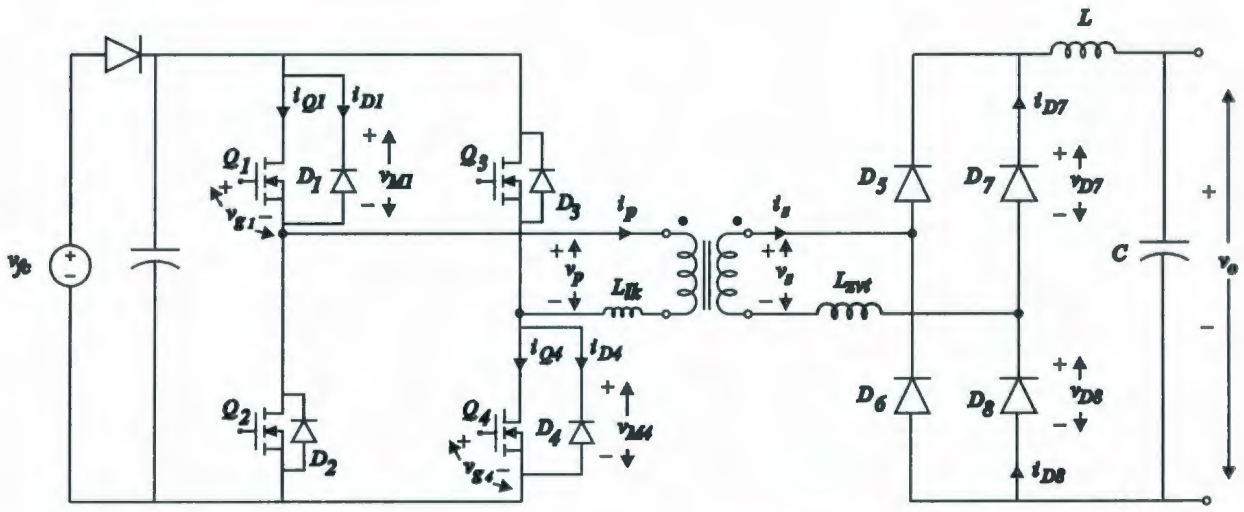


Figure 2.10: Simplified circuit schematic for the full-bridge zero voltage switching topology.

2.3 Full-bridge Forward Converter with Zero Voltage Switching

A detailed analysis of the switching waveforms of the traditional full-bridge topology have been presented in Section 2.2 highlighting switching, conduction, and reverse recovery losses for each device. As well, the nature of the oscillations produced by the transformer parasitics during commutation was investigated. The full-bridge topology operated with Zero Voltage Switching (ZVS) is an attractive alternative to reduce switching and reverse recovery losses [53–55]. Figure 2.10 shows a simplified circuit schematic of the full-bridge ZVS where an inductor L_{zvt} is included in series with the transformer secondary. The effect of L_{zvt} is reflected to the primary of the transformer using the primary and secondary turns ratio.

Unlike a traditional ZVS, the power converter has low input voltage (high current) and high output voltage (low current), which explains the choice of a secondary auxiliary inductor in Fig. 2.10. The objective of this inductor is to create

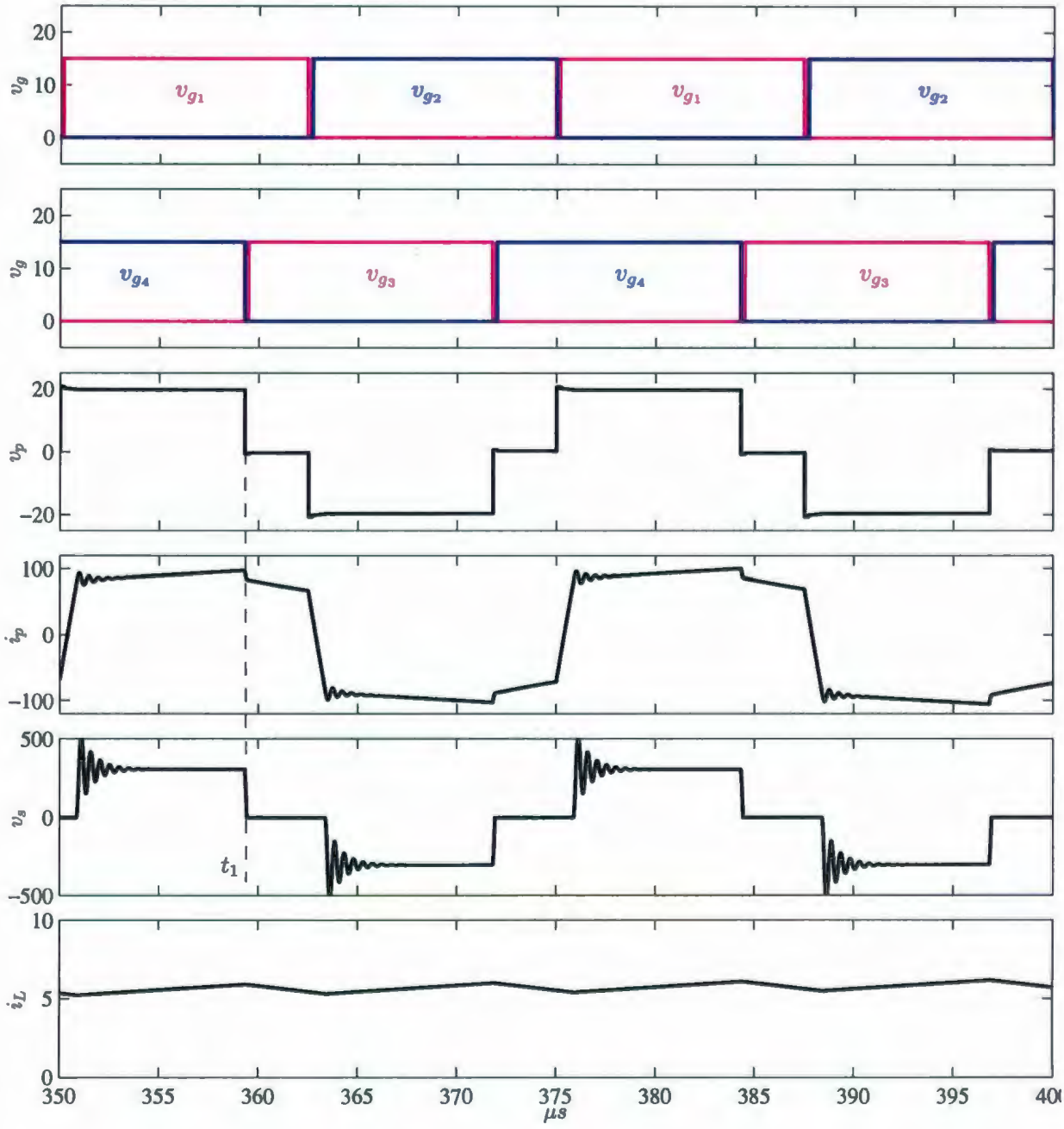


Figure 2.11: Full-bridge forward converter in ZVS operation: main primary and secondary voltage and current waveforms.

uninterrupted current flow in the primary of the transformer in order to generate zero voltage turn-on transitions for the MOSFETs. As well, the inductor limits di/dt in the output rectifiers, resulting in a reduction in reverse recovery losses. Phase shift PWM is employed to modulate the converter and the ZVS effect is achieved due to the dead time insertion between the upper and lower commutation sequences. Figure 2.11 shows the switching sequences and the main waveforms in the converter including gate signals v_g, transformer primary voltage v_p and current i_p, transformer secondary voltage v_s, and filter inductor current i_L.

An essential change in the voltage and current waveforms of MOSFET M_1, comprising Q_1 and D_1, is produced when the converter is operated with ZVS, which is depicted in Fig. 2.12. As can be seen, Q_1 turns-on at t_1 with ZVT when D_1 is in conduction. The current in Q_1 ramps up until it reaches the filter inductor current reflected to the primary at t_2. The turn-off instant for Q_1 is t_3, where it experiences a hard switching transition. The conduction interval is therefore given by $t_3 - t_1$. Diode D_1 behaves like a voltage clamp during the dead time interval $t_5 - t_6$. like in the full-bridge analyzed in Section 2.2. However, the current decreases slowly compared to the previous converter, which is explained by a higher equivalent series inductance $L_{lk} + N^2 \times L_{zvt}$ in the primary of the transformer. This provides additional time to turn-on $Q1$ before the diodes complete the reverse recovery process. Now, the diode does not suffer reverse recovery losses and the turn-on transition in the MOSFET occurs under zero drain-to-source voltage, improving the efficiency of the converter. The behavior of the lower side MOSFET M_2 (Q_2 and D_2) is similar to the above description.

The second leg of the converter comprising MOSFET M_3 (Q_3 and D_3) and MOSFET M_4 (Q_4 and D_4), presents a similar behavior as the full-bridge topology with phase shift PWM. The transitions in M_4 for phase-shift PWM and ZVS are the

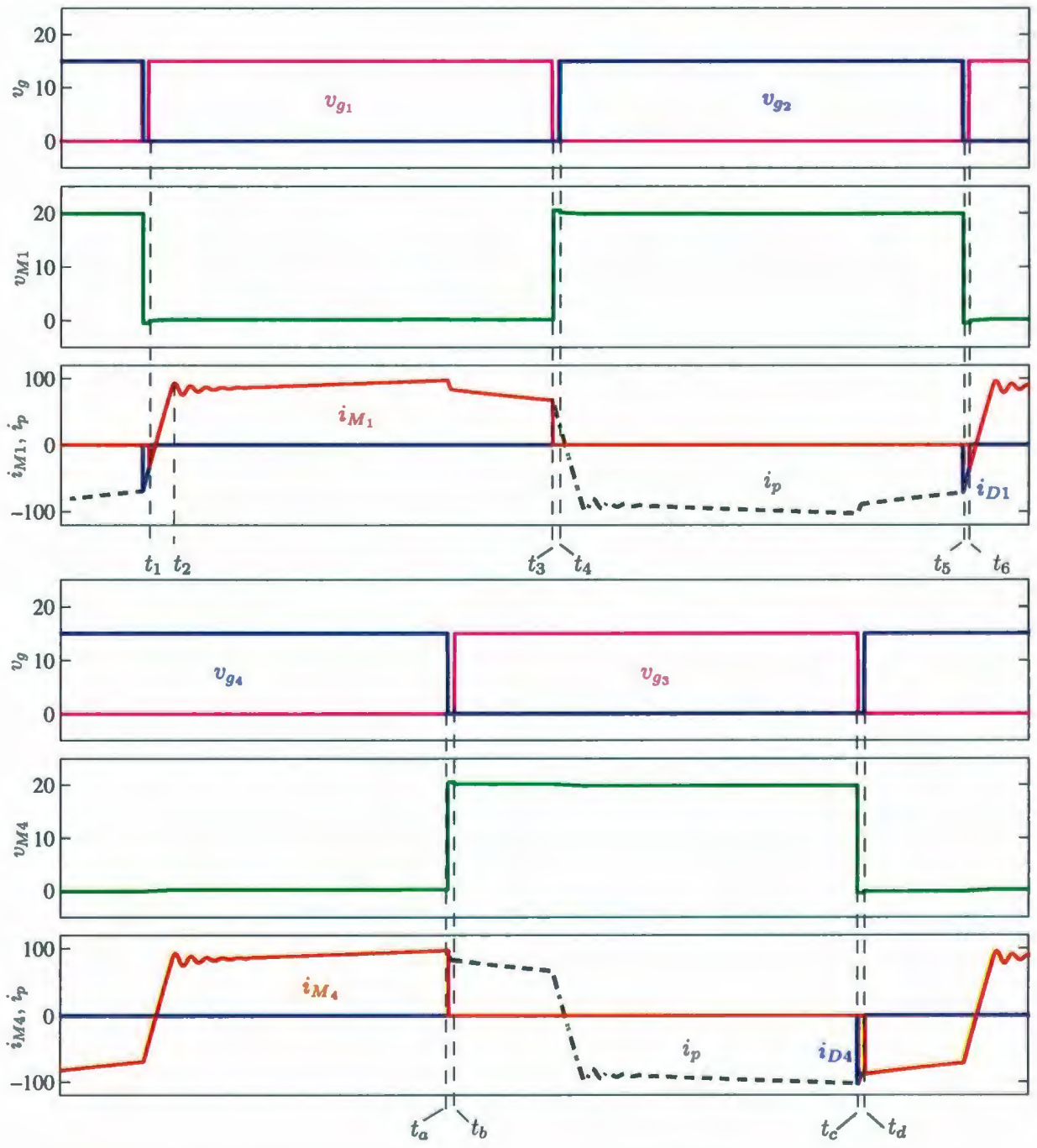


Figure 2.12: Full-bridge forward converter in ZVS operation: voltage and current waveforms for upper M_1 and lower M_4 MOSFETs.

same except for the fact that the current transitions in ZVS are limited by a larger series inductance. As shown in Fig. 2.12, Q_4 experiences hard switching turn-off at t_a and ZVT turn-on at t_d. The conduction interval occurs from t_d to t_a of the next switching cycle. As well, the conduction interval of D_4 occurs during the dead time interval $t_c - t_d$ with no reverse recovery losses.

The limitation in the rate of change of the transformer primary current introduced by the additional inductance L_{zvt} also presents advantages on the rectifier side. The moderate current rate of change helps to reduce the reverse recovery charges Q_{rr}, which is shown in Fig. 2.13. The voltage of the upper diode D_7 clearly reflects the loss of duty cycle in the secondary, which is occurs in the interval $t_1 - t_2$. As well, the reverse recovery losses at t_2 are reduced due to the moderate di/dt slope at t_2. However, the ringing peak voltage in the rectifier remains high. The conduction interval for D_7 is given by $t_3 - t_2$ of the following cycle. The lower side diode D_8 experiences the same reverse recovery conditions as D_7 with moderate di/dt and large ringing peak voltage. Clearly, the efficiency of the rectifier stage is much superior when compared to the phase-shift PWM.

Despite the advantages in terms of turn-on switching and reverse recovery reduction, a number of drawbacks associated with ZVS technique can be identified. Ringing or transformer oscillation, a major problem of the full-bridge topology, is inherited in the ZVS version of the converter. The problem remains unsolved because the zero voltage state on the secondary side of the transformer is not overcome nor addressed by this topology. On the contrary, the zero voltage state is much longer causing a reduction in the effective duty cycle [54, 55]. The zero voltage state in the secondary remains until the primary current reflected to the secondary reaches the filter inductor current level. Hence the pulse width is significantly reduced, affecting the actual power transfer capability of the power converter. This can be explained

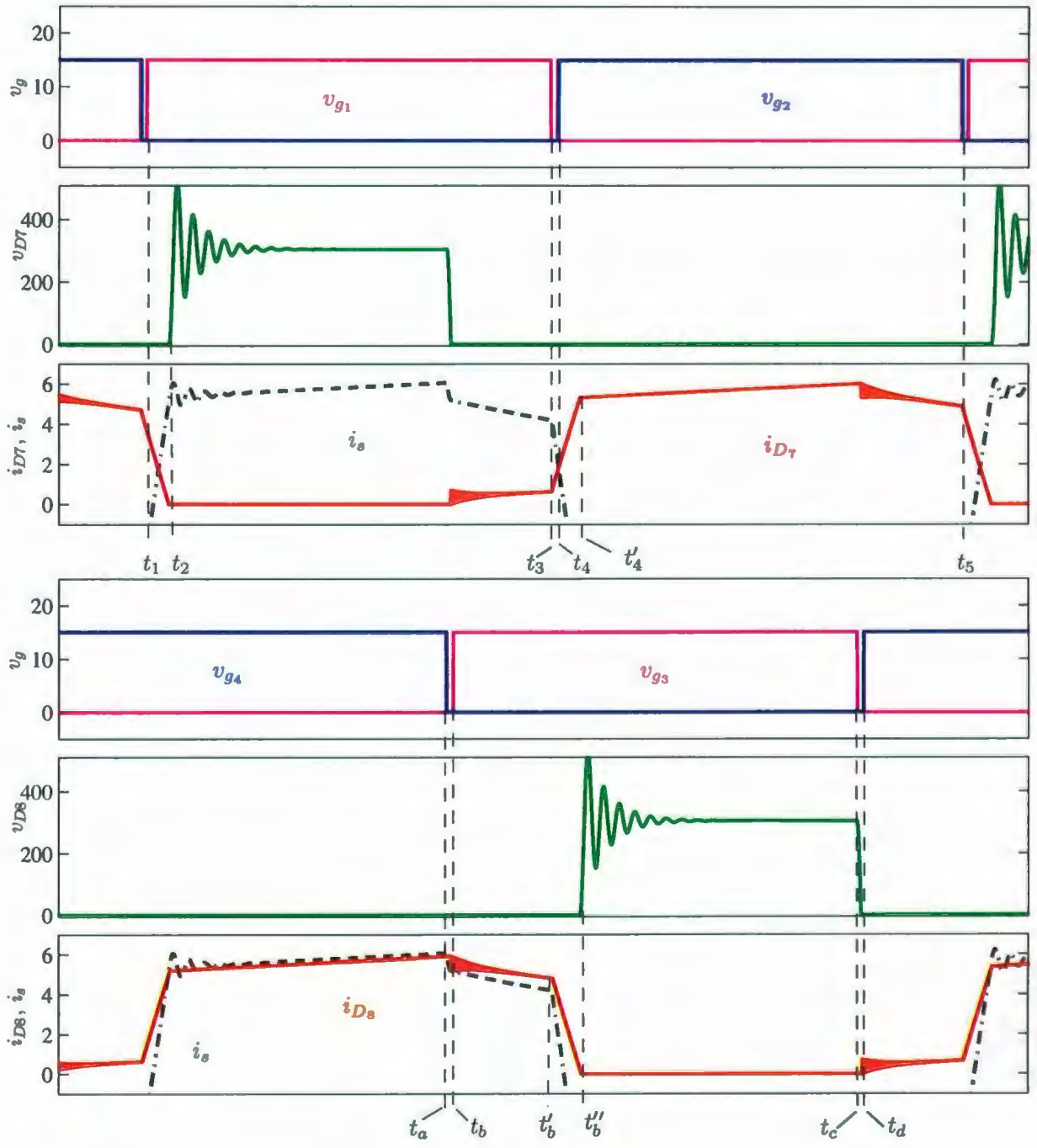


Figure 2.13: Full-bridge forward converter in ZVS operation: voltage and current waveforms for upper D_7 and lower D_8 diodes.

due to the fact that reduced secondary duty cycle results in lower output voltage when compared to traditional full-bridge, even though the duty cycle in the primary is exactly the same.

The wide voltage regulation characteristic of FC power sources presents a severe challenge that makes ZVS unsuitable for FC residential power conversion. Full-bridge ZVS is known to be an effective solution when the input voltage range is narrow [36]. Yet light loading conditions with fixed input voltage may cause the system to operate with hard switching and unnecessary high conduction losses. The combination of a ZVS converter with a FC system results in an unsatisfactory performance because the FC output voltage is highly dependent on the loading condition. The output voltage of a polymer-electrolyte FC under light loading conditions could easily double that of the full loading condition. For example, a commercial Ballard Nexa PEMFC the output voltage ranges between $22 - 50V$ depending on the loading level. Since the profile of energy consumption in residential and other applications varies from no load to full load depending on the time of the day, the FC cell power source is expected to operate over the full voltage range. This leads to a clear violation of the narrow input voltage requirement of the full-bridge ZVS topology. To further clarify this point, Fig. 2.11 presents a case when the duty cycle is around 70%. It can be seen that once the on state is over at t_1, the current in the primary of the transformer continues to flow, producing additional conduction power losses due to the energy trapped in L_{lk} and L_{zvt} inductances. The resulting primary circulating current i_p is not transferred to the output but produces unnecessary power losses. This is worsened when the converter is operated under light loading condition. The output current decreases and the FC voltage increases, pushing the switching transition outside the ZVS operating region. Since the duty cycle is reduced, the circulating current during the off state progressively degrades the efficiency of the

converter as the load decreases.

It is interesting to note that all the advantages of the full-bridge ZVS topology are only manifested with high power conditions. Yet, the transformer ringing problem remains unsolved and so does the reduction of the effective duty cycle. Unfortunately, this converter only shows weaknesses under medium to light loading levels in residential FC power generation so more advanced topologies need to be considered.

2.4 An Advanced Topology of the Full-Bridge Forward Converter

A topological modification of the full-bridge forward converter is proposed as part of this work to reduce switching stress and improve the converter efficiency over the entire range of operation of the system. A key element is introduced in the circuit to reduce the rate of current change di/dt in the rectifier diodes. This change not only reduces the recovery reverse losses in the rectifier but also provides the basis for tackling other critical issues such as switching and conduction losses in the MOSFETs, and transformer ringing. Figure 2.14 shows the circuit schematic where two small inductors (L_a and L_b) are added in series with the upper rectifier diodes (D_5 and D_7). A complete analysis of the switching waveforms for the proposed topology is presented in this section with a view to evaluating switching, conduction, and recovery reverse losses mechanisms for each device.

The proposed topological arrangement is not limited to phase shift PWM or ZVS; the modulation or switching sequence is flexible and the proposed topology is referred to as the full-bridge modified soft switching topology. The selected switching

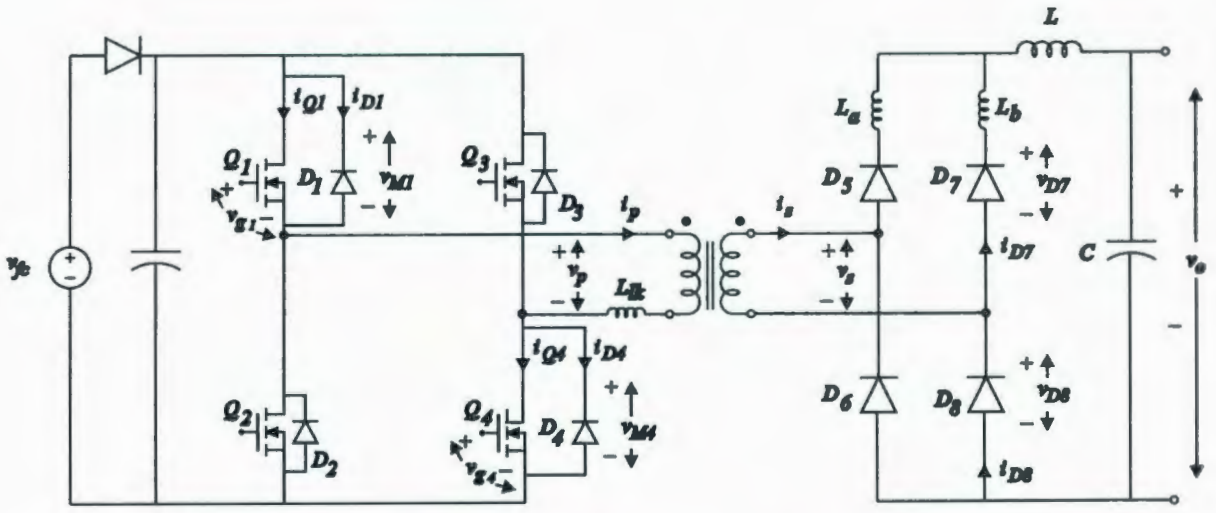


Figure 2.14: Simplified circuit schematic for the modified topology of the full-bridge forward converter.

sequence is presented in Fig. 2.15 and aims to reset the transformer primary current by transferring the energy accumulated in the leakage inductance back to the low voltage dc bus. The gate signals for Q_2 and Q_4 operate with a duty cycle slightly higher that 50% to create a brief zero voltage condition in the primary to ensure ZVS turn-on in both Q_2 and Q_4 (with zero reverse recovery losses in D_2 and D_4). When the zero voltage state is cleared, the energy in the leakage inductance is transferred to the low voltage dc bus through D_1 when Q_2 turns off or through D_3 when Q_4 turns off.

To successfully produce the desired effect, Q_2 (and Q_4) must operate with fixed duty cycle and the driving pulses for Q_1 (and Q_3) must be aligned to the right as depicted in Fig. 2.15 (v_{g_1} and v_{g_3}). Dead time insertion is generated between the upper and lower gate signals. Hence, the duty cycle applied to the primary of the transformer is controlled by Q_1 and Q_3 only.

By eliminating the zero voltage state on the secondary of the transformer, the selected topology presents a unique feature that helps to reduce transformer ringing

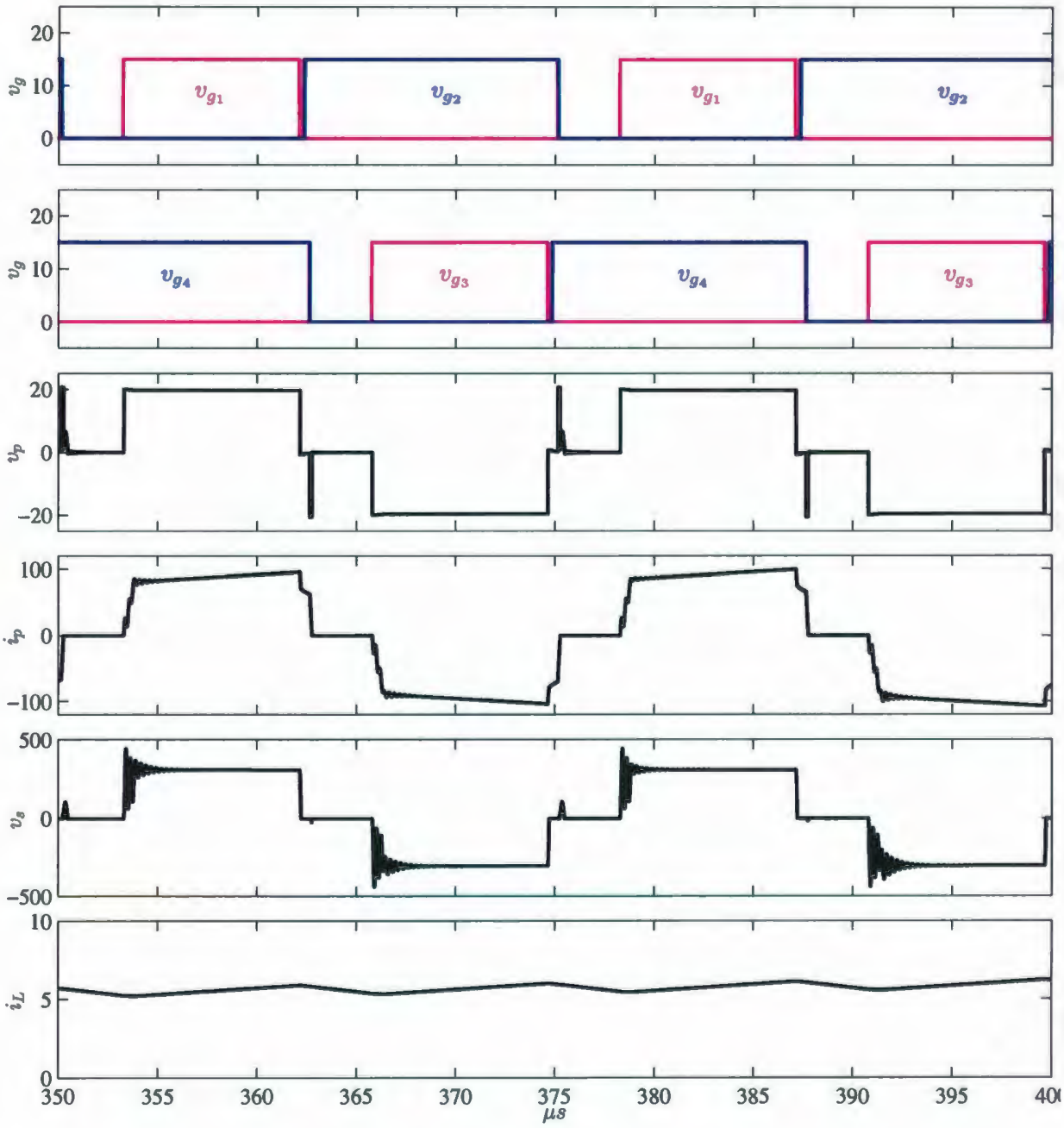


Figure 2.15: Full-bridge modified soft switching converter: main primary and secondary voltage and current waveforms.

problems. As can be seen in Fig. 2.15, the turn-on edge on the primary voltage v_p is partially reflected to the transformer secondary v_s, hence increasing the effective duty cycle and reducing transformer ringing.

By following the same process as the previously analyzed converter, the waveform of MOSFETs M_1 comprising Q_1 and its respective body diode D_1 is first investigated when the converter is operated under a heavy loading condition. Figure 2.16 shows the switching waveforms for M_1 and M_4 during a full cycle period, including the gate voltages (v_{g_1} and v_{g_4}) and drain-to-source voltages (v_{M1} and v_{M4}), and currents for the MOSFETs N-channel (i_{Q1} and i_{Q4}) and the body diodes (i_{D1} and i_{D4}).

An interesting effect in the current rate of change di/dt of Q_1 can be identified in the $t_1 - t_2$ interval, which is produced by the action of the inductors L_a and L_{lk}. It can be seen that at turn-on the current in Q_1 starts at zero at t_1 and slowly ramps up until it reaches the current level of the filter inductor reflected to the primary i'_L at t_2. The approximate slope of Q_1 current within $t_1 - t_2$ is given by $V_i/(L_{lk} + L'_a)$, where L'_a is the auxiliary inductor L_a reflected to the primary ($L_a << L$). This transition presents a quasi-zero current turn-on switching (ZCS) for Q_1 with reduced switching losses. The turn-on losses under ZCS are highly dependent on the MOSFET output capacitance $Coss$ and input voltage as given by,

$$P_{loss_{COSS}} = \frac{1}{2}\, C_{oss}\, F_{sw}\, {V_R}^2 \tag{2.3}$$

Clearly, the main factor in (2.3) is the converter input voltage ${V_R}^2$. Since the converter input voltage ranges between $22 - 50V$, the power losses associated with C_{oss} during turn-on are low when compared to typical $400V$ applications (i.e., telecom and server power supplies).

From instant t_2, i_{Q_1} continues to ramp up with slope $V_i - V_o'/(L_{lk} + L'_a + L')$ until

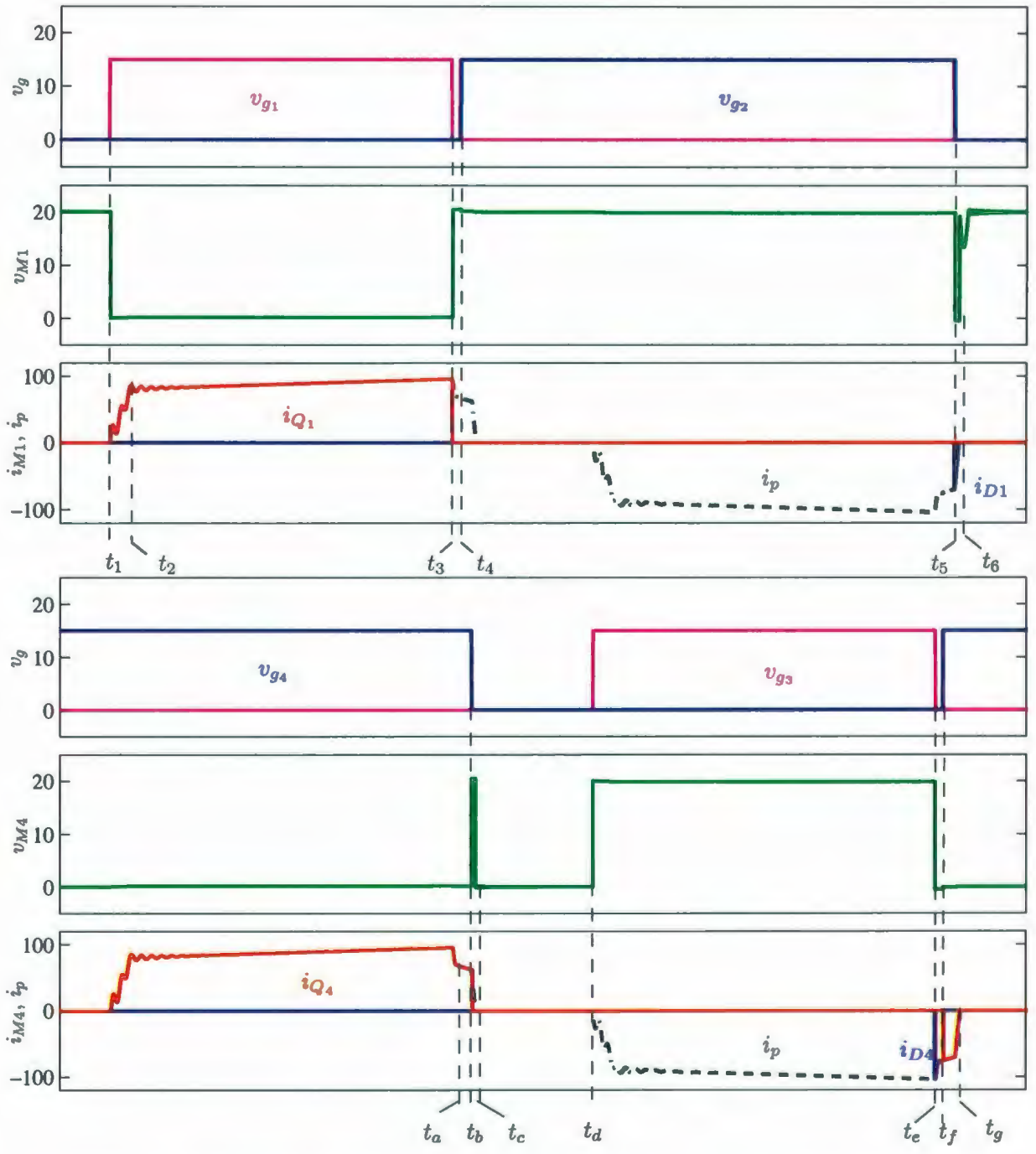


Figure 2.16: Full-bridge modified soft switching converter: voltage and current waveforms for upper M_1 and lower M_4 MOSFETs.

t_3, where Q_1 turns-off at under hard switching conditions like in ZVS. Later, starting at t_5 the body diode D_1 has a brief conduction interval $t_5 - t_6$ to return the energy of the leakage inductance L_{lk} to the input dc bus. The transformer primary current i_p is therefore reset to zero. The reverse recovery losses of D_1 is determined by L_{lk}, the forward conduction current and the input voltage V_i. In spite of the reverse recovery losses, one of the key advantages of forcing the transformer circulating current to zero is to minimize the conduction losses in the MOSFETS whic far outweigh the reverse recovery losses. As can be seen in Fig. 2.16, the conduction interval for Q_1 is given by the duty cycle of v_{g_1}. Unlike ZVS, the proposed concept prevents circulating current in the transformer and allows power to be transfered during the entire conduction interval. This is a key requirement in low-voltage, high-current applications where the conduction losses are substantial. Recall that conduction losses are given by $P_{loss_{CON}} = R_{ds_{ON}}\ {i_{Q_1}}^2$, where the MOSFET on resistance $R_{ds_{ON}}$ is a function of the device temperature. For example, the IRFB4110 has $3.7m\Omega$ at 25 C and $6m\Omega$ at 100 $°C$ (typical), resulting in $5W$ conduction losses for only $30A$ RMS at 100 $°C$. Clearly, minimizing the RMS current by means of eliminating circulating current through the switches becomes essential to maintain high efficiency. As well, paralleling MOSFETs to reduce $R_{ds_{ON}}$ is needed as the converter power rating increases. The upper switch M_3 presents the same waveforms as M_1 at different time instants.

The lower MOSFET M_4 operates with reduced conduction losses and ZVT as explained below. The turn on transition in the lower switch M_4 (and M_2) occurs when D_4 (and D_2) is under conduction, as depicted in Fig. 2.16 at instant t_f. The MOSFET turns on with ZVT and no reverse recovery losses for diode D_4 (and D_2). There is a brief reverse conduction interval $t_f - t_g$ in Q_4 (and Q_2) until the current in the primary of the transformer is cleared at t_g. Two slopes in the switch

current can be identified within $t_f - t_g$. $V_o'/(L_{lk} + L_a' + L')$ at the beginning, and an approximate fast transition slope $V_i/(L_{lk} + L_a')$ until the current reaches zero. Q_4 remains in on-state with zero current (no power losses) until Q_1 turns-on at t_1. The primary current i_p flows through both Q_1 and Q_1 during $t_1 - t_3$. However, Q_4 continues to conduct until Q_2 achieves soft switching turn-on during $t_a - t_e$. Three effects are illustrated in this interval. First, a small drop in the primary current is experienced at t_a due to the transformer core losses and distribution of leakage in the primary and secondary windings. Second, the current in Q_4 ramps down in the interval $t_a - t_b$ with a slope given by $-V_o'/(L_{lk} + L_a' + L')$. Finally, at t_b instant, Q_4 turns-off with hard switching, like the previously analyzed full-bridge converters. M_1 remains inactive until diode D_1 is forward biased starting at t_e, creating a current path for the primary current during the dead time interval $t_e - t_f$. As mentioned before, D_1 turns-off with soft switching at t_f.

In order to complete the analysis of the waveforms, the output rectifier should be investigated. The current and voltage waveforms for D_7 (upper) and D_8 (lower) diodes are presented in Fig. 2.17, where both conduction losses and reverse recovery instants can be identified. The analysis starts with diode D_7 which has the same behavior as D_5. The turn-off transition from forward bias to blocking is illustrated in the interval $t_1 - t_2$. The transformer secondary current begins to ramp down when v_{g_1} enables M_1. The transition is limited by L_b and L_{lk} and the slope can be approximated by, $-V_i''/(L_{lk}'' + L_b)$, where V_i'' and L_{lk}'' are the input voltage and primary leakage inductance reflected to the secondary. Both D_7 and D_5 experience moderate reverse recovery losses due to di/dt, as indicated at instant t_2 for D_7. As well, the ringing on v_{D_7} is reduced as shown at instant t_2, which also helps to reduce reverse recovery losses. From t_2 until t_3, D_7 remains blocked and is forward biased again at t_4', where the current ramps up with an approximate slope $V_i''/(L_{lk}'' + L_b)$

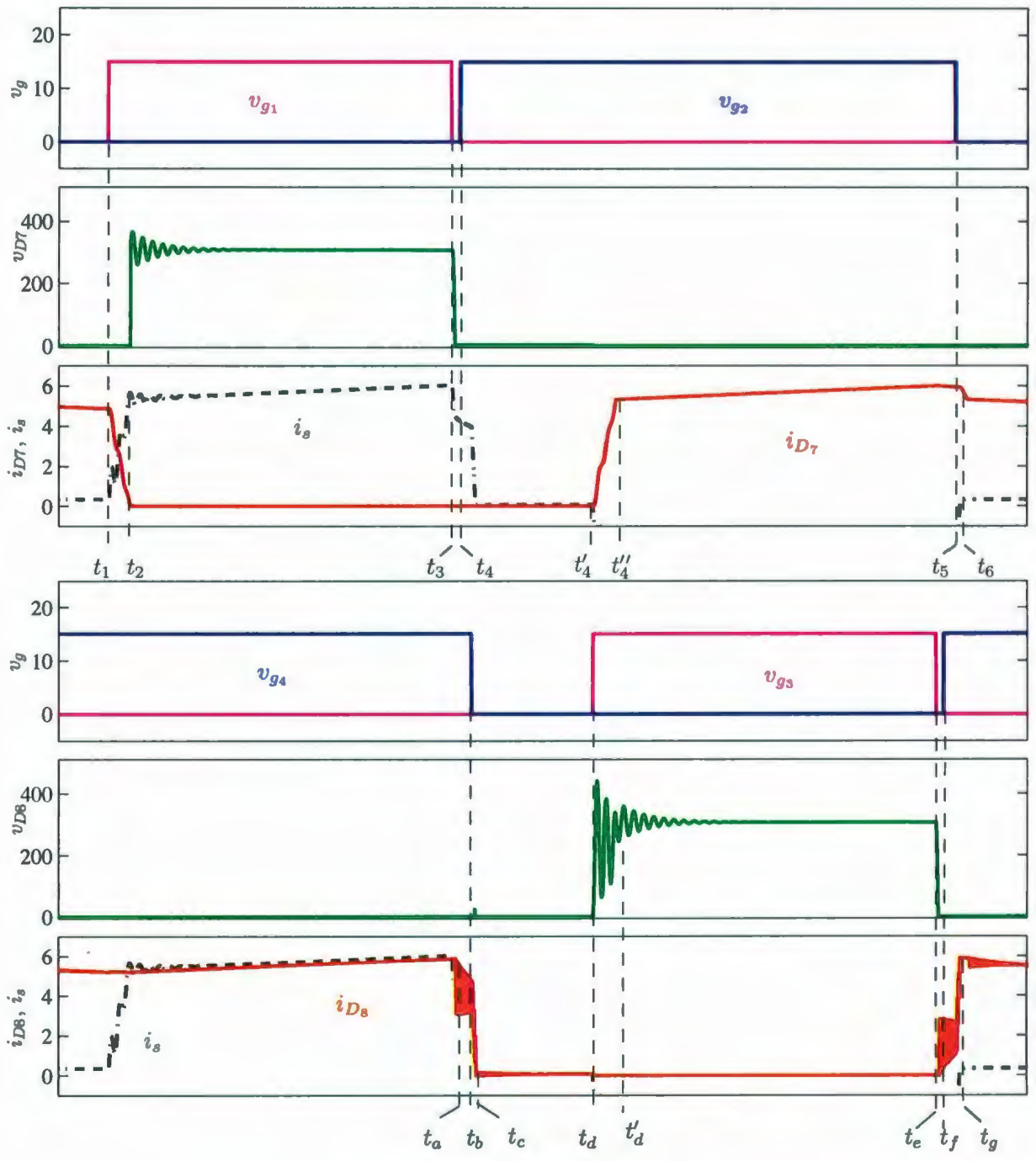


Figure 2.17: Full-bridge modified soft switching converter: voltage and current waveforms for upper D_7 and lower D_8 diodes.

until it reaches t_4''. This instant corresponds to the matching between current in L_b and the current of the output filter inductor L. Thereafter, from t_4'' to t_5, the slope of i_{D_7} is given by, $V_i'' - V_o/(L_{lk}'' + L_a + L)$.

At the end of the conduction of M_2 at t_5, a small drop in i_{D_7} is produced due to the transformer core losses and distribution of leakage in the primary and secondary windings which ends at t_6. Finally, the conduction interval in D_7 is given from t_4' to t_2 of the next switching cycle. While D_7 and D_5 present similar current waveforms as in the ZVS converter, the proposed topology and modulation sequence provides advantageous transformer ringing reduction. This helps to minimize or eliminate snubbers and reduce the blocking voltage of the rectifiers and its associated Q_{rr}.

The proposed topological arrangement presents a substantial improvement in the lower rectifiers D_6 and D_8 as follows. Figure 2.17 shows the dead time insertion between v_{g_1} and v_{g_2} during the interval $t_3 - t_4$ in combination with conduction overlap between v_{g_4} and v_{g_2} during the interval $t_4 - t_b$. During this period and due to the effect of L_a and L_b, diode D_8 experiences a fast transition from high conduction current to near zero current. When v_{g_3} drives M_3, the converter input voltage is partially reflected to the secondary and blocks D_8 immediately with a transition that virtually eliminates reverse recovery losses in D_8, considering the very low forward bias current (I_F) in D_8 at that instant. The blocking transition occurs in two intervals with moderate ringing, from t_d to t_d' while i_{D_7} ramps up, and from t_d' to t_e, where the full input voltage is reflected to the output of the rectifier. The conduction interval for D_8 is given from t_e to t_c of the following switching cycle.

One more technical challenge that exists in the ZVS topology, i.e., transformer ringing, is addressed in the proposed topology. As described in Section 2.2, transformer ringing in a traditional rectifier stage is associated with a zero voltage condition created by the filter inductor when the converter is operated in continuous

conduction mode (medium to high loading). In discontinuous conduction mode (light loading condition), the oscillations in the transformer depend on the turn-on time. Transformer oscillation results in undesirable effect such as high maximum reverse voltage rating for the diodes, excessive EMI, over voltage between windings, and power losses in auxiliary snubber circuits. The concept of avoiding a zero voltage condition on the transformer secondary is addressed in the proposed topology in the following manner. The inductors L_a and L_b prevent simultaneous conduction of D_5, D_6, D_7, and D_8 during initial turn-on intervals. This effect can be explained due to the opposition of current change by the inductors and the sequence in which the diodes are forward biased. As a result the turn-on pulse is partially reflected to the secondary of the transformer as if the converter were operating in discontinuous conduction mode. Hence, the oscillations are significantly reduced under any loading condition and partially depend on the turn-on time of the MOSFETs. As discussed before, the quasi-zero current turn-on transition allows prolonged turn-on times without affecting switching losses significantly. With the objective of highlighting the reduction in the transformer ringing, Fig. 2.17 shows simulation results of the effect of ringing in the rectifiers (v_{D_7} and v_{D_8}) for the proposed topological arrangement. While the voltage peak reaches $400V$ in this case, simulation results for the ZVS counterpart (Fig. 2.13), under the same conditions, shows that the voltage peak exceeds $500V$.

In summary, the waveforms presented in Fig. 2.17 for the modified soft switching topology reveal these significant improvements over the existing topologies:

1) The auxiliary inductors L_a and L_b shape the current waveforms of D_5 and D_7 during reverse recovery. Therefore, the inductor values can be selected to achieve a desired Q_{rr} in the upper diodes and hence control the total reverse recovery power losses.

2) Diodes D_6 and D_8 experience very low reverse recovery losses, unlike the existing ZVS, which is explained by near-zero forward current when the reduced reverse voltage is applied. The losses can be calculated using (2.2), where Q_{rr} is substantially reduced due to low I_F.

3) The presence of L_a and L_b significantly reduce oscillations and the peak reverse voltage applied to D_6 and D_8 that results from transformer ringing.

These improvements further increase the efficiency of the rectifier stage in addition to the efficiency gains of the power MOSFET stage. These features clearly highlight the superiority of the proposed modified topology over the existing ZVS arrangement.

2.5 High-frequency High-power Density Power Converter Prototype

A high-frequency, high-power density power stage was specifically developed to perform experimental tests of the advanced proposed topology and the selected control strategy. This flexible power stage comprises two separate printed circuit board (PCB) layouts for the power stage and the drivers. The power MOSFETs in the power board are symmetrically distributed and mounted on a single heatsink. The layout takes advantage of the entire area of the board by using a combination of power ground plane and polygon planes to reduce the current density. The input capacitor bank is also mounted on the power board to minimize the stray inductance along the path to the switches. As well, thin film snubber capacitors were mounted across each leg to suppress voltage spikes generated by distributed stray inductances during turn-off transitions.

Figure 2.18 shows four views of the power converter during its mounting process. As can be seen in the power board, the MOSFETs are placed on the bottom layer (power ground plane) ready to be attached to the heatsink (upper right view). This arrangement is flexible and allows the use of different MOSFETs and heatsinks to comply with thermal management requirements. The top layer of the power board includes bulk input capacitors and snubber capacitors distributed across the center of the board (lower left view). Since the pins of the MOSFETs (gate, drain, and source) are available on the top side of the power board, the drivers board is directly snapped-in to reduce the distance among them without interfering with the high current path of the power board. The drivers are isolated through a high frequency low power transformer that supplies each driver and optoisolators for the gating signal that comes from the control board.

As discussed in Section 3.1, the current in the input of the transformer has two switches in its circulation path. Since the output voltage of the FC could be as low as 20V (50A per kilowatt), the voltage drop across the switches must be minimized to reduce conduction losses, which are determined by the MOSFETs on-resistance R_{dsON}. By following this criterion, a number of switches in parallel has been arranged to limit the instantaneous conduction losses. Power losses in the switches not only reduces the overall efficiency of the converter but also requires a larger heat management system. In this design trade-off, cost per switch, driver peak current, and space must also be considered. The proposed design concept aims to minimize the distance between the bulk dc capacitors, snubbers, MOSFETs, drivers, and transformer to reduce the strenuous effect of distributed stray inductances.

By Following the same concepts described above, a 2.5kW power converter shown in Fig. 2.19 was developed, featuring high-current capability and high-efficiency. The

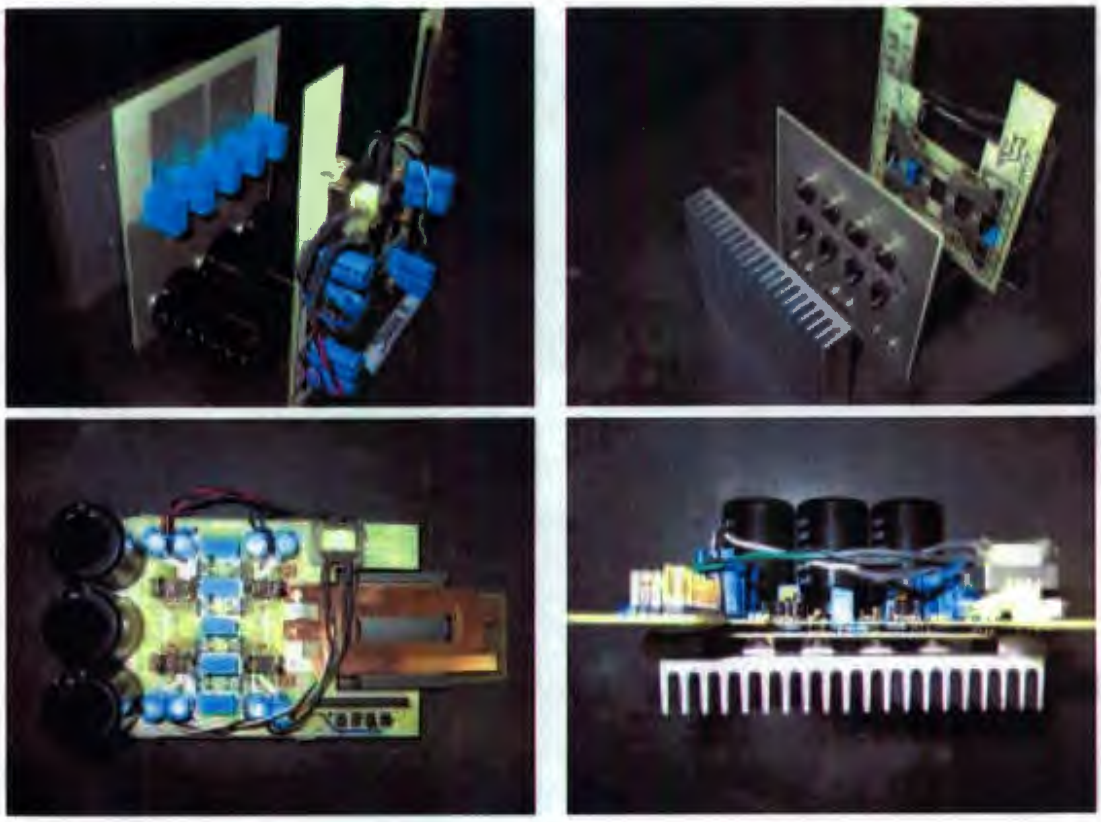


Figure 2.18: High-frequency power converter prototype.

components were strategically organized in a 6 oz copper clad. The thickness of the PCB was selected to maintain the current density within acceptable levels (recall that the input current may reach 125A). This concept replaces multilayer PCB designs and ensures low stray inductance. Similar to the previous converter, two main criteria were followed to produce this power converter: components distance minimization and symmetrical layout. Two distinctive sides can be identified in Fig. 2.19: hot layer, where the transistor, diodes, heatsinks, and magnetic elements are located (left view), and the cold layer where the capacitors (sensitive to temperature) and drivers are placed (right view). The heatsinks in the hot layer create channels to facilitate heat removal using forced air. The bottom or cold layer includes snubber and bulk capacitors which are symmetrically distributed at the minimum possible distance to the switches to minimize stray inductances. For example, the snubber capacitors (square blue case) are placed right on top of the switches. Any stray inductance between these two elements is purely due to the effect of the case terminals (i.e., TO220). As well, the converter input terminals are symmetrically distributed to equally supply the capacitor bank. Finally the driver, which is a critical component in the system, is snapped-in the terminals of the MOSFETs. Details of the design and development the power converter can be found in Appendix A.

2.6 Experimental Results and Validation

The power converter prototype presented in the previous section was employed to validate the proposed converter waveforms and measure efficiency gains. An arrangement of resistive loads was employed to perform the measurements. The converter was evaluated for the ZVS topology (Fig. 2.10) and the proposed modified topology (Fig. 2.14) using the parameters and parts in Table 2.1. For the ZVS operation, in-

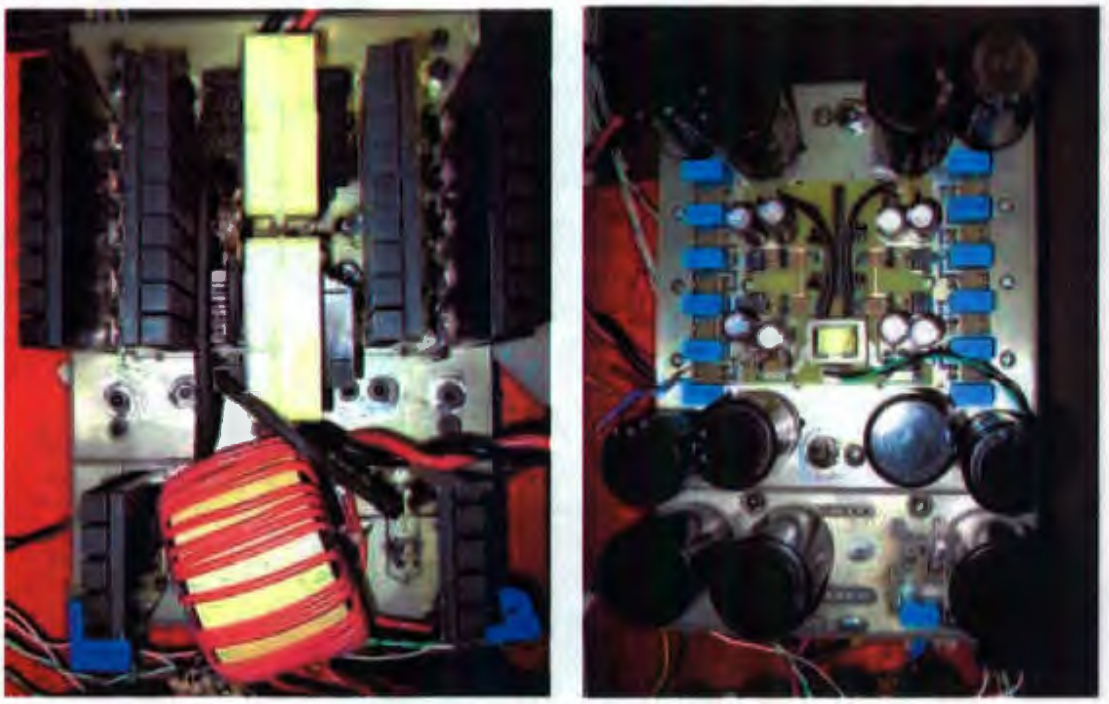


Figure 2.19: Power converter prototype.

ductor L_{zvt} was included and L_a and L_b removed. On the other hand, the proposed modified topology was operated using L_a and L_b and removing L_{zvt}.

2.6.1 Validation of Zero Voltage Switching Waveforms

The waveforms analyzed in Section 2.3 were verified by measuring a complete switching cycle in M_1, M_4, D_7, and D_8 under medium loading condition. The selected switching frequency was $40kHz$ to facilitate the visualization of the waveforms, which is the minimum admissible frequency to avoid saturation in the transformer core. Figure 2.20 shows MOSFET M_1 drain to source voltage (Ch1) and gate to source (Ch2) signals along with the secondary current waveform i_s (Ch4). Since minimization of stray inductances is a priority for such a high current input side (i.e., $66A$ for $P_o = 1.2kW$ and $v_{fc} = 18V$), current measurement in the primary is avoided and can

Table 2.1: Converter Parameters (ZVS and proposed)

Parameter	*Value/Part*
v_{fc}	18-40V
v_o	220V
$P_{o_{NOM}}$	1.5kW
M_1, M_2, M_3, M_4	2×$IRFB4110$
D_5, D_6, D_7, D_8	$DSEI2x30$-$10B$
L	1.33mH
L_{zvt}, L_a, L_b	10uH
C	680uF
F_{sw}	40-100kHz
Transf. Core	$3F3$-$E55/28/25$
Transf. primary turns N_p	2 (*foil*)
Transf. primary turns N_s	26 (*stranded*)

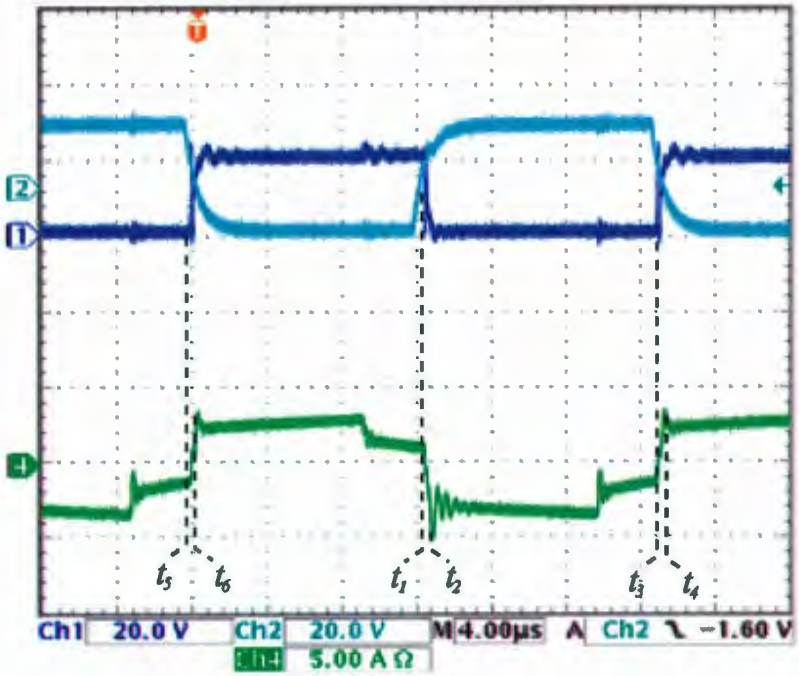


Figure 2.20: Lower side MOSFET M_1 waveforms under ZVS operation: Drain to source voltage (Ch1), gate to source signal (Ch2), and transformer secondary current (CH4).

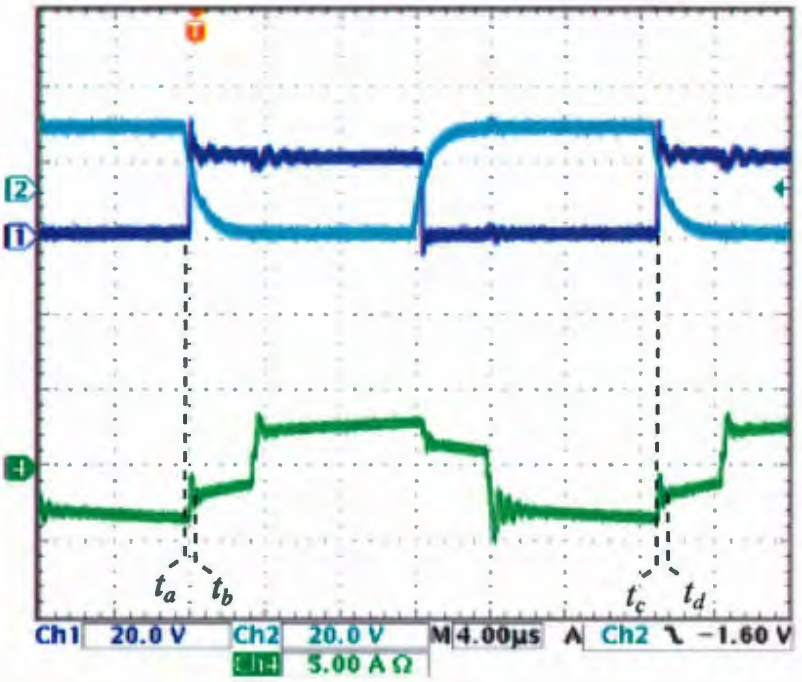


Figure 2.21: Lower side MOSFET M_4 waveforms under ZVS operation: Drain to source voltage (Ch1), gate to source signal (Ch2), and transformer secondary current (CH4).

be inferred from the secondary current. It can be seen in Fig. 2.20 that the turn-on transition occurs under ZVT (t_1) and the turn-off (t_3) experiences a hard switching transition, resulting in the conduction interval $t_1 - t_3$. During $t_5 - t_6$, diode D_1 behaves like a voltage clamp (dead time insertion).

Waveform measurements for MOSFET M_4 (lower side switch) are depicted in Fig. 2.21, where the hard switching turn-off and ZVT turn-on are indicated at t_a and t_d respectively. Diode D_4 conduction interval occurs during dead time insertion $t_c - t_d$ with no reverse recovery losses. All the waveforms are in accordance with the analysis performed in Section 2.3 for the input side of the power converter.

The moderate current rate of change in the rectifier side is shown in Fig. 2.22. The upper diode D_7 voltage conduction interval is given by $t_1 - t_2$. Reverse recovery occurs at t_2, where a small negative current peak can be seen due to the effect of Q_{rr}.

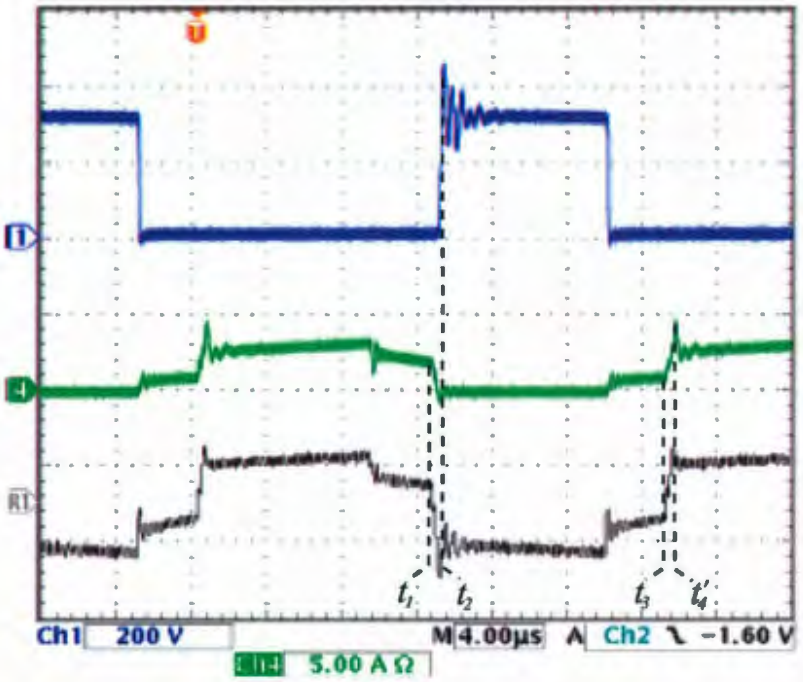


Figure 2.22: Upper side diode D_7 waveforms under ZVS operation: anode to cathode voltage (Ch1), diode current (Ch4), and transformer secondary current (R1).

As predicted in the simulations, the ringing peak voltage in D_7 is high, increasing the reverse recovery losses. The lower side diode D_8 waveforms are shown in Fig. 2.23, which experiences the same reverse recovery conditions as D_7 with moderate di/dt and large ringing peak voltage. As in the previous figures, the experimental waveforms are in accordance with the theoretical waveforms described in Section 2.3.

2.6.2 Validation of Modified Topology Waveforms

Similar to the ZVS case in the previous subsection, a complete switching cycle in M_1, M_4, D_7, and D_8 was measured under medium loading condition to validate the waveforms analyzed in Section 2.4. In order to facilitate the visualization, the switching frequency was set to $40kHz$. Figure 2.24 shows the waveforms of MOSFET

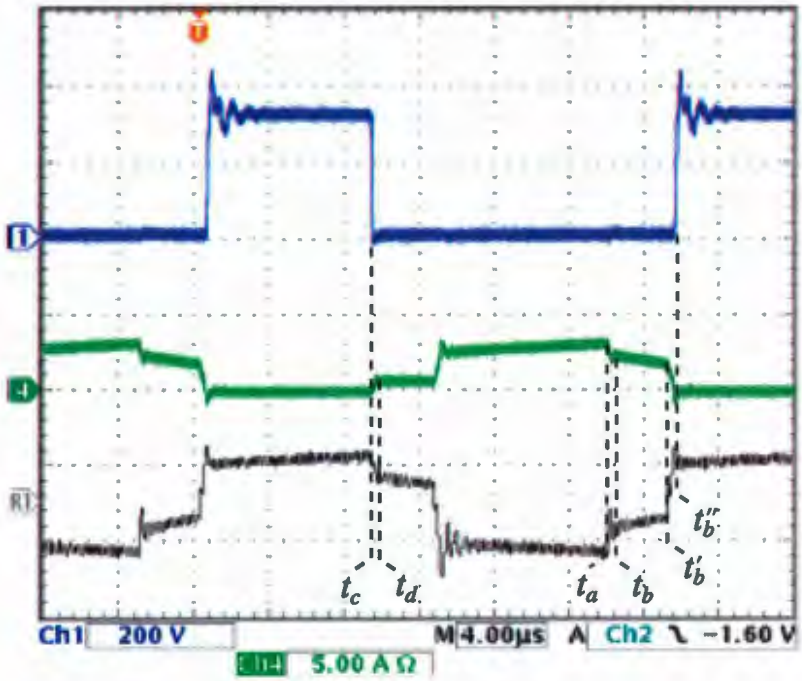


Figure 2.23: Lower side diode D_8 waveforms under ZVS operation: anode to cathode voltage (Ch1), diode current (Ch4), and transformer secondary current (R1).

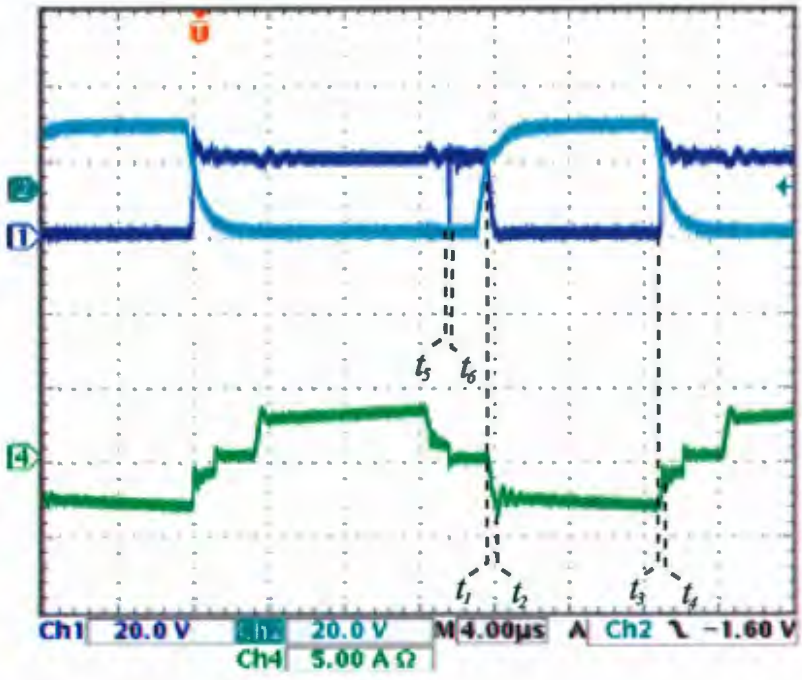


Figure 2.24: Upper side MOSFET M_1 waveforms in the proposed modified topology under medium loading condition: Drain to source voltage (Ch1), gate to source signal (Ch2), and transformer secondary current (CH4).

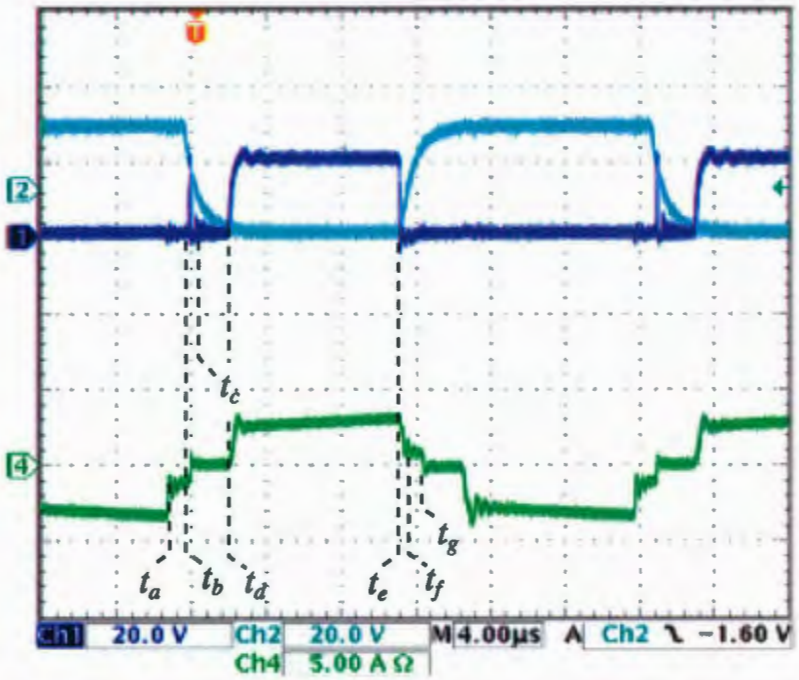


Figure 2.25: Lower side MOSFET M_4 waveforms in the proposed modified topology under medium loading condition: Drain to source voltage (Ch1), gate to source signal (Ch2), and transformer secondary current (CH4).

M_1, including gate and drain-to-source voltages, and the secondary transformer current. It can be seen that the MOSFET current starts at zero (ZCS) at t_1 and slowly ramps up until it reaches the current level of the filter inductor at t_2. The MOSFET turns-off at t_3 under hard switching conditions like in the ZVS topology, limiting the conduction interval to $t_1 - t_3$. The body diode D_1 conduction interval can be seen in $t_5 - t_6$, which returns the energy of the leakage inductance to the input dc bus and avoids circulating current in the primary.

Lower MOSFET M_4 waveforms are shown in Fig. 2.25 where the ZVT turn-on can be seen at instant t_f. At t_b instant, Q_4 turns-off with hard switching, like in the ZVS converter. As well, D_4 turns-off with soft switching at t_f. The conduction interval in M_4 is similar to that of M_1, showing reduced conduction losses.

The upper output rectifier waveforms are shown in Fig. 2.26. The turn-off

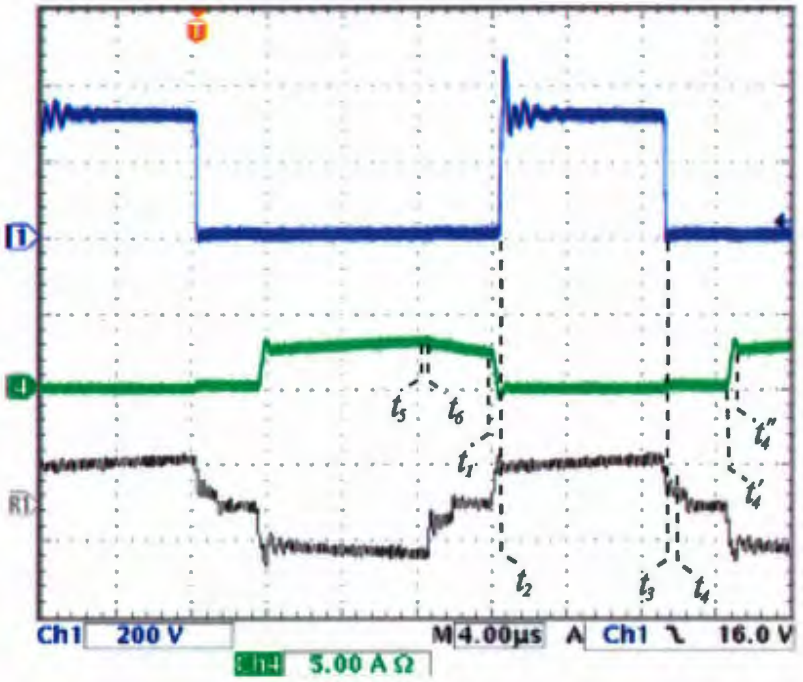


Figure 2.26: Upper side diode D_7 waveforms in the proposed modified topology under medium loading condition: anode to cathode voltage (Ch1), diode current (Ch4), and transformer secondary current (R1).

transition from forward bias to blocking is illustrated in interval $t_1 - t_2$. The effect of L_b and L_{lk} can be seen in the current transition, resulting in moderate reverse recovery losses at instant t_2. Instant t_4'' corresponds to the instant when the current in L_b matches the current in the output filter inductor L. From t_4'' to t_5, the slope of i_{D_7} is mainly due to L. The conduction interval is defined from t_4' to t_2 of the next switching cycle. As can be seen, the transformer oscillation are small and experience a fast damping (beginning at t_2). Only an initial peak is experienced due to the effect of the stray inductance in the current path (hall effect sensor measurement path) and L_b. This provides a clear indication that the proposed arrangement only requires a small local snubber connected from D_7 cathode to L input terminal, as opposed to the well known bulky snubber circuit in ZVS circuits.

The substantial improvement in the proposed modified topology is better appre-

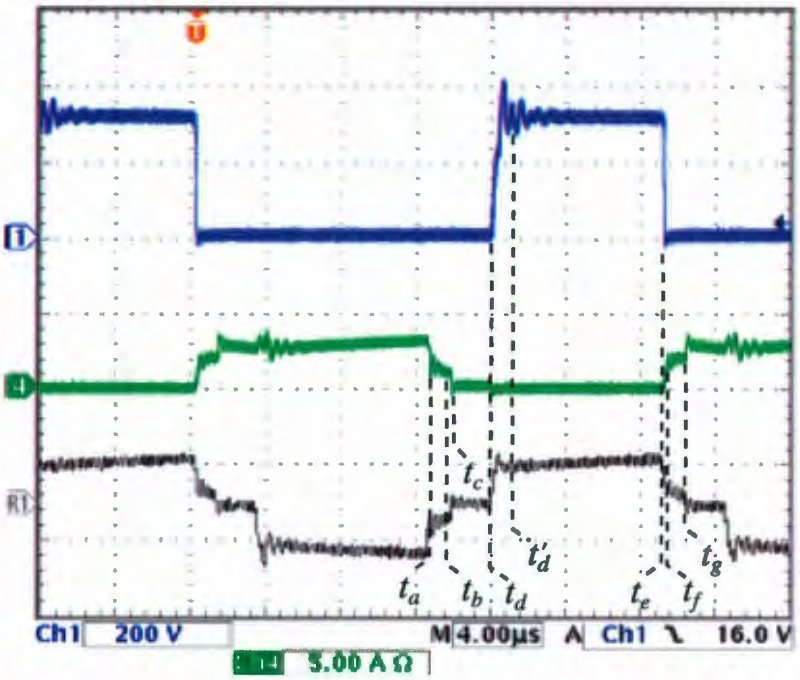


Figure 2.27: Lower side diode D_8 waveforms in the proposed modified topology under medium loading condition: anode to cathode voltage (Ch1), diode current (Ch4), and transformer secondary current (R1).

ciated in the experimental waveforms for D_8 depicted in Fig. 2.27. During $t_a - t_c$ period and due to the effect of L_a and L_b, diode D_8 experiences a fast transition from high conduction current to near zero current. At t_d the converter input voltage is partially reflected to the secondary and blocks D_8 immediately with a soft transition that produces very low reverse recovery losses in D_8. Two interval in the blocking transition with desirable moderate ringing can be seen, from t_d to t'_d while i_{D_7} ramps up, and from t'_d to t_e, where the input voltage is totally reflected to the output of the rectifier. Finally, the conduction interval in D_8 is given from t_e to t_c of the following switching cycle.

2.6.3 Comparative Efficiency Measurements

In this subsection, a comparative evaluation of combined switching and conduction losses is presented for ZVS and the proposed modified topology. The same power devices, power transformer, drivers, dead time insertion, heatsink and fan, and output filter was employed in both cases to ensure an adequate comparison (Table 2.1). Note that the objective of this section is to clarify the efficiency gains in the proposed modified topology rather than performing an absolute measurement of the converter efficiency. The efficiency measurement account for the power switches, PCB, connections and magnetic parts and does not include losses in the controller and drivers. For ZVS operation, the auxiliary L_{zvt} inductor was included while removing L_a and L_b. The proposed modified topology was operated using L_a and L_b while removing L_{zvt}.

The first test was performed for low input voltage $v_{fc} = 18V$ under variable loading conditions (50-1000W range), which is shown in Fig. 2.28. The efficiency of the proposed full-bridge modified topology (referred to as FB-M in the figure) is depicted with blue circle markers, while the full-bridge ZVS (FB-ZVS in the figure) is illustrated with black star markers. It can be seen that full-Bridge modified topology presents an efficiency gain beyond 1% from 50W to 400W when compared to full-bridge ZVS. From 400W the difference remains close to 1%. Since the losses in the power conversion process produce heat in the power stage, 1% efficiency gain results in more than 10% reduction in the thermal management requirements of the power converter. This lead to higher power density (volume per watt) and reduced cost.

The tests were replicated for higher input voltages, which are shown in Fig. 2.29 and Fig. 2.30 for $v_{fc} = 25V$ and $v_{fc} = 30V$ respectively. As expected, the efficiencies for both converters were reduced. However, the proposed full-bridge modified

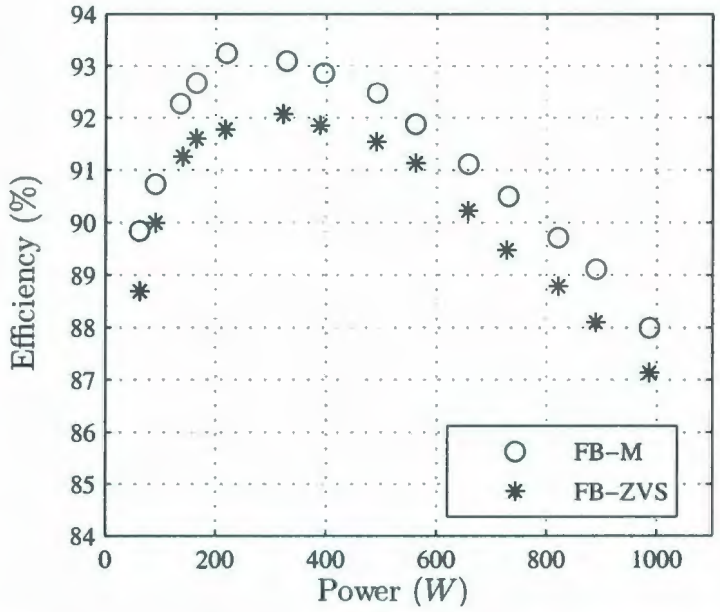


Figure 2.28: Comparative efficiency measurements for the proposed full-bridge modified topology (FB-M) and the full-bridge ZVS (FB-ZVS) with $v_{fc} = 18$.

topology widened its efficiency gain to approximately 1.5% and 2% for $v_{fc} = 25V$ and $v_{fc} = 30V$ respectively. This is a major improvement that can be explained as follows: When the input voltage increases, full-bridge ZVS topology experiences unnecessary conduction losses due to circulating current in the MOSFETs as a result of reduced duty cycle. As well, the converter is out of ZVS operation under light loading conditions and the rectifier reverse recovery losses increases due to the higher reflected input voltage in the secondary of the transformer (blocking voltage in the diodes). The proposed full-bridge modified topology avoids circulating current (major advantage) but increases turn-on losses in M_1 and M_3 due to higher accumulated energy in C_{oss}. Nevertheless, the reduction in conduction losses overshadows the turn-on losses in this low voltage application. The increase in the output rectifier blocking voltage mainly affects the upper diodes in the full-bridge modified topology (like in full-bridge ZVS), but the reverse recovery in the lower side diodes remains very low.

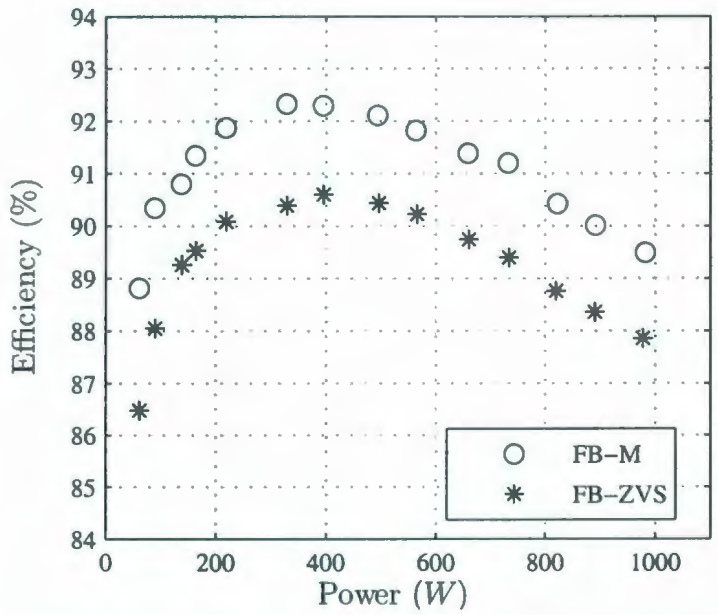


Figure 2.29: Comparative efficiency measurements for the proposed full-bridge modified topology (FB-M) and the full-bridge ZVS (FB-ZVS) with $v_{fc} = 25$.

The efficiency surface as a function of output power and FC voltage is presented for both converters in Fig. 2.32 and summarize the results presented in Figs. 2.28-2.30.

Even though efficiency characterization in power converters is traditionally performed using fixed input voltage (like in the previous cases), FC power conversion requires the use of a polarization curve. As described in Chapter 1 Section 1.1.1, the FC output voltage is a function of the operating conditions in the FC, the output current being the predominant factor. A comparative evaluation was carried out using the FC polarization curve in Table 2.2, which corresponds to a PEM Ballard Nexa 1.2kW in steady state operation. The results for both full-bridge modified topology and full-bridge ZVS are shown in Fig. 2.32. It can be seen that the efficiency of the proposed full-bridge modified topology is 2% better than full-bridge ZVS under any loading condition. An efficiency gain of 2% in a power converter with an overall effi-

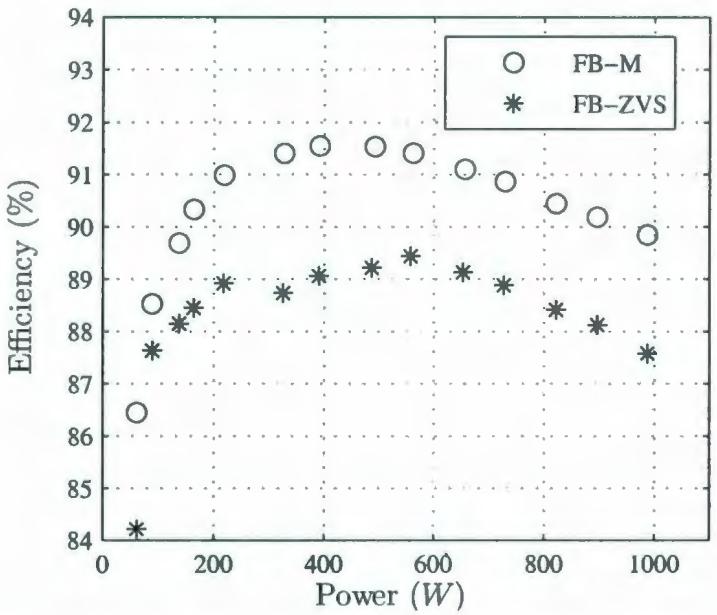


Figure 2.30: Comparative efficiency measurements for the proposed full-bridge modified topology (FB-M) and the full-bridge ZVS (FB-ZVS) with $v_{fc} = 30$.

ciency of 90% provides an improvement close to 20% in the thermal management of the power stage and allows the use of lower cost power semiconductors. This can be considered as an excellent improvement towards power density and cost of the power conversion stages. As well, the cumulative fuel savings (i.e., hydrogen or methanol) using the proposed modified topology is advantageous for any operating condition (light, medium, or heavy).

2.7 Summary

In this chapter, the full-bridge forward converter was selected as a base dc-dc topology and initially investigated under traditional hard switching phase shift PWM and ZVS operation. A modified topology and novel modulation sequence (modified soft switching) was proposed to improve the efficiency of the converter, taking into consid-

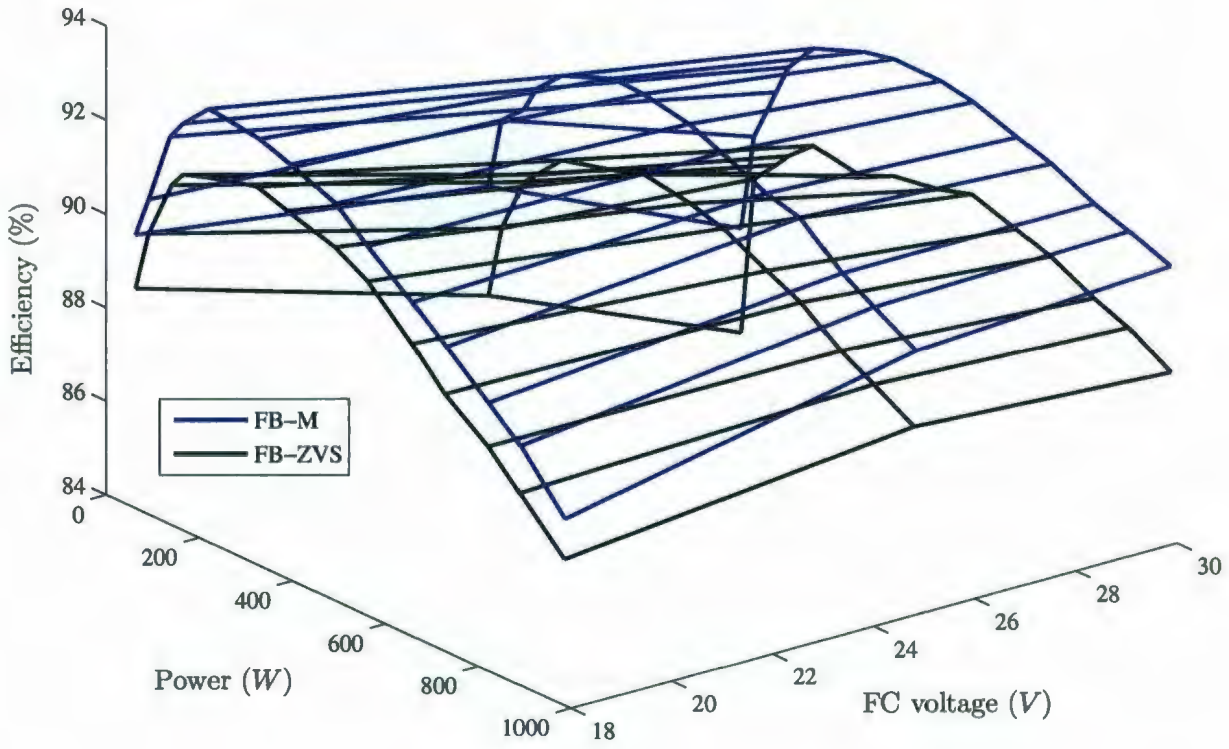


Figure 2.31: Comparative efficiency measurements for the proposed full-bridge modified topology (FB-M) and the full-bridge ZVS (FB-ZVS).

Table 2.2: Fuel Cell polarization curve points

v_{fc}	i_{fc}	P_{fc}
$42.8V$	$4.27A$	$183.0W$
$41.6V$	$5.74A$	$239.1W$
$39.87V$	$8.92A$	$356.0W$
$38.6V$	$10.95A$	$423.0W$
$36.84V$	$14.33A$	$528.2W$
$35.7V$	$16.95A$	$605.3W$
$33.83V$	$20.94A$	$708.6W$
$32.38V$	$24.52A$	$794.1W$
$30.07V$	$29.82A$	$896.8W$
$27.57V$	$35.77A$	$986.3W$
$22.03V$	$48.66A$	$1072.2W$

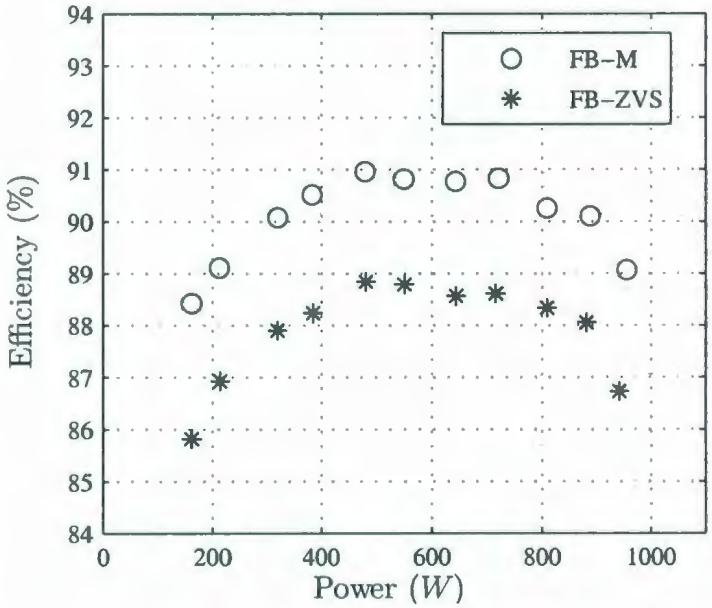


Figure 2.32: Comparative efficiency measurements for the proposed full-bridge modified (FB-M) and the full-bridge ZVS (FB-ZVS) using a polarization curve.

eration the voltage regulation nature of the polymer-electrolyte FC power source. A comprehensive analysis of the waveforms was carried out to characterize the converter power loss mechanisms and efficiency gains. The waveforms were experimentally validated using state-of-the-art prototypes specifically designed and developed for this purpose. Finally, comparative efficiency measurements were performed to highlight the efficiency gains under different loading conditions. It was demonstrated that the efficiency of the proposed full-bridge modified topology is 2% better than the full-bridge ZVS when operated with a FC power source under any loading condition. The proposed topology for dc-dc isolated power conversion overcomes major drawbacks of the traditional full-bridge forward converter that arise from its operation under the high input current and relaxed voltage regulation of the FC.

Chapter 3

System Level Behavior: Low Frequency Ripple Current Elimination

As alternative energy converters, Fuel Cell (FC) systems are characterized by a high level of interaction between the power source (FC), the power conditioning stage, and the load [21, 56]. For this reason an effective power conversion scheme requires coordinated operation of the entire system while minimizing power losses [57]. In this work, the interaction between the components of the system are identified and discussed with a view to maximize the power extraction in the FC while maintaining high power quality. A solution referred to as swinging bus is investigated to eliminate undesirable low frequency ripple current in the FC and reduce storage elements. As will be seen, all the stages in the system and their respective specifications are critical for a successful operation. In this chapter a study of the behavior of the power generation scheme at the system level is presented.

The conceptual block diagram of the proposed FC power generation system pre-

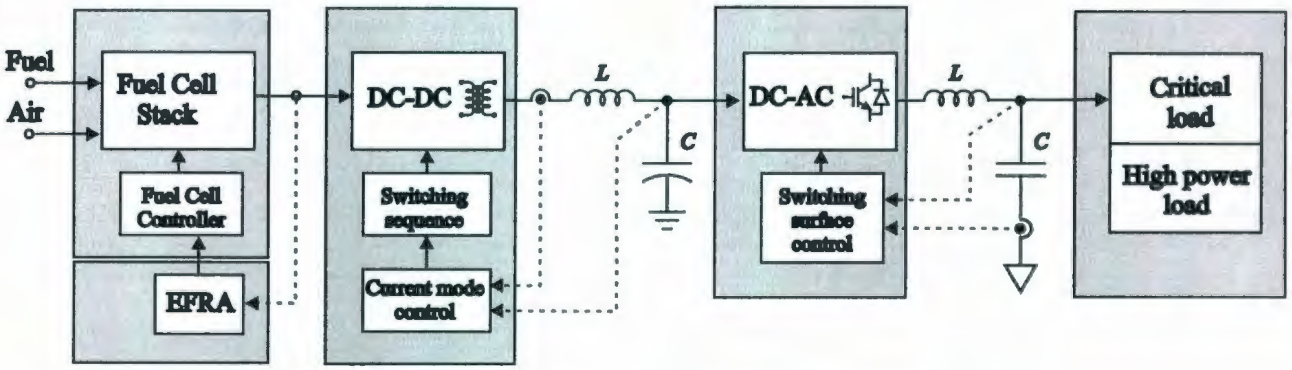


Figure 3.1: Conceptual Block Diagram of the Proposed FC Power Generation System.

sented in Chapter 1 is depicted again for conveniece in Fig. 3.1, where the four sub systems are shown as the FC cell stack and controller, isolated dc-dc converter, power inverter and load. In this arrangement, the operation of the system can be preliminary summarized in the following manner. The FC controller adjusts the operating point to match the power required by the load. The isolated dc-dc converter elevates the non-regulated dc output voltage of the FC and behaves like a current source that extracts energy from the FC with negligible low frequency ripple current. The output of the dc-dc converter feeds the inverter and acts as a swinging bus to absorb the low frequency ripple current generated by the inverter. The controller of the inverter generates the modulation pulses to drive the inverter power stage, producing high quality output power while rejecting the variations of the dc swinging bus. Note that the loading conditions for the inverter ranges from resistive to non-linear, high crest factor loads. The following section presents a description of the role and characteristic behavior of each stage within the system.

3.1 System Components Description

This section starts with a review of the dynamic behavior of a polymer-electrolyte FC focusing on the aspects that are relevant to stationary power conditioning. Two main characteristic behaviors are discussed, namely power availability and power reduction due to ripple current for fixed operating conditions. The analysis is followed by a definition of the requirement for the dc-dc converter stage and its control scheme. This stage aims to maximize power extraction from the FC by means of avoiding low frequency ripple current. Finally, the inverter stage (dc-ac) is addressed, highlighting the need for high quality output power under a wide input voltage range and loading conditions. As a result of the combined effects of the inverter operation and the ripple elimination technique in the dc-dc power stage, the dc bus capacitor voltage swings with double the line frequency to absorb low frequency ripple current.

3.1.1 Fuel Cell as a Power Source

Commercial FC power sources provide unregulated dc output voltage with high-current capability. As the output current increases the output voltage experiences a significant drop due to the output impedance of the cells. The steady state behavior of a polymer-electrolyte FC with fixed operating conditions can be represented with a non-linear polarization curve (v-i characteristics). If the operating conditions are modified, a new polarization curve is obtained. This change in the polarization curve occurs very slowly due to the high heat capacity of the cell and slow mass transport processes in the flow fields and electrodes. A fast dynamic behavior, however, takes place when the operating conditions are fixed and the output current changes [17]. When a constant power step is applied to the output, the FC is able to adjust its output current instantaneously to match the power demand. Moreover, the operating

point (OP) can depart significantly from the steady state polarization curve during transients, denoting the effect of the charging and discharging of the cell's double layer capacitance.

The double layer capacitance also has an important implication in operation with inverters. Low frequency ripple current on the dc power source, in this case the FC power system, is inherent to single-phase and three-phase inverters with unbalanced load. For single-phase inverters, the fundamental frequency of the ripple is double the line frequency in addition to harmonics. In order to illustrate the impact of ripple current in FCs, a single polymer-electrolyte cell was evaluated experimentally and the results presented in Chapter 1, Section 1.1. For conveniece, Fig. 1.6 is depicted again in Fig. 3.2(a) showing current extraction at 25Hz and 400Hz ripple current. As can be seen, the trajectory of the operating point has a hysteresis behavior and pivots at the dc operating point ($325mA$). The hysteresis behavior, which denotes a phase difference between voltage and current, is associated with the double layer capacitor. As the frequency increases (i.e., $400Hz$), the hysteresis is reduced and the power extraction increases as well.

Figure 3.2(b) presents the power extraction as a function of frequency and ripple amplitudes of 10%, 30% and 50% of the dc operating point ($325mA$). As expected, the curves show the decrease in power extraction when the amplitude of the ripple increases, while an increase in the ripple frequency helps to increase the power extraction.

Although the experimental tests were performed using a small laboratory polymer-electrolyte FC, these results and conclusions are valid for larger electrode areas and stacks where the current levels and voltages are larger. Having reviewed the power availability nature of polymer-electrolyte FC systems and how it is affected by ripple current, this work develops an integral scheme that coordinates the efforts between

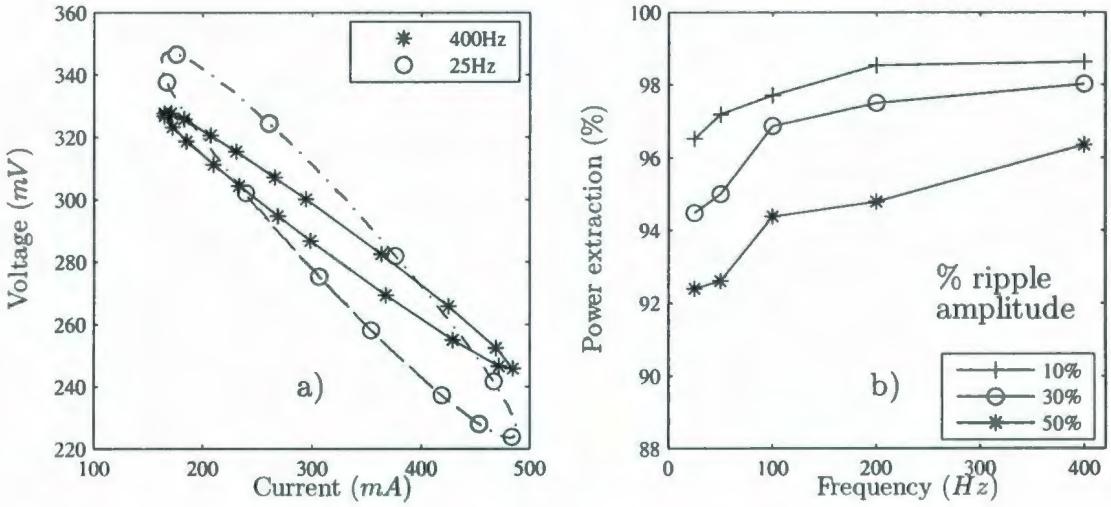


Figure 3.2: dc+ac current test of the DMFC for $25Hz$ and $400Hz$: a) Zoom of the v-i plot and b) FC power extraction with ripple current as a percentage of the power extraction without ripple.

the FC system and power conditioning stage to maximize the power extraction.

3.1.2 DC-DC Converter Stage

In the previous chapter, an advanced dc-dc power converter based on full bridge topology was presented featuring voltage boost, galvanic isolation, and improved efficiency. It has been demonstrated that the modified modulation or switching sequence combined with a mechanism to reduce stress in the rectifiers can reduce power losses and therefore the overall cost and size of the power converter (i.e., simplified arrangement for thermal management). As well, it has been seen that the waveforms in the output LC filter reflect the behavior of a buck derived type of topology.

Even though the topology selection is critical to achieve high efficiency dc-dc conversion and reliable operation, this chapter focuses on the way the dc-dc stage is operated. That is, the control scheme of the dc-dc stage rather than the topological

arrangement itself. Since the problem is treated with generality, the results are applicable to any buck derived topology (i.e., traditional full and half bridge, ZVS, etc.).

As discussed in the previous section, the effect of low frequency ripple current produces considerable reduction of power availability in the FC. When the amplitud of the ripple is reduced, the power extraction increases and can only achieve 100% extraction when the ripple current is zero (only constant dc current drawn from the FC). Therefore, the dc-dc power converter should be operated as a constant current source to avoid low frequency current ripple in the FC. The low frequency ripple current in the system is generated by the inverter input current, which has a fundamental frequency that is double the line frequency for single phase inverters. Since the inverter extracts low frequency ripple current from the filter capacitor of the dc-dc converter, any attempt to control a fixed voltage on this capacitor results in a reflection of the ripple to the input of the dc-dc converter (FC system). In this work, the concept of swinging bus is studied with the objective of eliminating the reflected ripple current.

A multi-loop outer voltage-mode and inner current-mode control strategy is developed in the following sections to control the isolated dc-dc converter. In this way, the FC current extraction only contains high frequency ripple determined by the dc-dc converter switching frequency and the characteristics of its input filter.

Figure 3.3 shows a conceptual block diagram of the proposed dc-dc scheme where the key waveforms are illustrated. It can be seen that the envelope of the current extracted by the inverter (i_o) is pulsating with half the line frequency period T_{line}. Since the dc-dc converter is controlled to produce a constant feed dc current i_L, the capacitor voltage v_o swings to absorb the low frequency ripple current i_o. Note that the ripple current in i_L has double the dc-dc converter switching frequency

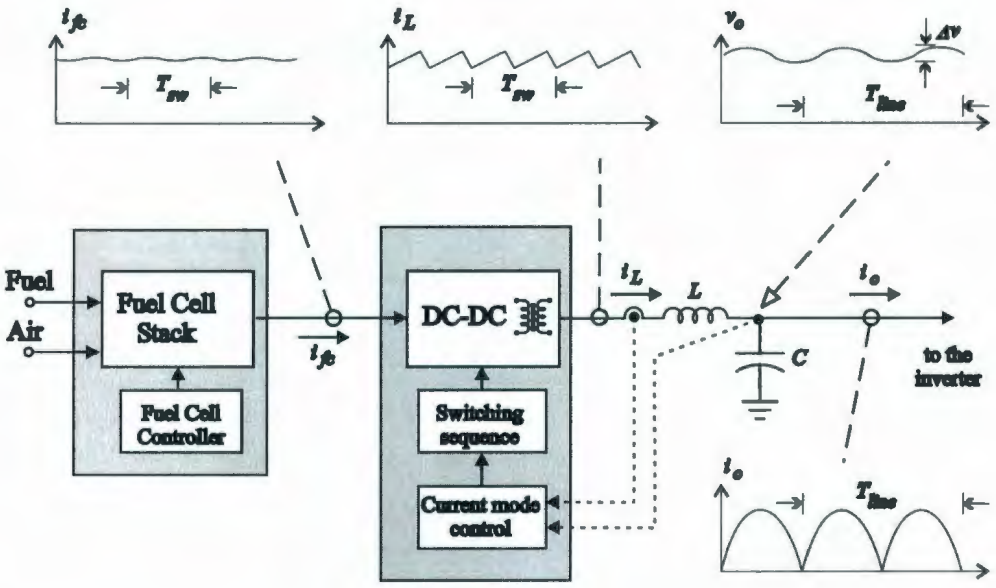


Figure 3.3: Low frequency ripple current elimination scheme.

which is much higher than the inverter output frequency. The output voltage of the dc-dc converter is maintained in average within a desired range by the action of the constant charging current, which is reflected to the FC system to maximize power extraction. The proposed control scheme, therefore effectively regulates the current injection into the filter capacitor at the expense of a voltage swing in the bus. The detailed investigation of the relationship between constant current injection and instantaneous output power is undertaken as part of the control scheme using different types of loading conditions and is presented in this chapter and Chapter 4.

3.1.3 Swinging Bus Inverter Control Strategy

The swinging bus concept described above is employed to absorb the 120Hz pulsating current generated by the inverter. As a result, the low frequency ripple current reflection in the FC is eliminated at the expense of the voltage swing in the input

terminals of the inverter. Since inverters are traditionally operated with stiff dc input voltages, a swinging bus presents an unprecedented challenge for the control scheme of the inverter. In order to comply with stringent standards for transient and steady state performance, a control scheme based on curved switching surfaces is developed in Chapter 4 to reject variations in the bus voltage while providing high quality output power. since the proposed control scheme is close to time optimal, this chapter assumes ideal operation in the inverter under any operating conditions.

In the following sections, an in-depth description of the behavior of the power generation scheme behavior at the system level is presented. First, the background information provided in the preceding sections is further analyzed to establish a low to medium frequency behavioral model. The model is then used to study critical interactions in both time and frequency domain (voltage and current waveforms) to identify the requirements for a successful realization of the system.

3.2 System Behavioral Model

In the previous sections, an introduction to the system components was described including the effects of ripple current in the FC, the control strategy for dc-dc conversion, and the swinging bus inverter. The dynamic behavior for each component can be viewed in two different timeframes: 1) high frequency range (i.e., switching frequency) and 2) low to medium frequency range (i.e., inverter output frequency and harmonics). It has been seen in Section 1.1.1 that the FC is presented with a low to medium frequency ripple current that affects the power extraction capability. It is desirable, therefore, to include this ripple range in the system-wide behavioral model.

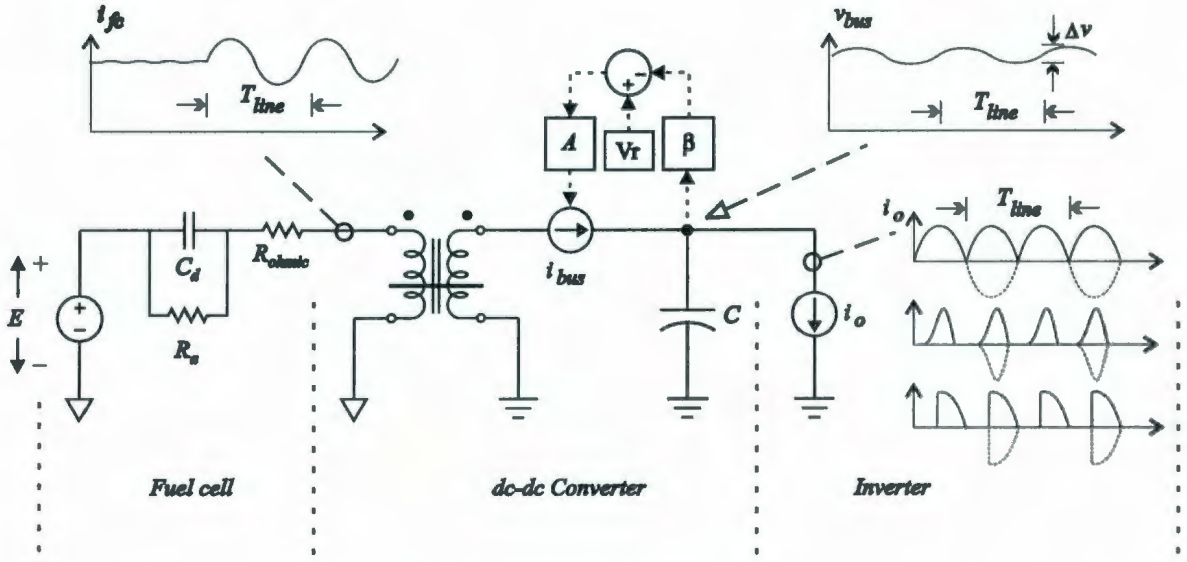


Figure 3.4: System behavioral model.

The analysis begins with the FC electrical equivalent model where three basic lumped passive components and a voltage source are included. This accounts for the activation, concentration, and ohmic voltage drops, the double layer capacitance, and the theoretical Nerds voltage. The FC equivalent model is presented in the first portion of Fig. 3.4, which is accurate enough to serve the purpose of the system level study.

The second stage in the system-wide model in Fig. 3.4 is the dc-dc converter which is presented by four elements: a) The dc-dc transformer is employed to represent the isolation and conversion ratio as a funtion of the FC output current and dynamic voltage change [36]; b) The current source accounts for an averaged model of the dc-dc converter inner current loop considering the large bandwidth and small ripple current in the filter inductor. The fast dynamic response of inner current loops in peak and averaging current techniques are well known and understood [58–60], and can exceed the output filter cutoff frequency. Consequently, the ideal controlled current source satisfies the purpose of low to medium frequency evaluation; c) The control loop for

the current source is an outer voltage loop. This controller is of particular interest and key to the successful operation of the overall system. The loop compensation, bandwidth, and dynamic behavior will be investigated in the following sections to ensure low frequency ripple current elimination in the FC; d) The last component in the dc-dc converter stage is the output filter capacitor, where the swinging bus effect takes place as indicated conceptually in Fig. 3.4. The capacitor is fed with constant current from the controlled current source and discharged by the inverter input current.

Finally, the inverter stage is also averaged and represented by a current source that reflects the module of the system output current that is extracted from the bus. Typical current waveforms i_o supplied by the dc bus to the inverter are depicted in Fig. 3.4.

3.3 Swinging Bus Analysis

The swinging bus principle of operation can be understood in terms of charge capacitor balance and with the aid of Fig. 3.5. In the first half of Fig. 3.5, the bus is operated with a traditional stiff control. In order to maintain fixed output voltage, the dc-dc controller injects pulsating current with double the inverter output frequency into the bus capacitor to maintain the instantaneous charge balance. The pulsating current waveform is directly reflected to the FC as indicated in Fig. 3.5(b). Note that the peak ripple current is large and contains 120Hz fundamental and harmonics producing significant losses in the FC stack. In order to obtain maximum power extraction from the FC, the operating mode is changed to constant current extraction and swinging bus voltage. This is illustrated in the second half of Fig. 3.5. In this case, the ca-

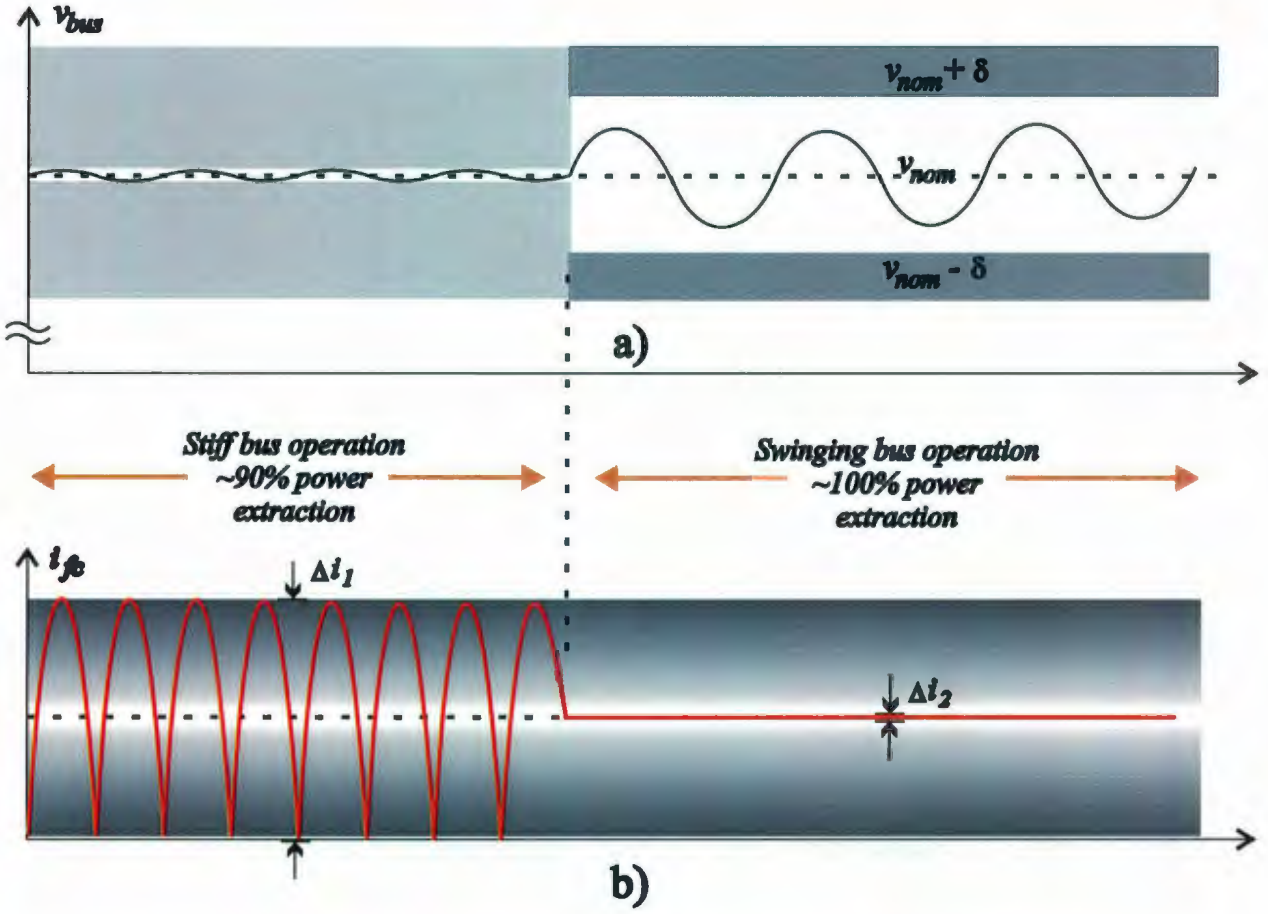


Figure 3.5: Swinging bus operation: charge capacitor balance principle.

pacitor current has a zero average every 1/120 seconds, fulfilling the charge balance requirement at the expense of the voltage swing. The relation between the capacitor value and the power rating of the inverter determines the swinging boundaries ($v_{nom} \pm \delta$), which are conceptually indicated in Fig. 3.5(a). Therefore, the capacitor value is selected to operate within the inverter operating range, while complying with operating life and ripple current capability.

Under this operating mode, the resulting swinging voltage waveform is a function of the inverter loading condition. The objective of this section is to characterize in time and frequency domains the behavior of the bus voltage under linear, non-linear, and pulsating type of loads. The results obtained in this section will serve as basis to develop the feedback (β) of the control loop.

3.3.1 Time Domain Behavior

The system operating under linear resistive load is analyzed first. Figure 3.6(a) shows a case example of a bus voltage with bus capacitor $C = 680\mu F$, nominal voltage 220V, and output operating peak current $9.6A$ (peak sinusoidal pulsating current for 1.5kW output power). As can be seen, the voltage swings with a fundamental of double the inverter output frequency, in addition to harmonic distortion. The current fed to the inverter i_o is illustrated in Fig. 3.6(b) with a solid line, which is basically a full wave rectification of the inverter output current. Note that the high frequency ripple current at the inverter switching frequency has been neglected (only the envelope is considered), as it only produces small high frequency voltage ripple in the capacitor. The capacitor current is also shown, in which the zero charge balance for every 1/120 seconds can be seen. This results from the subtraction between the constant input current supplied by the dc-dc converter and the output pulsating current fed to the

inverter. For the analyzed case, the small capacitor value produces a voltage swing close to 10% (peak to peak).

The second analyzed waveform is a controlled rectifier pulsating type of load. Figure 3.7(a) shows the bus voltage waveform indicating two intervals: 1) voltage ramp due to constant current charge, where the capacitor current is equal to the constant input current supplied by the dc-dc converter, and 2) portion of a sinusoidal-like discharge when the load is activated. It can be seen that the voltage excursion is larger when compared to linear load, even though the rms inverter input current is smaller. This is indicated in Figure 3.7(b) with a 90o firing angle in the load rectifier. As can be seen, the voltage also swings with a fundamental of double the inverter output frequency, except for the fact that the harmonic distortion is larger. Again, the high frequency ripple (inverter switching frequency) has been neglected for simplicity and only the envelope is considered. The capacitor maintains zero charge balance for every 1/120 seconds to maintain $220V$ average capacitor voltage. That is, the constant input current supplied by the dc-dc converter minus the output pulsating current fed to the inverter has a zero average.

The third waveform is a non-linear load with output current crest factor $CF = 2.3$ typically produced by a full wave rectifier connected to a small inductance and large output capacitor bank. Figure 3.8(a) shows the bus voltage waveform indicating two intervals: 1) a sharp voltage ramp produced by constant input current charge and zero output current, and 2) an abrupt voltage drop when the charges are transferred to the load with high crest factor current. The bus voltage resembles a dual-slope triangular waveform (close to a sawtooth) containing even and odd harmonics of the fundamental. In this case, the voltage peak to peak swing is the largest for all three cases analyzed. Figure 3.8(b) shows the envelopes of the capacitor current and output current supplied to the inverter. similar to the other cases, the constant input current

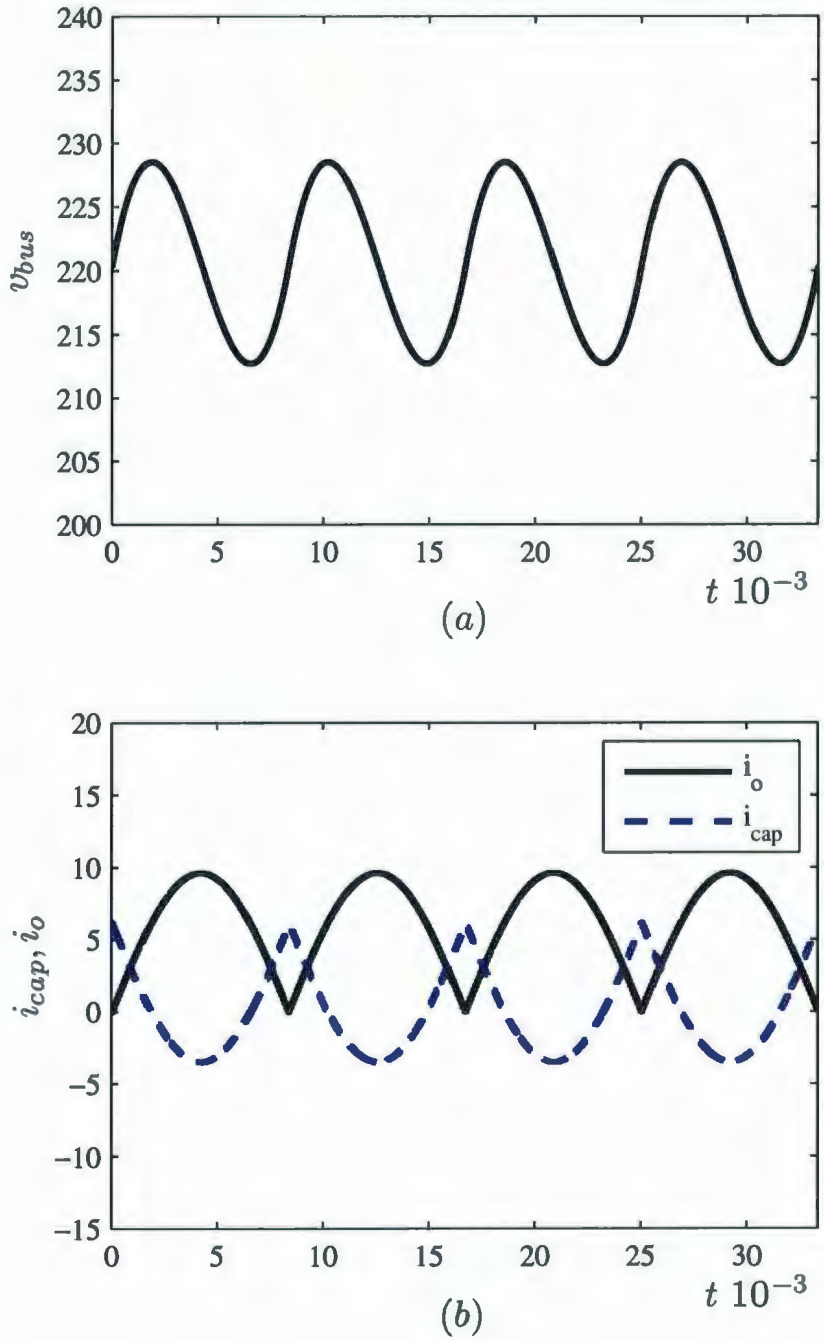


Figure 3.6: Swinging bus operation under linear resistive load: a) bus voltage and b) bus currents (output i_o and capacitor i_{cap}).

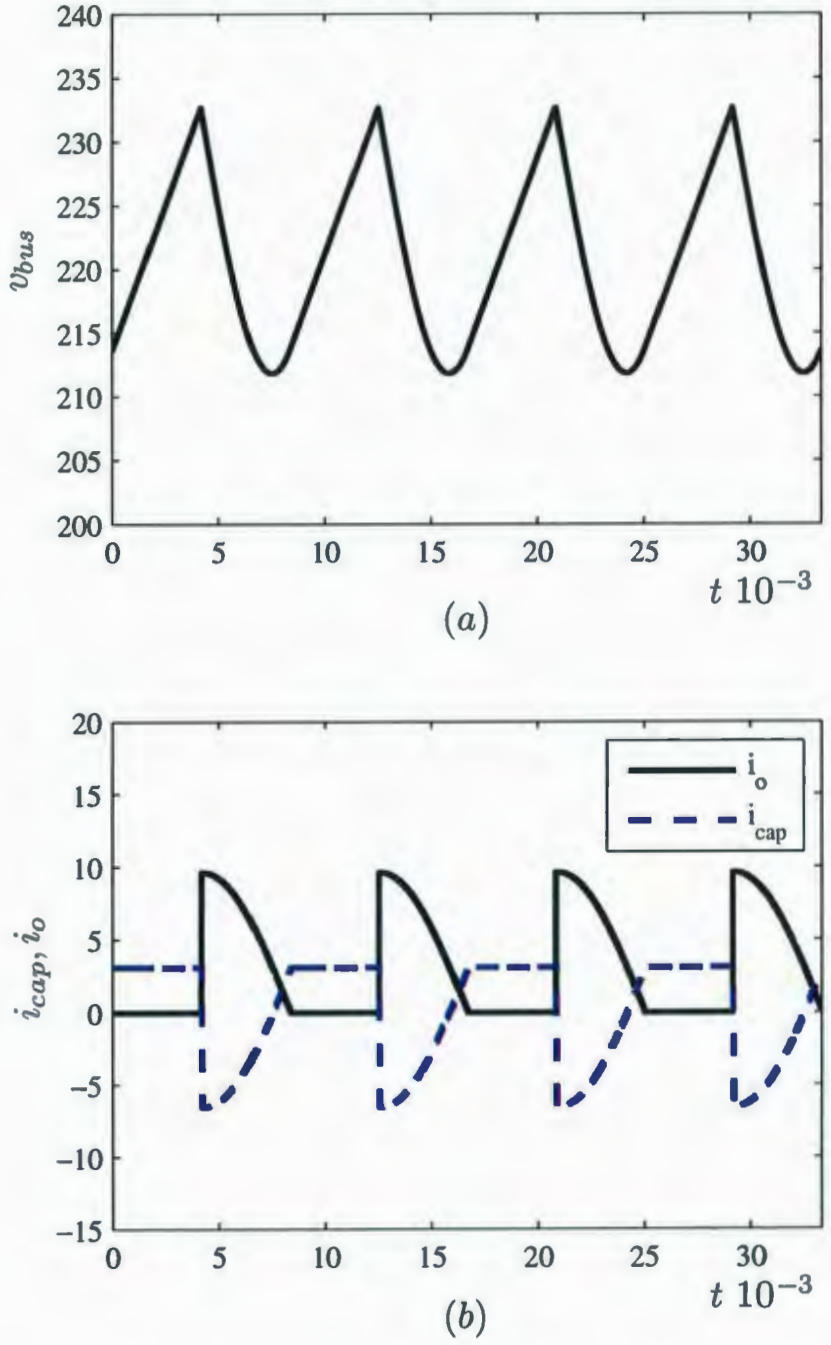


Figure 3.7: Swinging bus operation under controlled rectifier pulsating load: a) bus voltage and b) bus currents (output i_o and capacitor i_{cap}).

is set to obtain zero charge balance at $120Hz$ and maintain $220V$ bus voltage.

From the analyzed waveforms (Fig. 3.6 to Fig. 3.8), it can be seen that the bus voltage peak to peak excursion highly depends on the type of load. The swinging boundaries ($v_{nom}\pm\delta$), conceptually discussed and illustrated in (Fig. 3.5), define the inverter input voltage operating range not only as a function of the power rating but also as a function of the loading type. It can be concluded that non-linear high crest factor output current presents the worse case bus swing scenario and should be considered in the process of selecting the bus capacitor.

3.3.2 Frequency Domain Behavior

The analysis in time domain presented in the previous section allowed a better understanding of the bus behavior and the effect of swinging excursion under different type of loads. In order to further characterize the bus behavior, it is necessary to explore the spectral contents for each bus voltage waveform. This analysis will serve as the basis to develop the signal processing block required as part of the feedback (β) of the control loop.

The spectral contents are presented using the Discrete Fourier Transform (DFT) under two types of windows, rectangular and Hamming. The windowing effect is briefly discussed, as well as the impact of the number of samples and sampling frequency. It becomes important to include these practical limitations in sampling frequency, memory storage capability, and processing overhead due to the limited resources in low-cost DSP-based platforms employed for control in power electronics.

The sampling frequency for the bus voltage is considered from 3.6kHz to 36kHz, which is in accordance with the switching frequency of IGBT inverters in high-power and low-power applications respectively (sampling frequency is commonly synchro-

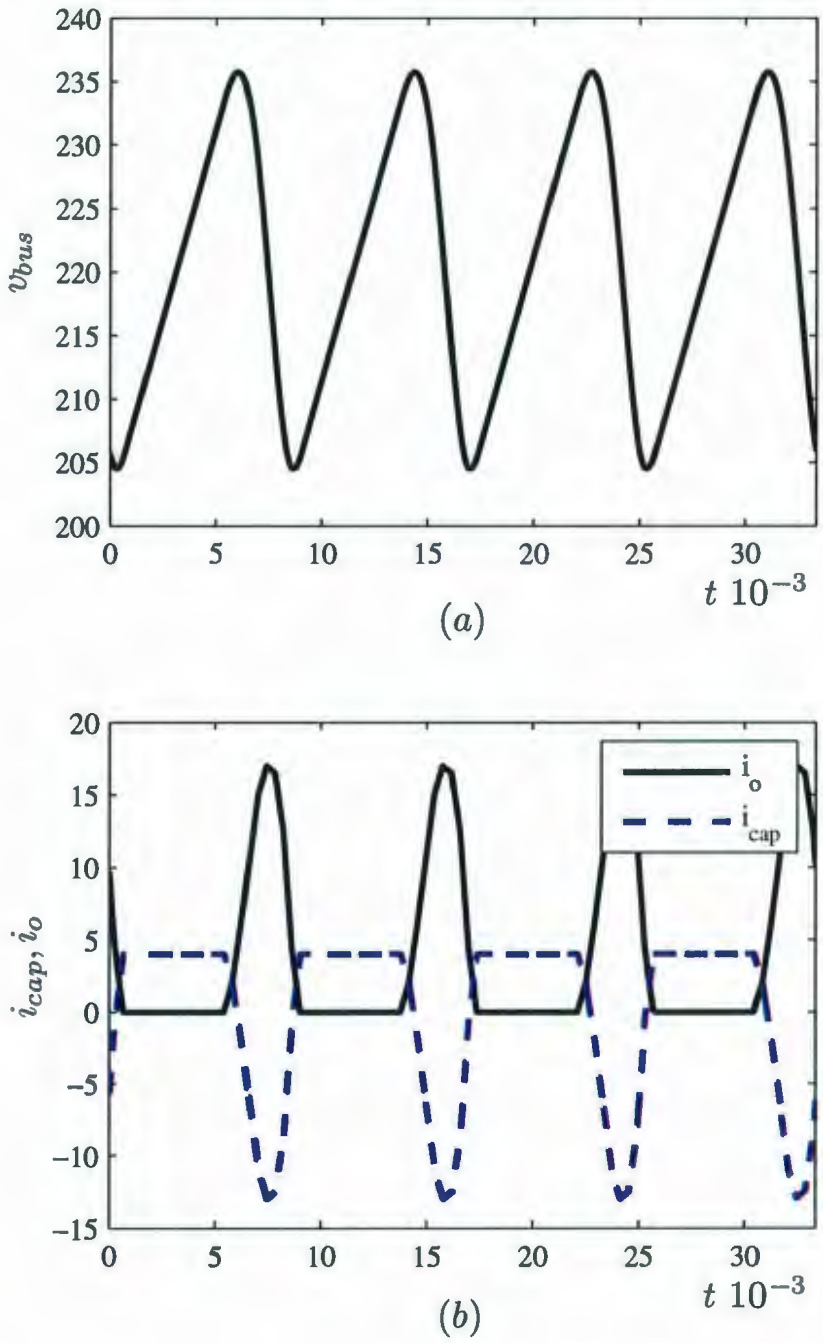


Figure 3.8: Swinging bus operation under high crest factor non-linear load: a) bus voltage and b) bus currents (output i_o and capacitor i_{cap}).

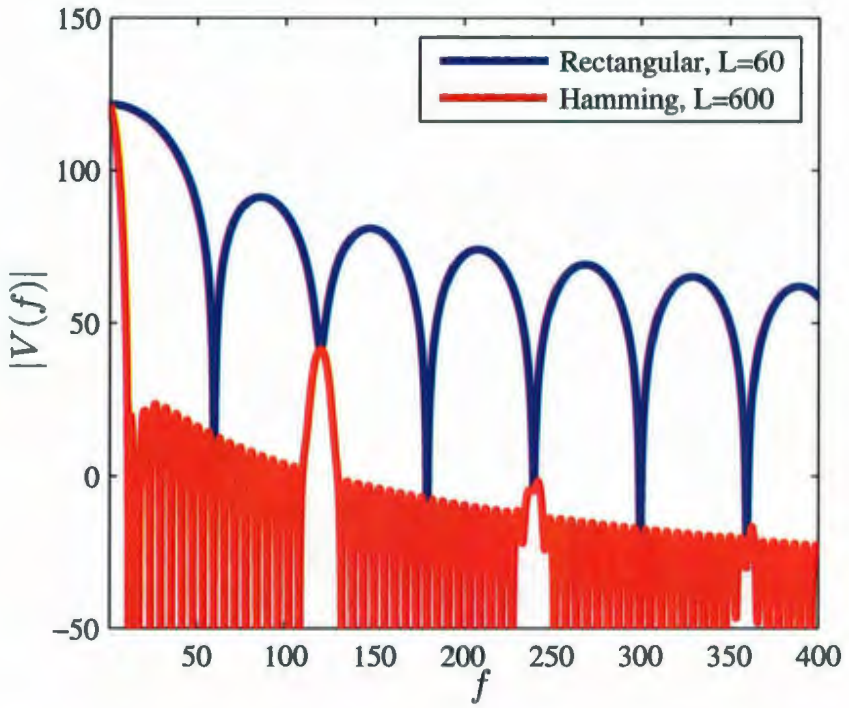


Figure 3.9: Bus voltage spectrum under linear loading condition.

nized with PWM frequency carrier). However, since the window is required to capture at least one fundamental cycle of the inverter output voltage (1/60 seconds), the higher the sampling frequency, the larger the number of points and processing overhead. For example for F_S = 36kHz, a 600-point window is required while only 60-point window is needed for F_S = 3.6kHz. Since it is desirable to use the minimum possible number of points to minimize memory usage and arithmetic operations, 60-point window is the preferred option. In fact, from the processing performance point of view, 2^N-point window would be ideal (i.e., N=6 for 64-point). As will be seen, sampling frequencies of about F_S = 3.6kHz are well above the highest harmonic content in the bus voltage waveforms and can be obtained by decimation in inverters with higher switching frequencies.

The spectrum of the bus voltage under linear loading conditions is examined

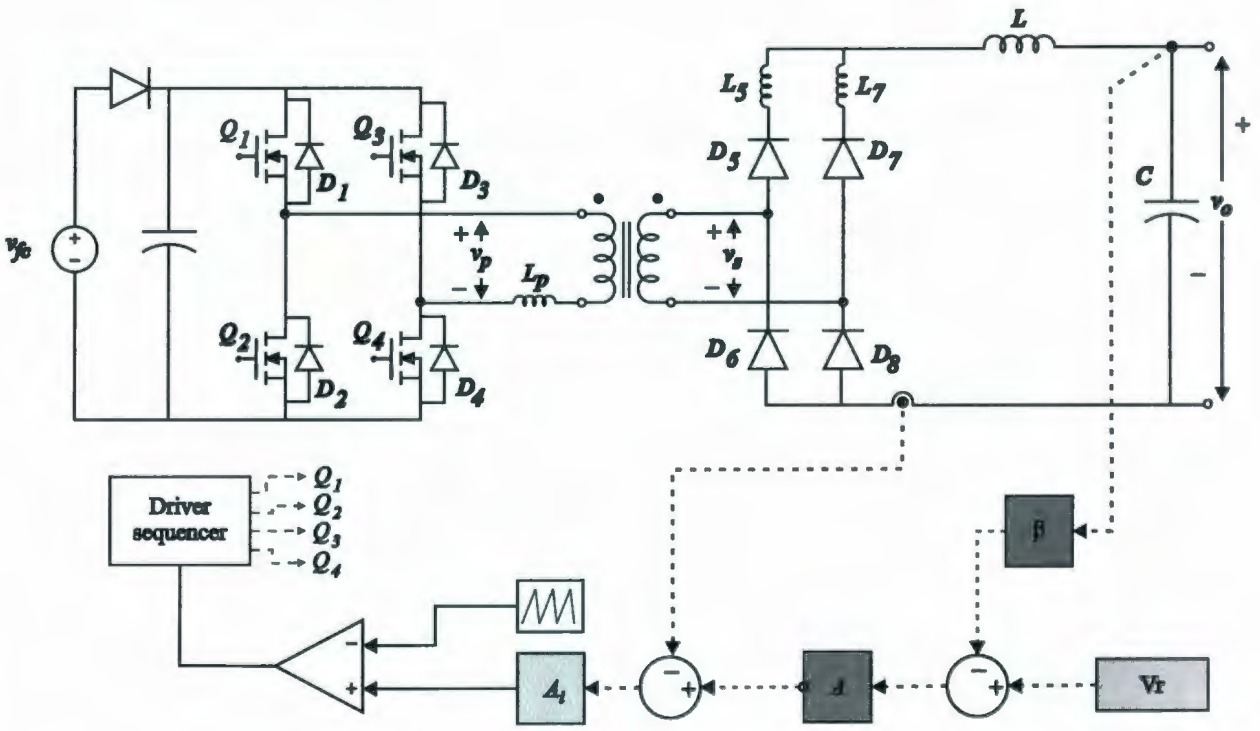


Figure 3.10: Dc-dc converter inner current and outer voltage loop.

first, which is shown in Fig. 3.9. Two different type of windows are employed with $F_S = 3.6$kHz: a) rectangular windows with a length of $L = 60$ points, covering one cycle of the inverter output frequency; and b) Hamming window with a length of $L = 600$, covering ten cycles. While the waveform under linear loading condition is a simple monotonic repetition for every cycle, the information contained in the DFT significantly varies due to the effect of window type and length. This can be seen in Fig. 3.9, where the peaks at dc, 120Hz, 240Hz, and 360Hz can be clearly seen with the Hamming window and barely resolved with the rectangular window. Even though a 600-point Hamming window is required to visualize the peaks, a smaller window (i.e., 60-point) can be used for data processing.

It can also be seen in Fig. 3.9 that the 120Hz component is predominant in the bus voltage (in addition to the strong dc component) with operation under linear

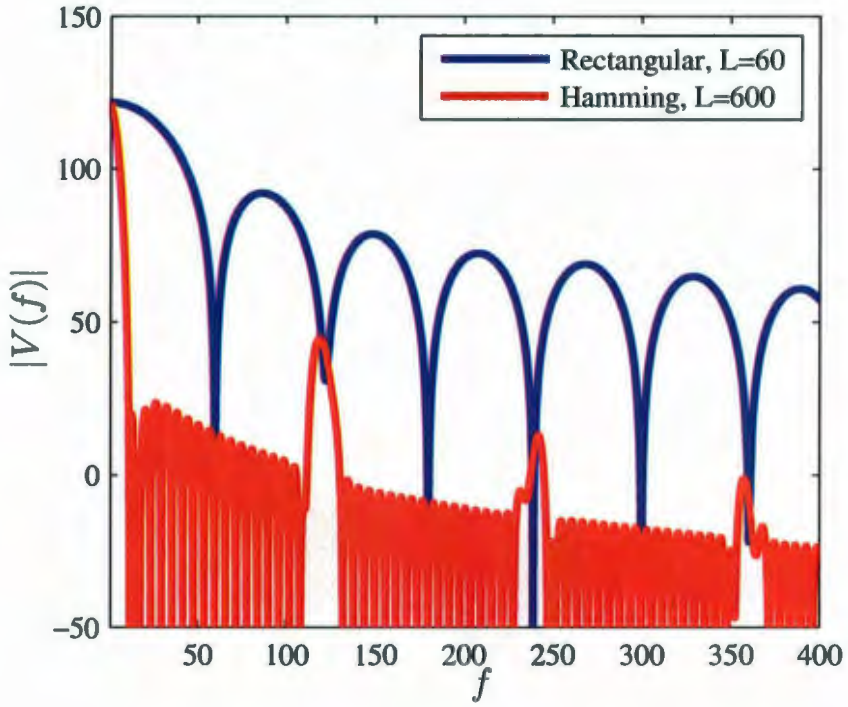


Figure 3.11: Bus voltage spectrum under controlled rectifier pulsating loading condition.

load. This frequency content can be considered as a perturbation to achieve constant current injection in the bus capacitor by means of controlling the average bus voltage. This is explained with the aid of the multi-loop control block diagram presented in Fig. 3.10. If the reference signal of the inner current loop were to be constant, then either the feedback loop (β) or the compensator (A_1) must eliminate the 120Hz perturbation from the bus signal. In the traditional approach to solve this problem, the compensator bandwidth (pole-zero) should be set low enough to eliminate 120Hz signal. Since the single pole provides poor stop band attenuation (-20dB/dec), the overall control bandwidth will be narrow, resulting in a sluggish dynamic response of the converter.

In order to eliminate the 120Hz and harmonics without reducing significantly the

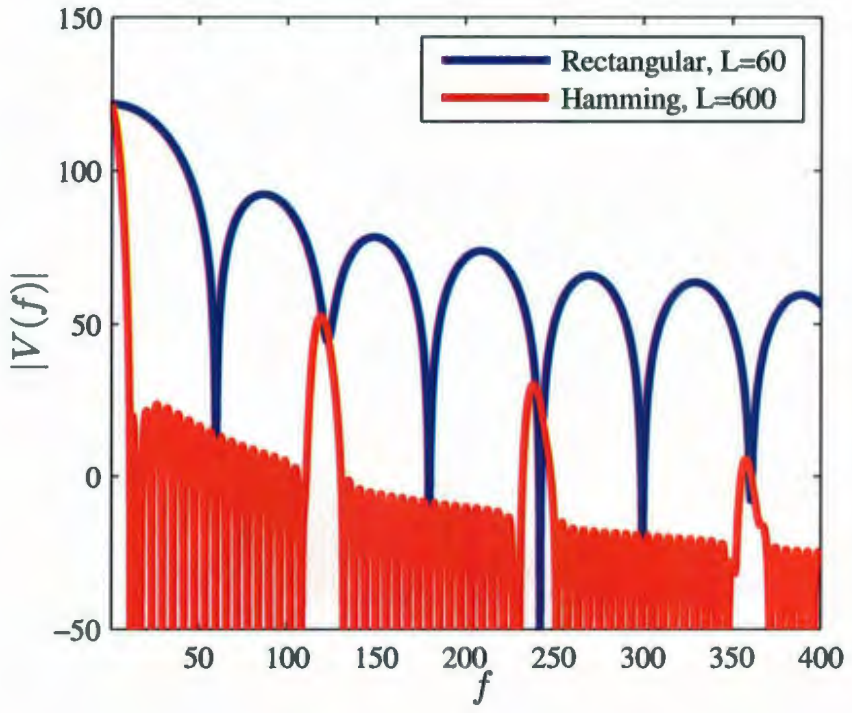


Figure 3.12: Bus voltage spectrum under non-linear loading condition.

control bandwidth of the system, the use of a digital filter with special characteristics is proposed. This filter is placed in the feedback loop (β) to abruptly eliminate the undesired components in the bus voltage feedback signal. However, before carrying out the filter design, the bus spectrum is investigated under pulsating and non-linear loading conditions. Figure 3.11 shows the DFT of the bus voltage under pulsating loading condition. Similar to the previous case, the sampling frequency of $F_S = 3.6$kHz with rectangular windows ($L = 60$) and Hamming window ($L = 600$) is considered. It can be seen that for this case the peaks at 120Hz, 240Hz, 360Hz are larger than the linear counterpart. Finally, the DFT under non-linear load is shown in Fig. 3.12, where the largest peaks at 240Hz and 360Hz can be seen.

From the examination of the DFT of the bus voltage under different loading conditions, the dominance of the fundamental component at 120Hz was identified. As well,

it has been seen that the harmonics at 240Hz and 360Hz become more relevant with pulsating and non-linear load. It is necessary to eliminate those components in the feedback loop (β) of the control system. For this purpose, a digital filter is selected and characterized with the objective of minimizing harware processing requirements in terms of sampling frequency, memory storage capability, and processing overhead.

3.4 Feedback Loop Signal Processing

In this section attention is momentarily focused to solve a fundamental signal processing problem in the feedback loop of the control block (β) in Fig. 3.4. From the behavioral model presented Fig. 3.4, the voltage loop controller of the dc-dc converter can be identified as the high-level system controller in the power generation system. This controller has a dynamic response in the medium frequency range, which is in accordance with the other low dynamics components in the behavioral model. Recall that the other stages in the system have a much higher dynamics and can be represented as ideal current sources (i.e., dc-dc inner current loop and inverter reflected load). The voltage loop controller becomes responsible to control power flow from the FC (constant current extraction) to the inverter input dc bus (swinging bus voltage). In doing so, the controller must comply with the requirement of providing constant current reference signal to the ideal current source in the dc-dc stage while mantaining the highest possible bandwidth.

The objective of this section is to develop a feedback loop using digital signal processing to eliminate the undesired spectral components in the bus voltage signal without deteriorating the phase margin and bandwidth in the voltage outer loop. A Moving Averaging Filter (MAF) is selected to obtain an efficient signal processing block of the swinging bus voltage, which results from a comparative analysis of

discrete time filters presented in Appendix B. Throughout this section, the characteristics of the selected filter are presented in detail to clarify some of the key features and fundamental equations. The effectiveness of the filter is finally evaluated with bus operation under linear, pulsating and non-linear loading conditions.

3.4.1 Moving Averaging Filter Characteristics

This subsection presents the algorithm and characteristic features of MAF. The filtering characteristics are discussed in discrete and continuous domains and represented in linear and logarithmic scale for a better interpretation. Thereafter, in order to demonstrate the MAF effectiveness for this application, the bus voltage under linear, pulsating and non-linear load are filtered and presented graphically.

It has been seen in the comparative analysis in Appendix B that MAF have optimal performance in time domain and limited performance in frequency domain. Nevertheless, since MAF has excellent attenuation characteristics at the frequencies of interest, the overall result is superior in both domains. Based on the comparative analysis the advantages of the MAF can be summarized as follows: the filter has the fastest step response; it is easy to implement; it has efficient computation time; it reduces random noise; it notches the 60Hz and its integer multiples.

The filter is mathematically described by,

$$\bar{v}_{bus}[n] = \frac{1}{M} \sum_{k=0}^{M-1} v_{bus}[n+k] \tag{3.1}$$

where M is the length of the kernel or number of averaging points. The equation provides a single result by convoluting the signal with a rectangular kernel. The

discrete operation can be also performed using a simple recursive algorithm as follows:

$$\bar{v}_{bus}[n] = \bar{v}_{bus}[n-1] + v_{bus}[n+p] - v_{bus}[n+p+1] \tag{3.2}$$

where,

$$p = \frac{(M-1)}{2}$$

As can be seen, the algorithm ca be readily implemented in a fixed point DSP as it only involves summations and subtractions. This is an important requirement as it allows the reduction of the system cost by integrating all the controllers of the power conversion system in one fixed-point DSP platform generally employed for control in power electronics. It should be noted that M values should be stored to process the algorithm (i.e., $M = 60$ for the selected case). Instead of processing the algorithm every $1/60$ seconds, the routine is performed at the sampling frequency ($F_s = 3.6kHz$) to reduce the delay introduced in the discretization and hence the phase lag.

The DFT analytical expression of the MAF is given by,

$$H(\omega) = \frac{1}{M}\frac{sin(\omega M/2)}{sin(\omega/2)} \tag{3.3}$$

which results from transforming a rectangular series of impulses (rectangular window). The expression denotes the presence of the notching effect every $2\pi/M$. Figure 3.13(a) shows the DFT of the MAF depicted in linear scale with $M = 60$. The horizontal axis in the plot represents the discrete angular frequency (top) and the continuous angular frequency (bottom) mapping for $F_s = 3.6kHz$. The figure explicitly shows the unity gain at dc and the periodic notches.

Even though the MAF can be implemented with a recursive algorithm, the filter can be understood in terms of a FIR filter as well (convolution). As expected, MAF

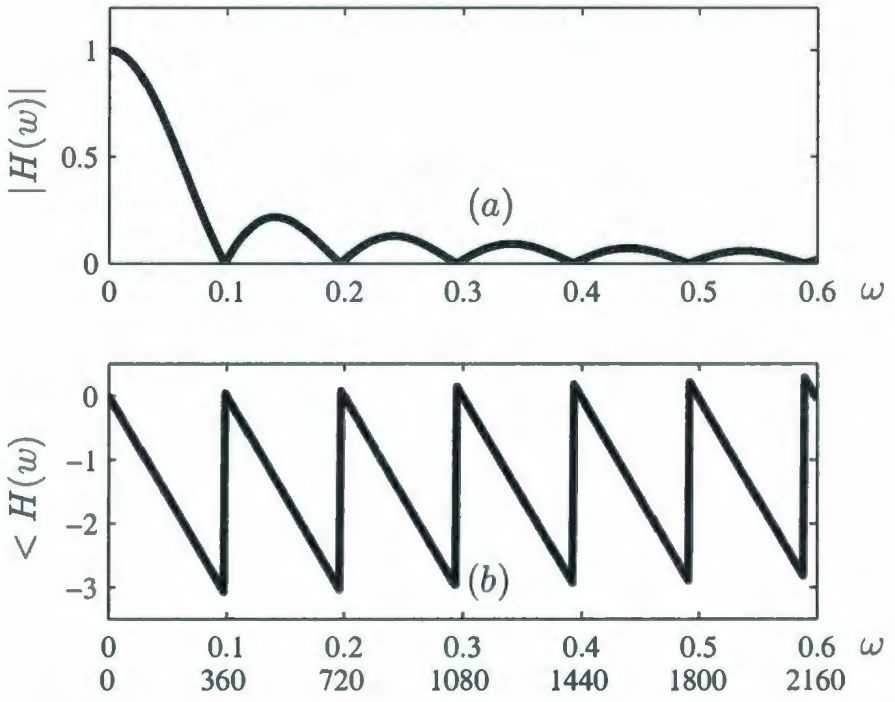


Figure 3.13: Moving Averaging Filter for 60-point and $F_s = 3.6kHz$: a) magnitude in linear scale, and b) phase in radians.

features linear phase which simplifies the understanding and evolution of the phase of the filter. Phase behavior is a complex topic in discrete filter design, yet a very important issue in the stability of a control system. Figure 3.13(b) shows the phase of the MAF depicted in linear scale with $M = 60$. The π jumps in the phase are in accordance with the locations of the discrete zeroes in the unit circle at the frequencies of interest.

While filter design and representation in linear scales is a common practice in discrete time signal processing, control using frequency response analysis is traditionally carried out in log-frequency axis and dB magnitude. Since the digital filter (feedback loop) becomes part of the control loop gain, it becomes necessary to represent the previous results in log scale to interpret them from a control point of view. Figures 3.14(a) and 3.14(b) show the magnitude and phase respectively in dB and logarithmic scales for the analyzed case (MAF, 60-point, $F_s = 3.6kHz$). As well, for comparison purposes, Fig. 3.14(a) and Fig. 3.14(b) show the loop gain magnitude and phase of the inner current loop controller presented in the full-bridge modified topology in Fig. 3.10. The parameter in the dc-dc converter are those listed in Chapter 2, Table 2.1. From the examination of Fig. 3.14(a) it can be inferred that the bandwidth of the feedback loop is significantly narrower than the bandwidth of an inner current loop controller [58, 59]. The feedback loop therefore dominates the dynamics of the system so the compensation (small-signal) needs to be designed according to the characteristics of the feedback loop filter. By simple inspection, it can be deduced that a digital Proportional-Integral (PI) compensator can successfully pull-up the phase and adjust the gain margin to successfully control the system.

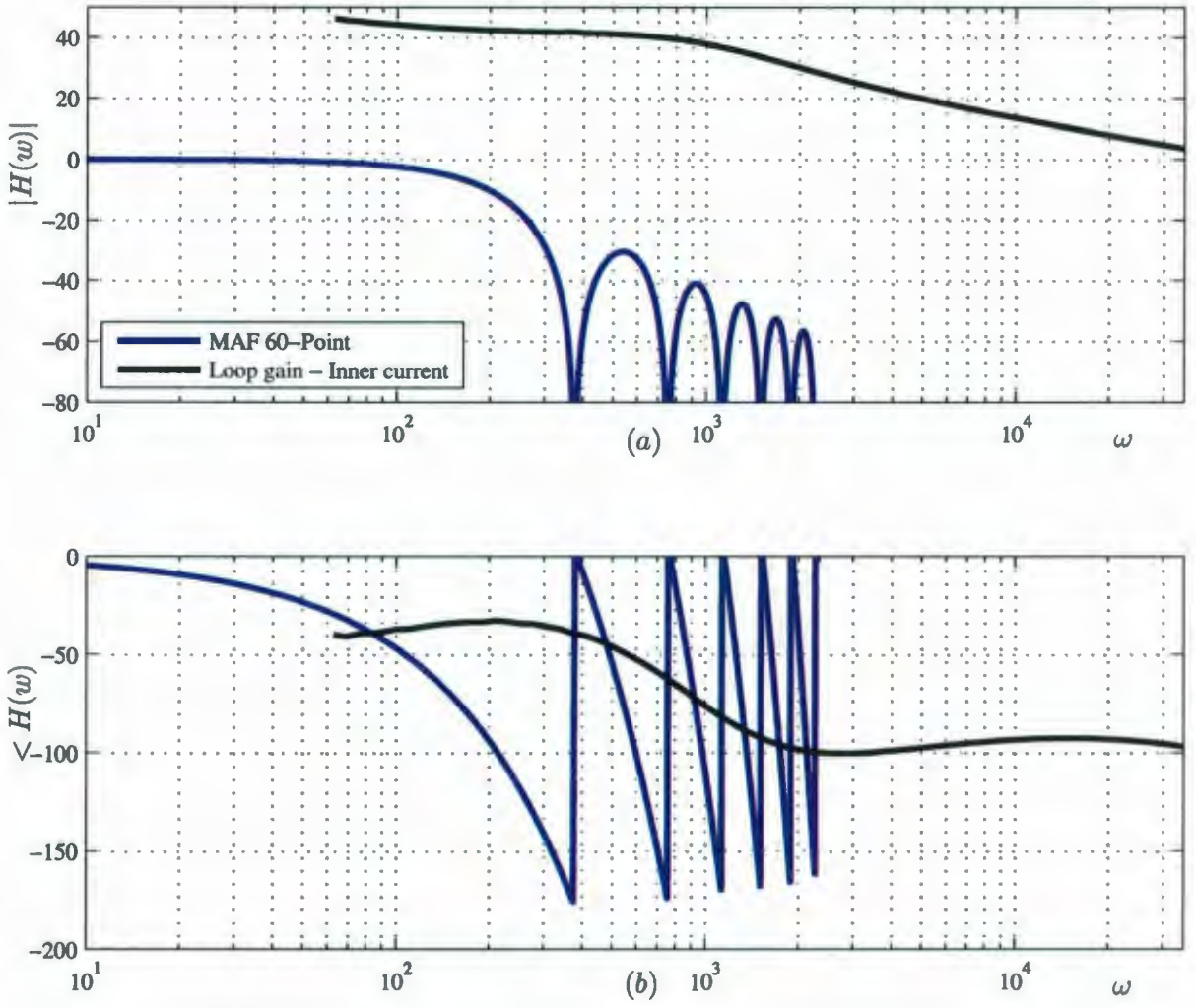


Figure 3.14: Moving Averaging Filter for 60-point and $F_s = 3.6kHz$: a) magnitude in dB, and b) phase in log scale.

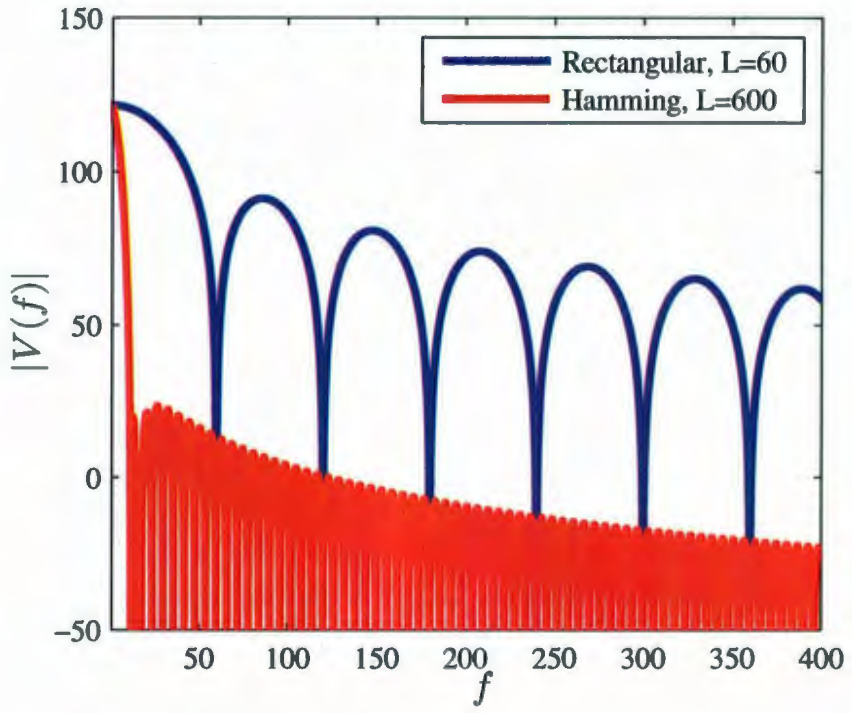


Figure 3.15: Filtered bus voltage spectrum under non-linear loading condition.

3.4.2 Spectrum of the Bus Voltage After Filtering

Throughout the previous subsection, the MAF characteristics were presented to clarify some of the key features and fundamental equations. The theoretical analysis anticipates effective cancelation of undesired components in the bus voltage while preserving simplicity in the practical implementation. In this subsection, the effectiveness of the digital filter is briefly evaluated by examining the spectrum of the bus voltage after filtering non-linear loading conditions.

The bus voltage signal in time domain were presented in Figs. 3.6-3.8 with their respective DTF transforms shown in Figs. 3.9-3.12 indicating peaks at $120Hz$ and harmonics (even and odd). The resulting spectrum after filtering for non-linear loading condition is presented in Fig. 3.15, which is the worse case scenario. Two types of windows are employed namely, Hamming with $L = 600$ and rectangular with $L = 60$.

The rectangular window is used to demonstrate that the spectrum cannot be properly resolved by using a single set of data (i.e., the 60 samples employed to process the MAF). The Hamming window in combination with $L = 600$ (ten sets of data) produces a spectrum with enough accuracy to show that the $120Hz$ has been filtered or eliminated. At the same time, it can be seen that the dc component remained intact. The small side lobes that surround the dc component are the effect of leakage pertaining to the window. It can be seen that the second and third harmonics that are characteristic of this waveforms have been also successfully filtered.

3.5 System in Steady State and Load Transient Operation

In the previous sections, the bus voltage in steady state operation was analyzed with a focus on the time and frequency domain behavior under different loading conditions. Now that the swinging bus principle of operation and signal processing aspects have been clarified, the operation of the entire system under steady state and load transient conditions is studied. The analysis and investigation were carried out in a simulation environment using PLECS, Matlab-Simulink, and custom S-functions. Two cases are investigated starting from steady state condition: a) small transient operation within the inverter input operating range ($v_{nom} \pm \delta$), and b) large transient operation when the bus voltage exceeds the limit of the inverter operating range.

The analysis is carried out with the aid of Fig. 3.16, where the measurement points of interest (voltages and currents) are indicated in the behavioral model. The waveforms are presented from the load to the power source to illustrate the interaction between the stages in the system in the following order: load current i_o (reflected from

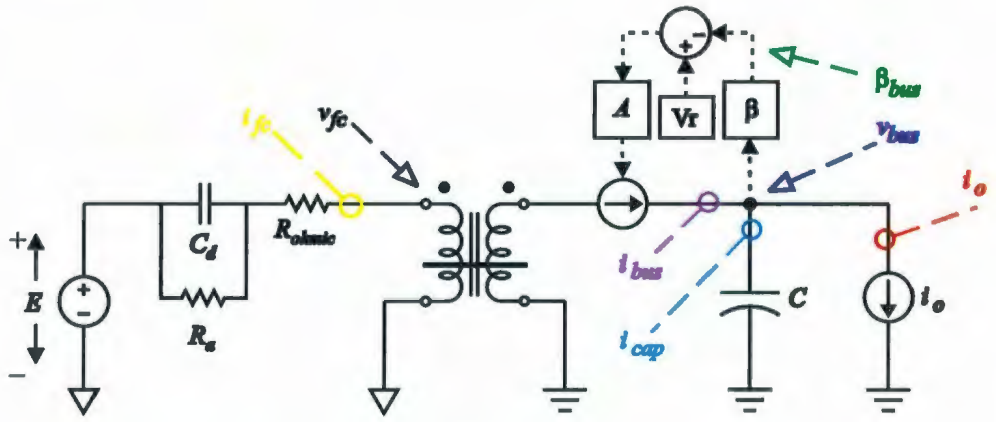


Figure 3.16: System behavioral model: measurement points.

the inverter load in the bus), bus capacitor current i_{cap}, bus voltage v_{bus}, feedback loop signal β_{bus}, bus current injection i_{bus}, FC output voltage v_{fc}, and FC output current i_{fc}.

3.5.1 Small Load Transient Operation

The system response is evaluated for load increments under 10% of the system rated power. The analyses begin in steady state operation prior to the application of the load change. Three typical type of loads employed in the previous sections are evaluated, resistive, pulsating and non-linear, except for the fact that the simulations are performed dynamically.

Figure 3.17 shows the system operating under linear type of load. Five regions in the time axis can be identified in the plot to show the steady state operation in the first portion followed by four systematic load increments. The output current i_o and capacitor current i_{cap} are illustrated in Fig 3.17(a), where the initial and later increase in amplitude can be seen. The moderate bus voltage swing v_{bus} due to the initial medium loading condition is depicted in the first portion Fig 3.17(b). Two basic effects occur as a result of the load current increase. First, the bus voltage

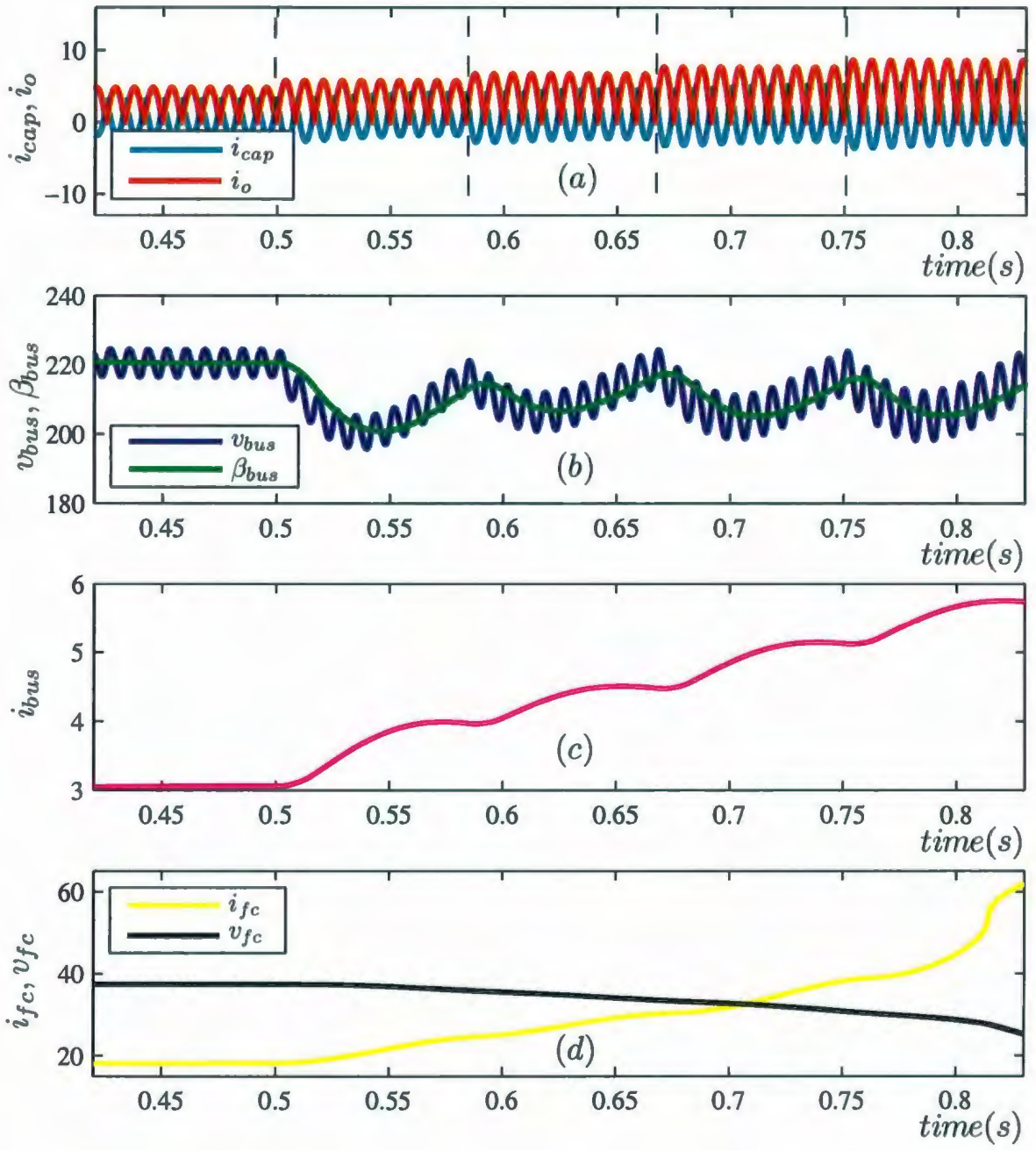


Figure 3.17: System dynamic operation under linear resistive load: a) output current and capacitor current, b) bus voltage and feedback signal, c) bus current, and d) FC output voltage and output current.

experiences a drop and later recovers. Second, the amplitude in the bus voltage swing increases. The bus voltage evolution is similar for every regular load increment. The bus current injection i_{bus} is shown in Fig. 3.17(c). First, the i_{bus} is constant until an initial load change occurs, resulting in an increase in the bus current. The bus current transitions are in accordance with the bus voltage evolution and therefore, a zero charge balance in the bus capacitor is mantained. When the bus current is settling to a constant dc level, a new load transient happens, which is followed by a similar evolution. Finally, the FC voltage v_{fc} and current i_{fc} are depicted in Fig. 3.17(d). The FC delivers the required output power by adjusting i_{fc} and v_{fc} until steady state is reached later in the simulation. The dc-dc transformer in the behavioral model trasfers power from the FC to the bus capacitor. It is important to note that the turns ratio of the trasformer is not constant and depends on v_{fc} and i_{bus} as variables. This can be seen in the i_{bus} evolution, which does not follow the waveform shape of i_{fc} during transients. However, the tranformer ratio ensures that the output power of the transformer matches its input power.

Figure 3.18 shows the system operating under non-linear type of load ($CF = 2.3$). In the first portion of the time axis, the system operates in steady state. Thereafter, four systematic load increments are applied. When the load increases the bus voltage experiences a drop and later recovers like in the previous case. As well, the amplitude of the swing increases when the load increases. Clearly, the bus voltage swing is larger than the other cases and so does the minimum value that results when a load change in applied. Figure 3.18(c) shows the bus current injection i_{bus}, which is constant in the beginning and is followed by increases. Again, like in the previous case, when the bus current is settling to a constant dc level, a new load transient happens, which is followed by a similar evolution. The FC voltage v_{fc} and current i_{fc} are depicted in Fig. 3.18(d), denoting a softer transition as compared to the previous case. It can

be concluded that the operating range of the inverter input voltage is affected by the voltage swing in steady state, and also the bus voltage drop under small load transients.

The results from Fig. 3.17and Fig. 3.18 are employed to define the inverter input voltage range ($v_{nom} \pm \delta$). Even though several cycles of the inverter output frequency are required to fully recover from a sudden load change, the bus voltage should remain within the specified range. In this case the minimum bus voltage is set to $v_{nom} - \delta = 180V$, which is close to the crest of the inverter sinusoidal output waveform ($120 \times \sqrt{2}$). Also, the bus nominal voltage (set at $220V$ in the simulation) can be regulated to provide adequate margin for the voltage drop under small load transients.

3.5.2 Large Load Transient Operation

It has been seen in the previous subsection that the bus voltage not only swings but also experiences a drop when a sudden load change is applied. In this subsection, the behavior of the system under large transients that are likely to force the bus voltage to go below the inverter nominal opearting voltage is examined. In order to overcome the effect of large transients, an adaptive control scheme is proposed which is conceptually shown in 3.19. The control scheme combines swinging bus operation with stiff bus operation. The swinging bus operation is employed when the bus voltage is within the range and the stiff bus operation is employed when the bus voltage is outside the inverter operating range. The objective is to obtain fast recovery in the bus voltage during large load transient at the expense of short duration ripple current operation.

Figure 3.20 shows the system operating under linear type of load. Three intervals in the time axis can be seen, steady state operation in the first portion, load transient,

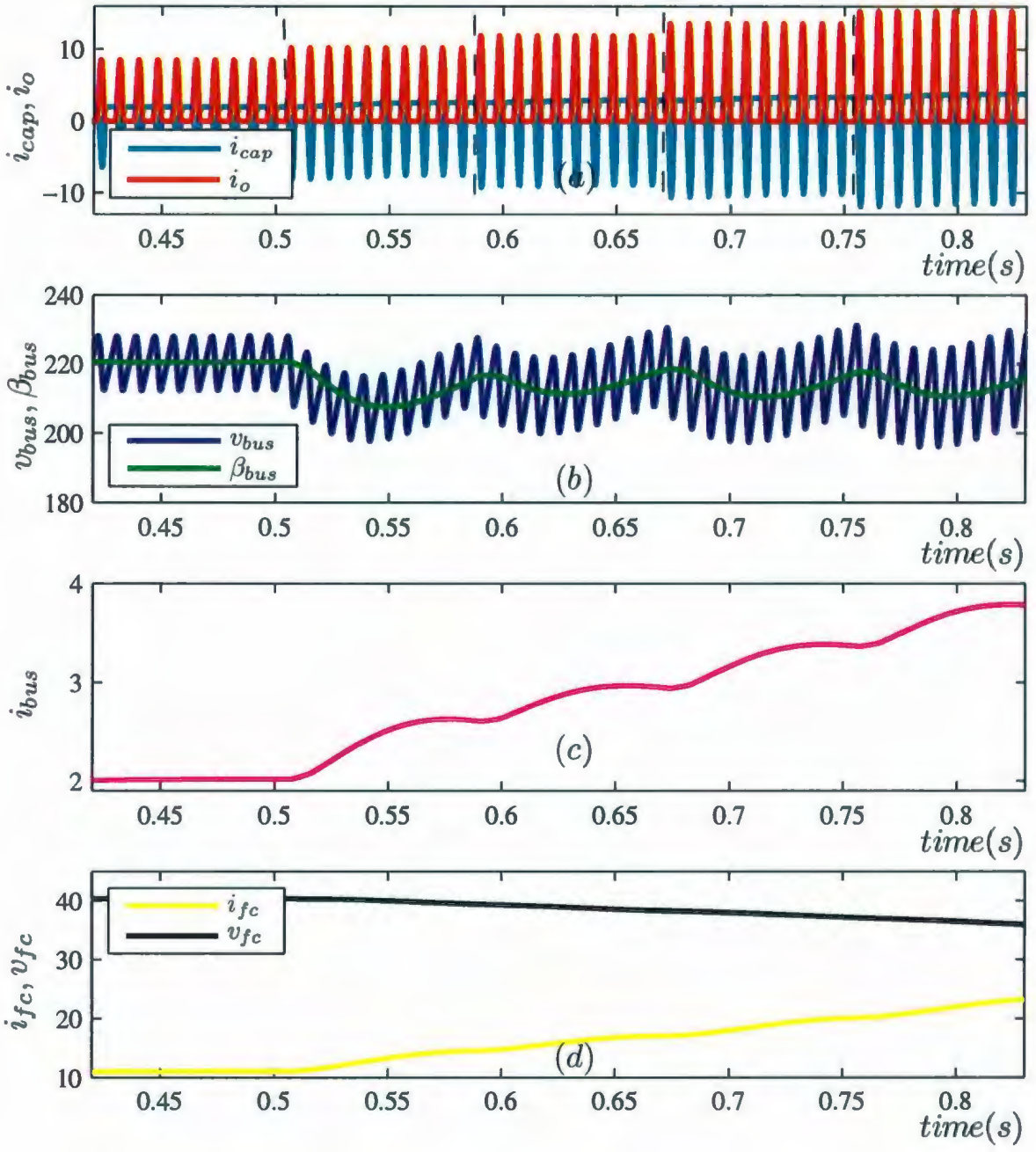


Figure 3.18: System dynamic operation under non-linear resistive load: a) output current and capacitor current, b) bus voltage and feedback signal, c) bus current, and d) FC output voltage and output current.

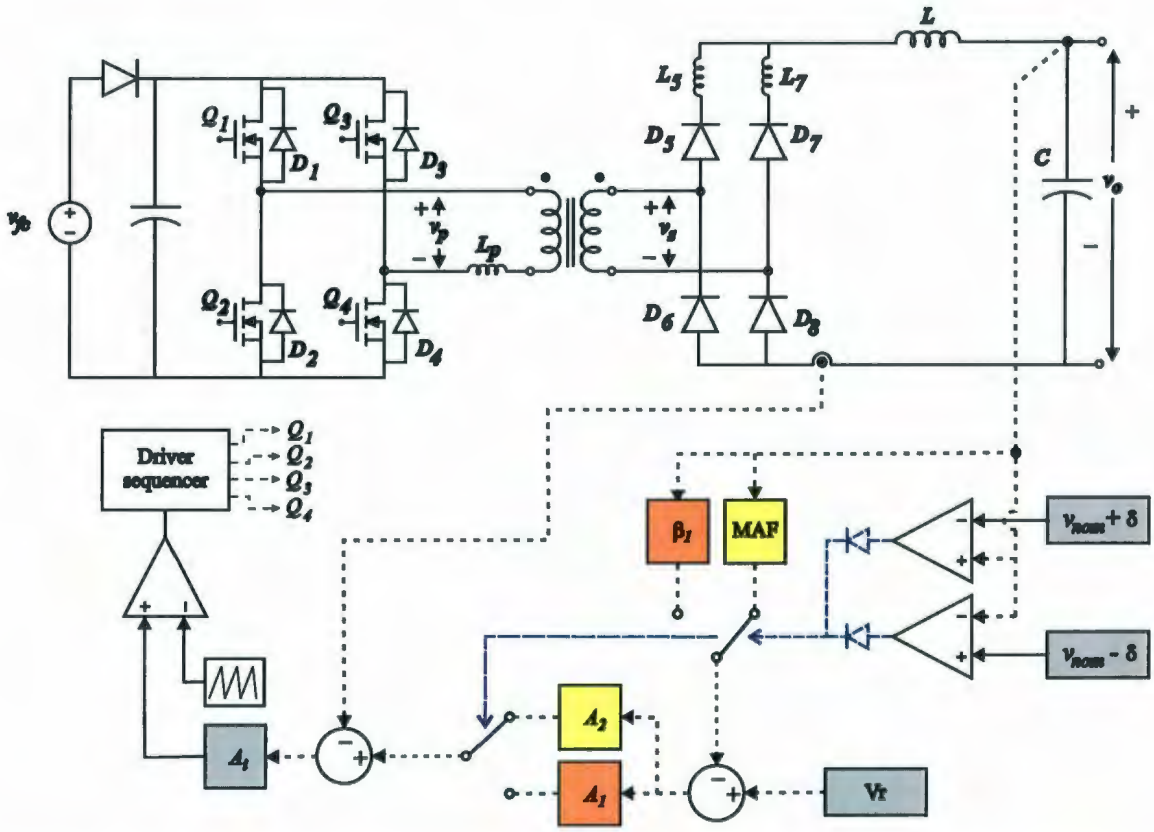


Figure 3.19: Adaptive control scheme for steady and large load transients operation.

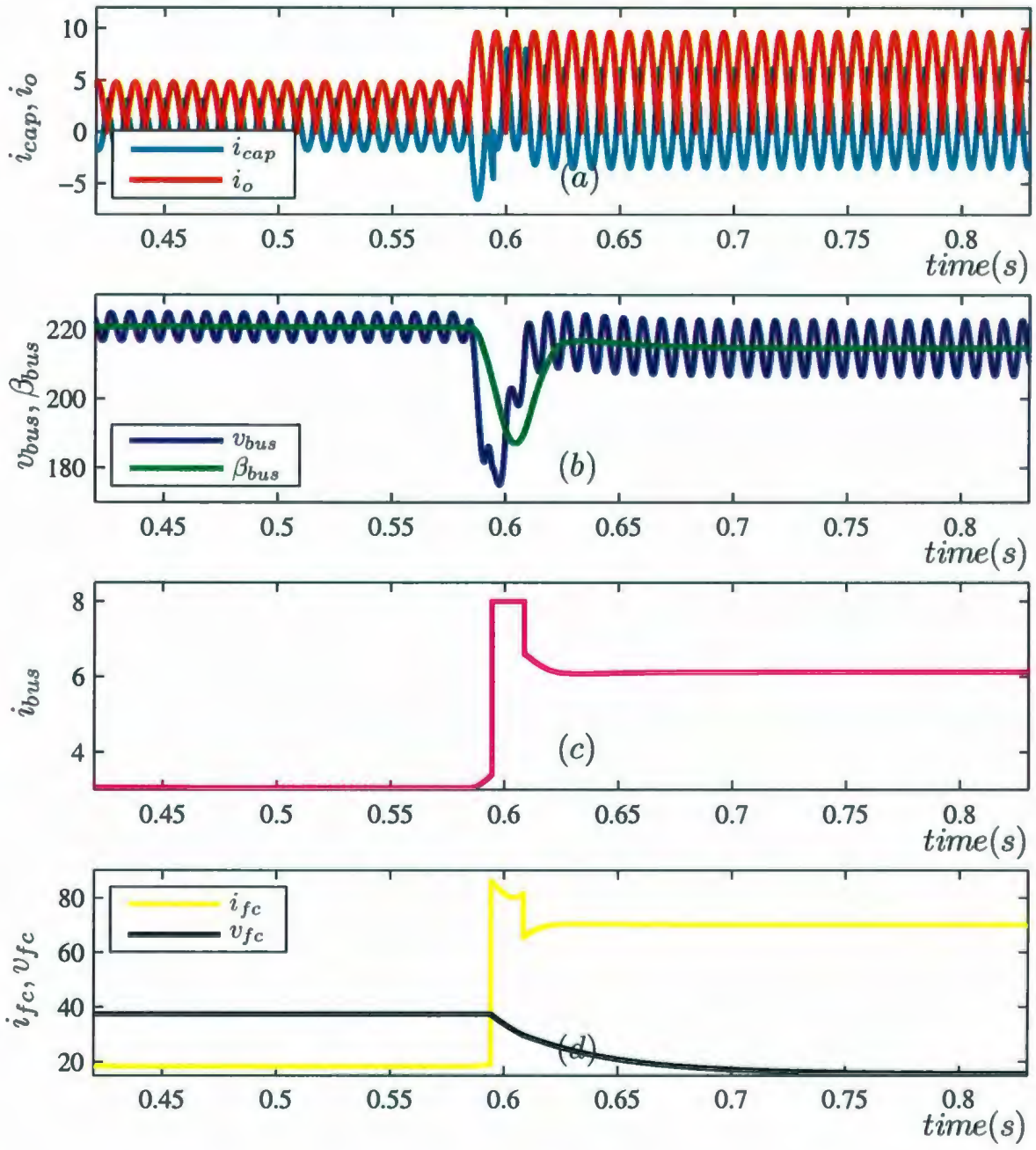


Figure 3.20: System large transient operation under linear resistive load: a) output current and capacitor current, b) bus voltage and feedback signal, c) bus current, and d) FC output voltage and output current.

and transient tail. The output current i_o and capacitor current i_{cap} are illustrated in Fig 3.20(a), where a sudden large increase in i_o is shown. The bus voltage v_{bus} is initially moderate, as shown in Fig. 3.17(b). When the load transient occurs, the bus voltage experiences a dramatical drop below the nominal minimum bus voltage ($180V$). The adaptive control changes to stiff bus operation to rapidly recover the bus voltage. In this particular case, the bus current i_{bus} shown in Fig. 3.20(c) reaches its maximum to inject charges in the bus capacitor to mantain a charge balance. Once the bus voltage is restored within the normal operating range, the controller returns to swinging bus operation to avoid ripple current in the FC. Similar to the previous cases, the voltage swing during the last interval is larger under this heavy loading condition. The FC voltage v_{fc} experiences a faster transition due to the discharge of the double layer capacitor C_d, as depicted in Fig. 3.20(d). As well, the FC current i_{fc} in the transient is inherently limited by the i_{bus} current.

3.6 Summary

In this chapter, the analysis of the FC power generation system has been presented at the system level covering the important interactions between the various components. A medium to low frequency behavioral model was presented to clarify the current reflection from the inverter load through the dc-dc converter and the FC. The importance of the bus voltage charge balance was identified as the key mechanism to successfully operate the system and establish the requirement for the inverter input range. As a result, the proposed swinging bus scheme was thoroughly evaluated in time and frequency domain. Signal processing aspects to control the dc-dc converter were also examined resulting in the selection of a discrete Moving Averaging Filter in the control feedback loop. The system operation under steady state and load transient

was investigated. An adaptive control scheme that combines swinging bus operation in steady state and stiff bus operation during large load transients was proposed and investigated by simulation. The system level analysis presented in this chapter provided a comprehensive view to the interactions between the various components of the system and developed a solution to successfully overcome them.

Chapter 4

Swinging Bus Inverter Using the Natural Switching Surface

In the process of converting unregulated dc voltage from the FC stack into ac (120/220V at 60/50Hz), a novel high efficiency intermediate power conversion stage was employed to provide voltage elevation and galvanic isolation while eliminating reflected ripple current. The last stage of the proposed high-performance power conversion system is the inverter (dc to ac conversion), which is addressed in this chapter. The objective of this subsystem is to produce high quality output power even under extreme operating conditions (wide input voltage range and loading capability). As discussed in Chapter 1 and 3, the low frequency ripple current generated by the inverter input current must be eliminated or absorbed by the dc-dc power conversion stage to prevent unacceptable reduction of power availability and efficiency in the FC. As a result of the combined effects of the inverter operation and the ripple elimination technique in the dc-dc power stage, the dc bus capacitor voltage swings with double the inverter output frequency to absorb low frequency ripple current. Since inverters are traditionally operated with stiff dc input voltages, the voltage swing at the input

terminals of the inverter (swinging bus) presents an unprecedented challenge for the control scheme of the inverter.

In order to comply with stringent standards for transient and steady state performance, a control scheme based on curved switching surfaces (SS) is proposed for the inverter. The use of curved SS to control power converters is an emerging method for fast transient response that has been gaining attention recently [41, 42, 61]. In this chapter, the analysis of a novel curved SS is performed using a versatile geometrical method in the normalized domain. As will be seen, the proposed normalization technique provides remarkable insight into the behavior of system, and the approach is general and applicable to any possible inverter. As a result of a rigorous evaluation, a control law for inverters defined as natural SS is proposed and thoroughly characterized for operation under fixed and swinging bus. Throughout this chapter, novel operating characteristics such as fixed switching frequency, monopolar, bipolar, and mixed operating modes are analytically investigated using the natural SS and validated through experimentation.

4.1 Introduction to Boundary Control in Inverters

Buck derived inverters, full- and half-bridge topologies, can be classified as simple cases of variable structure systems that can be controlled by boundary or geometric control [43, 62–66]. Among boundary controllers, sliding-mode using linear control laws and hysteresis band has been extensively investigated for both dc-dc buck converters and buck derived inverters [43, 66–74]. Under this control scheme, the state variables of the system experience fast natural transitions until the switching surface (SS) is intersected. Thereafter, sliding-mode regime around the SS surface forces continuous changes in the structure of the converter, producing a reduction in the

order of the system. The slow sliding transition (compared to natural trajectories) finally reaches the target operating point. In order to improve the dynamic response of buck derived converters, curved SSs were proposed to avoid sliding and reach the target operating point faster (by extending the natural transitions).

A particular case of second-order SS with enhanced dynamic response was derived using capacitor charge balance equations [42], and compared to the first-order SS. Subsequently, the natural unloaded SS for dc-dc buck converters was investigated [41] showing improved transient characteristics (compared to the second-order SS), especially under light loading conditions. Recently, a higher-order SS was presented to control full-bridge inverters, which was also derived from capacitor charge balance equations (like the second-order SS) [61]. In this case, the resistive loading condition was considered as part of the control law and averaging assumptions were made in the formulation of the control law.

By careful study and evaluation of previous work in the area, a number of fundamental technical problems were identified: a) Derivation of control laws using time domain averaging assumptions lead to formulation inaccuracies. This has particular impact on the large signal operation of the system. b) The concept of target operating point is only applicable to dc-dc converters [41]. Since inverters have a sinusoidal reference signal, the control objective must be treated as a target operating trajectory, rather than a target operating point. This aspect also affects the performance of the control law. c) The set of rules or management rules for a given curved SS will play an important role to achieve optimal results. For example, even though the proposed scheme in [61] has good dynamic behavior, the system operates with variable switching frequency due to the management rules. This produces undesirable electromagnetic perturbations and additional filtering problems. d) The involvement of unknown parameters in the control law must be

avoided (for example, the load resistance in the scheme proposed in [61]). The objective of a good control scheme is to compensate for unknown disturbances. e) Swinging bus operation for FC power conversion using curved SS has not been addressed in the literature.

This chapter proposes a number of advanced technical solutions to overcome the limitations described above. The analytical and experimental results presented in this chapter are significant advancement in the area of boundary control using curved SS. As will be seen, the control strategy and formulation method are not only applicable to FC power conversion but also relevant to inverters in general. In order to avoid inaccuracies introduced by simplification or assumptions, the analysis presented in this chapter is entirely performed using a versatile geometrical analysis. Both the output voltage and the capacitor current are considered as varying references to establish a more accurate control law with enhanced performance. This concept is defined as target operating trajectory instead of target operating point. The proposed normalization technique provides remarkable insight into the behavior of the inverters, leading to a pure geometrical treatment that is general and applicable to any possible inverter. As a result of the analysis, a control law for inverters defined as natural SS is proposed and thoroughly characterized under fixed and swinging bus conditions. In addition to the enhanced dynamic response, fixed frequency operation is one of the key features of the proposed control scheme. In order to formally demonstrate fixed frequency operation, a transformation from the natural SS to its PWM equivalent is performed revealing duality between boundary control using curved SS and traditional PWM. This is a significant advancement towards the unification and understanding of the traditional modulation scheme and modulation produced by curved SSs. Finally, an additional novel concept is explored: operation in mixed monopolar and bipolar mode using the natural SS. This new

mixed operating mode overcomes physical limitations of the inverter structure in monopolar mode around the region of zero voltage crossings. The problem associated with the operating modes are first identified and various solutions are investigated. Experimental results of a 1.5 kVA inverter operating at fixed moderate frequency are presented to validate the natural SS performance, illustrate the benefits of the normalization technique, and demonstrate the monopolar and mixed operating modes under fixed and swinging bus.

4.2 Normalization of Full Bridge Inverter Topology

Prior to performing the normalization, the analysis starts with a basic review of a full bridge inverter with its possible structures as shown Fig. 4.1 and Fig. 4.2. For simplicity the parasitic elements (e.g., switch voltage drop, capacitor equivalent series resistance (ESR), etc.) are neglected. The inverter can be represented with a system of differential equations as follows:

$$C\frac{dv_o}{dt} = i_L - i_o \tag{4.1}$$

$$L\frac{di_L}{dt} = v_{cc}\, u - v_o \tag{4.2}$$

As can be seen in Fig. 4.1, the voltage applied to the output filter can take two active levels, v_{cc} and $-v_{cc}$ depending on the state of the switches and the direction of the current. This is represented in (4.2) by $u = 1$ and $u = -1$ for v_{cc} and $-vcc$

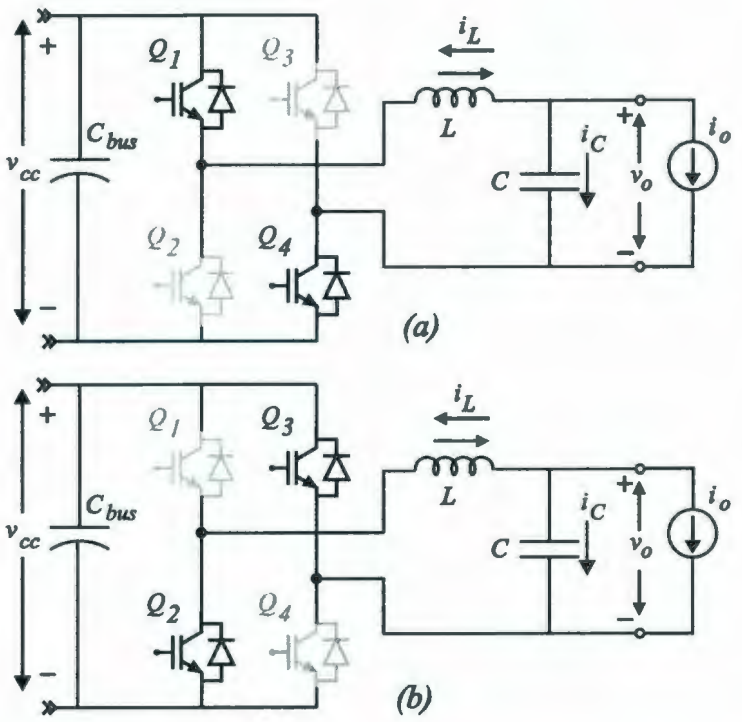


Figure 4.1: Full-bridge inverter structures: a) v_{cc} and b) $-vcc$ applied to the output filter.

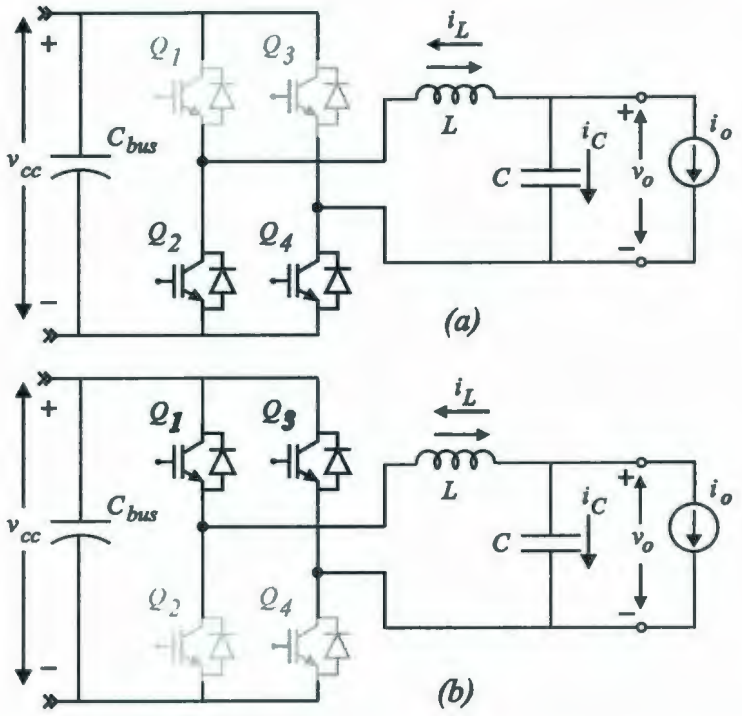


Figure 4.2: Full-bridge inverter structures: short circuit applied to the output filter.

respectively. A short circuit or zero state can also be applied to the output filter when $u = 0$ in (4.2) as depicted in Fig. 4.2. In order to simplify the mathematical representation of the inverter, a normalization technique is employed to disengage some of the parameters of the converter. The normalization is performed by using the filter characteristic impedance $Z_o = \sqrt{L/C}$, natural frequency $F_o = 1/T_o = 1/(2\pi\sqrt{LC})$, and the converter reference voltage v_r as base quantities:

$$v_{xn} = \frac{v_x}{v_r} \tag{4.3}$$

$$i_{xn} = \frac{i_x}{v_r} Z_o \tag{4.4}$$

yielding normalized differential equations,

$$\frac{dv_{on}}{dt} = \frac{i_{Ln} - i_{on}}{\sqrt{LC}} \tag{4.5}$$

$$\frac{di_{Ln}}{dt} = \frac{v_{ccn}\, u - v_{on}}{\sqrt{LC}} \tag{4.6}$$

where the subscript n indicates a normalized variable. Solving (4.5) and (4.6), and performing a change of variable to obtain time normalization $t_n = t/T_o$, a simplified solution independent of L and C is obtained as follows:

$$v_{on}(t_n) = [v_{on}(0) - v_{ccn}u]\, cos\,(2\pi t_n) + [i_{Ln}(0) - i_{on}]\, sin\,(2\pi t_n) + v_{ccn}u \tag{4.7}$$

$$i_{Ln}(t_n) = [i_{Ln}(0) - i_{on}]\, cos\,(2\pi t_n) - [v_{on}(0) - v_{ccn}u]\, sin\,(2\pi t_n) - i_{on} \tag{4.8}$$

As well, the normalized capacitor current (particularly important in this work) is obtained as follows:

$$i_{Cn}(t_n) = -\left[v_{on}(0) - v_{ccn}u\right] sin\left(2\pi t_n\right) + \left[i_{Ln}(0) - i_{on}\right] cos\left(2\pi t_n\right) \tag{4.9}$$

As shown in (4.7), (4.8), and (4.9) the behavior of the converter is mathematically represented in a normalized time domain (independent of L and C). This normalized mathematical representation establishes a number of important relations that will be investigated to obtain the natural trajectories of the system and a curved SS for high performance inverter control.

4.3 Derivation of the Inverter Natural Trajectories

This section provides an insightful analysis of the inverter control objectives. The analysis is presented using a unique normalized graphical representation which is valid for any possible inverter. Taking advantage of the generality of the normalized expressions derived in Section 4.2, the natural trajectories of the inverter towards an arbitrary target operating trajectory are derived. As will be seen, the findings provided in this and the following sections result in significant advancements in the area of inverter boundary control using curved SSs.

In order to successfully derive the desired control law, the initial conditions $i_{Ln}(0)$ and $v_{on}(0)$ based on the steady state operation of the inverter should be carefully evaluated. Even though the full-bridge inverter is a buck derived topology, the initial conditions in this application significantly vary from that of a buck dc-dc converter. This has notable impact on the mathematical derivation of the control law.

First, and unlike its dc-dc counterpart, the inverter deals with a sinusoidal varying

reference with a given amplitude v_{rp} and frequency f_L. Second, and not so evident, the filter capacitor does not have zero current in steady state operation. Instead, a leading sinusoidal current with ripple waveform is obtained in steady state operation. These two waveforms determine the target operating trajectory in the inverter as opposed to a single target operating point in the dc-dc counterpart.

Both the desired output voltage and capacitor current target trajectories can be represented in normalized form by the simple application of the base quantities and time variable transformation,

$$v_{rn}(t_n) = sin\left(\frac{\omega_L}{\omega_o} 2\pi t_n\right) \tag{4.10}$$

where the peak value of the output voltage v_{op} is used as the voltage base quantity. The corresponding normalized capacitor current trajectory is given by

$$i_{Crn}(t_n) = \frac{\omega_L}{\omega_o} cos\left(\frac{\omega_L}{\omega_o} 2\pi t_n\right) \tag{4.11}$$

Solving to eliminate t_n and since $cos\,(sin^{-1}x) = \sqrt{1-x^2}$, the target operating trajectory is given by,

$$v_{rn}^2 + \frac{i_{Crn}^2}{\omega_L/\omega_o} = 1 \tag{4.12}$$

which represents an ellipse with semiminor axis a and semimajor axis b,

$$\frac{(x)^2}{a^2} + \frac{(y)^2}{b^2} = 1. \tag{4.13}$$

It should be noted that the ratio between the inverter fundamental frequency ω_L and the filter natural frequency ω_o is a non-dimensional quantity. As will be explained, this ratio plays a critical role in the design of inverters using curved SSs. Figure 4.3

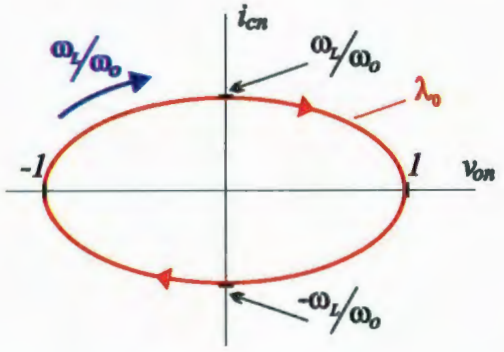


Figure 4.3: Inverter normalized target operating trajectory.

shows a graphical representation (phase plane) of the target operating trajectory (λ_0) in the normalized inverter. The following important concepts can be inferred from an examination of Fig. 4.3:

- The normalized rotational speed of the elliptical trajectory is less than 1 (The filter natural frequency is generally greater than the inverter fundamental frequency).
- The normalized capacitor peak current is equal to the normalized rotational speed.
- The appearance of the ellipse will approach a circle as ω_o approaches ω_L

Now, the initial conditions can be deduced from (4.11) and (4.10) to satisfy,

$$v_{on}(0) = v_{rn} \tag{4.14}$$

$$i_{Ln}(0) - i_{on} = i_{Crn} \tag{4.15}$$

in which the output voltage is equal to the normalized reference voltage and the normalized capacitor current should match the difference between the normalized output current and inductor current.

Now that the initial conditions have been successfully established, the converter natural trajectories that intersect the target operating trajectory can be derived. By employing a set of trigonometrical identities,

$$A\ sin(x) + B\ cos(x) = \sqrt{A^2 + B^2}\ sin[x + tan^{-1}(B/A)]$$

$$\text{and} \quad sin\left[cos^{-1}(x)\right] = \sqrt{1 - x^2},$$

t_n is eliminated from (4.7) and (4.9) yielding a generalized expression for the converter natural trajectories (transformation from parametric equations to Cartesian coordinates),

$$\lambda = {i_{Cn}}^2 - {i_{Crn}}^2 + (v_{on} - v_{ccn}u)^2 - (v_{rn} - v_{ccn}u)^2 \tag{4.16}$$

It is important to note that the natural trajectories presented in (4.16) are valid for any possible inverter regardless of the filter values (L and C), output voltage, fundamental frequency, filter cutoff frequency, and switching frequency.

The geometrical interpretation of the proposed natural trajectories is described in Section 4.4. First, the steady state output voltage is considered as a simple target operating point in which the capacitor current is equal to zero. Thereafter, a more elaborated description of the operation of the inverter with an actual target operating trajectory is developed.

4.4 Geometrical Analysis of the Natural Trajectories

The geometrical characteristics of the natural trajectories are initially evaluated using two simple target operating points. In this particular case $v_{rn} = 1$ combined with $i_{Crn} = 0$, and $v_{rn} = -1$ with $i_{Crn} = 0$ are employed. This, in combination with the switch control action ($u = 1$, $u = 0$, and $u = -1$) results in five possible natural trajectories:

$$\lambda_A = i_{Cn}^2 + (v_{on} - v_{ccn})^2 - (1 - v_{ccn})^2 = 0 \tag{4.17}$$

$$\lambda_B = i_{Cn}^2 + {v_{on}}^2 - 1 = 0 \tag{4.18}$$

$$\lambda_C = i_{Cn}^2 + (v_{on} + v_{ccn})^2 - (-1 + v_{ccn})^2 = 0 \tag{4.19}$$

$$\lambda_D = i_{Cn}^2 + (v_{on} + v_{ccn})^2 - (1 + v_{ccn})^2 = 0 \tag{4.20}$$

$$\lambda_E = i_{Cn}^2 + (v_{on} - v_{ccn})^2 - (-1 - v_{ccn})^2 = 0 \tag{4.21}$$

All five natural trajectories represent a perfect circle in a phase plane plot (normalized output voltage versus normalized capacitor current) that can alternatively described by

$$(x - x_o)^2 + y^2 = r^2 \tag{4.22}$$

where, $x = v_{on}$, $x_o = v_{ccn}\ u$, $y = i_{Cn}$, and $r = v_{rn} - v_{ccn}\ u$.

The natural trajectories are shown in Fig. 4.4 with remarkable simplicity. The dots located at $v_{on} = 1$ and $v_{on} = -1$ indicate the target operating points for a positive and negative voltage reference respectively. As can be seen in Fig. 4.4(a) and (b) the target operating point $v_{rn} = 1$ can be reached with four natural trajectories (circles). As well, the target operating point $v_{rn} = -1$ can be reached by four circles,

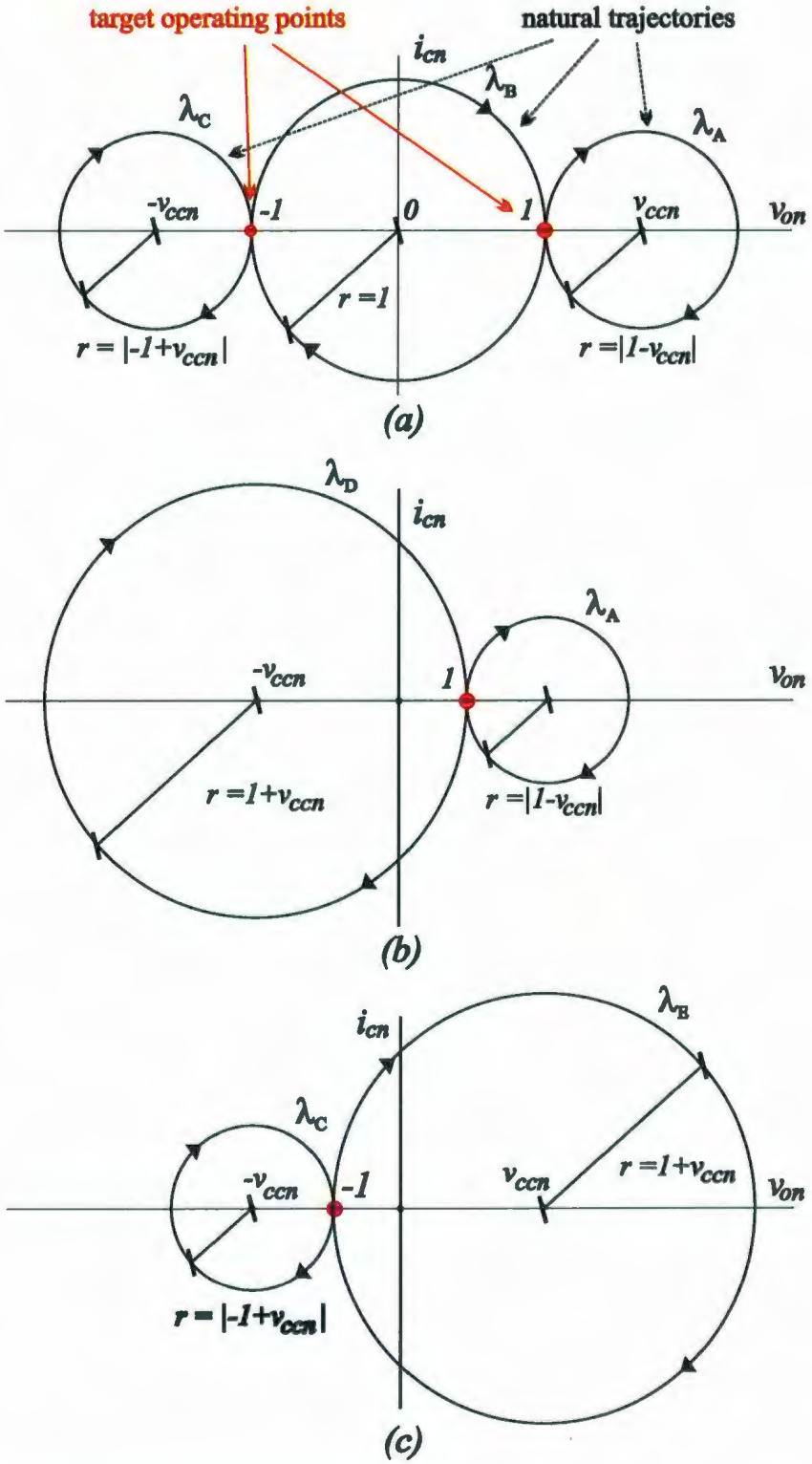


Figure 4.4: Inverter natural trajectories for $v_{rn} = 1$, $v_{rn} = -1$, and $i_{Crn} = 0$: a) Unipolar mode of operation, b) and c) Bipolar mode of operation.

as indicated in Fig. 4.4(a) and (c). A simple, yet powerful conclusion is obtained by visual inspection of Fig. 4.4: the inverter can be operated in unipolar mode (λ_A, λ_B, and λ_C) or bipolar mode (λ_A, λ_C, λ_D, λ_E) to achieve any desired operating point. This provides a unique modulation feature that will be investigated in Section 4.5.

The analysis is extended to a target operating trajectory instead of a single operating point. By combining the target operating trajectory (Fig. 4.3), equation (4.16), and the switch control action ($u = 1$, $u = 0$, and $u = -1$), three possible generalized natural trajectories are obtained as follows:

$$\lambda_1 = i_{Cn}^2 - i_{Crn}^2 + (v_{on} - v_{ccn})^2 - (v_{rn} - v_{ccn})^2 \tag{4.23}$$

$$\lambda_2 = i_{Cn}^2 - i_{Crn}^2 + (v_{on})^2 - (v_{rn})^2 \tag{4.24}$$

$$\lambda_3 = i_{Cn}^2 - i_{Crn}^2 + (v_{on} + v_{ccn})^2 - (v_{rn} + v_{ccn})^2 \tag{4.25}$$

As can be inferred from (4.23), (4.24), and (4.25), the natural trajectories contemplate any arbitrary target point or target trajectory defined by the reference output voltage v_{rn} and reference capacitor current i_{Crn}. In the particular case of an inverter v_{rn} and i_{Crn} are defined by (4.10) and (4.11). In order to illustrate this concept, Fig. 4.5 shows a conceptual graphical representation of the natural trajectories of (4.23), (4.24), and (4.25) that intersect an arbitrary point within the inverter desired operating trajectory.

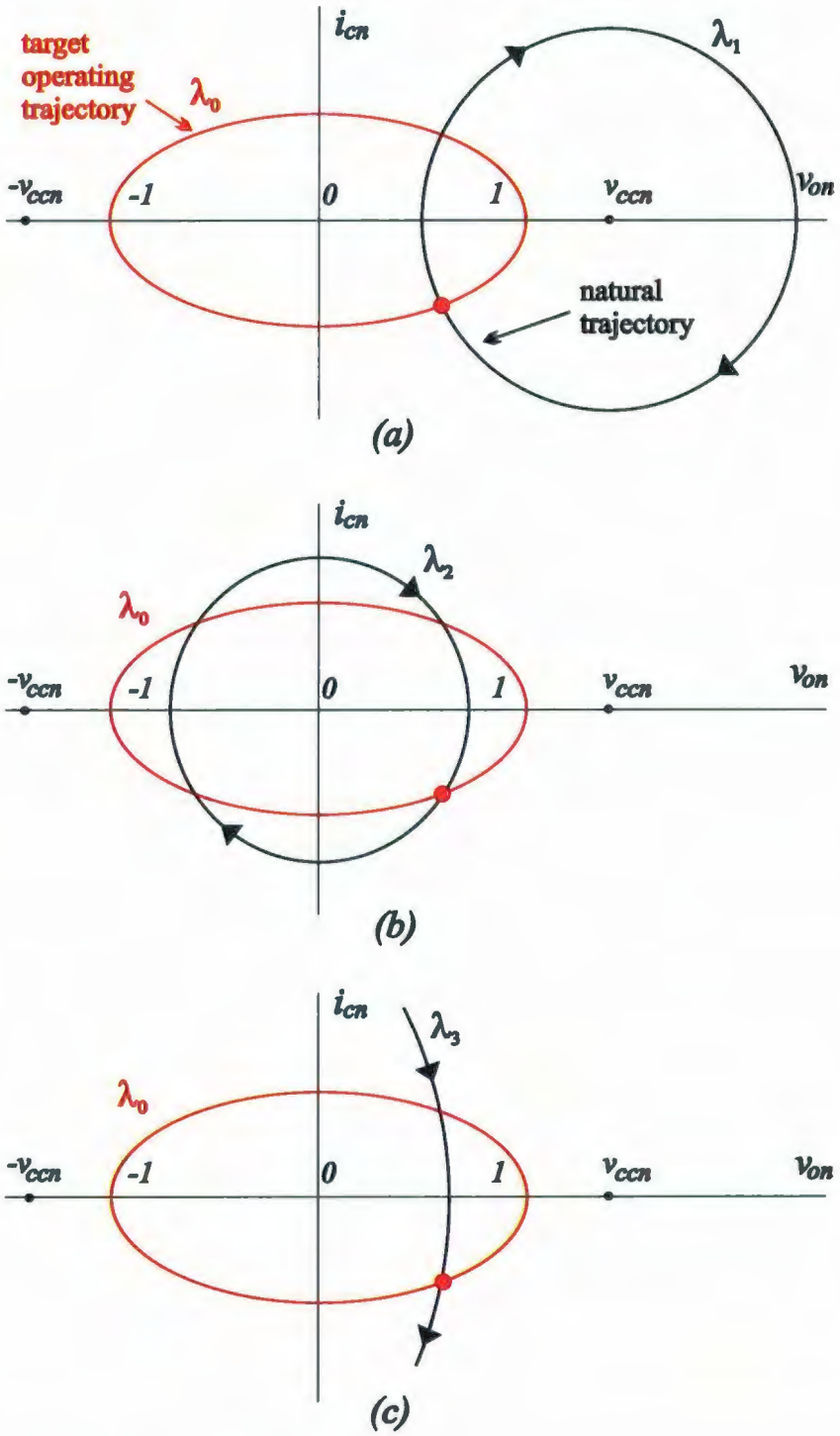


Figure 4.5: Intersection between inverter natural trajectories and the operating trajectory (arbitrary v_{rn} and i_{Crn}): a) λ_1, b) λ_2, and c) λ_3 natural trajectories.

4.5 Natural Switching Surfaces in Four Quadrants

In this section, the control laws are defined based on the study of the intersections of the natural trajectories defined by (4.16) and the desired operating trajectory or control objective defined by (4.10) and (4.11). The analysis is divided into four regions or quadrants of the (i_{Cn}-v_{on}) plot, shown in Fig. 4.6(a), where monopolar and bipolar modes of operation are studied.

4.5.1 Monopolar Mode of Operation

When the inverter is operated within quadrant I (positive i_{Cn} and v_{on}) and III (negative i_{Cn} and v_{on}), the same natural trajectory λ_2 (4.24) is selected as the control law and defined as σ_2. In the case when the inverter operates in quadrant II, the curved SS defined by λ_3 (4.25) is employed as a control law, denoted as σ_3. Finally, quadrant IV is ruled by λ_1 (4.23) and is governed by the control law, σ_1. The control laws can be, therefore, written as,

$$\sigma_1 = \lambda_1 = i_{Cn}^2 - i_{Crn}^2 + (v_{on} - v_{ccn})^2 - (v_{rn} - v_{ccn})^2 \tag{4.26}$$

$$\sigma_2 = \lambda_2 = i_{Cn}^2 - i_{Crn}^2 + (v_{on})^2 - (v_{rn})^2 \tag{4.27}$$

$$\sigma_3 = \lambda_3 = i_{Cn}^2 - i_{Crn}^2 + (v_{on} + v_{ccn})^2 - (v_{rn} + v_{ccn})^2 \tag{4.28}$$

The control laws in the various quadrants are depicted in Fig. 4.6(a). Figure 4.6(b) shows a conceptual diagram of the evolution of the curved SSs as the target operating trajectory moves in discrete steps around each of the quadrants. As can be seen in Fig. 4.6(b) and from a geometrical point of view, (4.26), (4.27), and

(4.28) simply adjust their radius to match or intersect a particular point of the target operating trajectory. This evolution results from a change of the reference values v_{rn} and i_{Crn} in (4.26), (4.27), and (4.28). The normalization technique proposed in this chapter leads to the simple geometrical representation described above.

From a structural point of view, and aided by Fig. 4.6(c), the inverter behaves in the following way. An arbitrary initial point is defined in the boundary of quadrant I and II with a final target point t_1, which lies far away from the initial point. The control law σ_2 that rules in quadrant I forces the inverter to operate with $u = 1$ until the surface σ_2 that intersects the target operating point is reached (refer to Fig. 4.1 and Fig. 4.2 for the inverter structures). Upon reaching σ_2 the structure of the inverter changes to $u = 0$ allowing the trajectory to be directed towards the target t_1. Thereafter, the trajectory intersects t_1 and continues to travel with $u = 0$ until t_2 becomes the new target (recall that the references v_{rn} and i_{Crn} are dynamically changing). The inverter again operates with $u = 1$ seeking to reach a new σ_2 that intersects t_2. The system continues to operate in the same fashion. A similar analysis applies for the graphical example in quadrant III (Fig. 4.6(c)). The control laws are formally defined by quadrant as,

$$\text{Quadrant I:} \quad \text{if } \sigma_2 > 0 \text{ then } u = 0, \text{ else } u = 1.$$

$$\text{Quadrant II:} \quad \text{if } \sigma_3 > 0 \text{ then } u = -1, \text{ else } u = 0.$$

$$\text{Quadrant III:} \quad \text{if } \sigma_2 > 0 \text{ then } u = 0, \text{ else } u = -1.$$

$$\text{Quadrant IV:} \quad \text{if } \sigma_1 > 0 \text{ then } u = 1, \text{ else } u = 0.$$

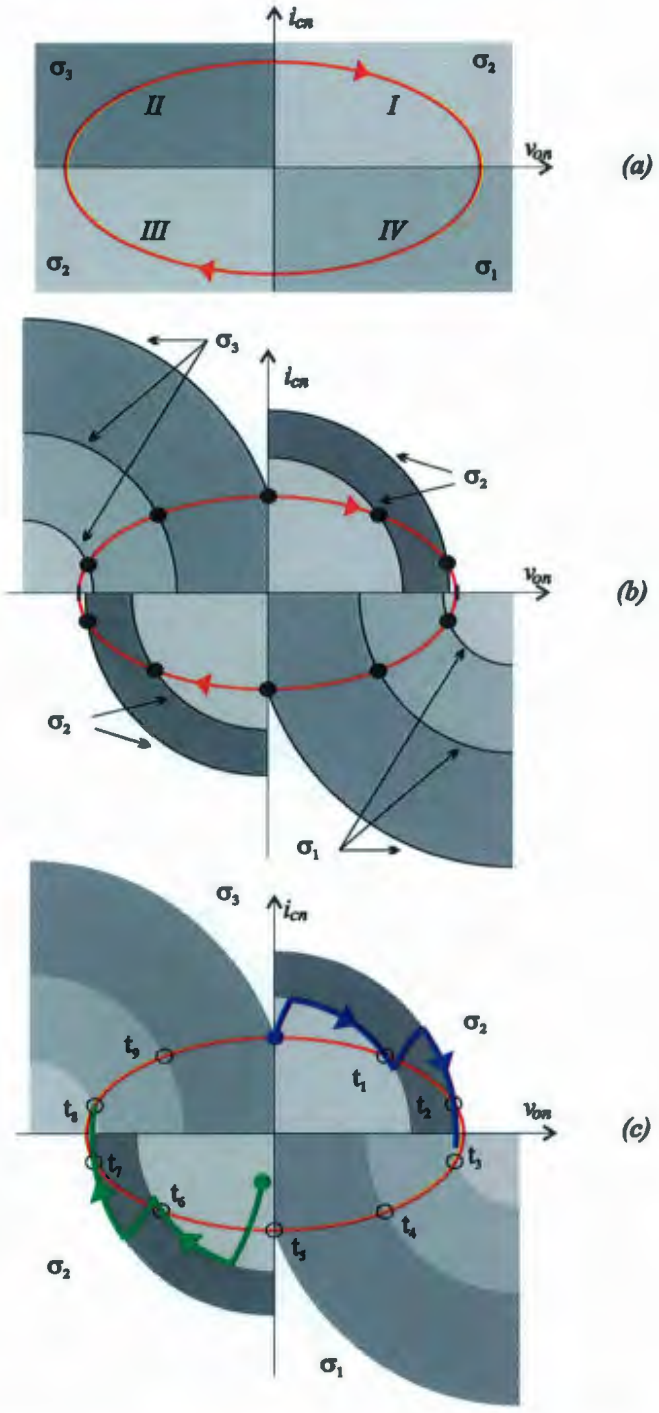


Figure 4.6: Natural SS for monopolar mode in four quadrants: a) control laws by quadrants, b) progression of the natural SS along the target operating trajectory, and c) conceptual evolution of the natural trajectories.

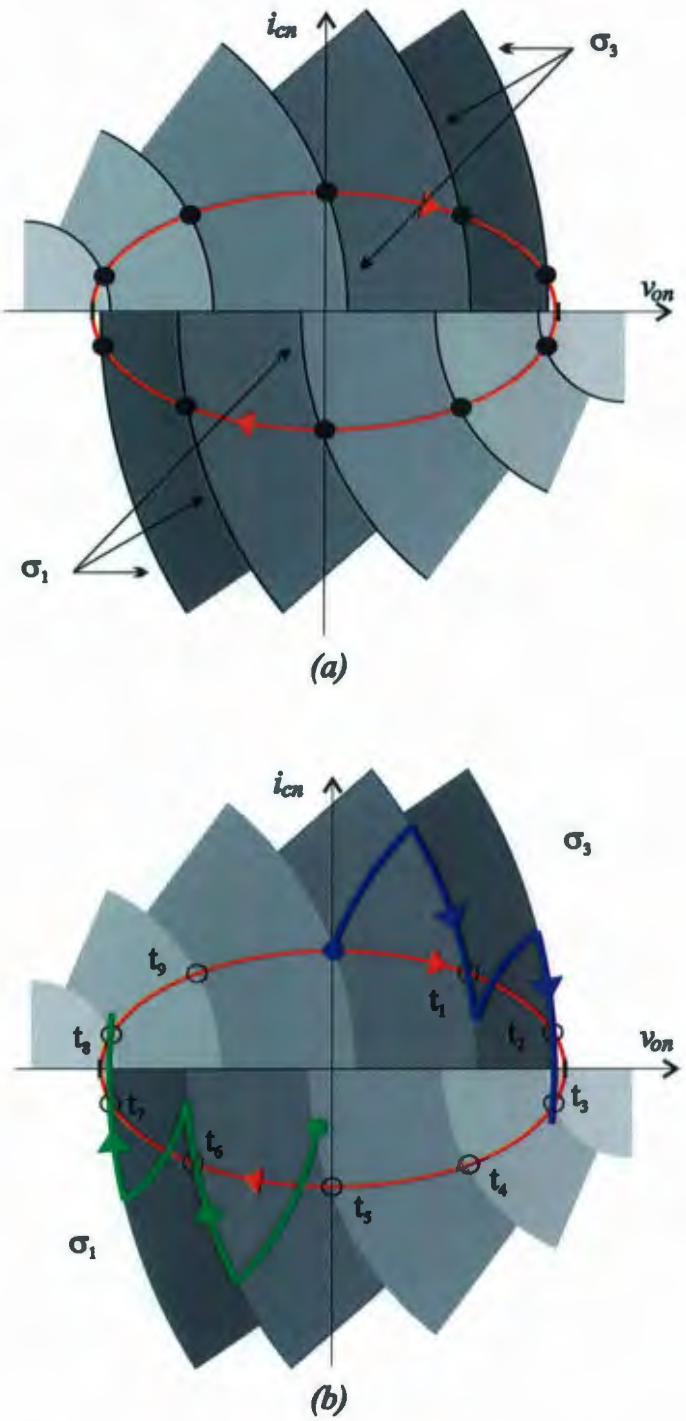


Figure 4.7: Natural SS for bipolar mode: a) progression of the natural SS along the target operating trajectory, and b) conceptual evolution of the natural trajectories.

4.5.2 Bipolar Mode of Operation

Bipolar mode of operation assumes that the inverter does not apply a zero voltage state of $u = 0$ to the output filter and the only allowed states are v_{cc} and $-v_{cc}$ or $u = 1$ and $u = -1$ respectively. This implies that the natural trajectory λ_2 (4.24) must be eliminated from the analysis. In addition to full-bridge inverters, this mode of operation is directly applicable to a half bridge inverter as well.

When the inverter is operated within quadrant I and II (positive i_{Cn}), the natural trajectory λ_3 (4.25) is selected as the control law, which has been already defined as σ_3 (4.28). In the case when the inverter operates in quadrant III and IV (negative i_{Cn}), the curved SS defined by λ_1 (4.23) is employed as a control law, denoted as σ_1 (4.26).

Figure 4.7(a) shows a conceptual diagram of the evolution of the curved SSs as the target operating trajectory moves in discrete steps around each of the quadrants. The control laws for bipolar mode are formally defined by quadrant as,

$$\text{Quadrant I and II:} \quad \text{if } \sigma_3 > 0 \text{ then } u = -1, \text{ else } u = 1.$$

$$\text{Quadrant III and IV:} \quad \text{if } \sigma_1 > 0 \text{ then } u = 1, \text{ else } u = -1.$$

A conceptual evolution of the natural trajectories is depicted in Fig. 4.7(b). As can be seen in Fig. 4.7(b), the excursion of the natural trajectories is much longer compared to Fig. 4.6(c), which results in more current and voltage ripple in the inverter output filter. From the modulation point of view, the increase in ripple is a main disadvantage of the bipolar mode. However, even though monopolar mode is known to provide a better a sinusoidal synthesis, it carries a serious physical limitation in the region of zero voltage cross under heavy resistive loading conditions,

as demonstrated in this work. This interesting behavior is demonstrated in the normalized geometrical domain in Section 4.7.

4.5.3 Simple Conceptual Definition of the Control Law

The behavior of the system using the natural SS can be synthesized in a simple conceptual definition. The only objective of the natural SS is to maintain the operating point around its perimeter or outer boundary, i.e., around the circumference of the natural switching SS. First, the operating point is directed towards the outside of the circle until the boundary is reached. Thereafter, a change in the structure of the system is performed (u changes) to force the operating point to follow the perimeter of the circle. Given the fact that the perimeter of the circle matches the target operating trajectory, the control objective is therefore achieved. Since the target operating trajectory changes dynamically, the radius of the natural SS is in constant expansion. That is, the circumference that represents the natural SS always experiences a radius increase as the reference (target operating trajectory) changes. The maximum radius corresponds to the limit or intersection between quadrants (i.e. quadrants I and IV). Once the transition from one quadrant to another is completed, the center of the natural SS changes and its radius is reset to minimum. The incremental changes in radius start again to successfully follow the target operating trajectory.

The graphical representation of the natural SS and the natural trajectories have been presented in Fig. 4.6 and Fig. 4.7 for monopolar and bipolar mode respectively. It is seen that the natural SS tracks the operating point around its perimeter in the normalized domain with center in $-v_{ccn}$, v_{ccn}, and 0 (only for monopolar mode). As described in Chapter 4, the inverter dc bus (v_{cc}) is expected to operate with variable

voltage (refered to as swinging bus) to eliminate low frequency ripple current in the FC. This effect produces a continous change in the location of the center of the natural SS. In the next section, the natural SS is studied to demostrate that high quality output power can be generated even in the presence of a severe swinging bus.

4.6 Swinging Bus Operation Using the Natural Switching Surface

The swinging bus concept described in Chapter 3 is employed to absorb the 120Hz pulsating current produced by the inverter. As a result, low frequency ripple current reflection in the FC is eliminated at the expense of the voltage swing at the input terminals of the inverter. Since inverters are traditionally operated with stiff dc input voltages, a swinging bus presents an unprecedented challenge for the control scheme of the inverter. In this section, the effect of the swinging bus is incorporated in the analysis of the natural SS with the objective of producing high quality output power under any operating condition, while accommodating the swinging voltage on the dc link.

Operation under swinging bus results in v_{ccn} variations that affect the natural trajectories and hence, the geometrical location of the natural SS (4.26-4.28). The bus voltage variation occurs in a cyclic fashion and reflects the constant current charge and pulsating current discharge of the bus capacitor C_{bus}. While the constant current is supplied by the dc-dc converter (from the FC), the pulsating discharge current depends on the nature of the inverter load. For illustration purposes, this section analyzes the behavior of the system under resistive load.

As described in Chapter 4, the low frequency ripple current has a fundamental

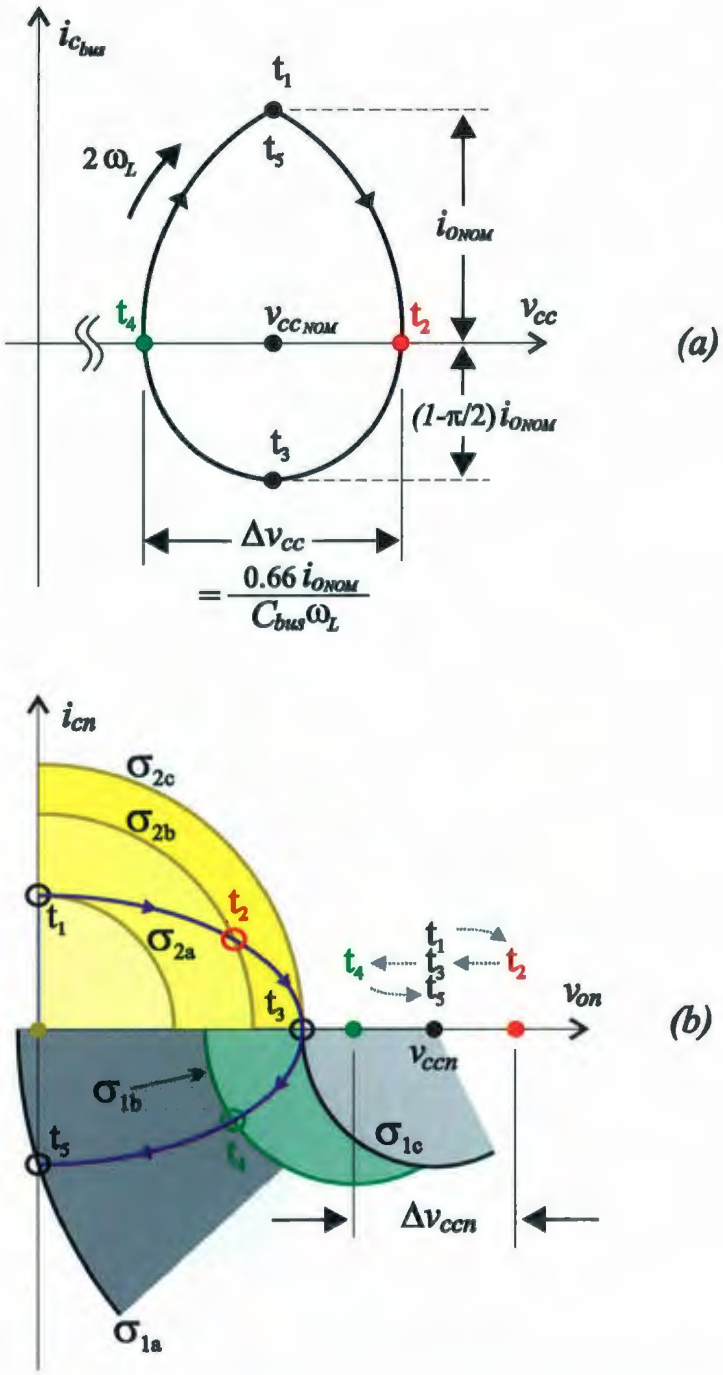


Figure 4.8: Swinging bus operation using the natural SS: a) bus capacitor evolution and b) conceptual evolution of the natural trajectories.

frequency that is double the output frequency of single phase inverters. The current versus voltage representation of the bus capacitor C_{bus} under full resistive load is shown in Fig. 4.8(a), where the cyclic behavior can be seen. Four distinctive points are indicated in the bus capacitor characteristic:

- t_1 represents the start of a semicycle (where v_{cc} is nominal)
- t_2 corresponds to the instant where the inverter load current equals the dc-dc converter constant current (maximum bus voltage occurs)
- t_3 denotes the instant of negative peak current in the capacitor at nominal bus voltage
- t_4 corresponds to the instant where the inverter current matches the dc-dc converter current (minimum bus voltage)

These four point are mapped into the inverter phase plane (normalized output voltage versus normalized capacitor current) to visualize the dynamic evolution of the natural SS, which is shown in Fig. 4.8(b). The instants t_1, t_2, t_3, and t_4 are indicated in the elliptical target trajectory as circles. As well, the bus voltage evolution is also indicated with t_1, t_2, t_3, and t_4 as dots.

The analysis is divided into two regions, Quadrant I and IV. The behavior in Quadrant I is governed by σ_2,

$$\sigma_2 = i_{Cn}^2 - i_{Crn}^2 + (v_{on})^2 - (v_{rn})^2, \tag{4.29}$$

which is independent of v_{ccn} and has center in 0. The SS is therefore not affected by variations in the bus voltage. For example, the natural SS that intersects the target operating trajectory (σ_{2b}) remains as a circumference with center in 0, in spite of

the maximum bus voltage occurrence at t_2. It can be deduced that the bus voltage variation only affects the natural trajectory during on-state ($u = 1$). When the natural trajectory intersects the natural SS, the control law changes the switch to off-state ($u = 0$) to successfully reach the target operating trajectory. It can be therefore concluded that operation in Quadrant I successfully rejects any variations in the bus voltage. This outstanding property also applies to operation in Quadrant III.

When the converter is operated in Quadrant IV, the behavior is reversed in the following way. As described in Section 4.5.1, the control law in Quadrant IV is,

$$\sigma_1 = i_{Cn}^2 - i_{Crn}^2 + (v_{on} - v_{ccn})^2 - (v_{rn} - v_{ccn})^2, \tag{4.30}$$

which depends on v_{ccn}. In this case, the natural SS (circumference) represented by σ_1 has center in the bus voltage. The analysis begins with the instant t_3, which is in the boundary of Quadrants I and IV. The starting point for the analysis denotes the instant where the inverter delivers maximum output current. As depicted in (Fig. 4.8(b)), the bus voltage is nominal, leading to excellent bus utilization. This important finding clarifies that crest of the output voltage occurs when the bus voltage is nominal, so operation under swinging bus does affect bus voltage availability during that critical interval. It is therefore concluded that the natural SS at instant t_3 is exactly the same in swinging and fixed bus operation. That is, the geometrical location of the natural SS in swinging bus operation at t_3 is the same as the geometrical location for fixed bus operation.

So far, it has been demonstrated that the geometrical location of the natural SS is not affected by the operation under swinging bus in Quadrant I and the intersection between Quadrant I and IV. What follows is the analysis of the natural SS at t_4, which corresponds to the instant of minimum bus voltage. Similar to the previous

cases in Quadrant IV, the center of the circumference represented by the natural SS (σ_1 in this case) corresponds to the bus voltage. The displacement of the center of the natural SS at t_4 is illustrated in Fig. 4.8(b) which shows the reduction in v_{ccn}. Even though the location of the natural SS has changed, the system operates in a fixed voltage fashion with a reduced value. In this case, it becomes necessary to measure the bus voltage to accurately compute the curved SS. Since the output voltage is measured in the isolated dc-dc converter, no extra hardware or instrumentation is required.

The bus voltage characteristic in Quadrant IV can be summarized as follows: The bus voltage between t_3 and t_4 instants experiences a progressive reduction until the minimum voltage is reached at t_4. From t_4 onwards, the bus voltage recovers to achieve its nominal value at t_5, which is the intersection between Quadrant IV and III. For simplicity and clarity, the reactive current that circulates through the filter has been neglected.

The use of the natural SS under fixed and swinging bus has been demonstrated throughout Section 4.5 and 4.6 respectively. The analysis has been carried out with a geometrical normalized approach providing valuable insight and generality. The aim of these two sections was to introduce the natural SS, illustrate its evolution on each Quadrant (in monopolar and bipolar mode), and evaluate the worse operating instant under swinging bus. So far, a few intersections between the converter natural trajectories and the target operating trajectory (4.12) have been considered. This sample representation allowed the analysis to focus on the behavior of the proposed curved SS. In the following section, the operation of the inverter with fixed frequency is investigated. Recall that fixed frequency helps to reduce electromagnetic interference and reduces the size of the EMI filter. As will be seen, this important feature is achieved when the references v_{rn} and i_{Crn} are generated in discrete steps.

4.7 Fixed Frequency Operation

This section investigates how the switching frequency is spontaneously imposed by the reference discrete events. The undesired chattering characteristic of sliding-mode control around a switching surface [67] is avoided by the single control action that the natural SS performs on every discrete reference change. In order to demonstrate this behavior, a transformation from the natural SS to its PWM equivalent is performed based on geometrical analysis.

The inverter control objective is based on reconstructing or shaping the target operating trajectory using the natural trajectories of the variable structure system. In the normalized representation, any of the natural trajectories (λ_1, λ_2, λ_3) requires one normalized time unit t_n to perform a full 360° circle. On the other hand, the reference or target operating trajectory typically needs more than one unit of normalized time to complete one elliptical turn. The required time is represented by the relation between the output filter natural frequency to the output fundamental frequency $t_n = \omega_o/\omega_L$. In the process of reproducing the target operating trajectory, the fast moving natural trajectories must intersect the target by exactly the number of times dictated by the switching frequency. Therefore, when the normalized switching frequency is introduced, the natural trajectories will have $360°/F_{swn}$ degrees to hit a single point in the target operating trajectory, where $F_{swn} = F_{sw}/(2\pi\omega_o)$.

Now that the angular relationships have been established, the fixed frequency dynamic evolution of the system using the natural SS can be investigated. The following normalized example is employed to illustrate the system behavior. For the sake of simplicity the filter natural frequency (base quantity) is selected to be 6 times the output frequency of the inverter and the switching frequency 10 times the filter natural frequency (or 60 times the inverter output frequency) yielding the normalized

quantities:

$$F_{on} = 1 \text{ or } 360°$$

$$F_{Ln} = 0.1666 \text{ or } 2160°$$

$$F_{swn} = 10 \text{ or } 36°$$

The initial conditions of the system are defined as $i_{Crn} = \omega_L/\omega_o = 0.1666$ and $v_{rn} = 0$ which is located in the semiminor point of the target operating trajectory as indicated in Fig. 4.9(a). The objective of the inverter is to hit the next point (circles in Fig. 4.9(a)) in one control action. In order to do so, the natural trajectory λ_1 ($u = 1$) directs rapidly the operating point towards the SS $\sigma_2(v_{rn_1}, i_{Crn_1})$ that intersects the target operating trajectory. Thereafter, the control action changes the structure of the system to $u = 0$ to follow the natural trajectory λ_2. Since one switching period involves 36°, the sum of both angular trajectories is

$$\angle\lambda_1 + \angle\lambda_2 = \frac{360°}{F_{swn}} = 36° \tag{4.31}$$

The angular trajectory $\angle\lambda_1$ can be obtained by calculating the intersection point of the circles represented by λ_1 and λ_2,

$$v_{inter} = \frac{(d^2 - r^2 + R^2)}{2d} \tag{4.32}$$

$$i_{inter} = \sqrt{4d^2R^2 - (d^2 - r^2 + R^2)^2}/2d \tag{4.33}$$

where,

$$d = v_{ccn} \tag{4.34}$$

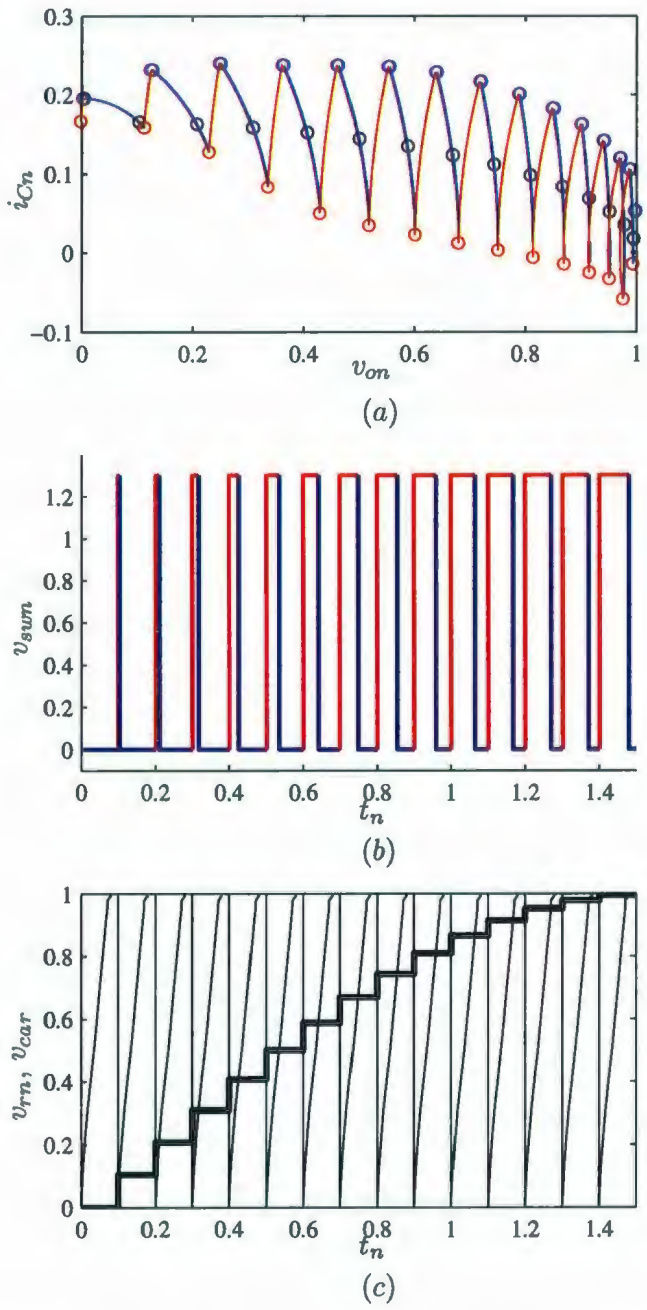


Figure 4.9: Fixed frequency operation case example for $F_{Ln} = 0.1666$, $F_{swn} = 10$, and $v_{ccn} = 1.3$: a) intersection between the natural trajectories and the target operating trajectory, b) pulse width in normalized time domain, and c) equivalent PWM carrier in normalized time domain.

$$R = \sqrt{i_{Crn}^2 + v_{rn}^2} \tag{4.35}$$

$$r = (v_{rn(init)} - vccn)^2 + i_{Crn(init)}^2 \tag{4.36}$$

Finally the initial, final, and angular excursion are calculated using

$$\angle\lambda_{1(init)} = tan^{-1}\left(\frac{i_{Crn(init)}}{v_{ccn} - v_{rn(init)}}\right) \tag{4.37}$$

$$\angle\lambda_{1(end)} = tan^{-1}\left(\frac{i_{inter}}{v_{ccn} - v_{inter}}\right) \tag{4.38}$$

$$\Delta\angle\lambda_1 = \angle\lambda_{1(end)} - \angle\lambda_{1(init)} \tag{4.39}$$

respectively. Choosing an arbitrary normalized input voltage $v_{ccn} = 1.3$ yields $\Delta\angle\lambda_1 = 1.29°$, which reflects a very narrow pulse. In the same manner, the angular excursion for λ_2 trajectory is given by

$$\Delta\angle\lambda_2 = \frac{360°}{F_{swn}} - \Delta\angle\lambda_1 \tag{4.40}$$

yielding a wide $\Delta\angle\lambda_2 = 34.71$ pulse. In the process of transforming the natural SS into its PWM equivalent, the angles are first converted into normalized time as follows:

$$\Delta t_n(\lambda_1) = \frac{\Delta\angle\lambda_1}{360°} \tag{4.41}$$

$$\Delta t_n(\lambda_2) = \frac{\Delta\angle\lambda_2}{360°} \tag{4.42}$$

resulting in $\Delta t_n(\lambda_1) = 0.0036$ and $\Delta t_n(\lambda_2) = 0.0964$. With a new reference change, the process continues to behave in the same fashion and the pulse durations can be calculated following the same procedure as in (4.32-4.42). Figure 4.9(b) shows the equivalent pulse width of the analyzed example in quadrant I.

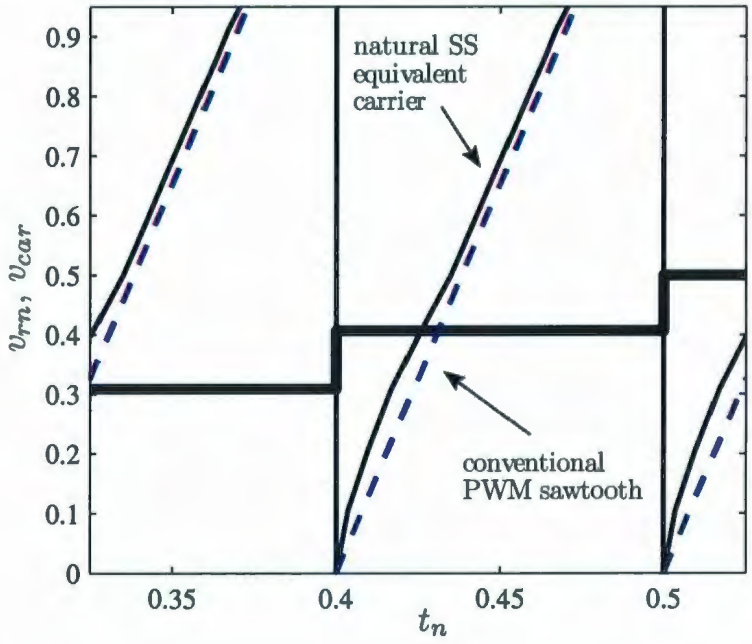


Figure 4.10: Reconstruction of the natural SS equivalent carrier for the analyzed case example.

The next step in the analysis is to obtain the equivalent modulator carrier that would produce the same effect as the natural SS in quadrant I as shown in Fig. 4.9(c). As will be seen a duality between the natural SS and PWM type of modulation exists. Figure 4.10 shows a detailed representation of the equivalent carrier that has been reconstructed point to point from Cartesian coordinates to normalized time domain. It is interesting and surprising to note the similarities between a sawtooth type of carrier (dashed lines) and the natural SS (bold lines). However, as indicated in Fig. 4.10, the natural SS equivalent carrier has a modified shape compared to a sawtooth. This carrier reshaping effect creates a modified PWM that successfully compensates for deficiencies in the conventional PWM. Note that the modified or equivalent PWM created by the natural SS produces a pulse width reduction, especially in the low voltage region. This is more notable in inverters with low switching frequencies.

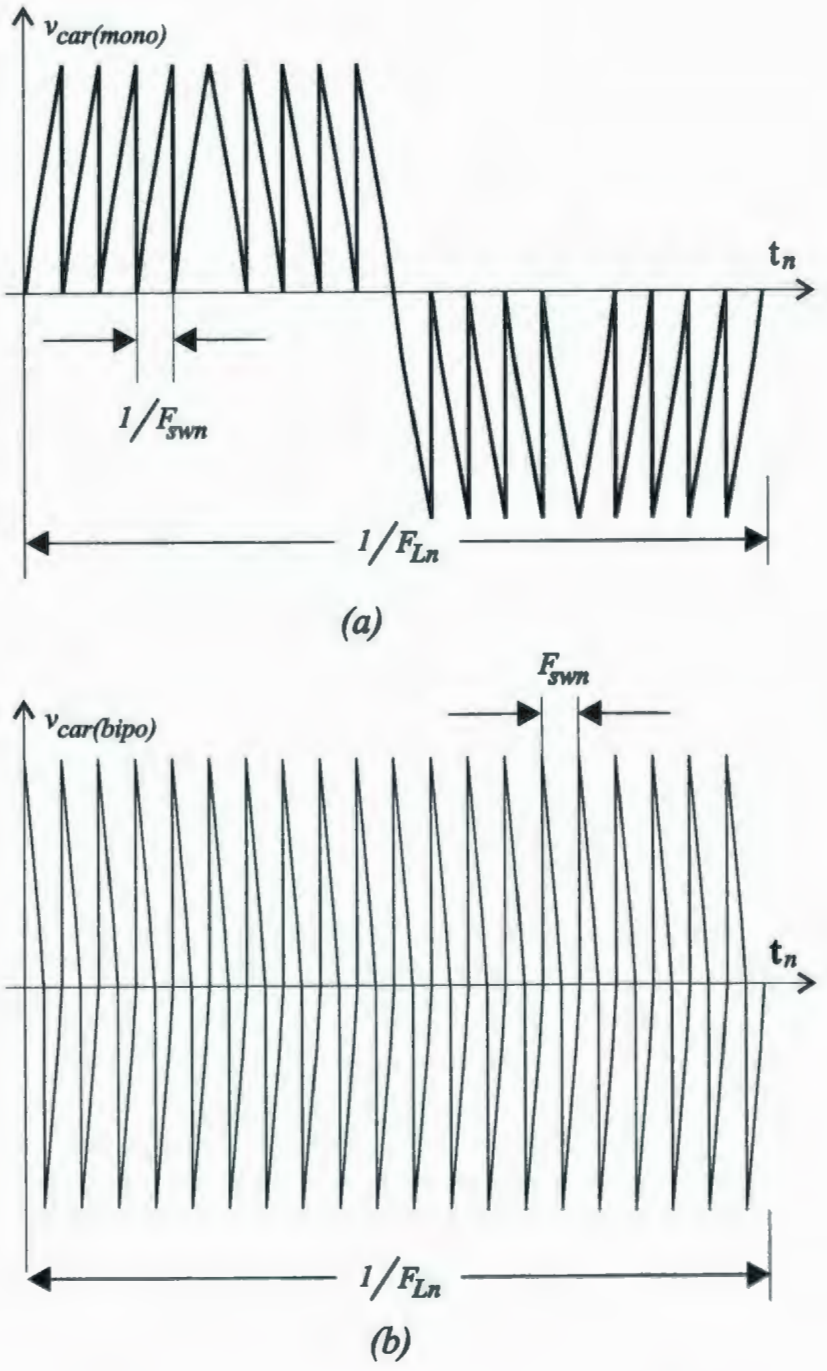


Figure 4.11: Conceptual equivalent carriers for the natural SS: a) monopolar and b) bipolar modes of operation.

The results presented in Fig. 4.10 not only demonstrate that the natural SS operates with fixed frequency but also highlights the existence of duality between PWM and curved SS with discrete references. These conceptual waveforms indicate that modification in the conventional PWM carrier can improve the operating performance of inverters.

It should be noted that a change from one quadrant to another produces a change of slope in the equivalent sawtooth-like carrier. This is illustrated in Fig. 4.11(a) with a conceptual representation of the natural SS equivalent carrier in monopolar mode. Figure 4.11(b) shows a conceptual equivalent carrier when the inverter is operated in bipolar mode. In the next section, the advantages of using the natural SS in monopolar and bipolar modes are explored and combined to create a novel mixed operating mode. As will be seen, significant improvement in the power quality can be achieved in mixed mode under heavy loading conditions.

4.8 Operation in Mixed Monopolar and Bipolar Mode

It has been seen in Sections 4.5 and 4.7 that the natural SS can be used to control the inverter in monopolar and bipolar mode. In this section, the normalized approach is employed to analyze the inverter under heavy resistive loading conditions ($R_l \approx Z_o$) to clarify that a physical limitation exists in the system in the region of zero output voltage crossing. It will be seen that despite the control strategy, when inverters are operated in monopolar mode under heavy resistive loading conditions, the output voltage presents distortion around the zero crossing region. The loading condition in this work is defined as a relative quantity that is related to the filter characteristic

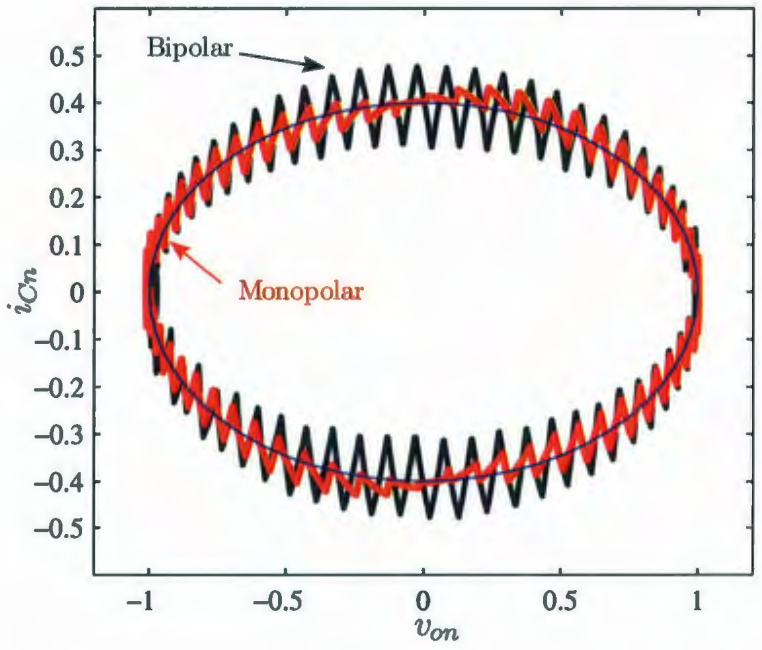


Figure 4.12: Monopolar and bipolar modes of operation under light loading condition for $F_{Ln} = 0.4$, $F_{swn} = 24$, and $v_{ccn} = 1.3$

impedance Z_o and not an arbitrary nominal or rated output power of the system.

First, the behavior of the converter is analyzed under no load or light loading condition in monopolar and bipolar mode. A case example with $F_{Ln} = 0.4$, $F_{swn} = 24$, and $v_{ccn} = 1.3$ is employed for illustrative purposes. Note that normalized analysis only requires three parameter (as opposed to several parameters of the inverter including L, C, output voltage v_o, input voltage vcc, output power P_o, fundamental output frequency F_L, filter cutoff frequency Fo, and switching frequency F_{sw}). Figure 4.12 shows the phase plane where the monopolar and bipolar modes are overlapped in the same plot. The reduced ripple shown in the monopolar case under light loading condition is clearly an advantage over the bipolar counterpart. However, as shown in Fig. 4.13, when a heavy loading condition ($R_{ln} = 1$ or $R_l = Z_o$) is applied to the inverter, the monopolar mode presents a distortion in the vicinity of the zero cross-

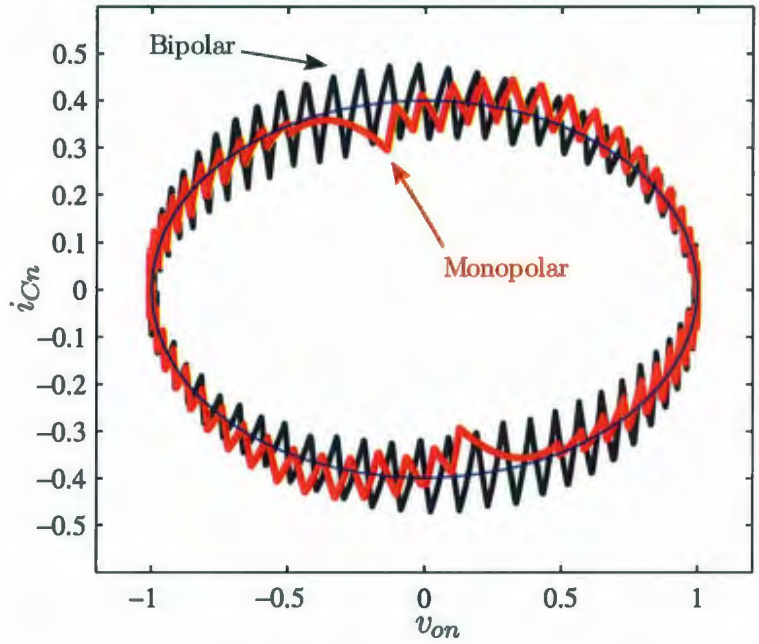


Figure 4.13: Monopolar and bipolar modes of operation under heavy loading condition for $F_{Ln} = 0.4$, $F_{swn} = 24$, and $v_{ccn} = 1.3$.

ing point ($v_{on} = 0$), whereas the bipolar mode does not exhibit such behavior. It is extremely important to note that this behavior is inherent to the physical limitation of the system and not the control strategy. In order to clarify this inherent behavior, a closer look at the trajectory near $v_{on} = 0$ is shown in Fig. 4.14. Since full-bridge topology allows three possible structures, $u = 1$, $u = 0$, and $u = -1$, all three cases are carefully analyzed. In Fig. 4.14, the system operates in monopolar mode until a decision point is reached. If the inverter continues to operate in monopolar mode ($u = -1$ or $u = 0$ are the only options), the correct control decision would be to remain with $u = 0$. Despite making the right control decision, the operating point departs from the target operating trajectory creating undesirable distortion. Nevertheless, this problem can be eliminated if the system is transitionally operated in bipolar mode. As indicated in Fig. 4.14, the trajectory with $u = 1$ (bipolar mode)

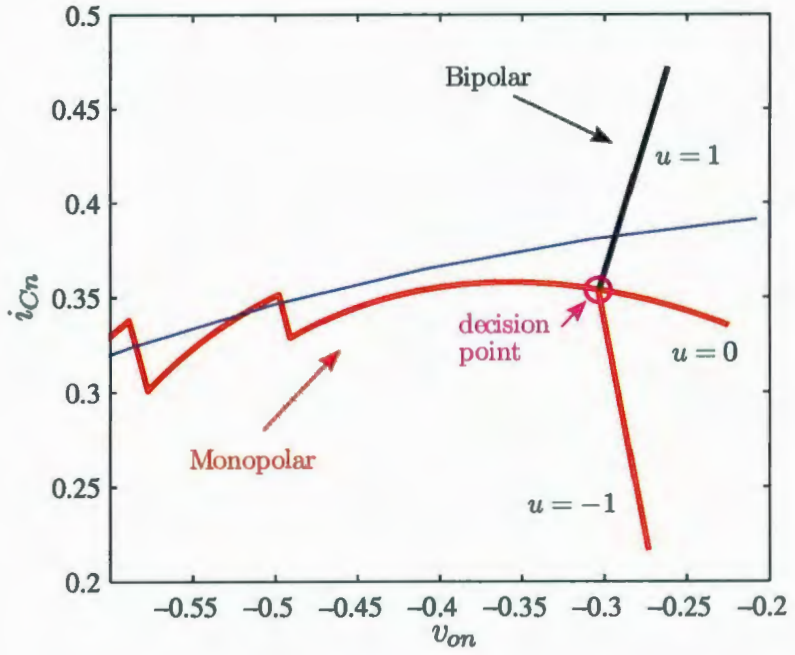


Figure 4.14: Detailed representation of the decision point.

successfully directs the operating point toward the target trajectory. This establishes the basis for the mixed mode, which combines the advantages of monopolar reduced ripple and bipolar distortion elimination in the vicinity of the zero crossing of the output voltage.

Mixed operating mode is illustrated in Fig. 4.15 for light loading and Fig. 4.16 for heavy loading ($R_{ln} = 1$) conditions. It can be seen that the distortion is successfully overcome by the mixed operating mode using the natural SS proposed in this work. A close look at Fig. 4.15 and Fig. 4.16 reveals that the trajectories under heavy loading condition are slightly damped. Finally, a conceptual representation of the equivalent PWM carrier for mixed mode operation is shown in Fig. 4.17.

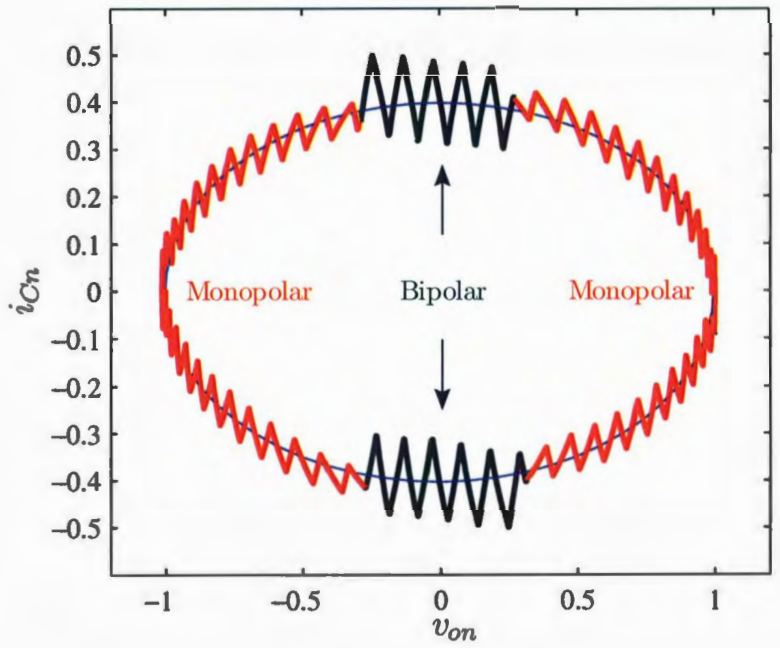


Figure 4.15: Mixed mode of operation under light loading condition for $F_{Ln} = 0.4$, $F_{swn} = 24$, and $v_{ccn} = 1.3$.

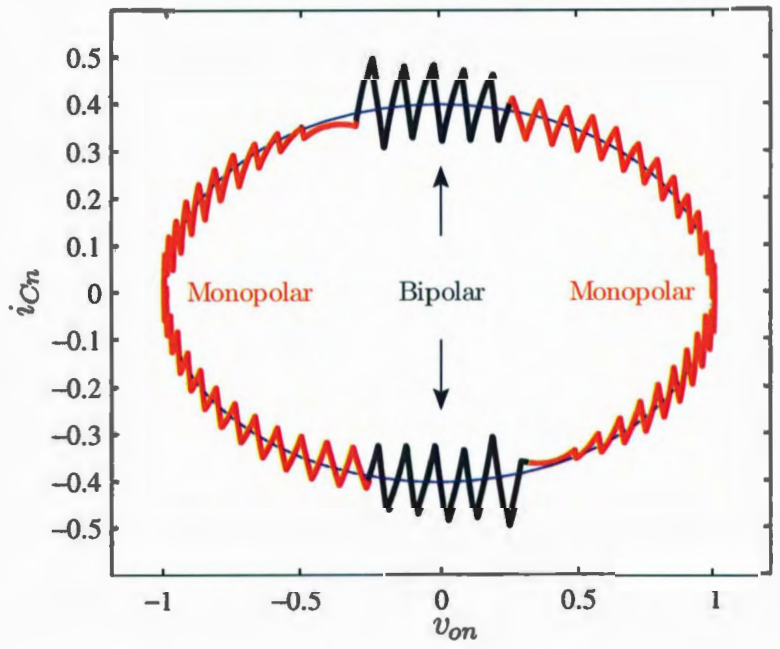


Figure 4.16: Mixed mode of operation under heavy loading condition for $F_{Ln} = 0.4$, $F_{swn} = 24$, and $v_{ccn} = 1.3$.

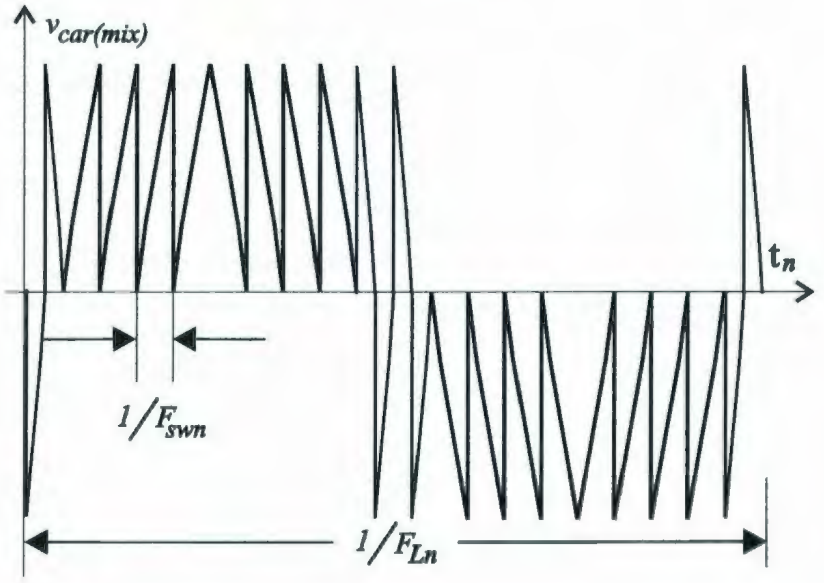


Figure 4.17: Conceptual equivalent carrier for the natural SS in mixed mode of operation.

4.9 Mixed Mode Operation Under Swinging Bus

In this section, the variations in the dc bus are incorporated in the analysis of the mixed operating mode. As well, the effect of the filter reactive current in the bus voltage is discussed. The analysis is first presented in a phase plane and then expanded in the time domain to illustrate some peculiarities that results from this mode of operation.

The same case example used in Section 4.8 is employed for illustrative purposes with $F_{Ln} = 0.4$, $F_{swn} = 24$, and $v_{ccn} = 1.3$ (nominal). However, due to the constant current injection from the dc-dc converter, the pulsating current of the inverter, and mostly important, the value of the bus capacitor, v_{ccn} presents voltage swings of 30% (peak-to-peak). Figure 4.18 shows the behavior of the system under swinging bus in Quadrant I and IV. Two curved SS (σ_2) are indicated in Quadrant I denoting the instant of maximum bus voltage (t_2) and nominal bus voltage (t_1, t_3). When Fig. 4.18 is compared with the theoretical analysis presented in Section 4.6, a slight shift in

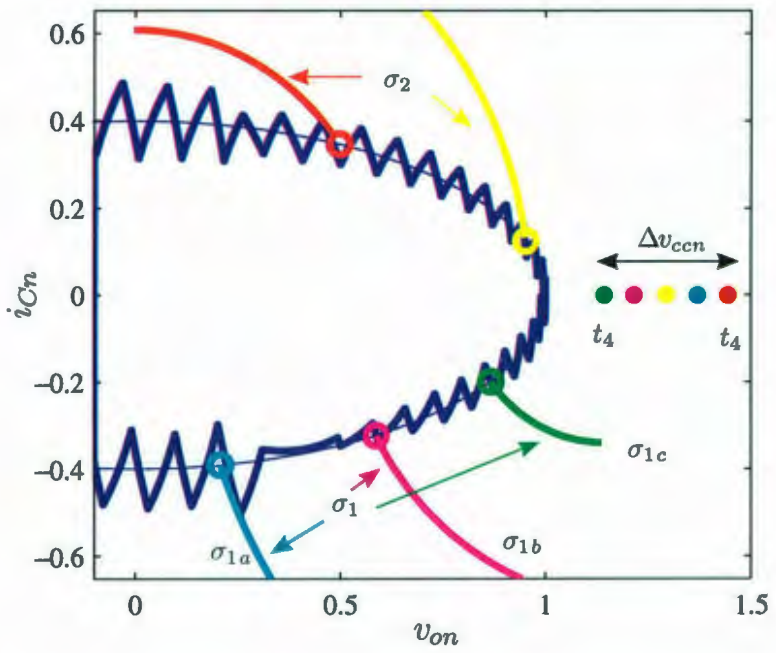


Figure 4.18: Swinging bus operation with 30% voltage variation: Quadrant I and Quadrant IV.

the instant of maximum and nominal bus voltage can be identified. This behavior is explained by the presence of the reactive power (or current) that circulates through the LC output filter. In this case, the normalized peak capacitor current reaches $F_{Ln} = 0.4$, as explained in Section 4.3, which is a fairly large reactive current in the filter that has been selected to illustrate this concept. A reduction in the reactive current, which is associated with higher switching frequencies and higher natural frequencies in the filter, leads to a minimization of this shifting effect in the maximum and nominal bus voltage instants.

The analysis is extended to Quadrant IV (negative i_{Cn} in Fig. 4.18), where three curved SSs are shown. The first curved SS (σ_{1c}) represents the instant of minimum bus voltage. At instant t_4 the intersection between the natural SS and the target operating trajectory occurs, corresponding to minimun bus voltage. Since the system

is operating in monopolar mode in this region of Quadrant IV, the behavior follows the same principle described in Section 4.6. That is, the center of the natural SS (σ_1 in general) is the bus voltage at that instant. Again, when Fig. 4.18 is compared with the analysis in Section 4.6, a slight shift in the instant of minimum bus voltage can be identified. This is also explained by the additional reactive current that circulates through the *LC* filter. After reaching the minimum bus voltage, a progressive recovery occurs until a 50% negative swing after 4 switching cycles in the studied case example is reached. This is indicated be the curved SS (σ_{1b}) in Fig. 4.18 that is also located in the region of monopolar operation. The bus voltage continues to increase reaching the region of bipolar operating mode within Quadrant IV. Figure 4.18 shows the curved SS (σ_{1a}) when the bus voltage reaches 50% positive swing, at the intersection between the natural SS and the target operating trajectory, which corresponds to the dc bus voltage. It is interesting to note that the curved SS in Quadrant IV in both monopolar and bipolar mode is exactly the same (as described in Section 4.5.1 and 4.5.2),

$$\sigma_1 = i_{Cn}^2 - i_{Crn}^2 + (v_{on} - v_{ccn})^2 - (v_{rn} - v_{ccn})^2$$

Therefore, the mixed mode operation is also governed by σ_1 in Quadrant IV. The only difference between monopolar and bipolar mode in this Quadrant is that the structure $u = 0$ (refer to Fig. 4.1) is forbidden in the region of bipolar mode. Instead, the structure $u = -1$ (refer to Fig. 4.2) is enforced. As the bus voltage increases, the system continues to operate with σ_1 in bipolar mode and transitions to Quadrant III. The center of the natural SS (v_{ccn}) in the first portion of Quadrant III remains variable until the monopolar region is reached.

So far, the behavior of the natural SS in mixed mode under swinging bus has been analyzed in a phase plane. While this representation benefits the geometrical

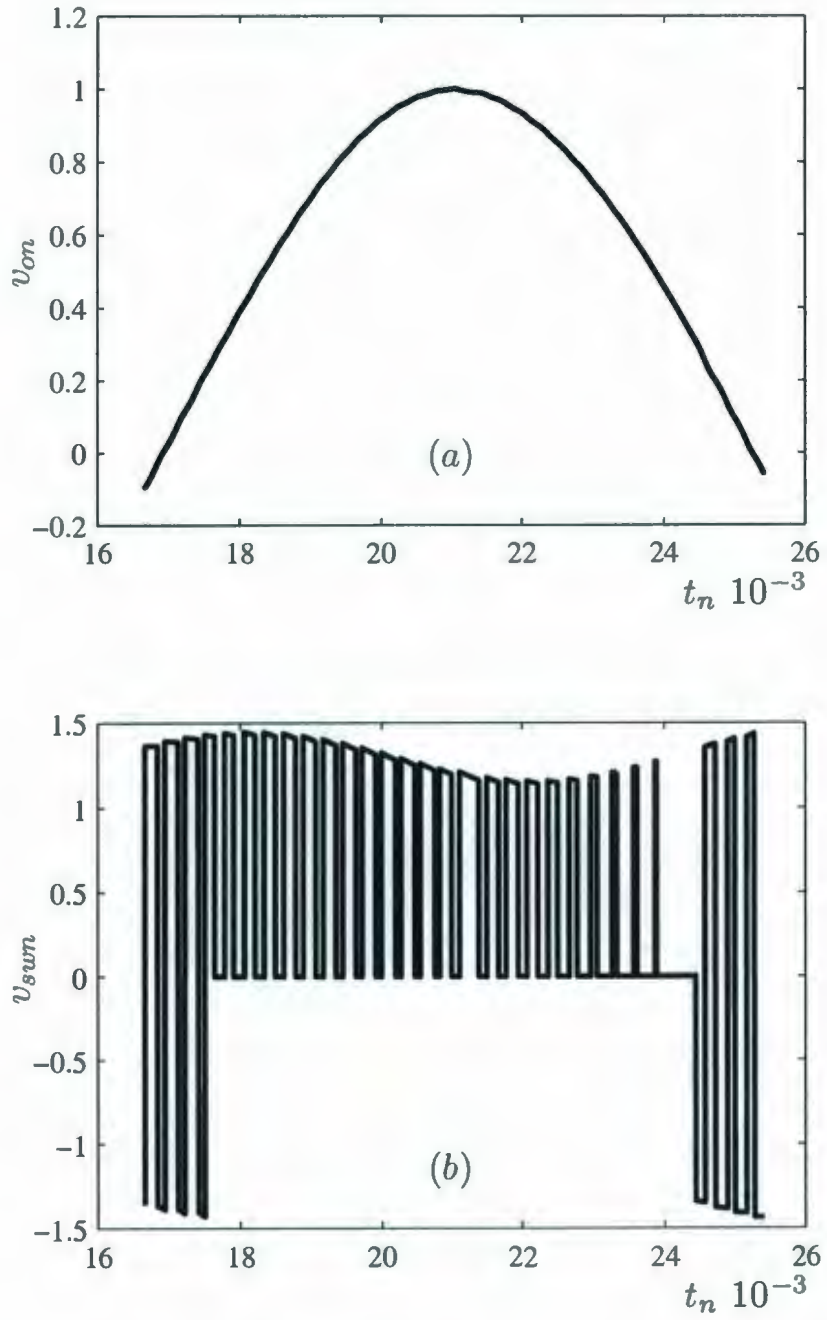


Figure 4.19: Swinging bus operation with 30% voltage variation: a) normalized output voltage (v_{on}) and b) switching sequence applied to the LC filter.

interpretation of the system behavior, other interesting insights can be deduced with a traditional time domain representation. In order to provide more insight into the system behavior under swinging bus, the following analysis is carried out in the time domain.

The study in the time domain employs the same case example that has been investigated throughout this section. Since the system presents a repetitive behavior in steady state operation, a detailed examination of one semicycle is presented. Figure 4.19(a) shows one semicycle of the normalized output voltage of the inverter (v_{on}) that results from employing the natural SS. A detailed switching sequence is presented in Figure 4.19(b), which is applied to the output LC filter to produce the desired output voltage. The effect of the bus swing in the effective area of the pulse is remarkable. As can be seen, the traditional concept of PWM is combined with Amplitude Modulation (AM) that results from the swinging bus. In spite of the substantial bus variations, the natural SS is able to successfully generate a modulation that produces high quality sinusoidal output. A closer representation of the bus behavior is depicted in Fig. 4.20(a). It can be seen that in addition to the 30% bus swing, a high frequency ripple occurs in the bus voltage. This effect can be explained with the aid of Fig. 4.20(b) that shows the current in the bus capacitor. The current in the bus capacitor is the difference between the constant current injection from the dc-dc converter and the pulsating current supplied to the inverter. Even though the inverter pulsating current has a large fundamental that is double the output frequency of the inverter, the inverter switching frequency is responsible for the high frequency ripple (both current and voltage). These two components of the current are to be considered to calculate the lifetime of the bus capacitor bank. When the inverter operates in steady state, the net current in the bus is zero, which ensures a fixed average bus voltage. The behavior of the bus during negative semicycle presents exactly the same

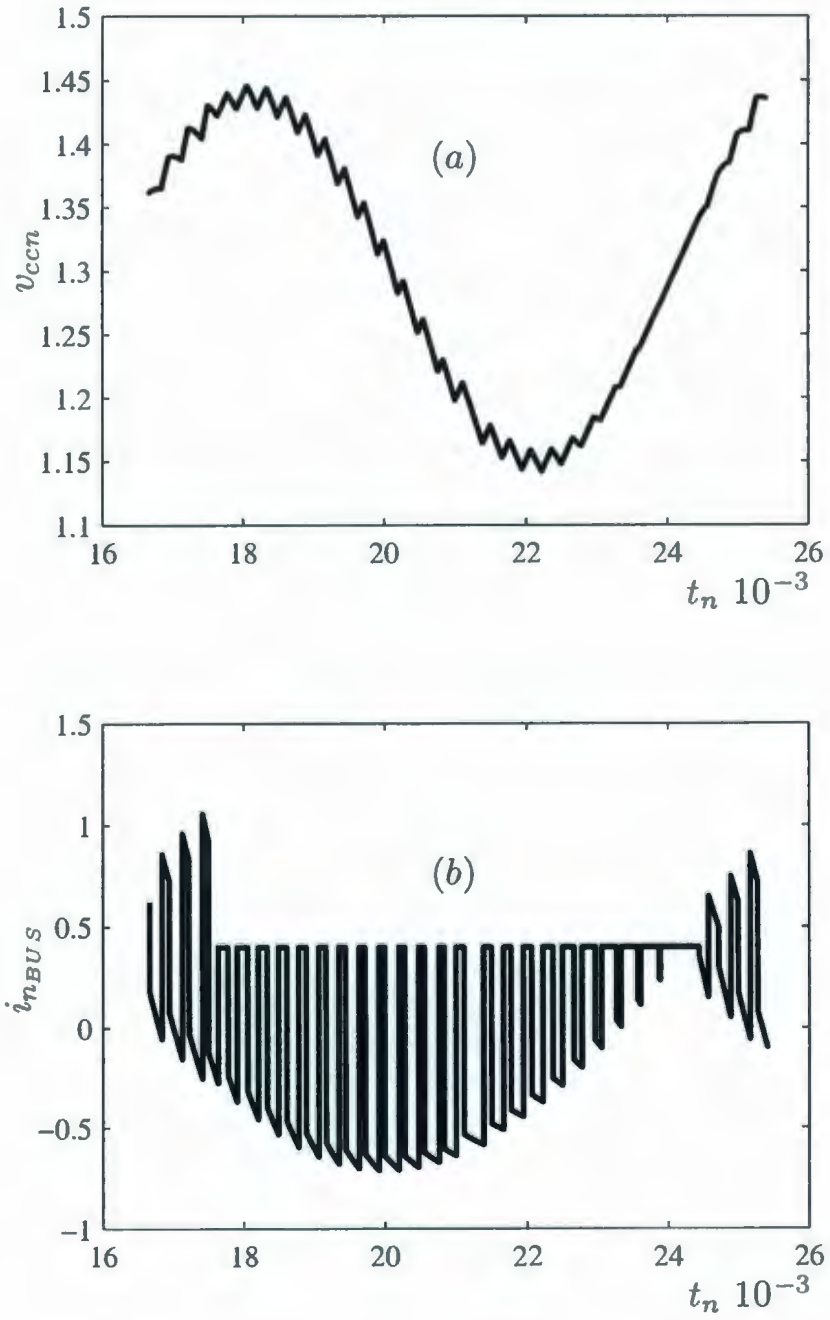


Figure 4.20: Swinging bus operation with 30% voltage variation: a) normalized bus voltage (v_{ccn}) and b) normalized bus capacitor current.

waveforms shown in Fig. 4.20(a) and Fig. 4.20(b). Further insight and validation of mixed operating mode under swinging bus is presented in the following section.

4.10 Design Procedure and Experimental Results

Experimental results of a 1.5 kVA inverter operating at fixed moderate frequency are presented in this section to validate the performance of the natural SS, illustrate the benefits of the normalization technique, and demonstrate the mixed operating mode under fixed and swinging bus. First, a simple design procedure based on the normalization technique is performed. The design specifications for the inverter are shown in Table 4.1 with their equivalent normalized quantities. The results obtained from the normalized design procedure were employed to build a prototype. Experimental evaluation of the inverter included resistive, non-linear high crest factor, inductive, pulsating, and a combination of the previous. The resistive load was employed to test the system under light, medium and full loading condition (1.5kW) to study the behavior with monopolar and mixed mode of operation. The non-linear load was evaluated using high crest factor (CF=2.33), which is typical in computers and electronics apparatus. In this case, the power rating was reduced to compensate for the poor power factor of the load. The behavior of the control scheme in the crest of the sine wave was analyzed in this case. The pulsating load was tested to verify the transient operation with a current step type of load. This was implemented using a full bridge controlled rectifier with an output resistive load. The inductive load as well as a combination of the previous loads was also evaluated to demonstrate the correct operation of the proposed scheme under lagging output current.

Table 4.1: Design Specifications

value	*norm. value*
$v_o = 120\ V$	$v_{on} = v_o/v_{op} = 0.707$
$v_{op} = 120\sqrt{2}\ V$	$v_{opn} = v_{op}/v_{op} = 1$
$v_{cc} = 220\ V$	$v_{ccn} = v_{cc}/v_{op} = 1.3$
$P_o = 1.5\ kW$	
$F_L = 60\ Hz$	

4.10.1 Normalized Design Procedure

By following a criteria based on steady state ripple calculation, the output voltage ripple is arbitrarily selected to have a maximum of $\Delta v_o = \pm 1\ V$ (or $\Delta v_{on} = \pm 0.006$). Assuming that the voltage ripple takes its maximum when $v_o = v_{cc}/2$ or $D = 0.5$ the current normalized ripple is calculated by combining (4.23) and (4.24),

$$\Delta i_{Cn} = \sqrt{v_{ccn}\Delta v_{on} + \Delta v_{on}} \tag{4.43}$$

yielding $\Delta i_{Cn} = \pm 0.088$.

An important normalized quantity is therefore obtained,

$$F_{swn} = \frac{F_{sw}}{F_o} = \frac{360}{4\ tan^{-1}\left(2\Delta i_{Cn}/v_{ccn}\right)} \tag{4.44}$$

which establishes the ratio ($F_{swn} = 11.7$) between the switching frequency F_{sw} and the filter natural frequency F_o. In order to facilitate the visualization of the results, a moderate switching frequency of $F_{sw} = 3.6kHz$ is selected resulting in $\omega_o = 1933\ rad/s$. Finally, by performing a simple denormalization, the filter parameters are calculated

based on the filter natural frequency and power rating of the inverter as follows:

$$C = \frac{1}{Z_o \omega_o} = 54\mu F \tag{4.45}$$

$$L = Z_o^2 C = 5mH, \tag{4.46}$$

where the characteristic impedance of the filter is given by,

$$Z_o = \frac{v_o^2}{P_o}, \tag{4.47}$$

which depends on the power rating of the inverter yielding $Z_o = 9.6\Omega$.

Now that the parameter have been defined, the capacitor normalized peak current can be verified by employing,

$$\omega_{Ln} = \frac{\omega_L}{\omega_o}, \tag{4.48}$$

resulting in $w_{Ln} = 0.195$, which is more than twice the ripple current Δi_{Cn} (4.43) (refer to Fig. 4.3 for details).

The procedure presented above followed a normalized ripple design criteria. It has been seen that the normalized frequency quantities play a key role in the design of inverters using curved SSs. Nevertheless, other design techniques based on dynamic regulation/recovery criteria and load crest factor criteria are promissing topics for future work.

4.10.2 Experimental Results in Monopolar Mode

The designed inverter operating in monopolar mode with the natural SS under light loading condition is shown in Fig. 4.21 and Fig. 4.22 for time domain and phase

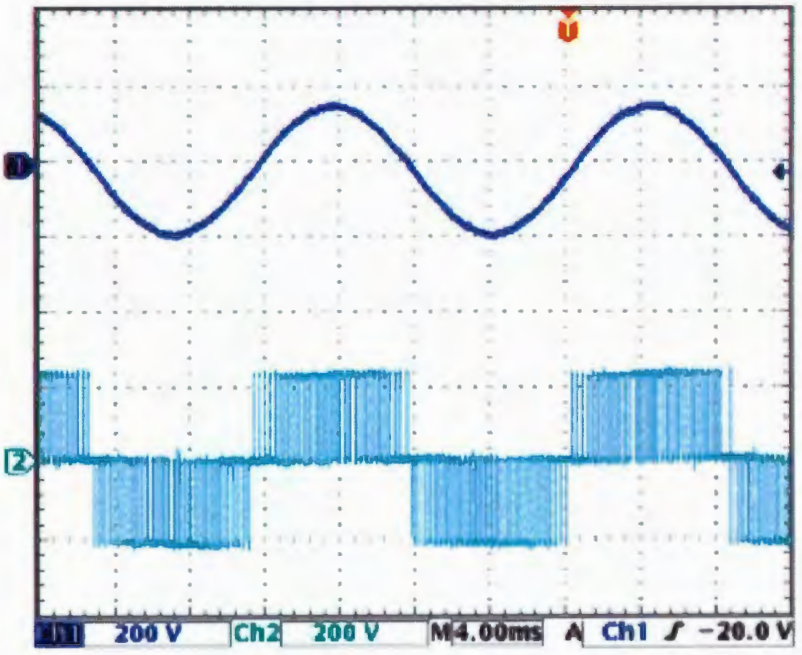


Figure 4.21: Monopolar mode of operation using the natural SS: output voltage (Ch1), and switch state (Ch2) under light loading condition.

plane plots respectively (output voltage versus capacitor current). As predicted by the theory, the control strategy is able to successfully produce high quality output voltage (1.4% harmonic distortion) even at moderate switching frequencies. A detailed capture of the system operation in Quadrant I is presented in Fig 4.23. It can be seen that the pulses are produced in a PWM-like fashion with fixed frequency, in accordance with the analysis presented in Section 4.7.

Monopolar mode under heavy resistive loading condition ($R_l \approx Z_o$) was experimentally evaluated and shown in Fig. 4.24. Even though the natural SS in monopolar mode takes the correct control decision, distortion in the proximity of the zero voltage cross occurs due to a physical limitation in the system (as explained in Section 4.8). The phase plane presented in Fig. 4.25 provides clear experimental evidence of this phenomenon. Note that the damped trajectories cannot closely follow the target operating trajectory (ellipse) in the region of zero voltage cross. This effect resulted

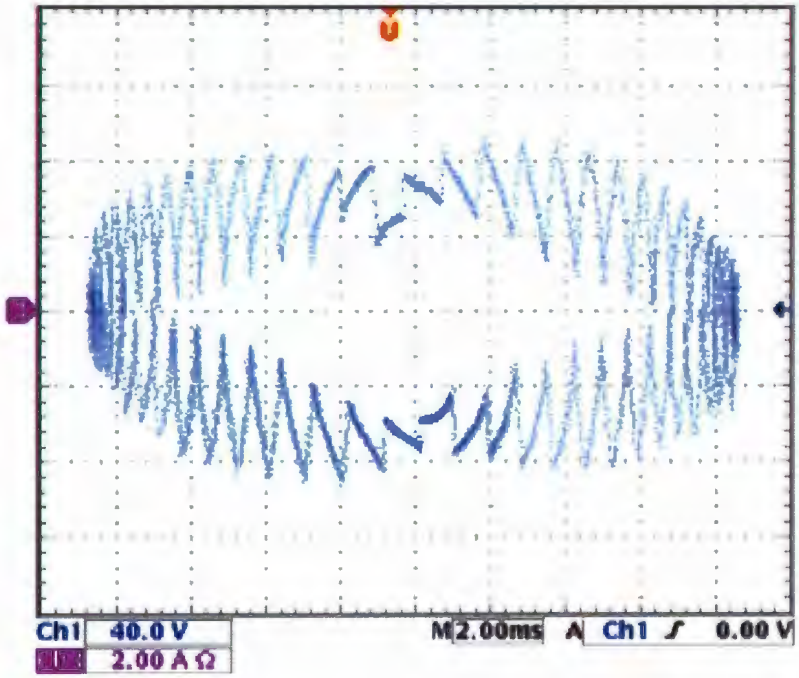


Figure 4.22: Monopolar mode of operation using the natural SS: output voltage versus capacitor current plot under light loading condition.

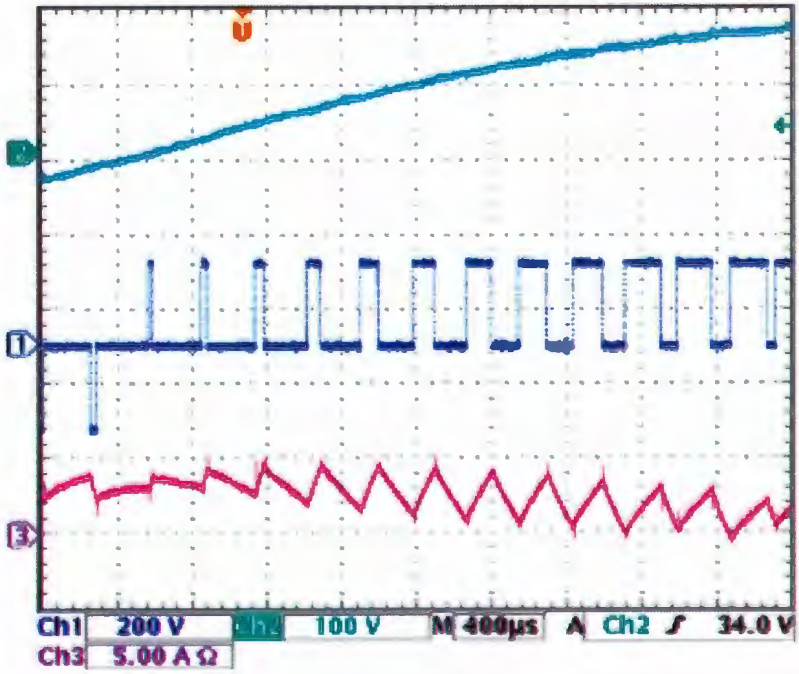


Figure 4.23: System operating in Quadrant I with fixed frequency.

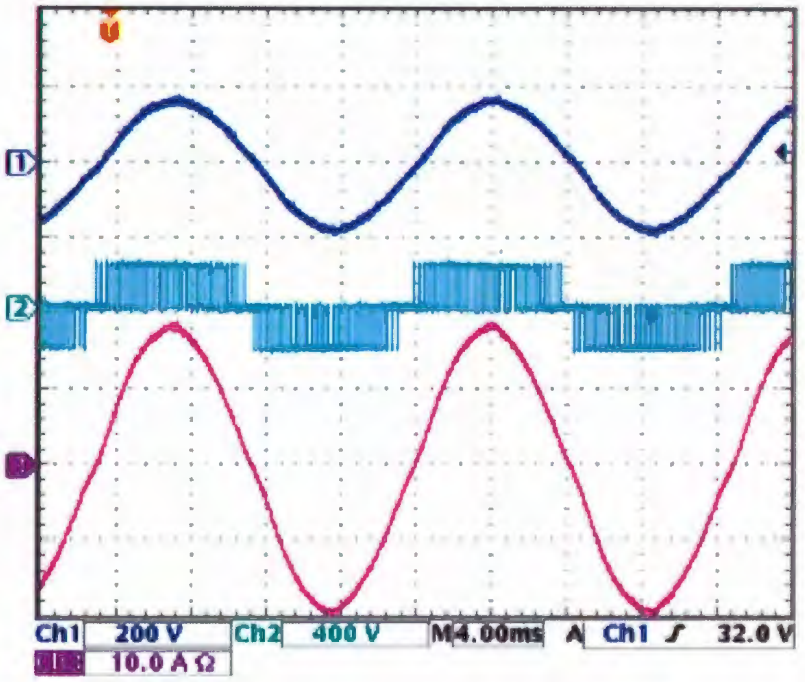


Figure 4.24: Monopolar mode of operation using the natural SS: output voltage (Ch1), switch state (Ch2), and output current (Ch3) under heavy loading condition.

in an increase in the output voltage harmonic distortion (2.6% THD compared to 1.4% THD under light loading condition). As will be seen, mixed operating mode using the natural SS successfully overcomes the physical limitation inherent in the monopolar mode.

For the sake of completeness, experimental results in monopolar mode under non-linear load was evaluated with the following conditions: full-bridge rectifier, load series inductance $L_s = 950uH$, dc capacitor bank $C_{out} = 6000uF$, and $R_{load} = 35\Omega$ producing an output current crest factor $CF = 2.33$, peak current $i_{o(peak)} = 16.33A$, and power factor $PF = 0.72$. As can be seen in Fig. 4.26, the natural SS successfully rejects the non-linear load perturbation by maintaining the switch in on-state around the crest region ($u = 1$ for positive and $u = -1$ for negative semi cycle respectively). Under this operating condition, the system presented 2.3% THD (only 0.9% increase compared to light loading condition) that is mainly attributed to the physical limit

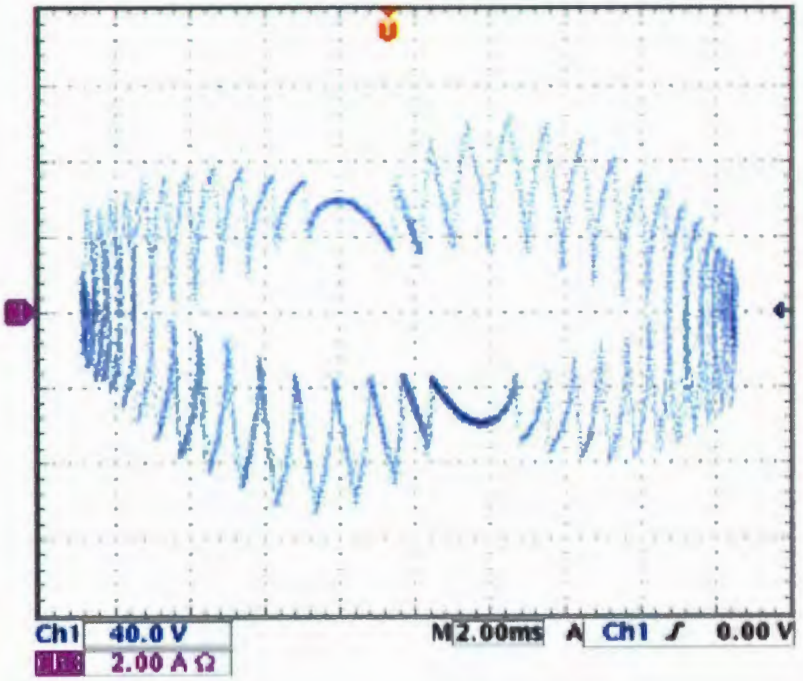


Figure 4.25: Monopolar mode of operation using the natural SS: output voltage versus capacitor current plot under heavy loading condition.

imposed by the filter inductor L and input voltage v_{cc} combined with the high load crest factor. Note that when the switch is saturating on the crest (best possible control action), the transient evolution depends on the parameters of the converter only. This denotes the importance of the parameter selection to meet different design criteria (i.e., dynamic regulation, recovery time, steady state ripple, under different loading conditions).

4.10.3 Experimental Results in Mixed Mode

This section demonstrates through experimental results how the natural SS operated in mixed mode can improve the power quality of full-bridge inverters. The system is first evaluated under light loading condition using the same parameters obtained with the normalized design procedure. The results are shown in Fig. 4.27 (time domain)

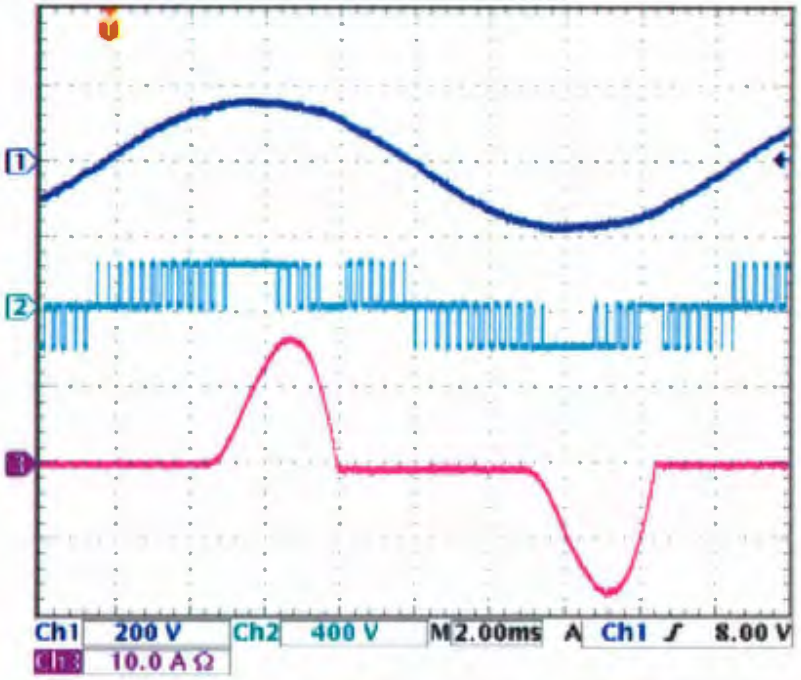


Figure 4.26: Monopolar mode of operation using the natural SS: output voltage (Ch1), switch state (Ch2), and output current (Ch3) under non-linear loading condition.

and Fig. 4.28 (phase plane), in which the operation in bipolar mode around the zero crossing of the output voltage can be observed. Even though the capacitor ripple current increases in this region due to the bipolar modulation (noticeable at 3.6kHz), a slight reduction of 0.2% THD in mixed mode is obtained (compared to monopolar mode), yielding 1.2% THD. In addition to this modest improvement, a significant enhancement will be seen under full loading condition.

As anticipated by the analysis presented in Section 4.8, the natural SS in mixed mode was able to maintain the harmonic distortion level under full resistive loading condition. The harmonic distortion remained at 1.2% reporting a significant reduction (1.4%) compared to the 2.6% THD measured in monopolar mode. The resulting waveforms are shown in Fig. 4.29 Fig. 4.30, where the likelihood of the full loading and light loading (Fig. 4.27 and Fig. 4.28) is remarkable. This clearly highlights the advantages of mixed mode over monopolar mode of operation, especially under heavy

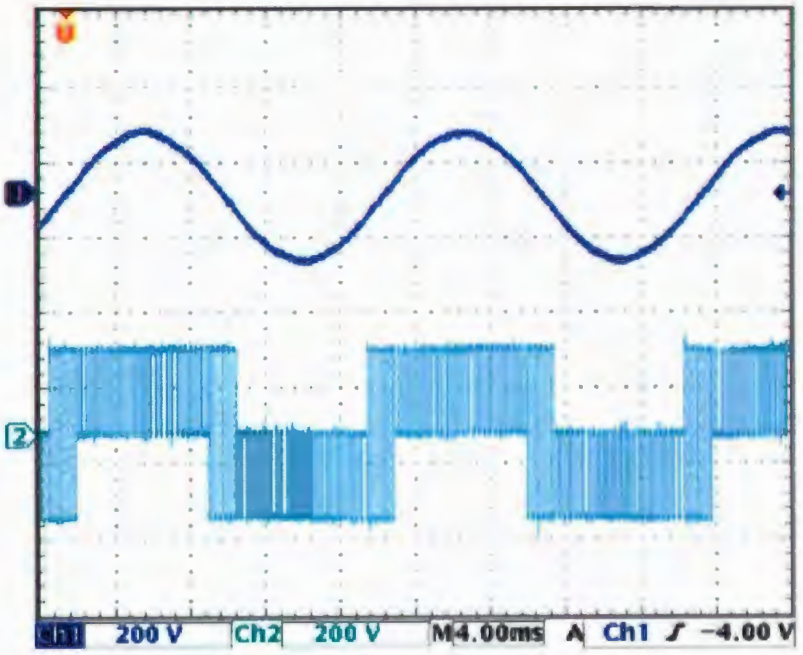


Figure 4.27: Mixed mode of operation using the natural SS: output voltage (Ch1), and switch state (Ch2) under light loading condition.

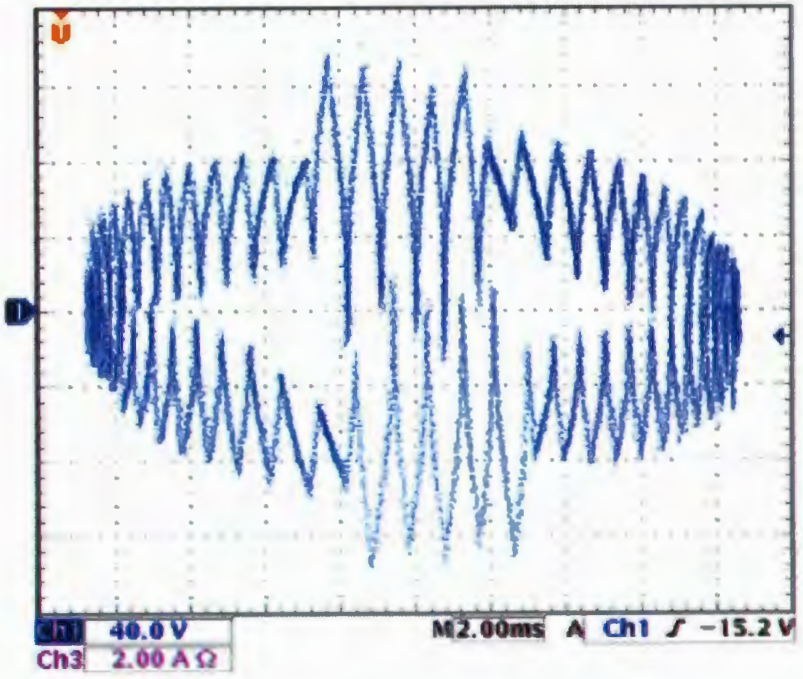


Figure 4.28: Mixed mode of operation using the natural SS: output voltage versus capacitor current plot under light loading condition.

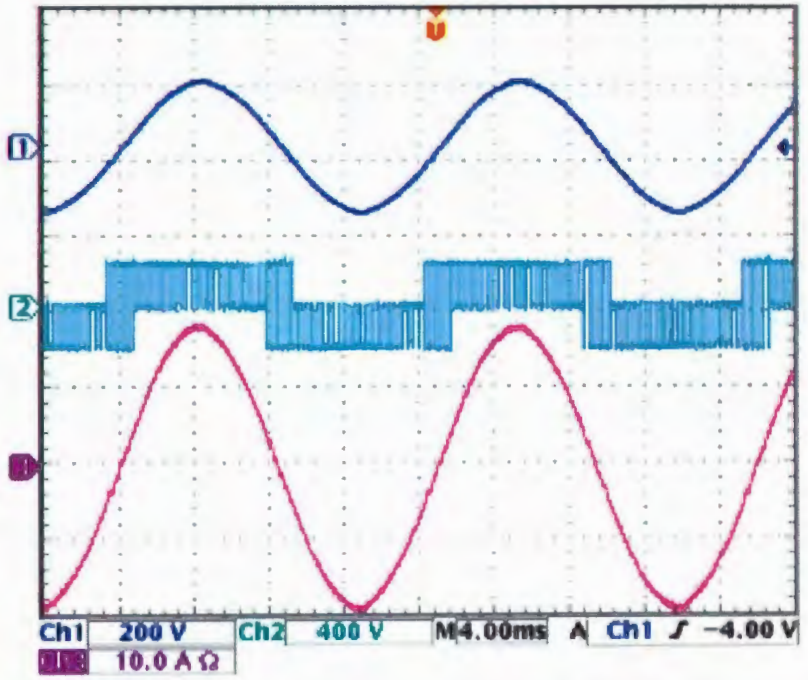


Figure 4.29: Mixed mode of operation using the natural SS: output voltage (Ch1), switch state (Ch2), and output current (Ch3) under heavy loading condition.

loading conditions.

Finally, mixed mode using the natural SS under non-linear load was evaluated with the same conditions as the monopolar mode. The results presented in Fig. 4.31, confirm that mixed mode behaves in the same way as the monopolar mode under high crest factor non-linear loads, reporting a similar total harmonic distortion (2.2% THD).

It has been demonstrated in this section that the natural SS (both monopolar and mixed modes) not only was able to produce high quality output voltage at moderate fixed switching frequency (3.6kHz) but also presented stiff regulation (0.25%) in the entire range of operation, from $120.3V$ with no load to 120 with full load.

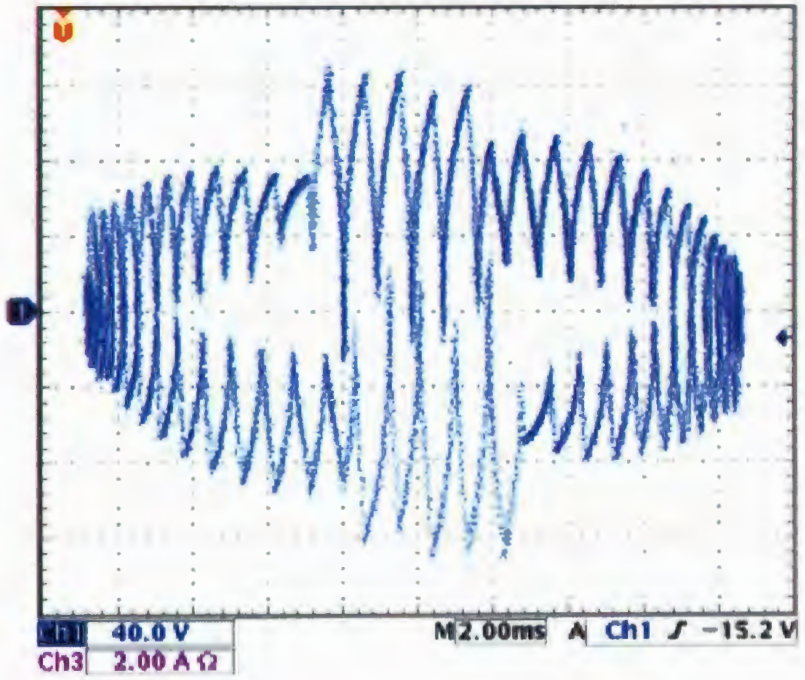


Figure 4.30: Mixed mode of operation using the natural SS: output voltage versus capacitor current plot under heavy loading condition.

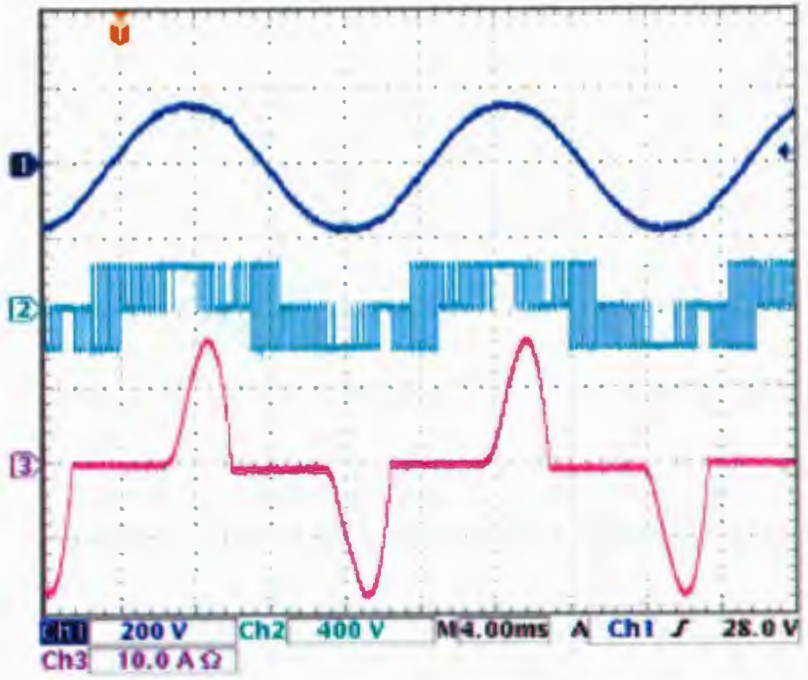


Figure 4.31: Mixed mode of operation using the natural SS: output voltage (Ch1), switch state (Ch2), and output current (Ch3) under non-linear loading condition.

4.10.4 Experimental Results in Mixed Mode Under Swinging Bus

In this subsection the experimental results are extended to operation under variable bus and swinging bus. The first set of experiments demonstrates the regulation of the natural SS when the bus voltage is changed from $170Vdc$ to $260Vdc$ in steps of $10V$ (41% total variation). The bus voltage is maintained constant for several cycles and the measurements are made in steady state operation. The results are presented in tabular form and classified by cases:

- Case 1: Maintaining a fixed v_{ccn} value in the control law (despite actual variations in the bus voltage). This is to demonstrate the robustness of the control law (parameter mismatch). The experiments are carried out under light and heavy loading conditions.

- Case 2: Measuring the bus voltage and using $vccn$ as a variable in the control law (following the changes in the bus voltage). This is to demonstrate improvements in the performance of the system. The experiments are carried out under light and heavy loading conditions.

Table 4.2 shows the steady state performance of the system for Case 1 under light loading conditions and Table 4.3 under heavy loading conditions. It can be seen that the regulation is maintained well bellow 1% within $200V$ to $250V$ range and remains below 2% under $200V$. These results are outstanding considering that the center of the natural SS (v_{ccn}) is maintained fixed when the bus voltage is in fact changing (refer to Sections 4.5 and 4.9 for details on the swinging bus principle of operation). As well, the THD remains at 1.5% or less in most cases, except for the low voltages measurements under full load. This slight increase in the THD is caused

Table 4.2: Case 1 - Bus variation under light loading conditions

Bus voltage (v_{cc})	*Output voltage* (v_o)	*Regulation %*	*THD*
170	118.0	1.67	1.5
180	118.5	1.25	1.3
190	119.0	0.83	1.3
200	119.7	0.25	1.3
210	120.1	0.08	1.3
220	120.3	0.25	1.2
230	120.6	0.50	1.2
240	120.7	0.58	1.1
250	121.0	0.83	1.2
260	121.4	1.17	1.3

Table 4.3: Case 1 - Bus variation under heavy loading conditions

Bus voltage (v_{cc})	*Output voltage* (v_o)	*Regulation %*	*THD*
170	117.8	1.83	1.6
180	118.8	1.00	1.9
190	118.7	1.08	1.5
200	119.5	0.42	1.3
210	119.9	0.08	1.4
220	120.0	0.00	1.2
230	120.1	0.08	1.1
240	120.3	0.25	1.0
250	120.6	0.50	1.1
260	120.9	0.75	1.3

Table 4.4: Case 2 - Bus variation under light loading conditions (measured v_{ccn})

Bus voltage (v_{cc})	*Output voltage* (v_o)	*Regulation %*	*THD*
170	118.6	1.17	1.2
180	119.2	0.67	1.1
190	119.5	0.42	1.1
200	120.0	0.00	1.2
210	120.2	0.17	1.3
220	120.1	0.08	1.2
230	120.4	0.33	1.7
240	120.5	0.42	1.3
250	120.6	0.50	1.3
260	120.7	0.58	1.6

by the proximity of the output voltage peak ($169.7V$) to the bus voltage, limiting the possibilities of a proper output voltage crest synthesis. The switching sequence is likely to remain in on-state in the region of the crest.

The following set of experiments reflects the performance for Case 2, where the bus voltage is measured and included as part of the control law. Table 4.4 shows the steady state performance of the inverter under light loading conditions and Table 4.5 under heavy loading conditions. As a results of incorporating the bus measurement, the regulation remains well below 1% within a bus voltage range of 180V to 260V. In general, an improvement in the regulation is visible throughout the entire range of operation. The THD is also maintained and even improved in some cases. The effect of low bus voltage (close to the output voltage peak) is also noticeable with a slight increase in the THD. As in the previous set of experiments, the switching sequence is likely to remain in on-state in the region of the crest.

What follows is the experimental validation of the natural SS under swinging bus operation. The experiments were carried out under heavy loading condition and the bus capacitor was selected to produce 10% voltage swing with constant current injec-

Table 4.5: Case 2 - Bus variation under heavy loading conditions (measured v_{ccn})

Bus voltage (v_{cc})	*Output voltage* (v_o)	*Regulation %*	*THD*
170	118.7	1.08	1.1
180	119.0	0.83	1.4
190	119.0	0.83	1.0
200	120.0	0.00	1.3
210	120.0	0.00	1.3
220	120.0	0.00	1.2
230	119.8	0.17	1.2
240	119.7	0.25	1.1
250	120.0	0.00	1.5
260	120.0	0.00	1.4

tion from the dc-dc converter. The effect of the swinging bus in the modulation of the pulses is depicted in Fig. 4.32. As can be seen, the switching sequence has an envelope that reflects the changes in the bus voltage. Note that in fig 4.32 the oscilloscope scales are 40.0V per division for the dc bus voltage (Ch1) and 100.0V per division for the switch state (Ch2). The output voltage of the system that results from this switching sequence is shown in Fig. 4.33. The measurements in Fig. 4.32 and Fig. 4.33 were taken under the same operating conditions to illustrate the steady state behavior of the bus voltage and the output voltage respectively. As predicted by the theory, the natural SS was able to accommodate the swinging bus effect and successfully produce high quality output voltage (1.8% THD) even at moderate switching frequencies. The slight increase in the THD is mainly related to limitations in the signal conditioning stage (bus voltage measurement circuit) rather than the natural SS. As the setup signal integrity improves, the resulting waveforms approximate more and more those of the theoretical analysis. Nevertheless, the control scheme has proven to the robust to noisy signals in general (i.e., capacitor voltage measurement).

Finally, the system is evaluated under a severe drop in the bus voltage, which

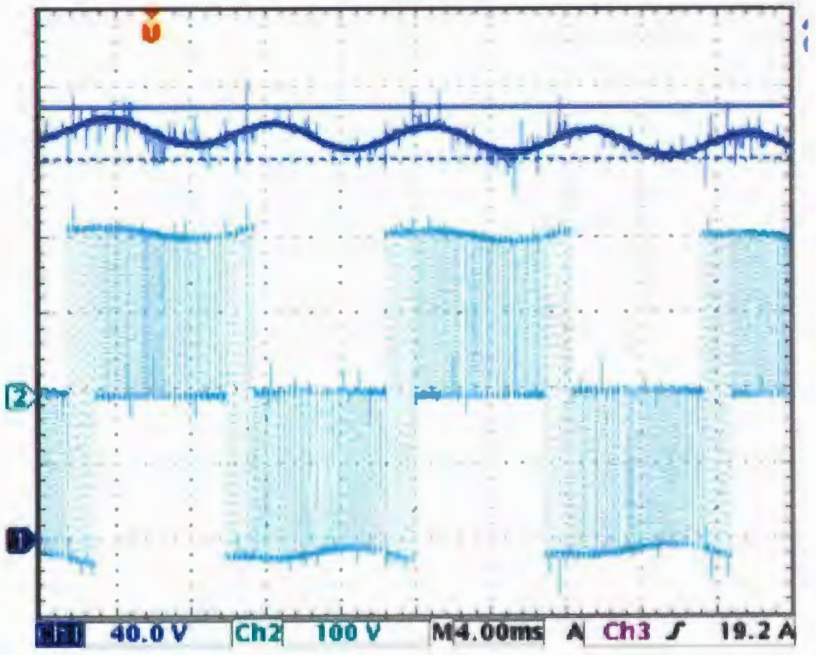


Figure 4.32: Swinging bus operation using the natural SS in mixed mode: dc bus voltage (Ch1), and switch state (Ch2).

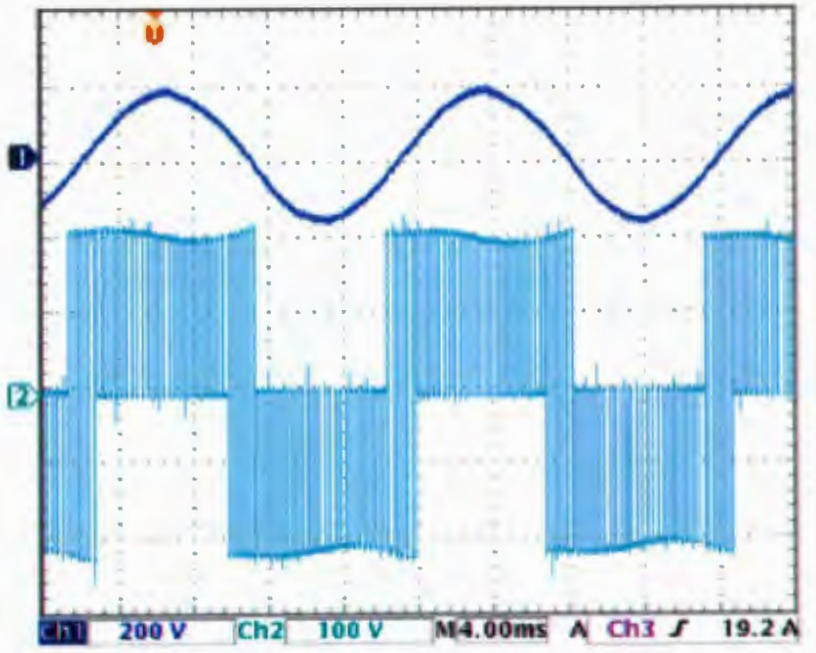


Figure 4.33: Swinging bus operation using the natural SS in mixed mode: output voltage (Ch1), and switch state (Ch2).

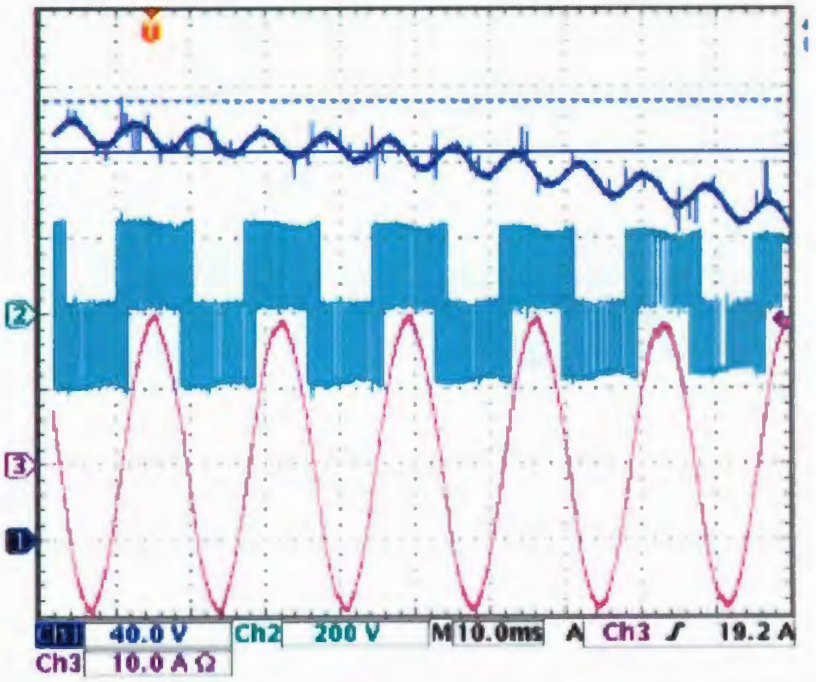


Figure 4.34: Swinging bus operation using the natural SS in mixed mode: dc bus voltage (Ch1), switch state (Ch2), and output current (Ch3) under heavy resistive loading condition.

is shown in Fig. 4.34. It can be seen that the bus voltage experiences a progressive voltage decrease from 230V (peak bus voltage value) to 160V (end of the oscilloscope capture). In spite of this severe transient under full load, the control scheme is able to compensate for voltage reduction and continue to supply the load. This result highlights the input voltage flexibility of the swinging bus inverter.

4.11 Summary

A curved switching surface (SS) referred to as natural SS for inverter control was derived in this chapter, showing superior characteristics under fixed and swinging bus operation. Both the output voltage and capacitor current were considered as varying references leading to a precise control law formulation with enhanced performance. The analysis was entirely carried out using a versatile geometrical method in

the normalized time domain, which avoids inaccuracies introduced by simplification or assumptions in charge balance methods. The proposed normalization technique provided remarkable insight into the behavior of the system, leading to a pure geometrical treatment that is general and applicable to any possible buck derived inverter. The natural SS was thoroughly investigated in monopolar, bipolar mode, and a novel mixed mode under fixed and swinging bus operation. It was demonstrated (analytically and experimentally) that this new mixed operating mode using the natural SS overcomes physical limitations of the inverter around the region of zero voltage crossing in monopolar mode. In addition to the enhanced dynamic response, fixed frequency operation was realized by employing discrete reference events. A transformation from the natural SS to its PWM equivalent was performed revealing the duality between boundary control using curved SS and the traditional PWM scheme. This is a significant advancement towards the unification and understanding of traditional modulation and modulation produced by curved SSs.

A design procedure in normalized domain was presented and illustrated with a 1.5kVA design example operating at a moderate switching frequency of 3.6kHz. The performance of the natural SS was evaluated experimentally with fixed bus and swinging bus in monopolar and mixed modes, achieving excellent regulation, low THD, and fast dynamic response.

Chapter 5

Embedded Monitoring and Diagnosis of Fuel Cell systems

A complete description and analysis of the components required to operate a FC generation system has been presented in the preceding chapters of this work. This included a number of subsystems, topologies, and control strategies required to operate the power conditioning stage of the FC power generation system. Yet one more critical component is required to realize a fully functional system, which has not been addressed by any of the proposed FC power generation schemes: in-situ FC monitoring and diagnosis system.

So far, measurement instruments that have been used in research laboratories to characterize and diagnose FC systems employ impedance spectroscopy and voltammetry [44, 45]. These precision instruments are costly and bulky, as they are meant to test a wide variety of electrochemical based systems. Interesting techniques to evaluate effects such as drying and flooding have been developed based on the measurement of the cell output impedance [46]. These techniques are derived from Frequency Response Analysis (FRA) methodology, which has also been

used extensively to characterize electrochemical systems in general. By using FRA technique the impedance of a system can be measured at different frequency values within a given spectrum of interest. The instrument injects a small AC perturbation signal to the FC and performs measurements of the voltage and current response [47]. This technique allows the characterization of different electrochemical processes that are produced at different timescales, which are fundamental for proper operation of the FC. For example, in a Proton Exchange Membrane Fuel Cell (PEMFC), the high-frequency response depends mainly on the electrode kinetic response, while the low-frequency response can be attributed to water management [48]. By computing the real and imaginary components of the impedance, the parameters of an equivalent electrical circuit of the system can be identified [21].

In this chapter, an embedded frequency response analyzer (EFRA) for FC systems based on a low-cost digital signal processor (DSP) is presented. The proposed measurement system is based on a technique known as lock-in amplification (LIA), which allows very accurate and precise ac measurements, even in the presence of high noise levels. This is a fundamental requirement since the FC output voltage contains ripple due to the effect of the converter switching frequency and the auxiliary equipment that are also supplied by the FC. The objective of this chapter is to develop this indispensable instrument with a simple hardware architecture and low power consumption, so it can be easily integrated as part of the FC control system or embedded in the FC power conditioning stage. By doing so, advanced features such as real-time monitoring and diagnosis will be available as part of the FC power generation system. The system is capable of measuring automatically the frequency response of the FC at different operating points, even when the FC is operating with load. These measurements can be used to characterize the FC at design stage and to perform on-line

monitoring of the FC state during continuous operation. The proposed hardware and signal processing technique are described in this chapter including experimental results of a 1.2kW PEMFC system.

5.1 Frequency Response Analysis in Fuel Cells

Measurement instruments for FC characterization that are commercially available [44, 45], mainly focus on electrochemistry techniques such as impedance spectroscopy and voltammetry. The main drawbacks of these instruments are lack of flexibility and high cost. In addition, such instruments cannot be reprogrammed to perform custom automated tests. Furthermore, an electronic load module [75, 76] is also required as part of the measurement device resulting in a bulky system. As an alternative to this commercial apparatus, a measurement system based on Fast Fourier Transform (FFT) has been developed [77] to characterize FC systems. However, FFT lacks noise immunity and good resolution at low frequencies.

Frequency Response Analysis (FRA) provides a very useful technique for FC characterization. FRA technique measures the impedance of a system at different frequency values within a given spectrum of interest. The instrument injects a small AC perturbation signal to the FC and performs measurements of the voltage and current response [47]. This technique allows the characterization of different electrochemical processes that are produced at different timescales such as electrode kinetic response and water management in PEMFC [48]. The FRA measurement is used to compute the real and imaginary components of the FC output impedance, leading to an identification of the parameters of the equivalent electrical circuit [21]. Since the AC perturbation signal has small amplitude, it can be superimposed on a DC signal allowing the measurement of the system at different operating points. The method

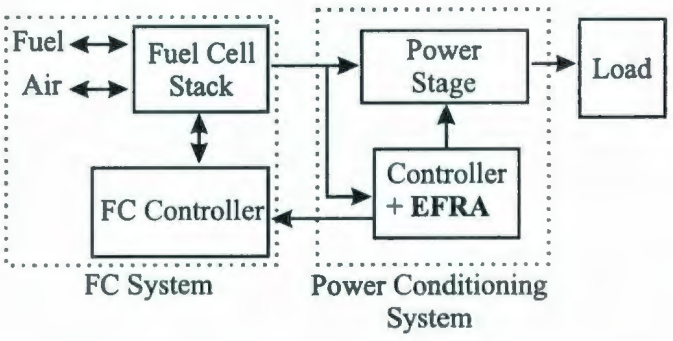
is therefore meant to provide measurements of the FC system (highly non-linear) at a quiescent operating point

This chapter presents a measurement instrument prototype based on a low-cost Digital Signal Processor (DSP). The proposed instrument performs FRA at programmable operating points, allowing automatic characterization of FCs. In comparison with commercial instruments, low-cost, low-power consumption and small size are the main advantages of the proposed system.

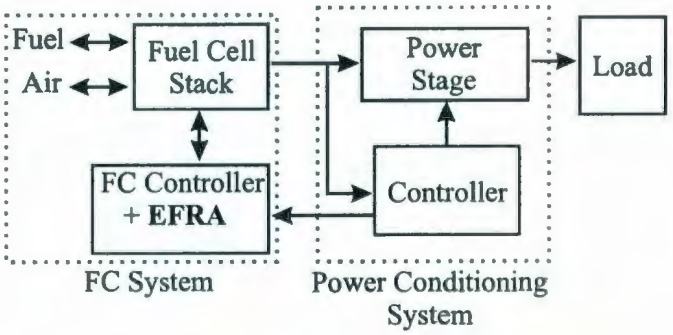
5.2 The Embedded Frequency Response Analyzer (EFRA)

The simplicity of the hardware architecture of the proposed FRA allows it to be easily integrated as part of the FC control system or embedded in the FC power conditioning stage. Such arrangement allows real-time monitoring and diagnosis of a real FC application. The proposed Embedded Frequency Response Analyzer (EFRA) is useful in the diagnosis of possible failures or performance evaluation during the FC operation.

Figure 5.1 shows two possible applications of the proposed EFRA. Fig. 5.1(a) shows the EFRA embedded into the power conditioning system. The EFRA algorithms can be implemented in the same processor that controls the power conditioning stage. In this application, the EFRA is linked with the FC controller, which regulates the FC operating parameters based on the on-line measurements. The EFRA measurements can also alert the power conditioning to prevent system failures. Fig. 5.1(b) shows another application example, where the EFRA is embedded in the FC system controller. Here the EFRA measures and regulates automatically the FC variables



(a)



(b)

Figure 5.1: Possible applications of the proposed EFRA: FRA embedded in a) the power conditioning system, and b) FC system.

to ensure proper FC operating conditions. It can also prevent FC damages in case of system failures or incorrect FC utilization.

5.3 Measurement Technique

The proposed system uses a measurement technique known as lock-in amplification (LIA) [78], which allows very accurate and precise AC measurements, even in the presence of high noise levels. The LIA uses a reference signal that can be generated by the same instrument or can be generated externally. In this work, the reference is generated by the instrument, which is embedded in the FC control system. The

general expression for the internal reference is,

$$r(t) = sin(2\pi f_s t) \tag{5.1}$$

The LIA input signal $i(t)$ is composed of a sinusoidal signal of frequency f_s added to a generic function that represents noise and the harmonic distortion, called $n(t)$:

$$i(t) = A\ sin(2\pi f_s t + \theta) + n(t) \tag{5.2}$$

A digital LIA amplifies and digitizes this signal. The DSP software multiplies the input signal by the in-phase and in-quadrature (shifted 90 degrees) components of the reference as given by,

$$P_p(t_i) = Ai(t_i) \times r_p(t_i) = \frac{1}{2} A\ cos(\theta) - \frac{1}{2} A\ cos(4\pi f_s t_i + \theta) + n_p(t_i) \tag{5.3}$$

$$P_q(t_i) = Ai(t_i) \times r_q(t_i) = \frac{1}{2} A\ sin(\theta) - \frac{1}{2} A\ sin(4\pi f_s t_i + \theta) + n_q(t_i) \tag{5.4}$$

where r_p and r_q represent the references in-phase and in-quadrature respectively, n_p and n_q represent the noise functions after the products, and the i^{th} sampling instant is represented by t_i.

By filtering the AC components and keeping only the mean value (the DC signal), two signals with the in-phase and in-quadrature components of the input signal are obtained as

$$x = 2\overline{P}_p \approx A\ cos(\theta) \tag{5.5}$$

$$y = 2\overline{P}_q \approx A\ sin(\theta) \tag{5.6}$$

Thus, the magnitude and phase of the input signal can be computed as

$$M = \sqrt{x^2 + y^2} = A \tag{5.7}$$

$$Ph = tan^{-1}\left(\frac{y}{x}\right) = \theta \tag{5.8}$$

where $tan^{-1}(y/x)$ computes the inverse tangent function of y/x and takes into account the signs of both variables in order to give the correct quadrant.

5.4 System Implementation

A prototype of the proposed instrument was implemented using a low-cost fixed-point DSP (TMS320LF240xA). Since fixed-point DSPs are commonly used in power electronics applications, this system can be easily embedded in the FC controller or the power conditioning stage.

5.4.1 Software and Hardware Description

Figure 5.2 shows a conceptual block diagram of the proposed system. The DSP generates a current reference that is composed of a small AC signal superimposed on a DC operating point. This reference signal feeds a closed-loop current source that controls the load of the FC. The current regulator is implemented with an operational amplifier driving a MOSFET working in the active region. Current measurement is performed using a precision sensing resistor.

Measured signals (current and voltage) are amplified using low-noise and wide bandwidth operational amplifiers. The bandwidth of the signal conditioning must be wide enough to avoid phase shifts that may lead to errors in the impedance measure-

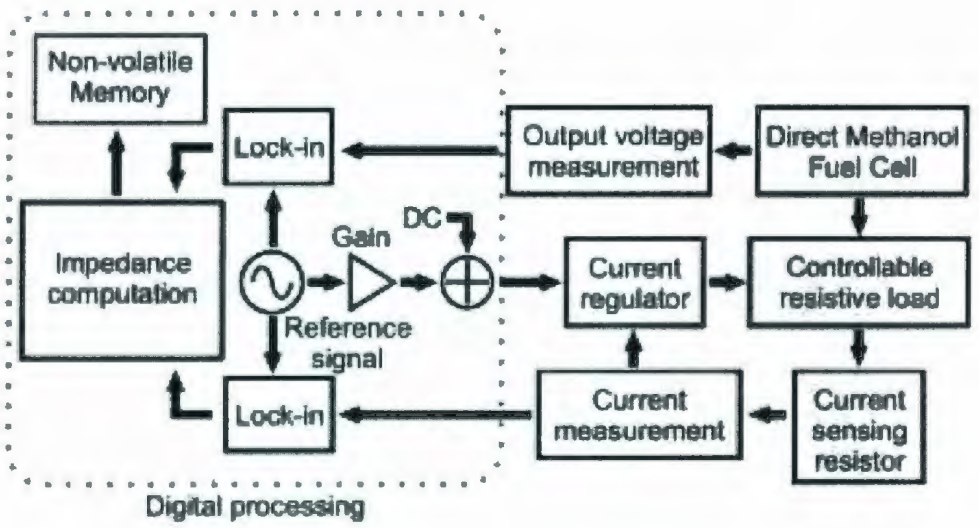


Figure 5.2: Conceptual block diagram of the embedded instrument.

ments.

The current and voltage measurements are digitized using the DSP on-chip analog-to-digital converters (ADC) at a sample rate of 50kHz. Each ADC conversion generates an interrupt that runs the following routines:

- Current reference generation: the DSP computes the current reference value and sends it to a serial digital-to-analog converter.
- Lock-in algorithm computation: two identical lock-in algorithms are computed, as shown in Fig.5.3. With the current and voltage measurements, the DSP computes the electrical impedance at the measured frequency and stores it in memory.

The lock-in block implements the mathematical operations described in the previous section. First, the input signal (voltage or current) is multiplied by the in-phase and in-quadrature references. After that, the mean value is obtained by filtering the AC components, which is proportional to the peak value of the input signal at the reference frequency.

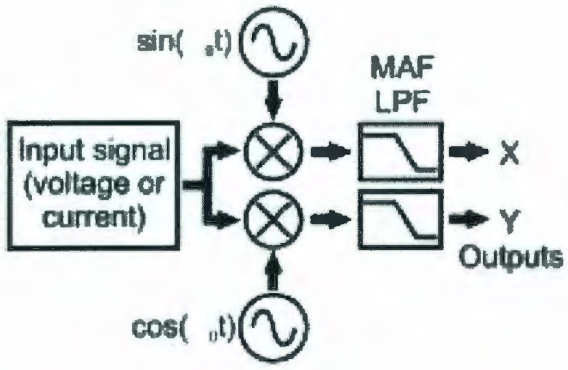


Figure 5.3: Lock-in amplification block diagram.

In order to efficiently filter out the reference harmonics produced in (5.3) and (5.4), a Moving Average Filter (MAF) is employed as a low-pass filter (LPF). This filter performs the average of k periods of the reference signal, where k is an integer number. By incrementing the number of averaged periods k, the signal-to-noise ratio (SNR) of the measurements is also incremented. Figure 5.3 shows a block diagram of two LIA including the MAF. The outputs of the LIA are two DC values that correspond to the in-phase and in-quadrature values of the input signal. From the measured voltage and current, the complex impedance is computed as:

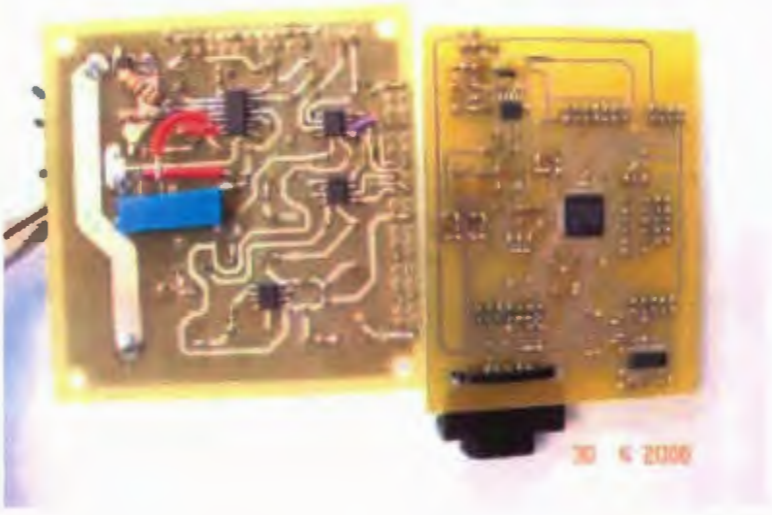
$$Z(\omega_0) = R(\omega_0) + jX(\omega_0) \tag{5.9}$$

$$R(\omega_0) = Re\{\frac{V(\omega_0)}{I(\omega_0)}\} = \frac{V_X I_X + V_Y I_Y}{{I_X}^2 + {I_Y}^2} \tag{5.10}$$

$$X(\omega_0) = Im\{\frac{V(\omega_0)}{I(\omega_0)}\} = \frac{V_Y I_X - V_X I_Y}{{I_X}^2 + {I_Y}^2} \tag{5.11}$$

where V_X, V_Y, I_X and I_Y are the in-phase and in-quadrature components of the measured voltage and current, respectively. The instrument takes the impedance measurements at many frequencies (N), configured by the user, in order to obtain

(*a*)



(*b*)

Figure 5.4: DSP board and instrumentation prototype: a) Top view and b) bottom view.

the frequency response in the required range of frequency. The connection between the instrument and other equipment is performed through a CAN bus that ensures robust high-speed data transmission under noisy electrical environments [79]. A picture of the system prototype is shown in Fig. 5.4.

5.4.2 Measurement Sequence

The implemented prototype operates in stand alone mode and performs the measurements automatically. A PC is only used to configure the measurement parameters and to download the measurement data through the CAN bus. A screen-shot of the PC software is shown in Fig. 5.5. The procedure required to measure the frequency response of the FC is described as follows:

1. The user generates a configuration file that stores the measurement parameters. These parameters are sent to the DSP through the CAN bus. The measurement parameters are shown in Table 5.1. The PC software computes the N frequency values distributed logarithmically within the specified frequency range.

2. The DSP starts the measurement process triggered by an external signal (push button, digital input or CAN message).

    - First, the no-load voltage is measured by setting to zero the current reference.
    - The current reference is set to a fixed DC value and the DC impedance is measured.
    - Finally, the DSP starts the N-point frequency response measurement. Before measuring each frequency point, the DSP waits a settling time to avoid measurement errors due to current and voltage transients.

Table 5.1: Definition of Measurement Parameters

FRA parameters	*Meaning*
N	*Number of freq. points*
f_{min}	*Minimum freq. value*
f_{max}	*Maximum freq. value*
k	*Number of cycles per freq.*
T_{min}	*Minimum time per freq.*
T_{max}	*Maximum time per freq.*
T_{wait}	*Wait time before each measurement*

3. When the EFRA finishes the frequency scan, it stores the measured values in memory and waits for a new measurement. The data is stored in memory until it is downloaded to the PC through the CAN bus.

5.5 Experimental Results: Fuel Cell Electrical Equivalent Circuit

The performance of the proposed instrument was first evaluated using a FC equivalent circuit implemented with a discrete passive network. The electrical equivalent circuit presented in the introductory chapter (Section 1.1) is shown in Figure 5.6. As discussed in Section 1.1, the model accounts for voltage drop or irreversibility produced by activation losses, fuel crossover, internal currents, ohmic losses, and mass transport. Even though FCs are highly non-linear systems, a linear electrical equivalent circuit represents approximately the electrical behavior of FC when operated with small signal at a quiescent operating point. For this reason, the instrument was first evaluated using a known network that matches the FC equivalent electrical model.

The results using the EFRA for the electrical equivalent circuit in Fig. 5.6 were

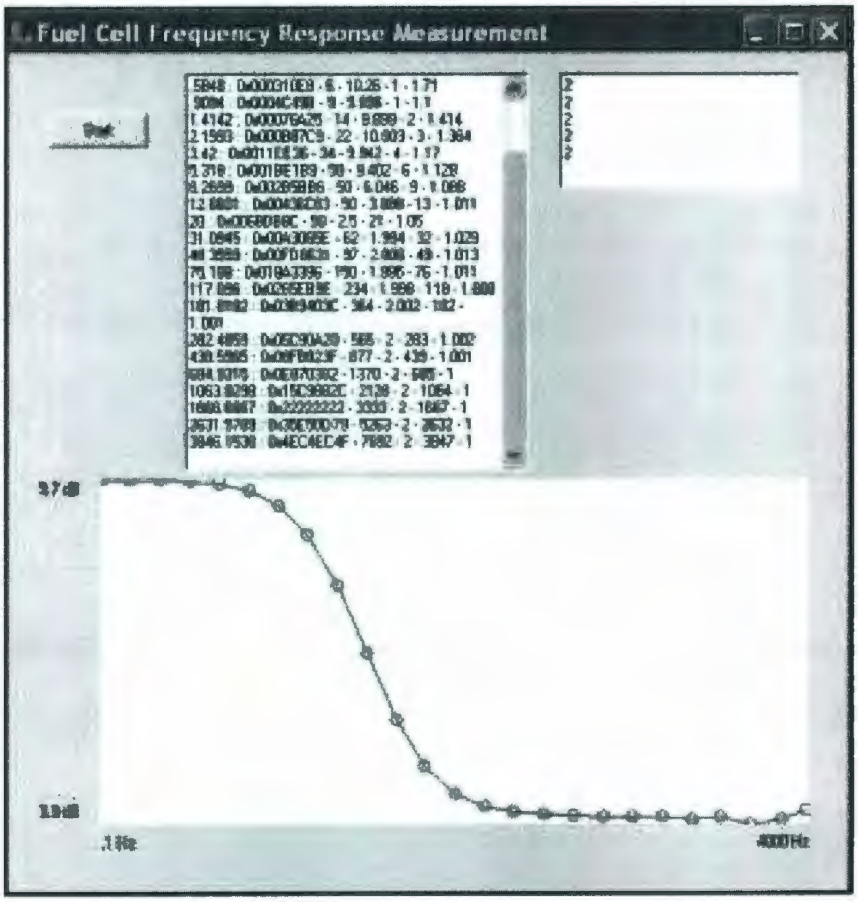


Figure 5.5: Windows user interface: EFRA programming and download tool.

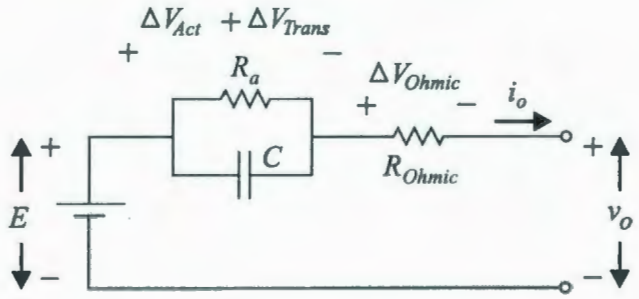


Figure 5.6: Electrical equivalent model of the FC.

Table 5.2: Circuit Measurement Parameters

Circuit parameters	*Value*
Ra	1.07 Ω
$Rohmic$	1.00 Ω
C	36,000 μF
ESR	80 $m\Omega$
ESL	50 μH
FRA parameters	*Value*
N	25 *points*
$fmin$	0.1 Hz
$fmax$	5 kHz
k	50 *cycles*
$Tmin$	10 s
$Tmax$	20 s
$Twait$	1 s

compared to both the theoretical behavior of the network as well as the response using a Commercial Frequency Response Analyzer (CFRA) [44]. Fig. 5.7 and Fig. 5.8 show the frequency response (magnitude and phase respectively) and Fig. 5.9 the Nyquist impedance diagram for the FC electrical equivalent circuit using the parameters in Table 5.2. As can be noted in Fig. 5.7, Fig. 5.8 and Fig. 5.9 the EFRA accurately fits the response obtained with the CFRA. Moreover, when the ESR and ESL values of the capacitor are included in the electrical equivalent circuit, both analyzers perfectly match the theoretical frequency response and impedance diagram.

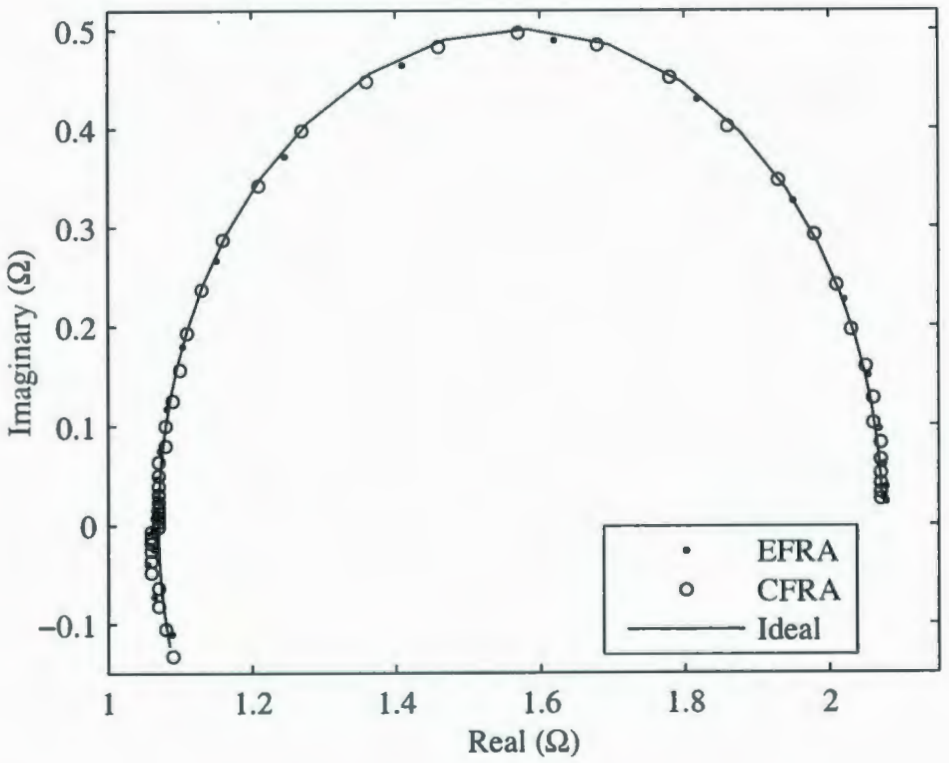


Figure 5.7: Bode magnitude plot: Embedded FRA (EFRA), commercial FRA (CFRA), and ideal response.

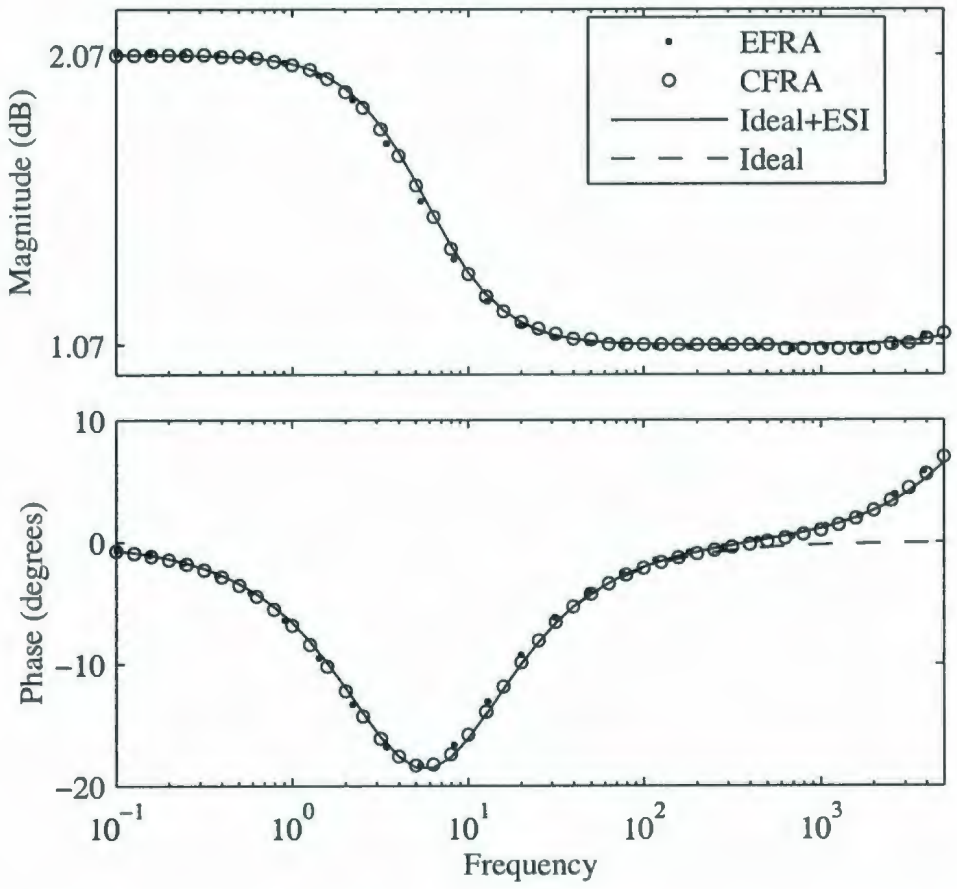


Figure 5.8: Bode phase plot: Embedded FRA (EFRA), commercial FRA (CFRA), and ideal response.

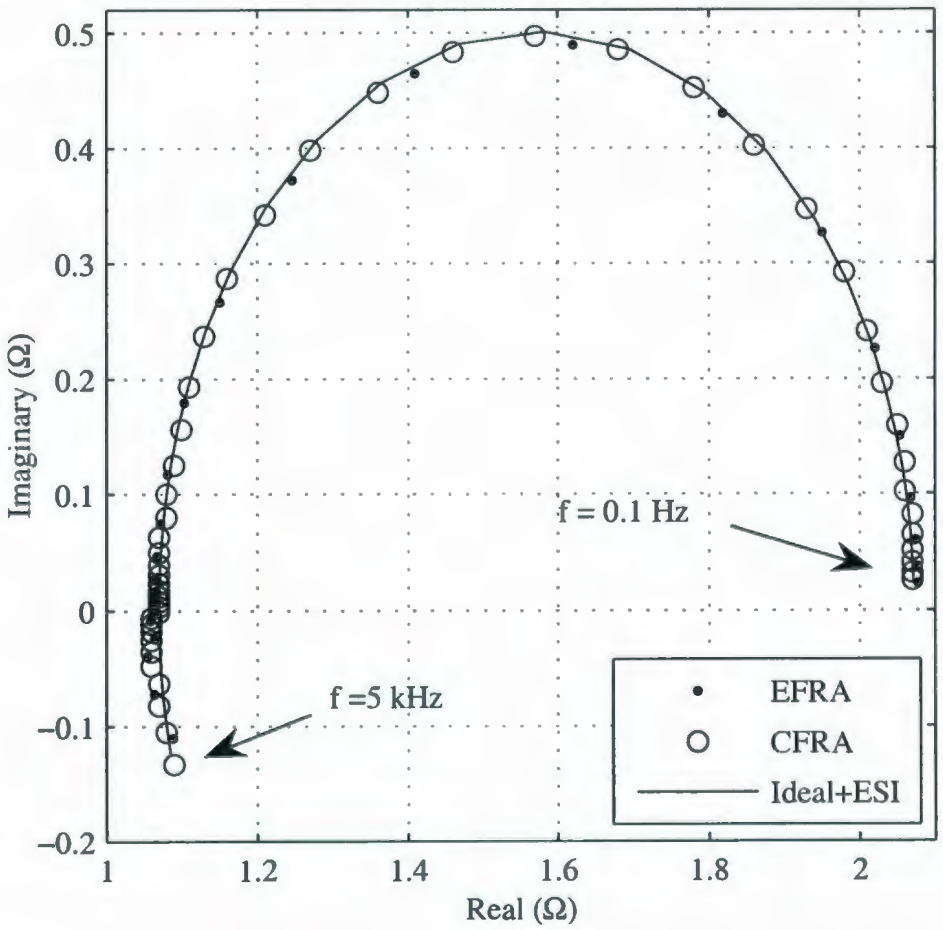


Figure 5.9: Nyquist impedance plot: Embedded FRA (EFRA), Commercial FRA (CFRA), and ideal response.

Table 5.3: Measurement Parameters

FRA parameters	*value*
N	30 *points*
f_{min}	0.1 Hz
f_{max}	5 kHz
k	50 *cycles*
T_{min}	10 s
T_{max}	20 s
T_{wait}	1 s

5.6 Experimental Results: Proton Exchange Membrane Fuel Cell

The proposed EFRA is used to perform frequency response analysis of a Ballard Nexa 1.2kW PEMFC system [80] operating with a fixed fuel pressure of 1.6 barg and variable air flow rate (automatically controlled by the system). The experimental measurements consist of extracting a fixed DC current superimposed by a small AC signal with variable frequency. The DC current sets the operating point of the FC, and the AC signal is used to measure the impedance of the FC at different frequencies. The measured frequency response is used to compute the parameters of the FC equivalent circuit.

The frequency response of the PEMFC at three different operating points was performed using the parameters of Table 5.3. Figure 5.10 and Fig. 5.11 show the magnitude and phase of the frequency response. Figure 5.12 shows the resulting impedance diagram. It can be noted in this plot that the impedance values for low frequencies vary significantly at different operating points.

From the Nyquist impedance plot in Fig. 5.12, the parameters of the FC equivalent electrical circuit can be obtained as follows. Since the charge double layer capacitor

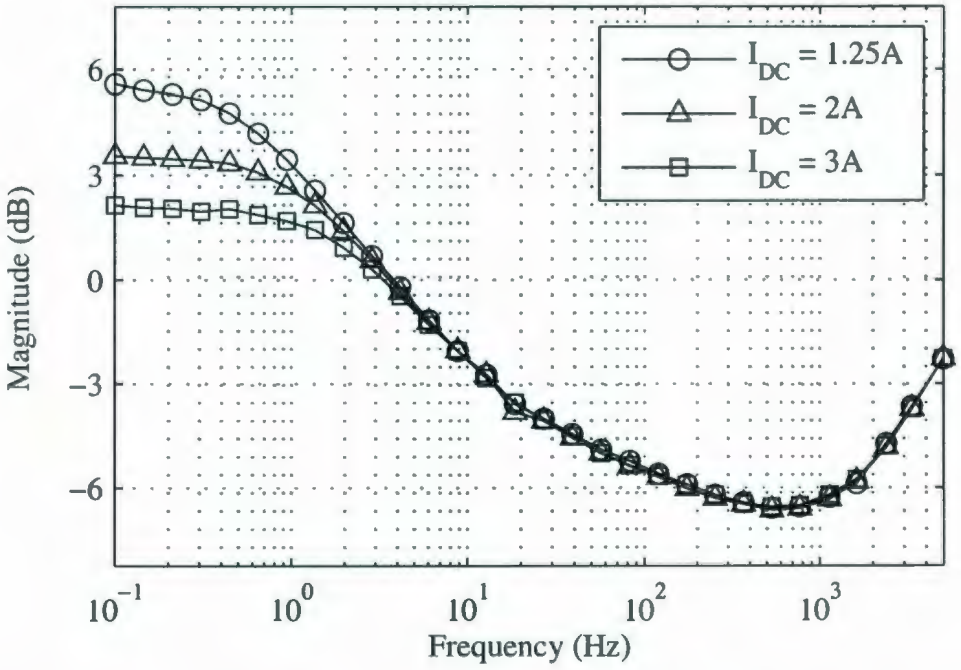


Figure 5.10: Bode magnitude plot of a PEMFC using the EFRA for three operating points.

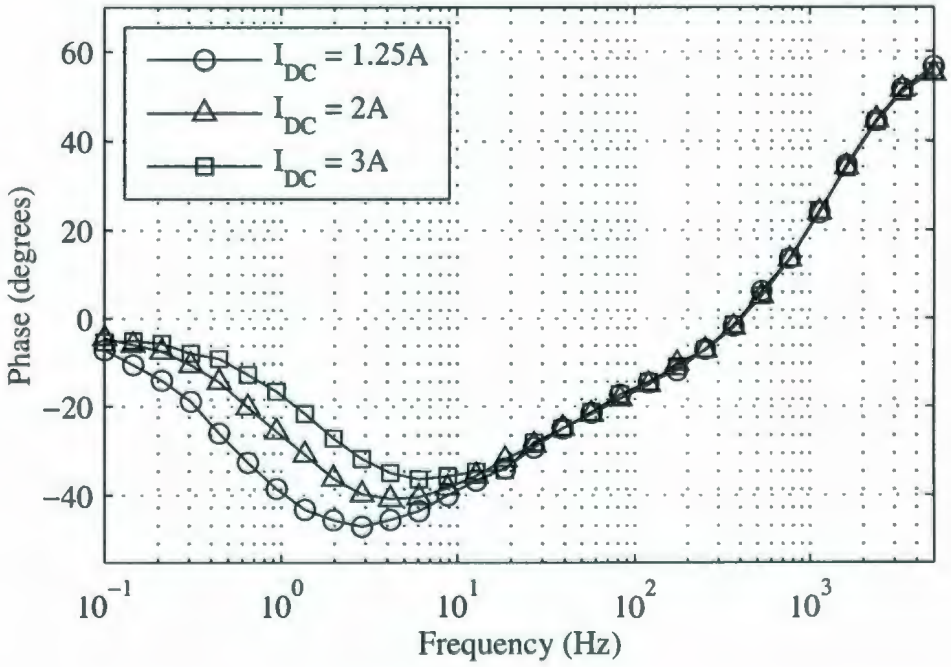


Figure 5.11: Bode phase plot of a PEMFC using the EFRA for three operating points.

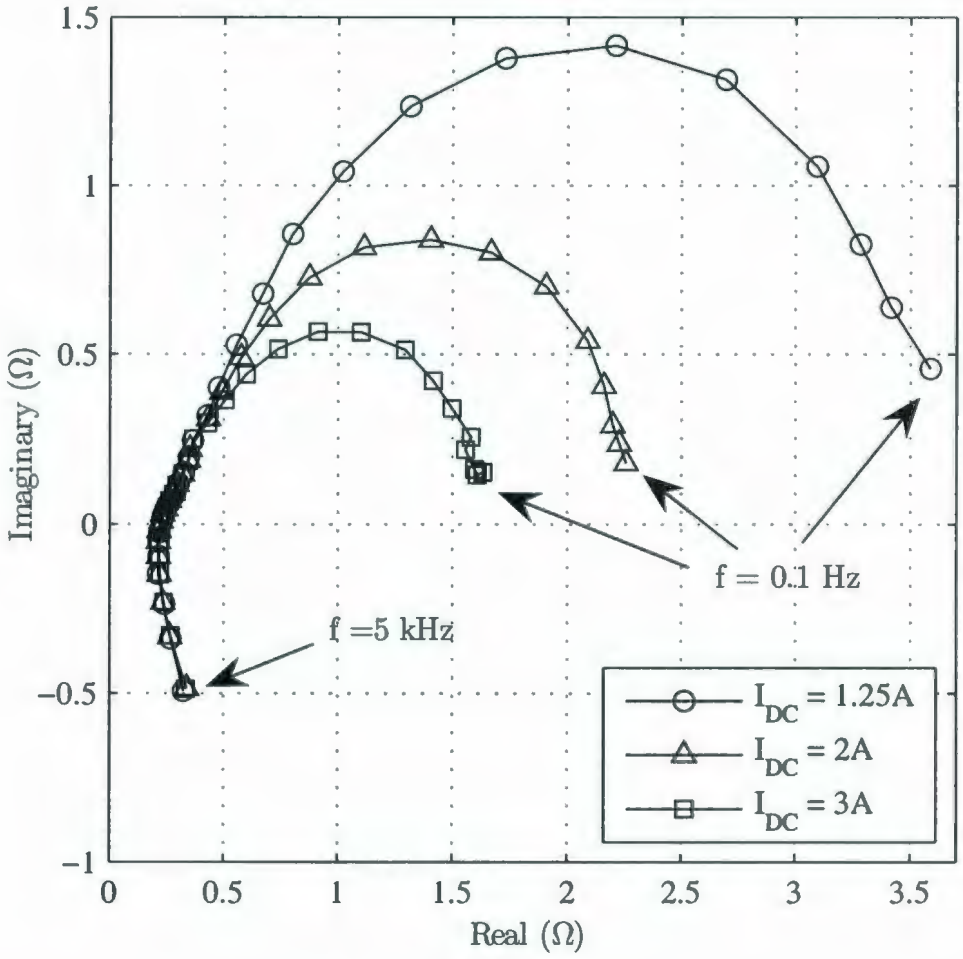


Figure 5.12: Nyquist impedance plot of a PEMFC using the EFRA for three operating points.

Table 5.4: Equivalent Circuit Parameters Estimation

I_{dc}	R_{Ohmic}	R_a
$1.25A$	$220m\Omega$	$3335m\Omega$
$2A$	$220m\Omega$	$2030m\Omega$
$3A$	$220m\Omega$	$1430m\Omega$

C has large impedance for low frequencies, the low frequency points (0.1 Hz) in the Nyquist impedance plot indicates approximately the sum of R_a and R_{Ohmic}. On the other hand, C presents very low impedance at high frequencies. Particularly, when the imaginary component is equal to zero at high frequencies, the impedance diagram indicates R_{Ohmic} value, which is equal for the three evaluated operating points. Hence, by evaluating two specific frequencies, these important parameters can be estimated using the EFRA providing a valuable tool for on-line monitoring, diagnosis, and characterization of FC. Table 5.4 shows the estimated values for the evaluated operating points.

Finally, Fig. 5.13 shows the ac components of the output voltage for currents of different frequencies extracted by the EFRA. It can be noted that the FC output voltage contains ripple as well as noise due to the load and the auxiliary equipment, which is also supplied by the FC (e.g. air blower and electronic control board). As the frequency of the sinusoidal current extracted by the EFRA increases, the signal to noise ratio decreases dramatically (here signal is considered as the ac voltage component of the same frequency as the EFRA current). As predicted by the lock-in amplification theory, the proposed instrument was able to obtain accurate and precise measurements even in the presence of high noise levels.

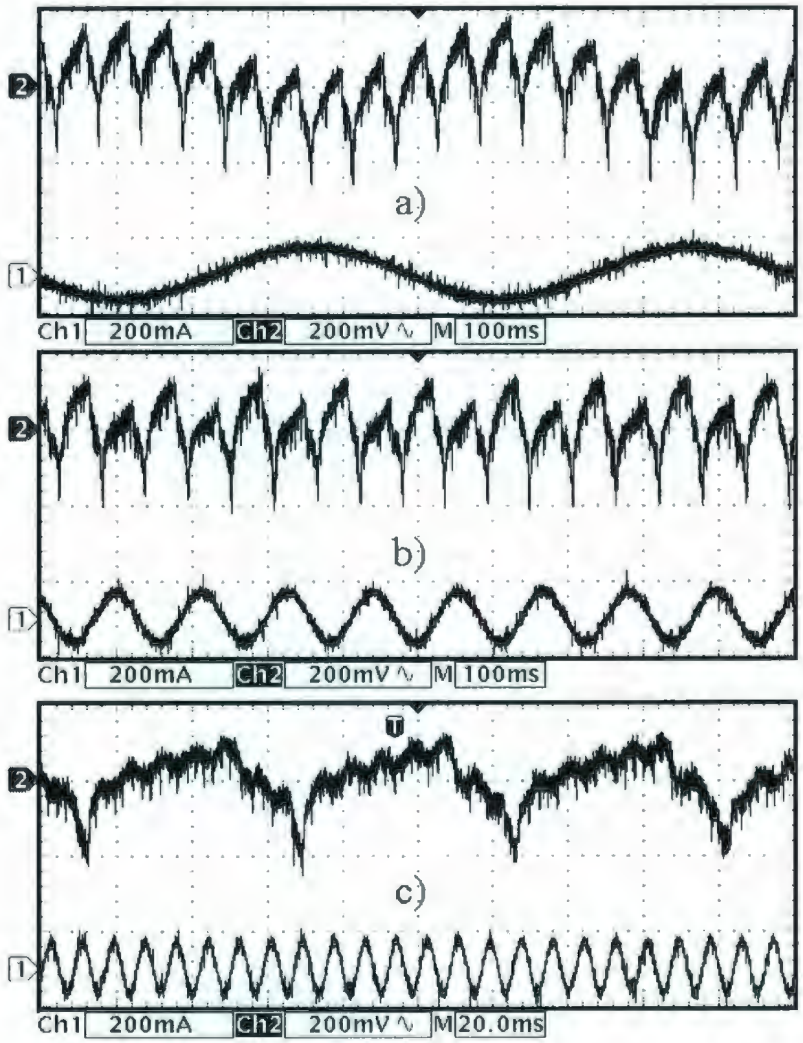


Figure 5.13: EFRA current extraction waveform (Ch1) and PEMFC output voltage waveform (Ch2): a) Current extraction frequency below ripple voltage frequency, b) current extraction frequency close to ripple voltage frequency, and c) current extraction frequency beyond ripple voltage frequency.

5.7 Summary

A measurement instrument for FC monitoring and characterization based on a low cost DSP was presented in this chapter. Due to its simple hardware architecture and low power consumption, it can be easily integrated as part of the FC control system or embedded in the FC power conditioning stage. Such arrangement allows performing real-time monitoring and diagnosis of a real FC application. A robust digital lock-in amplification technique provides the required accuracy to the measurements under noisy electrical environments. Hence, the embedded instrument can be used on-line, while a power electronics stage is extracting power from the FC.

The proposed embedded instrument can be used in the diagnosis of possible failures or in the evaluation of the FC performance during its operation. As well, the proposed instrument allows the equivalent circuit parameters of the FC to be estimated.

Chapter 6

Conclusions

Stand-alone Fuel Cell (FC) power generation systems present strong interaction between the load, the power conditioning stage and the FC stack, making design and coordinated operation a remarkable challenge. Residential power supply, building power supply, and portable power supply are some of the potential applications for FC systems, comprising high energy standards in terms of efficiency, low emissions, and quiet operation. A high-performance FC power conversion system was presented in this work covering key aspects such as power quality, power extraction, system behavior, efficiency, dynamic response, and monitoring.

6.1 Concluding Summary and Future Work

The principle of operation of polymer-electrolyte FC systems (both PEMFC and DMFC) was described in Chapter 1. The steady state and dynamic behavior of these power sources was discussed in detail. It was seen that the FC provides unregulated dc output voltage and a power conditioning stage is required. Two key concepts were

emphasized, namely power availability and power reduction under low frequency ripple current, which were analyzed experimentally and explained with the aid of an electrical equivalent model of the FC.

The voltage regulation nature of the polymer-electrolyte FC was taken into consideration to develop a dc-dc isolated power converter. The full-bridge forward converter was preliminary selected as a base topology and studied under traditional hard switching phase shift PWM and ZVS operation. Since the FC is a low-voltage high-current source, the circulating current in the primary produces very high conduction losses due to the MOSFETs $R_{ds_{ON}}$, resistance of the copper traces and transformer windings. This is opposed to traditional high-voltage applications of the full-bridge forward converter where low-current is experienced (i.e., telecom power supplies). For FC systems, it was found that unnecessary conduction losses in the primary should be avoided. As well, the turn-on losses associated with the output capacitance (Coss) of the MOSFETs were much lower than that of a traditional high input voltage application. Recall that the energy in Coss is a function of the square of the input voltage. Therefore, the efficiency gains in operating under ZVS in the MOSFETs are small or negligible. When the output rectifier was examined (high voltage side), it was seen that reverse recovery losses were attenuated due to limited di/dt introduced by the auxiliary leakage inductance in ZVS. However, the excessive transformer ringing in the secondary that is characteristic of this topology, aggravated the overall reverse recovery losses and forced the use of snubbers.

A modified topology of the full-bridge forward converter was proposed to overcome the problems outlined above. The voltage regulation nature of the polymer-electrolyte FC and the loading conditions from 0 to 100% were considered as part of the investigation. Two auxiliary inductors were included in the output rectifier to

reduce reverse recovery losses and transformer ringing. A novel modulation sequence to achieve soft switching and minimize unnecessary conduction losses was proposed to operate the converter to further improve its efficiency. Comparative efficiency measurements were performed using state-of-the-art prototypes to demonstrate that the efficiency of the proposed full-bridge modified topology improved by 2% over the full-bridge ZVS when operated with a FC power source under any loading condition. Future work in the area will include aspects of power modularity, paralleling and redundancy, control architectures of multiple converters, as well as the development of a small-signal model for the proposed modified topology. Other possible applications for the proposed topology such as low-voltage photovoltaic power conversion will also be investigated.

The interaction between the various components of the system were identified and discussed. A strategy referred to as swinging bus was investigated to eliminate undesirable low frequency ripple current in the FC. The objective was to maximize the power extraction while maintaining high power quality. The investigation was carried out with the aid of a system behavioral model that covered medium to low frequency range of the dynamic system. In this way, the current reflection from the inverter load through the dc-dc converter and the FC were clarified. The importance of the dc bus voltage charge balance in the swinging bus scheme was identified as the key mechanism to successfully operate the system and establish the requirement for the inverter input range. The proposed swinging bus scheme was thoroughly evaluated in time and frequency domain, and a feedback loop using discrete-time signal processing was implemented. Finally, the system steady and dynamic operation was investigated using a combination of swinging and stiff bus operation. It was seen that the bus voltage not only had cyclic swings but it also

experienced a drop when a sudden load change was applied. When the system experienced a large load transient, the bus voltage dropped below the inverter nominal operating voltage forcing the system to operate under stiff bus. In this way, a fast recovery in the bus voltage was achieved at the expense of short duration ripple current operation.

Future work will include the analysis of the system under special operating conditions such as, startup, shutdown, standby, sleep mode, overload, hold up time during purging, and general protections.

The inverter power conversion stage was addressed with the objective of producing high quality output voltage under demanding operating conditions (wide input voltage range and loading capability). The low frequency ripple current generated by the inverter was absorbed by the dc-dc power converter to prevent power availability reduction in the FC. As a result, the bus capacitor voltage varied cyclically with double the inverter output frequency to absorb low frequency ripple current, presenting an unprecedented challenge for the control scheme of the inverter. In order to comply with stringent standards for transient and steady state performance, a control scheme based on curved switching surfaces (SS) was proposed for the inverter. A novel curved SS referred to as natural SS was derived using a versatile geometrical method in the normalized domain, providing remarkable insight into the behavior of inverter. The natural SS was thoroughly investigated in monopolar, bipolar mode, and a novel mixed mode under fixed and swinging bus operation showing superior characteristics. The new mixed mode demonstrated the ability to overcome physical limitations of the inverter around the region of zero voltage crossing in monopolar mode. Duality between boundary control using curved SS and the traditional PWM carrier was revealed using a transformation. This is

a significant advancement towards the unification and understanding of traditional modulation and modulation produced by curved SSs.

An effective normalized design procedure was presented and illustrated with a 1.5kVA design example operating at a moderate switching frequency of 3.6kHz to highlight the benefits of the normalization technique. The performance of the natural SS was first evaluated experimentally with fixed bus in monopolar and mixed mode, reporting 1.4% THD and 1.2% THD respectively under light loading condition. Despite the moderate switching frequency, the inverter in mixed mode was able to maintain 1.2% THD under heavy resistive loading condition. The results were extended to variable and swinging bus operation, achieving excellent regulation, low THD, and fast dynamic response. As well, the behavior under high crest factor non-linear load also reported excellent performance.

Future work in this area will include the study of boundary control using curved SS for other topologies and application. The normalization and geometrical method will be extended to other topologies as well and combined with design of controllers in the normalized domain. The mixed mode modulation will be used to create new PWM carriers to achieve enhanced performance and implemented in digital platforms such as DSPs.

An Embedded Frequency Response Analyzer (EFRA) was proposed to perform online monitoring of the FC. The objective of this sub-system was to provide real-time measurement of the cell output impedance to predict different electrochemical processes produced at different timescales. This information can be used to prevent effects such as drying and flooding and to compute the real and imaginary components of the cell impedance to fit the parameters of an equivalent electrical circuit. The proposed EFRA measurement system was based on a technique known as lock-in

amplification (LIA), which allows very accurate and precise ac measurements, even in the presence of high noise levels (i.e., switching noise and voltage ripple). The instrument was implemented in a low-cost DSP with a simple hardware architecture and low power consumption, so it can be easily integrated as part of the FC control system or embedded in the FC power conditioning stage. Such arrangement allows performing real-time monitoring and diagnosis of a real FC application.

Impedance track for electrochemical based sources is a promising area of research. The importance of such methods is comparable to the strategies used to supervise the state of charge in systems based on batteries (i.e., laptop computers, hybrid vehicles and UPS systems). Future work will include dynamic control of FC stacks to achieve optimal operating conditions using the EFRA.

FC power generation finds application in a number of stand alone areas: residential power generation, building co-generation (schools, hospitals, and buildings), portable power, vehicle auxiliary power (i.e., automobile, trucks, ships, etc). In residential power generation, the power consumption ranges from a few kilowatts to tens of kilowatts. In this case, the loading condition changes depending on the time of the day. For example, the system may operate under light or no loading conditions during the night and at full loading condition early in the morning. The system should therefore be able to operate with high efficiency in the entire power range, requirement that has been fulfilled in this work. In residential applications the loading condition can suddenly change from zero to full power. For this reason, the power generation system should be able to cope with large load transients while maintaining power quality. This can be achieved by the coordinated operation of the dc-dc converter and inverter power stages as described in Chapters 2, 3 and 4. As well, the type of load can significantly vary comprising resistive, non-linear with

high crest factor, inductive, and a combination of them. In section 4.10 the proposed system was evaluated under all this possibilities with excellent results.

Building co-generation presents a simpler case scenario. While the overall power rating is much higher than in residential (hundreds of kilowatts), the instantaneous percentage change in loading conditions is not as severe as the residential application. That is, the system can reach full loading condition after a large number of small loads have been activated sequentially. Such behavior prevents the system from entering in large transient operation (explained in Section 3.5) thus, simplifying the task of the system controller.

Portable power is another potential area of application for the proposed system. For portable apparatus that require dc voltage the proposed dc-dc topology would be employed, which should be connected directly to supply the load. The transformer ratio and the rating of the output rectifier should be modified to match the input specifications of the system to be supplied. In the case of ac loads, the full proposed system would be employed following the same principle of operation and behavior explained in this work. As well, the possibility of supplying both dc and ac load can be considered as part of the arrangement. While the ac load is supplied by the inverter, the dc load can be connected to the dc bus or an auxiliary output of the dc bus. Finally, vehicle auxiliary power supply finds characteristics similar to those of the portable power application, which may require combining dc and ac loads.

6.2 Specific Contributions

Four critical sub-systems which were identified and investigated in this work are summarized below along with the major contributions and outcomes.

A) Isolated dc-dc power converter topology (Chapter 2): This included an investigation of the existing power converter topologies and the analysis of power losses and switching stress. As a result of the evaluation, a base topology was selected. A topological modification and switching sequence were proposed to achieve maximum performance and high efficiency, taking into consideration the voltage regulation nature of polymer-electrolyte FCs.

The major contributions of the work include: modified modulation sequence to minimize power losses in low-voltage high-current full-bridge forward converters; modified topology for transformer ringing reduction and minimization of reverse recovery losses in the output rectifier stage. Technical papers describing these major contributions are currently under preparation for publication.

B) Control strategy for low frequency ripple current elimination (Chapter 3): The proposed power conversion scheme was controlled to eliminate ripple current reflection on the FC. Novel concepts of constant current extraction in the input and swinging bus output voltage of the dc-dc converter were investigated at the system level. The swinging bus voltage is a result of the combined action of the constant current injection from the dc-dc stage and the low frequency ripple current from the inverter.

The major contributions in this chapter include: swinging bus analysis in time and frequency domains; dynamic operation using the system behavioral model; feedback loop processing using discrete-time signal processing. The work in this chapter is in preparation for publication.

C) Inverter control strategy for swinging dc bus operation (Chapter 4): As a result of employing a ripple current elimination technique, the inverter input voltage (dc-dc converter output) swings, creating an unprecedented challenge for the control scheme of the inverter. This chapter investigated boundary control using

curved switching surfaces (non-linear control) as an alternative method to ensure high power quality under steady and dynamic operation. The following contributions were made: a novel control law using a curved switching surface; new mixed mode modulation scheme for single phase inverters; demonstration of duality between curved switching surfaces and PWM carriers; normalized analysis and simplified geometrical representation of buck derived inverters. The following publications cover the non-linear control scheme for inverters using boundary control, as well as related work on normalization technique, curved switching surfaces and modulation schemes.

- M. Ordonez, J.E. Quaicoe, and M.T. Iqbal, "Advanced Boundary Control of Inverters Using the Natural Switching Surface: Normalized Geometrical Derivation," accepted for publication, *IEEE Transactions on Power Electronics*, 2008.

- M. Ordonez, J.E. Quaicoe, and M.T. Iqbal "Advanced Boundary Control of Inverters Using the Natural Switching Surface: Normalized Geometrical Derivation," *in Proc. IEEE Power Electronics Specialist Conference, PESC'08, Island of Rhodes (Greece), June 2008.*

- M. Ordonez, M.T. Iqbal, and J.E. Quaicoe "Selection of a Curved Switching Surface for Buck Converters," *IEEE Transactions on Power Electronics, vol. 21, Issue 4, pp. 1148-1153, July 2006.*

- M. Ordonez, J.E. Quaicoe, and M.T. Iqbal "Critical Parameters in the Transient Response of Synchronous Buck Converters," in Proc. IEEE Power Electronics Specialist Conference, PESC'07, Orlando (USA), June 2007.

D) Monitoring and Diagnosis of FC systems (Chapter 5): In addition to the power conditioning stage, an additional feature was identified to obtain reliable operation of the FC power generation system namely, a method to monitor and

diagnose the FC system. An embedded frequency response analyzer for on-line monitoring of FCs was proposed to provide a useful diagnostic instrument for possible failures or performance evaluation during the operation of the FC. The contributions in this chapter include: a method to measure the FC impedance in the presence of high noise levels; embedded real-time implementation using a low-cost DSP which is also employed to control the power conversion stages. The following publications resulting from the contributions cover frequency response analysis of FC systems, lock-in amplification and digital signal processing.

- M. Ordonez, M.O. Sonnaillon, M.T. Iqbal, J.E. Quaicoe, and F.J. Bonetto "An embedded DSP-based Frequency Response Analyzer for Fuel Cells Monitoring and Characterization," in Proc. IEEE Power Electronics Specialist Conference, PESC'06, Jeju (Korea), pp. 2198-2203, June 2006.

- M.O. Sonnaillon, R.Urteaga, F.J. Bonetto, and M. Ordonez "Implementation of a High Frequency Digital Lock-In Amplifier," in Proc. IEEE Canadian Conf. on Electrical and Computer Engineering, Saskatoon (Canada) 2005, pp. 1198-1201.

In addition to the major contributions described above, related and complementary investigation of the analysis, modeling, characterization of the FC in steady state and dynamic operation in Chapter 1 resulted in the following publications:

- M. Ordonez, P. Pickup, J.E. Quaicoe, and M.T. Iqbal, "Electrical Dynamic Response of a Direct Methanol Fuel Cell," *IEEE Power Electronics Soc. Newsletter, vol. 19, number 1, 2007.*

- M. Ordonez, M.T. Iqbal, J.E. Quaicoe, and L.M. Lye "Modeling and Optimization of Direct Methanol Fuel Cells Using Statistical Design of Experiment

Methodology," in Proc. IEEE Canadian Conf. on Electrical and Computer Engineering, Ottawa (Canada) 2006, pp. 1327-1330.

- M. Ordonez, M.T. Iqbal, J.E. Quaicoe, and L.M. Lye "Modeling of Fuel Cell Systems Using Design of Experiment Methodology," Newfoundland Electrical and Computer Engineering Conference, NECEC 05', St. John's (Canada), 2005.

Appendix A

Power Converter Design Considerations

The power coverter presented in section 2.5 allows an input voltage range of 20-60 V and a nominal RMS input current of 125A. Even though the power MOSFETs can handle 7.5kW (at 60 and 125A), the maximum output power is limited by the power rating of the transformer and the rectifier to 2.5kW. The nominal output voltage is 210 V, which is used to supply the inverter power stage. The minimum switching frequency is $40kHz$ to keep the transformers out of the saturation region. However, the switching frequency can be increased up to $80kHz$ without significant skin effect losses. The maximum switching frequency is limited by the current capability of the drivers. As well, the efficiency of the converter is reduced due to switching losses as the switching frequency increases. The maximum instantaneous peak current is 500A which has been accidentally tested by saturating the transformer core. The transformers temperature rise is estimated to be $45°C$ at maximum power.

A.1 Description of the Power Stage and Drivers

The circuit schematic for the power stage is depicted in Fig. A.1. Given the high current and low voltage levels expected on the input side of the converter, the power MOSFETs have been selected following the criteria of minimizing the voltage drop across the switches and conduction losses. Each switch comprises five IRFB4110 HEXFET power MOSFETs in parallel for a combined on resistance $R_{dsON} = 0.9m\Omega$ at $25°C$. This low level on-resistance ensures very low drop across the MOSFETs and low conduction losses (i.e., at 100A the power losses are 1.8W per MOSFET). Each leg is protected by 5 snubber capacitors across the dc bus. The bulk capacitor bank includes $8\times680\mu F$ to absorb part of the high frequency ripple current and extend the lifetime of the capacitors, which is a function of the ripple current and operating temperature. The full-bridge output rectifier has 1200V fast recovery diodes to cope with the transformer output voltage (800V) when the input voltage is close to 60V. In order to prevent the output voltage from exceeding 1200V due to transformer ringing (hard switching operation), an RCD voltage clamp is included at the output of the rectifier.

The circuit schematic for the isolated driver is presented in Fig. A.2. Each driver is supplied by a small power transformer E25/10/9 with multiple outputs. The transformer pulses are supplied by the system auxiliary power supply (not described here) with 47% duty cycle and fixed amplitude. A voltage doubler rectifier is employed to generate a dual supply with floating ground for each driver. The driver has an input connector that is compatible with the 240x family of Texas Instruments DSPs. The triggering signals generated by the DSP are enhanced by a pre-driver circuit to allow reliable operation of any commercial optocoupler under high dv/dt signals on the power side. This consideration is particularly important for the upper side

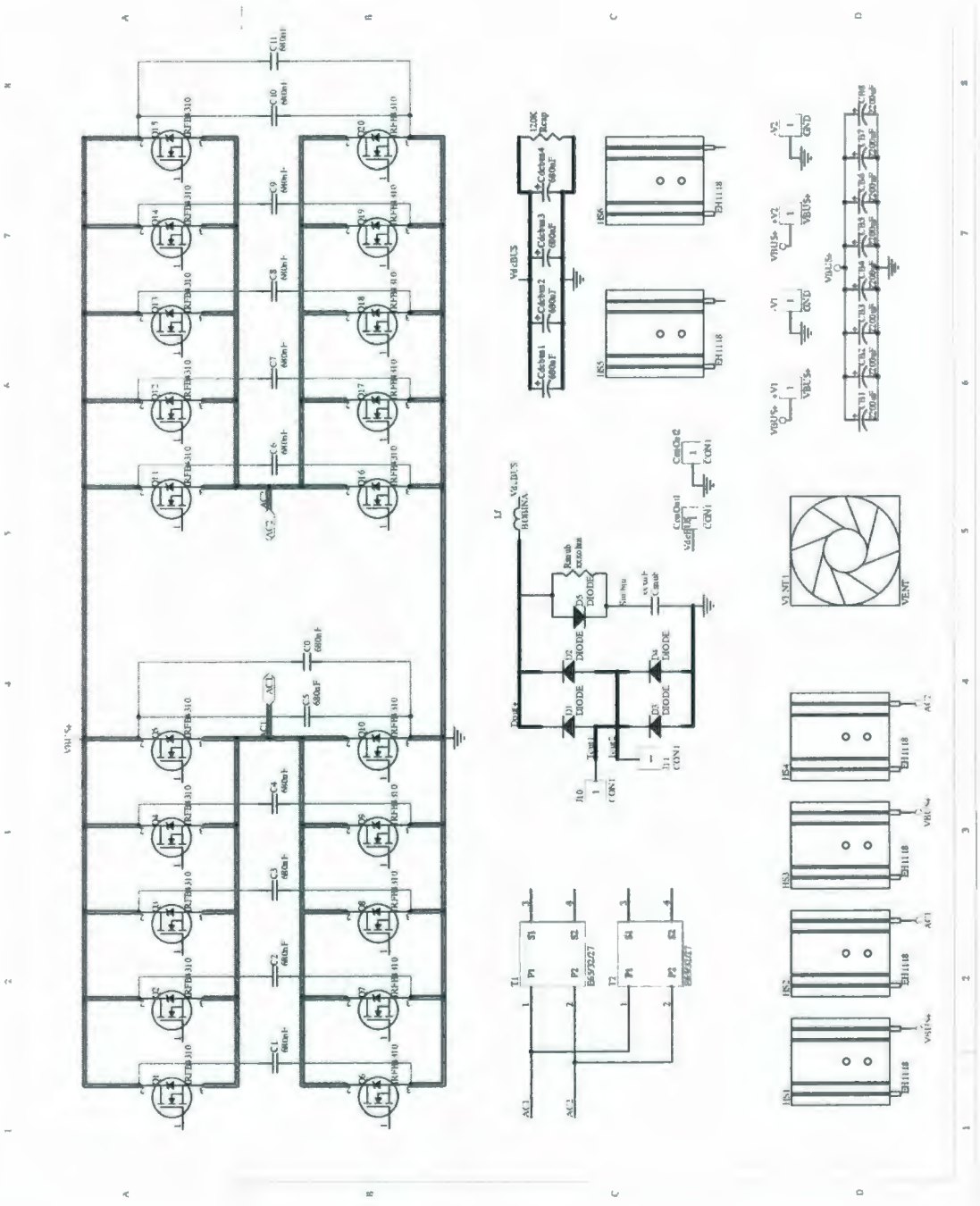


Figure A.1: Circuit schematic of the power converter prototype.

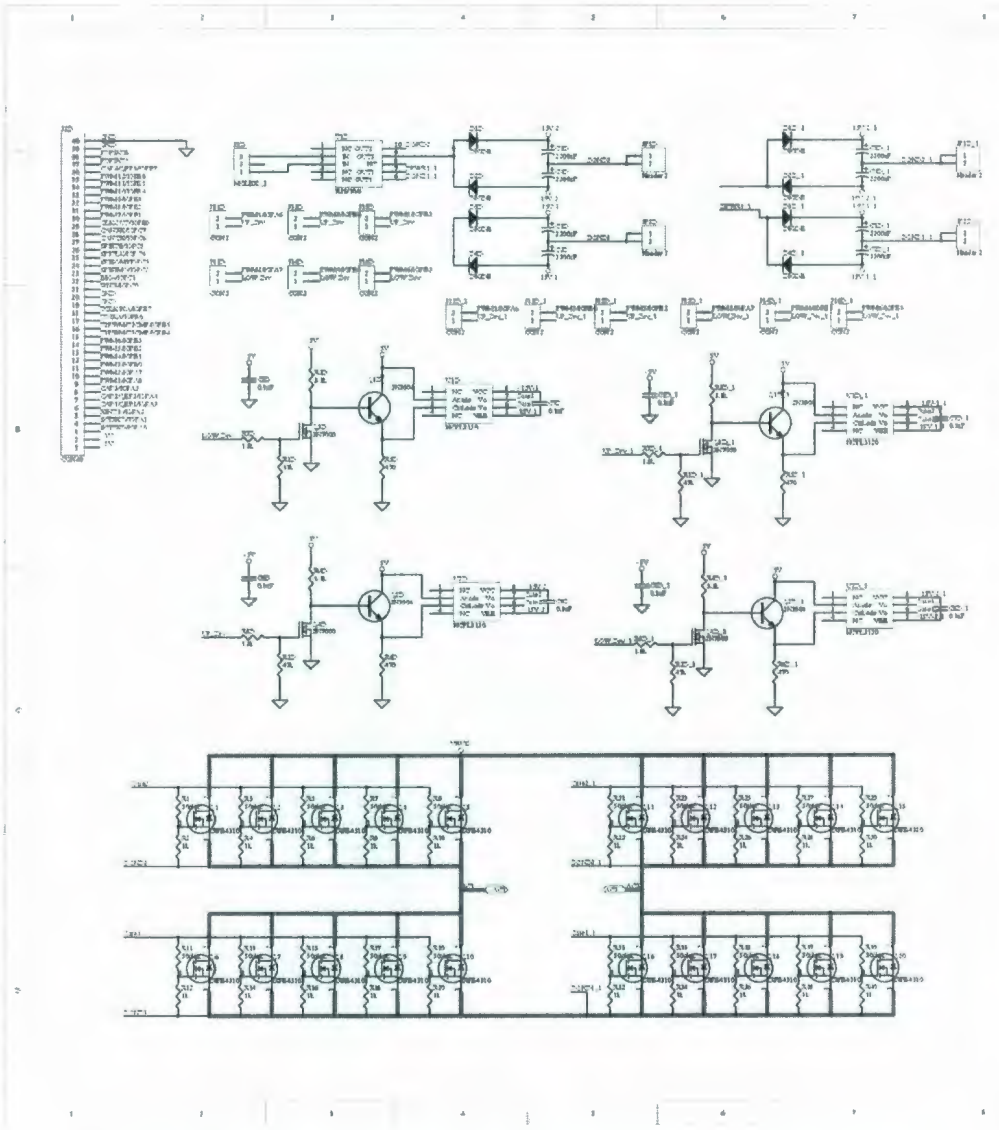


Figure A.2: Circuit schematic of the isolated drivers prototype.

drivers. The lower side drivers are also isolated to reject the noise produced by high currents in the power ground. Given the robustness of the power and signal circuits illustrated in the circuit schematic, any discrete or integrated totem pole circuit arrangement can be incorporated to meet the peak current requirements to charge the gate equivalent capacitance of the power MOSFETs. Low inductance metal-film resistors are employed for the gate and gate-to-source resistors. The gate-to-source resistor prevents false triggering when the power stage supply is connected and the drivers are not enabled. The MOSFETS in the circuit schematic are only for the purpose of illustrating the connection between the drivers and the power switches.

A.2 Layout of the Power Stage and Driver

The elements contained in the circuit schematic of Fig. A.2 were strategically organized in a 6 oz copper clad. The thickness of the printed circuit board (PCB) was selected to maintain the current density within acceptable levels (recall that the input current may reach $125A$). This concept replaces multilayer PCB designs and ensures low stray inductance in the track of the PCB. Two main criteria were followed to produce this industrial grade power converter: components distance minimization and symmetrical layout. Figure A.3 shows the bottom layer of the power board where the low-voltage high-current section (left view) and the high-voltage low-current section (right view) can be identified. As can be seen, the high-voltage side has significantly larger clearances to increase the electrical breakdown voltage between tracks and pads. The bottom layer in both low- and high-voltage sides is a solid ground plane that helps to create a minimum inductance path for the current. The PCB top layer shown in Fig. A.4 is also divided into low- and high-voltage sides. The low-voltage area (left view) has three polygon planes for v_{cc} and the transformer input termi-

Figure A.3: Power converter PCB bottom layer.

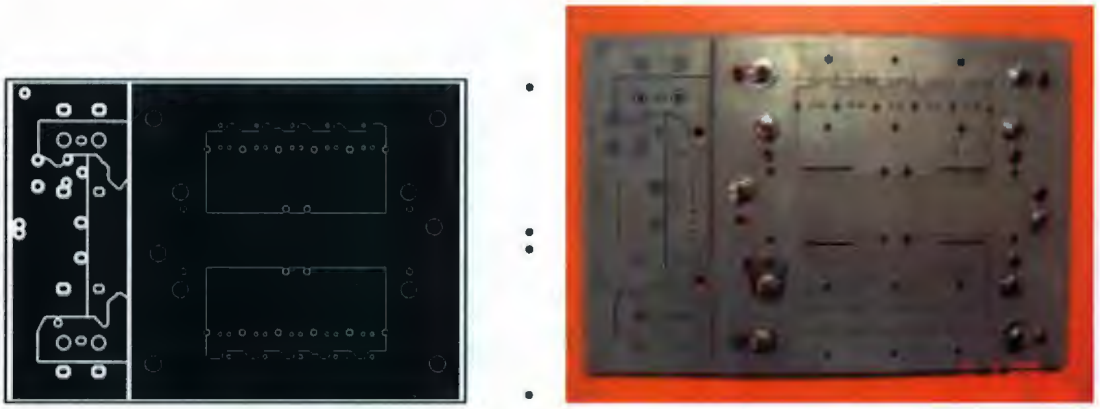


Figure A.4: Power converter PCB top layer.

nals (inner planes). The pads for the upper power MOSFETs are distributed in the boundary of v_{cc} and the transformer terminals (upper and lower side of the board) while the low side MOSFETs are placed through the planes for the transformer input terminals. As well, space in the center of the board is reserved to snap-in two high frequency transformers while minimizing the stray inductance of the connection. The high voltage side (right view) features an arrangement which is similar to the low voltage side, except that the center of the board includes the filter inductor.

The driver was constructed in a double sided 1 oz copper clad. The PCB layout is depicted in Fig. A.5, showing the top and bottom layers. The PCB design has a

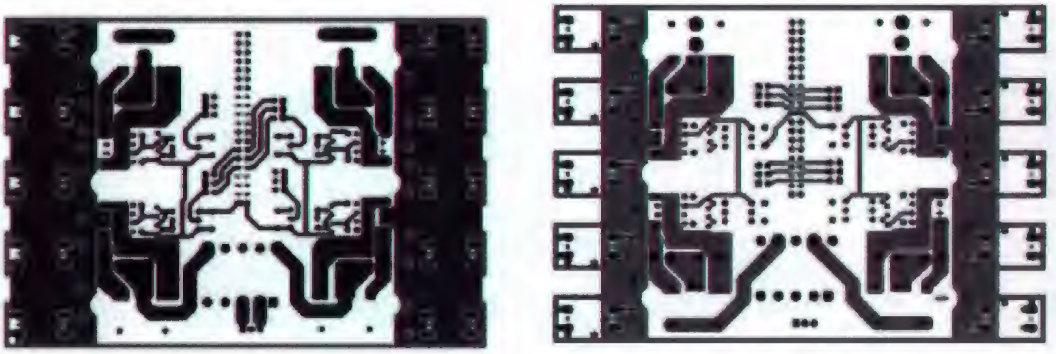


Figure A.5: Driver PCB design.

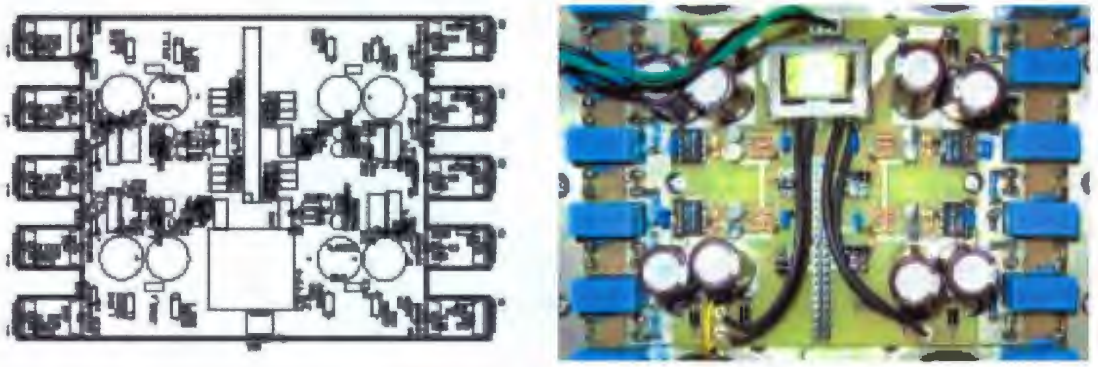


Figure A.6: Driver prototype.

number of polygon planes that connects each voltage doubler with the corresponding optocoupler gate driver while minimizing stray inductances. As well, the floating ground of each driver is connected to the MOSFET sources using a ground plane to also minimize parasitics and provide an even gate charge during turn-on and turn-off transitions. The gate driver chips are placed as close as possible to the MOSFETs to improve the effectiveness and reliability of this critical stage. The final arrangement is shown in Fig. A.6 where the proximity of the snubbers and the drivers to the power switches can be appreciated. The pins of the power MOSFETs can be identified in between the snubber capacitors.

Appendix B

Comparative Analysis of Digital Filters for DSP Implementation

Five basic approaches to filter design were investigated, namely, Infinite Impulse Response (IIR) Butterworth, Chebyshev, and Elliptic; Finite Impulse Response (FIR) windowed, and Moving Averaging Filter (MAF). A comparative analysis was carried out using a case example to evaluate their practical achievable specifications, computational requirements, and time domain response for each case. A discrete cutoff frequency $w_c = 0.1049$ was selected to achieve $f_c = 60Hz$ mapping in continuous time with a sampling frequency $F_s = 3.6$kHz. Instead of defining the ripple in the stopband and passband, the highest possible order Chebyshev, Butterworth, and Elliptical IIR filters were initially calculated. The maximum achievable order in this case was only four, which is limited by round off noise of single precision when small coefficients are obtained for such a narrow filter. Figures B.1 and B.2 show the resulting frequency response in linear and logarithm scale respectively. As can be noted, the Chebyshev filter has slightly sharper roll-off than Butterworth and Elliptical counterparts at the expense of ripple in the passband, producing significant error at dc. In this applica-

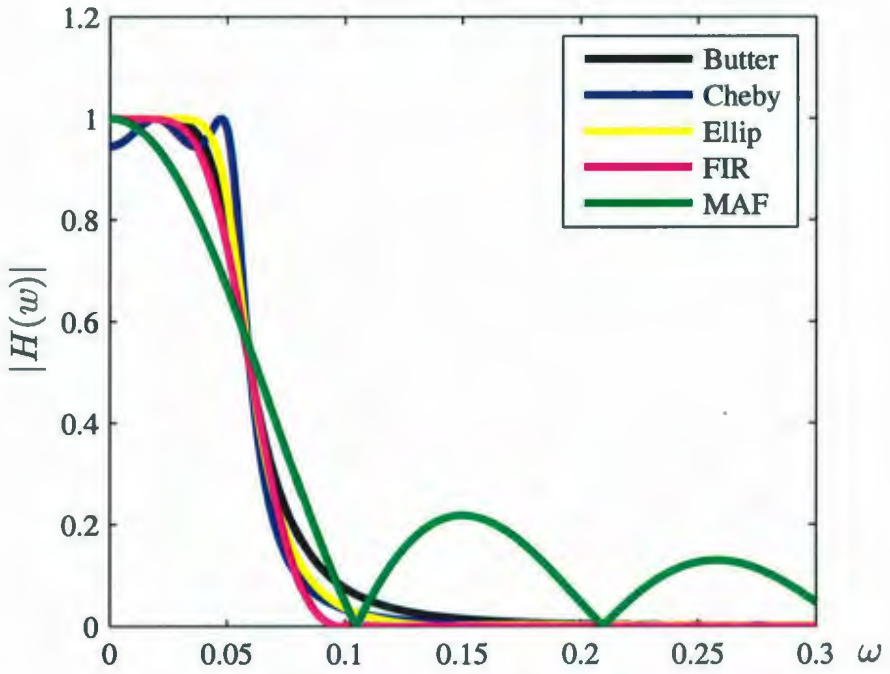


Figure B.1: Comparative frequency responses in linear scale of discrete time filters with $w_c = 0.1047$: Butterworth (4^{th}), Chebyshev (4^{th}), Elliptic (4^{th}), windowed FIR (120-point), and MAF (60-point).

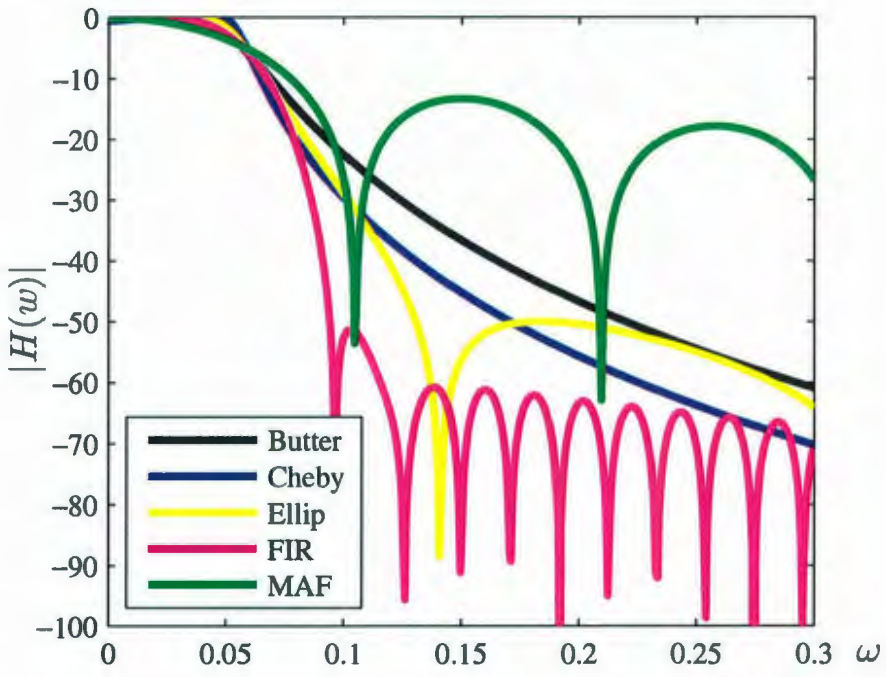


Figure B.2: Comparative frequency responses in dB of discrete time filters with $w_c = 0.1049$: Butterworth (4^{th}), Chebyshev (4^{th}), Elliptic (4^{th}), windowed FIR (120-point), and MAF (60-point).

tion, the accuracy of dc is important to obtain an accurate measurement of the bus dc component. As well, the Elliptical filter also contains ripple in smaller degree that cannot be seen in the plot. On the other hand, Butterworth features a flat response with comparable roll-off. It is the preferred IIR choice for this application. Nevertheless, roll-off is not a key requirement so the other options need to be carefully examined and compared to IIR.

A Hamming-window based FIR filter with similar roll-off and $M = 120$ was calculated, which is also illustrated in Fig. B.1 and Fig. B.2. The stopband attenuation is comparable to IIR; however, the kernel length is noticeably long and requires significant computing time. Even though FIR is the only option that provides flexibility to achieve enhanced performance with a single filter (i.e., through Kaiser method),

the required processing power to perform real-time filtering makes it impracticable. Finally, a 60-point MAF, was evaluated displaying overall limited performance in the frequency domain with softer roll-off transition and large stopband lobes. However, MAF provides the following three key desirable features that make it the most suitable filter for the studied application: 1) The practical implementation is straightforward and very efficient. Only additions and shifts operations are required; 2) The filter is error-free at dc, reproducing accurately the bus voltage dc component; 3) The attenuation band contains pull-down notching effect (discrete zeros) at 60Hz and multiples. This could effectively eliminate the spectral components described in section 1.3.2. of the bus voltage under linear, pulsating, and non-linear load. Since no other components rather than 120Hz and harmonics are expected, the selective notching of MAF successfully complies with the objective of the filter.

Since the characteristic of the feedback loop filter forms part of the gain loop, the filter phase behavior is a critical consideration to maintain proper phase margin in the overall compensation scheme. In order to confirm the suitability of MAF, a comparative graphical representation of the phase behaviors is presented in Fig. B.3. The plot in linear scale illustrates the intricate non-linear progression of IIR filter, and linear phase evolution in FIR and MAF. Of most critical importance is how fast the phases arrive to $-\pi$ (or $-180o$). Clearly and unlike IIR and FIR, MAF provides the largest frequency intersection with $-\pi$. This important consideration provides advantageous phase margin in the loop gain compensation scheme.

Finally, the time domain behavior of the filters is examined to find out the settling time required to produce a final result. For this purpose, the step responses for the five analyzed cases are shown in Fig. B.4. Clearly, the settling time of the MAF (straight line) is well below the other filters, with the FIR being the worse case. It can be concluded that the MAF is an excellent option to perform a fast real-time

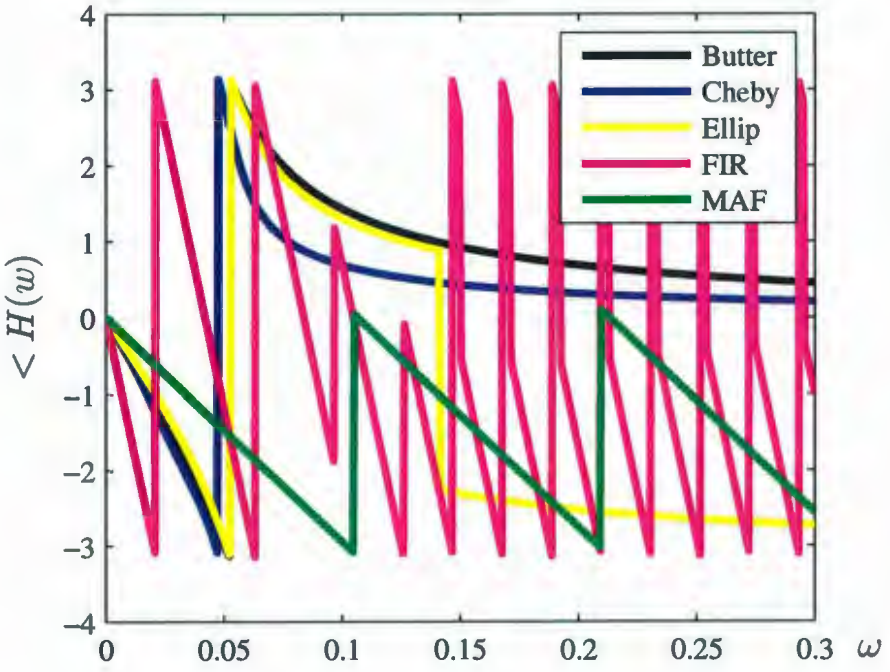


Figure B.3: Comparative phase responses of discrete time filters with $w_c = 0.1049$: Butterworth (4^{th}), Chebyshev (4^{th}), Elliptic (4^{th}), windowed FIR (120-point), and MAF (60-point).

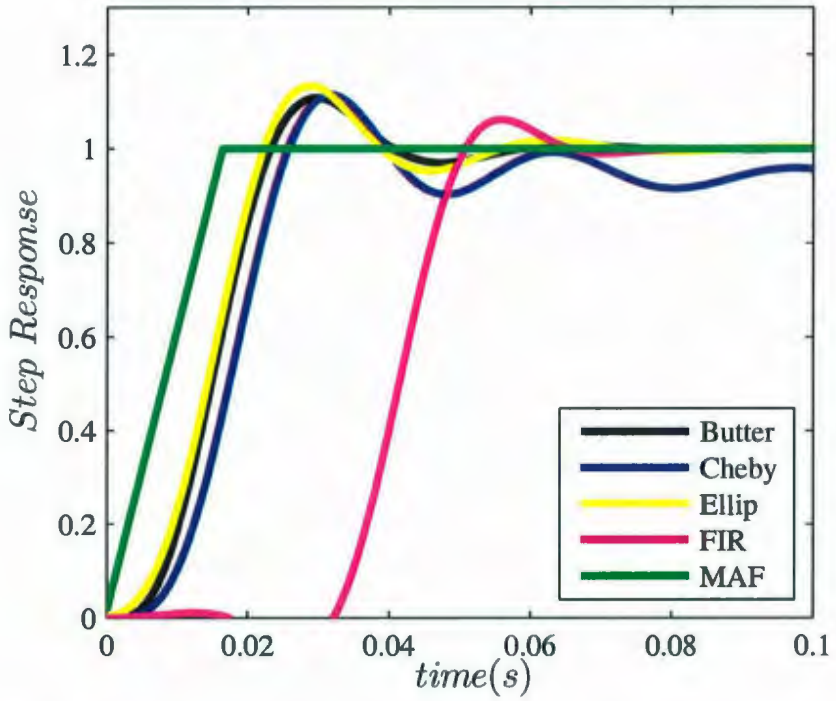


Figure B.4: Comparative step responses of discrete time filters with $w_c = 0.1049$: Butterworth (4^{th}), Chebyshev (4^{th}), Elliptic (4^{th}), windowed FIR (120-point), and MAF (60-point).

filtering of the undesired components, and to provide additional phase margin without compromising the accuracy of the dc component measurement.

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