SIMULATION OF CURRENT MODE CONTROL SCHEMES FOR POWER FACTOR CORRECTION CIRCUITS

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by

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Abstract

This thesis deals with a comparative study of the features of constant frequency and variable frequency current control schemes for power factor correction in AC-DC converter circuits.

Various current control schemes for achieving nearly unity power factor at the input and to minimize the total harmonic distortion (THD) are in use in various applications such as television, radio receivers, AC-motor drives, DC-motor drives and uninterruptible power supplies (UPS).

Analytical models of Constant Frequency Continuous Current (CFCC), Constant Frequency Discontinuous Current (CFDC), Zero-Current Zero-Voltage Switching (ZCS-ZVS) and Variable Current Hysteresis Control (VCHC) are developed and used to evaluate the performance of the power factor correction circuit. The main features of these control schemes are highlighted and the performance characteristics are obtained through computer simulation for the same circuit conditions. Design examples of each control scheme, and power loss calculation associated with the active switching device are also provided. It is shown that active current waveshaping through constant and variable frequency control schemes posseses many attractive features.

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Chapter 1

INTRODUCTION

Power electronics is gaining widespread popularity and is playing a key role in several residential, commercial and industrial applications. Almost invariably in such systems like television, radio receivers, light dimmers, AC-motor drives, DC-servo drives, uninterruptible power supplies (UPS), magnet power supplies and high power induction heating equipment, the 60 Hz input voltage is first rectified into a DC voltage. The DC voltage is subsequently converted into the voltages and currents of appropriate magnitude, frequency and phase to meet the load requirements. In all cases, the source voltage is obtained from the utility supply.

Electric utility supply quality issues, including harmonics and quasi static waveform excursions are now top priority issues for equipment manufacturers, users and electric utility personnel. Harmonics, super and sub-harmonics, and interharmonics, can cause system equipment malfunctioning, increased losses in the utility lines, increased distortion of the supply voltage, interference with other electrical equipment, personnel safety problems, over-burdened neutral wires, ground potential rise, light flickering,

computer data loss and memory malfunctioning, erratic process control and other associated problems. The most serious problem associated with harmonics is the loss of efficient energy utilization due to lower distortion power factor.

The DC output voltage of an AC-DC converter should be as ripple-free as possible. For this reason, a large capacitor is connected as a filter on the DC side. Since this capacitor is charged to a value close to the peak AC magnitude the rectifier then draws a highly distorted current from the utility which leads to current harmonic generation.

One approach to minimize this impact is to filter the harmonic currents and the electromagnetic interference (EMI) produced by the power electronic loads. A better alternative, in spite of a small increase in the initial cost, may be to design the power electronic equipment such that the harmonic current generation and the EMI are prevented or minimized in the first place. With the potential for proliferation of power electronics equipment and enforcement of harmonic standards such as IEEE 519, IEC 555, there is an increasing need for active current waveshaping through appropriate control schemes.

1.1 HARMONIC STANDARDS AND RECOMMENDED PRACTICES

In view of the proliferation of power electronic equipment connected to the utility system, many national and international agencies have been considering limits on harmonic current injection to maintain good power quality. Various standards and guidelines have been established that specify limits on the magnitudes of harmonic currents and total harmonic distortion (THD). Some of these are:

1) EN 50 006, " The Limitation of Disturbances in Electric Supply Networks caused by Domestic and Similar Appliances Equipped with Electronic Devices", European Standard prepared by Comité Européen de Normalisation Electrotechnique, CENELEC.
2) IEC Norm 555-3, prepared by the International Electrical Commission.
3) West German Standards VDE 0838 for household appliances, VDE 0160 for converters and VDE 0712 for fluorescent lamp ballasts.
4) IEEE Guide for Harmonic Control and Reactive Compensation of Static Power Converters, ANSI/IEEE Std. 519-1981.

Some of the standards of harmonic current and voltage are shown in Table 1.1 to Table 1.3 [2,3]. Table 1.1 shows typical harmonics in a single phase input current waveform with no line filtering . The harmonic currents (I_h) are expressed as the ratio of the fundamental current (I_1). From Table 1.1 it can be seen that without the use of input

filter, the input current waveform consists of large harmonic magnitudes.

Table 1.1: Typical Harmonics in a single-phase input current with no line filtering

h	3	5	7	9	11	13	15	17
$\left(\frac{I_h}{I_1}\right)\%$	73.2	36.6	8.1	5.7	4.1	2.9	0.8	0.4

Table 1.2 shows the permitted harmonic currents for any consumer at the point of common coupling (PCC). A tolerance of + 10% or 0.5A (whichever is the greater) is permissible, provided it applies to no more than two harmonics. Table 1.3 shows the harmonic voltage distortion at any point on the utility system.

Table1. 2: Permitted harmonic currents for any consumer at PCC

Utility input voltage at PCC (kV)	Harmonic number and current per phase at PCC (A rms.)													
	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0.415	48	34	22	56	11	40	9	8	7	19	6	16	5	5
6.6 and 11	13	8	6	10	4	8	3	3	3	7	2	6	2	2
33	11	7	5	9	4	6	3	2	2	6	2	5	2	1
132	5	4	3	4	2	3	1	1	1	3	1	3	1	1

Table 1.3 : Harmonic voltage distortion limits at any point on the utility system

Utility input voltage at PCC	Total Harmonic voltage Distortion (%)	Individual harmonic voltage Distortion (%)	
		Odd	Even
0.415	5	4	2
6.6 and 11	4	3	1.75
33 and 66	3	2	1
132	1.5	1	0.5

In order to meet the various harmonic standards several techniques have been proposed to minimize the harmonics in the AC-DC converter. In general, there are three approaches that can be used to shape the line current. The first approach uses energy storage and magnetic components to minimize the harmonics. This approach is referred to as the passive technique. The second approach, known as current injection technique, attempts to reduce or minimize the current harmonics by injecting a third harmonic current into the input. The third approach, referred to as the active technique, employs switching techniques to shape the current waveform. The subsequent section explains the details and principles of the different techniques.

1.2 HARMONIC MINIMIZATION USING PASSIVE TECHNIQUES

This technique uses mainly passive devices, capacitors and inductors to minimize the current harmonics. A single phase implementation of the Power Factor Correction (PFC) circuit employs a low pass filter method.

Using a low pass filter at the input side for harmonic minimization is one of the basic passive control methods. As the harmonic component of the input current has frequencies which are multiples of the base frequency, most of the high frequency harmonics can be eliminated or reduced using a low pass filter. The cut off frequency of the low pass filter can be designed so that any frequency above the designed cut off frequency will be attenuated. The result is a reduction in the harmonics fed back into the utility supply. The exact design of the cut off frequency of a low pass filter is the major disadvantage of this scheme. To attenuate the designed higher frequencies, the cut off frequency should remain constant throughout the operation of AC-DC converter. Moreover, the ideal low pass frequency response, i.e. sharp passband and stop band, is hard to implement in any practical circuit. Figure 1.1 shows a single-phase AC-DC rectifier with an input low pass filter network.

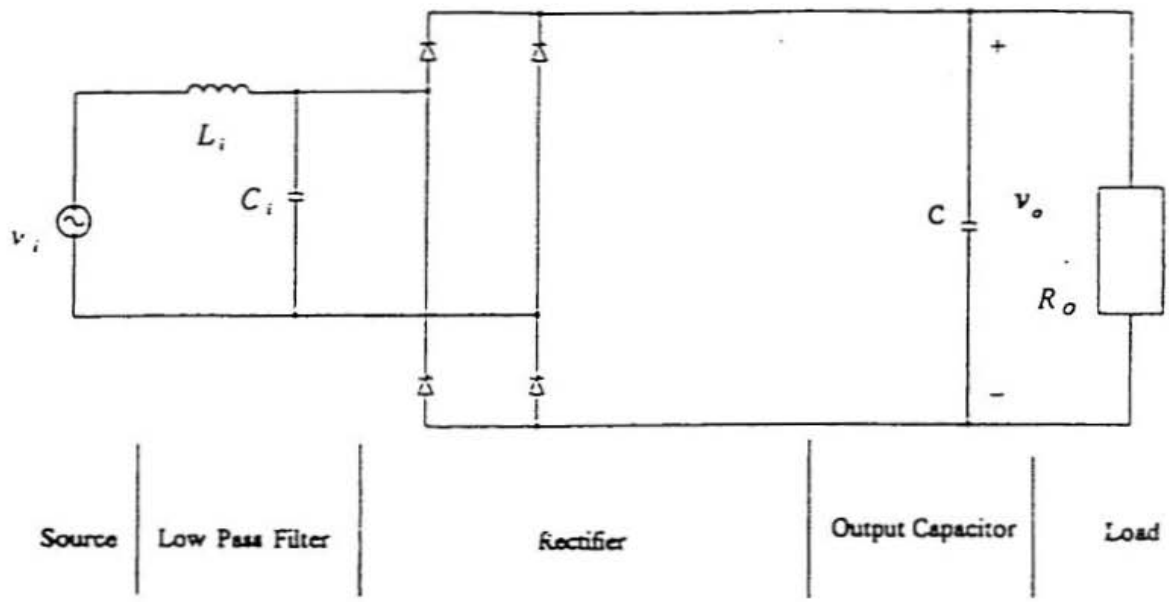


Figure 1.1: Single-phase AC-DC converter circuit with an input low-pass filter

1.3 CURRENT INJECTION METHOD

Figure 1.2 shows one type of the current injection method in a three-phase AC-DC converter system. This approach involves an interconnection of a three-phase limb core star/delta transformer between the AC and DC sides of the diode rectifier topology. The capacitors on the DC side provide the mid-point for the DC output voltage. The secondary of the transformer is connected in delta and is unloaded. It has been shown that due to the 120 degree conduction intervals of each diode, the voltage drop between the transformer neutral and the output capacitor midpoint is essentially a third harmonic component [4, 5]. The resultant third harmonic current circulates between the AC and DC side of the rectifier bridge. Recently, variations of the basic current injection method have

been proposed [6]. It has been shown that the third harmonic current drastically reduces the input current harmonics and improves the input power factor.

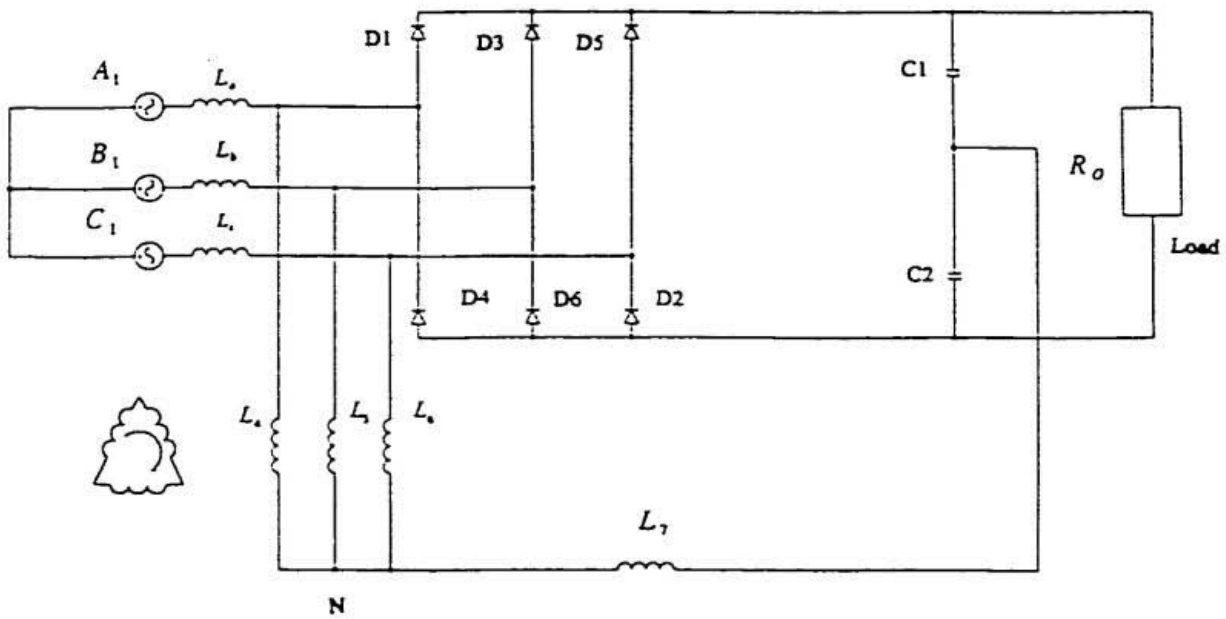


Figure 1.2 : Current injection method in three-phase AC-DC converter

The main advantages of this method are as follows.

- The scheme is passive and does not interfere with the AC-DC rectification process of the diode rectifier topology.
- The transformer draws negligible fundamental current from the input source (equal to the excitation current) since the delta connected secondary is unloaded.
- The circulating third harmonic current is automatically generated by the midpoint arrangement of the output capacitors.
- The delta connected secondary permits a path for zero sequence third harmonic currents to circulate, thereby automatically balancing the flux in the transformer core.

The passive harmonic elimination/minimization approach require bulky, expensive filters or magnetic components at the input side of the AC-DC converters. For most residential, commercial applications and some industrial applications, the current injection method is too expensive. Hence, different control schemes are being developed for both three-phase and single-phase rectifier systems, which eliminate the usage of any expensive devices but still maintain the nearly unity input power factor with minimum allowable input current harmonics.

1.4 HARMONIC MINIMIZATION USING ACTIVE TECHNIQUES

Harmonic minimization using active techniques can be classified into two categories, namely, Pulse Width Modulation switching of the converter devices and Pulse Width Modulation switching of auxiliary devices.

1.4.1 PULSE WIDTH MODULATION SWITCHING OF THE CONVERTER DEVICES

Pulse Width Modulation (PWM) technique is widely used in AC-DC converters to minimize the input current harmonics. In this scheme, the ON/OFF time of the rectifier switches, are controlled by the width of the PWM pulses. The PWM pulses are generated by comparing a carrier waveform with a modulating waveform. Many different methods of obtaining the modulating signal have been proposed in the literature [7-17].

The advantage of PWM schemes is that the size of the overall system is small. However, the major limitation of PWM schemes is that it requires a complex synchronization logic circuit. This is because the switches in the rectifier network are required to switch ON/OFF in synchronism with the supply voltage. The dominant PWM fixed switching frequency techniques are the Adaptive Phase Control (APC) technique and the Predicted Current Control with Fixed Frequency (PCFF) technique.

1.4.1.1 ADAPTIVE PHASE CONTROL

The adaptive phase control (APC) scheme is one of the traditional fixed switching frequency PWM methods used to improve the input power factor and minimize the total harmonic distortion for three-phase AC-DC converters. A block diagram of the control scheme is shown in fig 1.3. In this scheme, the phase of the line current with respect to the phase voltage is continuously detected and used as a control input to generate the necessary PWM switching patterns. Because of its adaptability, the control logic is independent of any circuit parameter. In general the PWM controller generates the switching pattern of the six switches in the three-phase rectifier by comparing the three-phase modulating voltages and a carrier triangular wave. The frequency of the triangular wave determines the switching frequency of the rectifier switches. The scheme uses separate regulation loops for phase regulation and amplitude regulation of the line current. By using proper modulation technique for the switching pattern of the switches, PWM AC-DC converters have been demonstrated to have attractive features in terms of reduced line harmonics distortion, nearly unity power factor, small filter components on both the ac and dc side of the converter [18,19].

The drawback of the APC scheme is its complex synchronization logic. Zero-crossing detectors which are used in this scheme to detect the zero crossings of the phase voltage and the fundamental component of the line current become difficult to measure for high frequency applications.

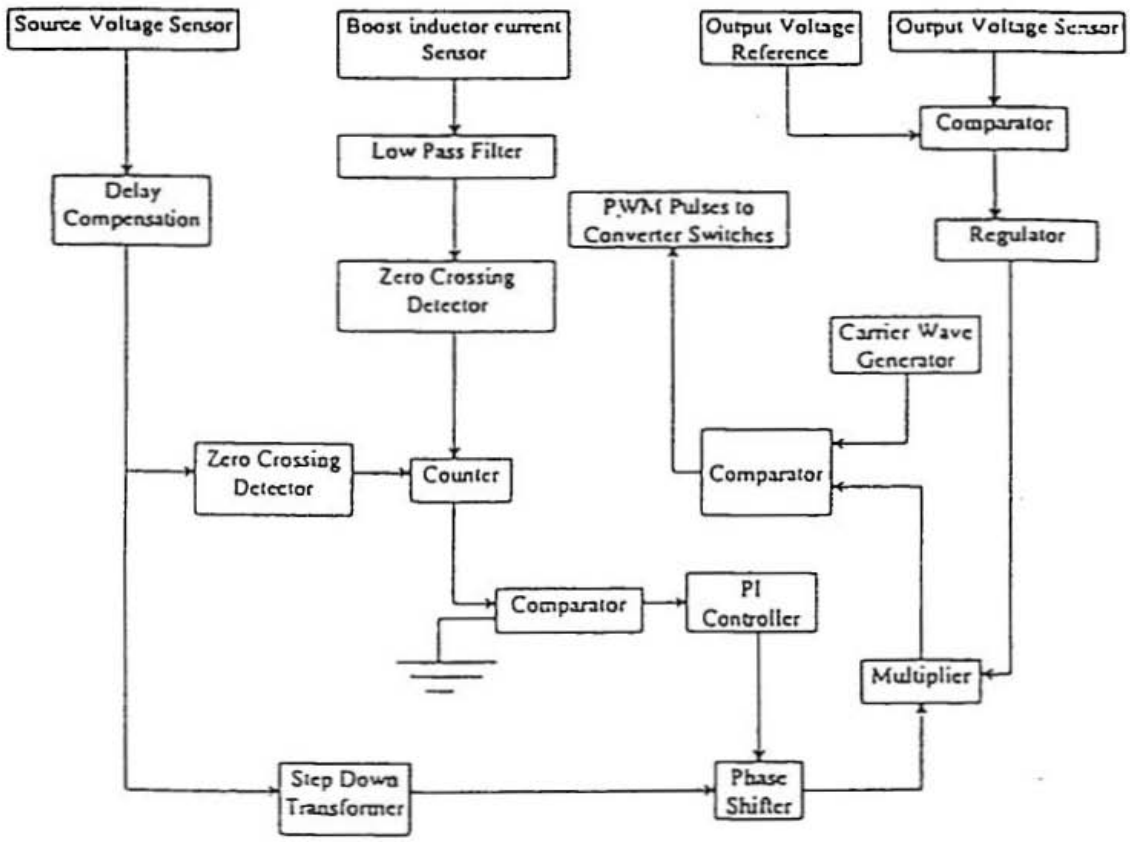


Figure 1.3 : Block diagram of Adaptive Phase Control method [18]

1.4.1.2 PREDICTED CURRENT CONTROL

The predicted current control with fixed switching frequency (PCFF) is another PWM method used to improve the input power factor and minimize the total harmonic distortion for three-phase AC-DC converters. Figure 1.4 shows the block diagram of a PCFF control scheme. In this technique, the modulating voltage required to control the line current is calculated based on the parameters of the power circuit and the switching frequency. This voltage is then compared to a carrier wave to generate quasi-optimal switching pattern to regulate the line current [20]. This scheme is favourable for high power applications because of its well-defined switching pattern which results in predictable stress on the switching devices.

However, the major shortcoming of the PCFF control scheme is that its control principle is parameter dependent. Exact knowledge of the power circuit parameters is required to implement the control logic. In practice, however, these parameters vary due to variation in temperature, nonlinearity and saturation of the magnetic core. Parasitic components, such as equivalent series resistance associated with output capacitor, contribute to the circuit considerably when the switching frequency is high. These variations are unpredictable and hence difficult to compensate.

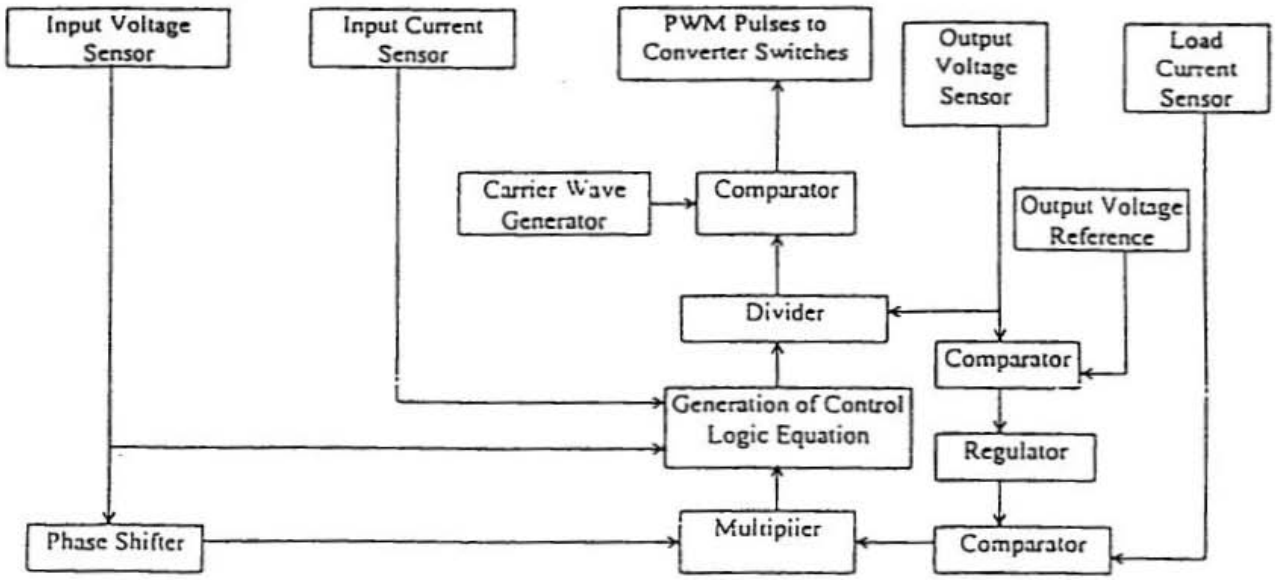


Figure 1.4: Block diagram of PCFF control scheme [19]

1.4.2 PULSE WIDTH MODULATION SWITCHING OF AUXILIARY DEVICES

In this scheme, the PWM pulses are applied to auxiliary devices usually connected at the output side of the rectifier circuit. The auxiliary switches are pulse-width modulated according to a control algorithm so as to achieve harmonic reduction in the input current waveform. The advantage of this scheme is that no complex synchronization logic circuit is required.

1.4.2.1 ACTIVE POWER FACTOR CORRECTION CIRCUIT

With the maturing of static power converter technology and the remarkable progress in the development of power semiconductor devices, several converter topologies for active power factor correction circuits have been successfully implemented [21,23,24].

The choice of the power electronic converter is based on the following considerations

- In general, the electrical isolation between the utility input and the output of the power electronic system is either not needed (like in AC and DC-motor drives), or it can be provided in the second converter stage as in switch-mode DC power supplies.
- In most applications it is acceptable and in many cases it is desirable to regulate the DC output voltage.
- The input current drawn should ideally be at a unity power factor so that the power electronic interface emulates a resistor supplied by the utility source. This also implies that the power flow should be always unidirectional, from the utility source to the power electronic equipment.
- The cost, power losses and size of the current shaping circuit should be as small as possible.

Among the converter topologies published [21,23,24], the most popular schemes employ the boost converter concept to shape the input current so as to improve the input power factor to near unity. This is because in the boost converter topology, the auxiliary

switch is now controlled alone and controlled switches are not required in the rectifier circuit.

The prevalent single-phase active power factor correction (PFC) circuit is shown in fig 1.5. It consists of a boost inductor, standard diode bridge rectifier followed by a switch and an output capacitor. Figures 1.6(a) and 1.6(b) show the topological changes of the boost converter during ON and OFF conditions of the switch respectively. The ON and OFF times of the boost switch (S) are controlled by the PWM signal generated from the various current control schemes.

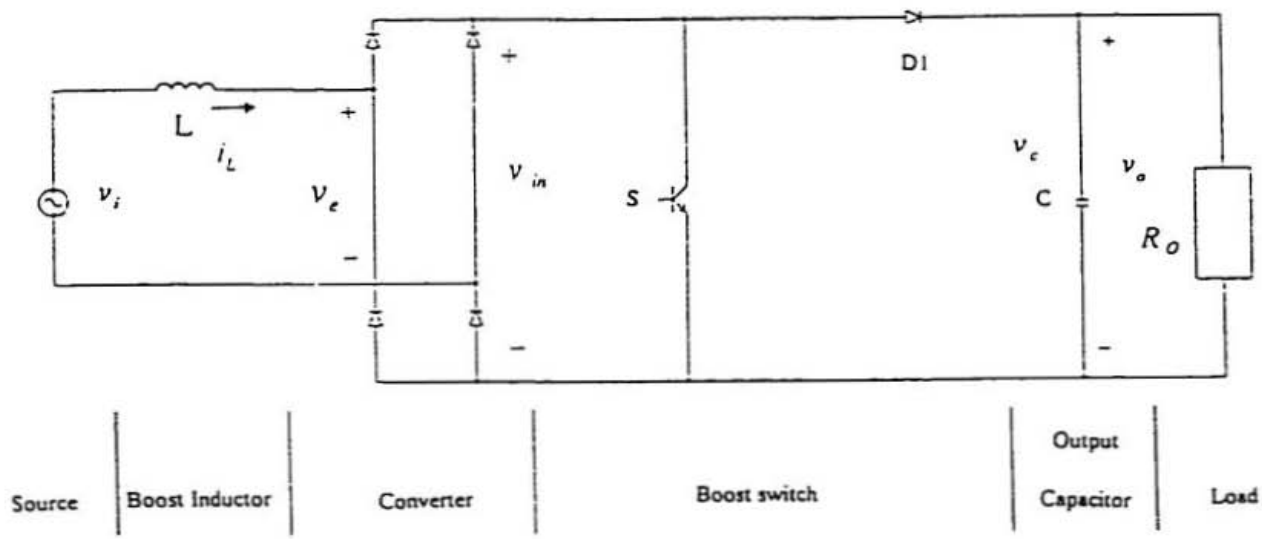


Figure 1.5: The single-phase PFC circuit

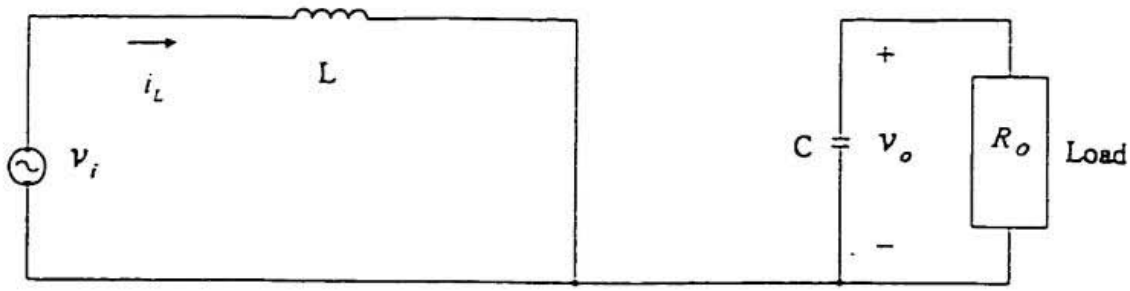


Figure 1.6(a): Equivalent circuit - ON state

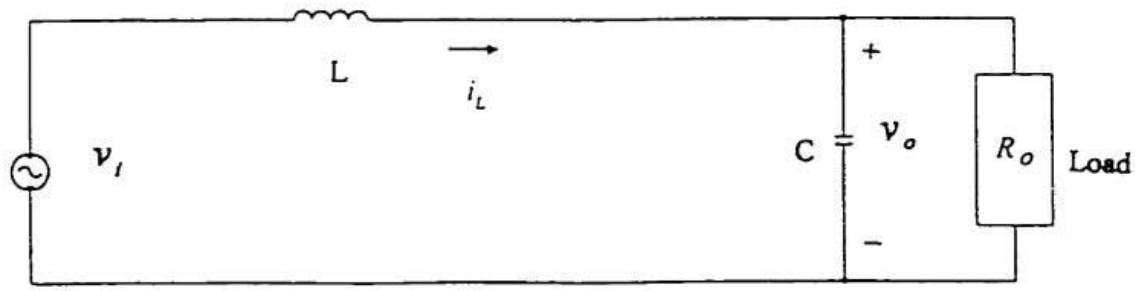


Figure 1.6(b): Equivalent circuit - OFF state

During the ON state the boost switch (S) provides a short circuit path through the AC source, the pair of diagonal diodes and the inductor (L). Consequently, the current in the inductor increases at a rate proportional to the instantaneous value of the input voltage. The output capacitor (C) meanwhile discharges through the load and provides the regulated power to it. During the OFF state the current in the boost inductor decreases since the output voltage is much higher than the instantaneous input voltage. At the end of this stage the output capacitor (C) is charged to its maximum value. The ideal operating waveforms of the converter are shown in fig 1.7.

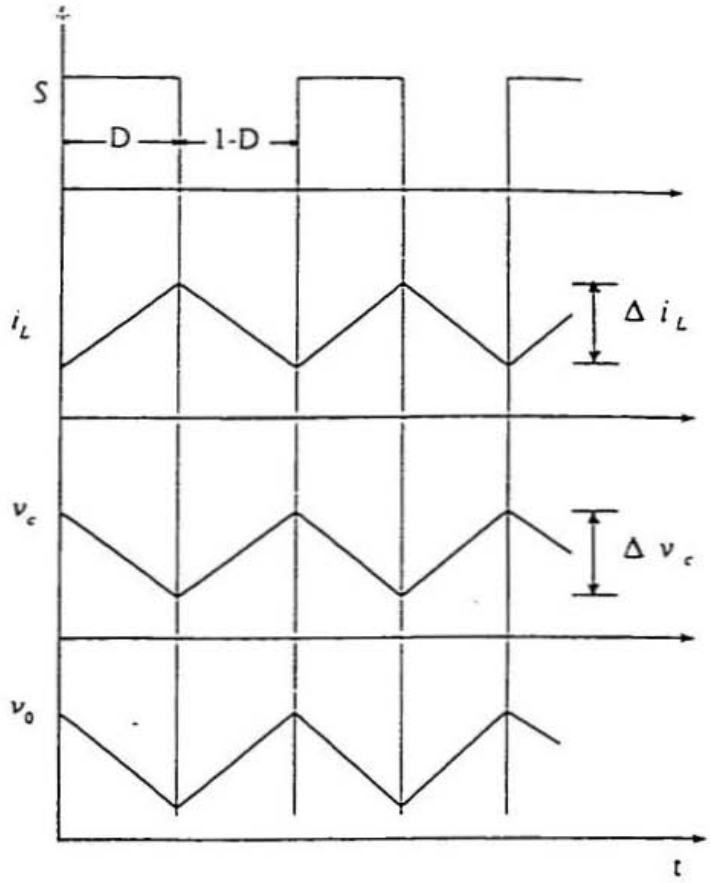


Figure 1.7: Ideal operating waveform of boost converter

1.4.2.2 CONTROL SCHEMES FOR THE SINGLE PHASE AC-DC CONVERTER

It has been shown that the current-mode controllers are superior to the PWM duty-ratio controllers used for APC and PCFF techniques [22]. The major advantages of the current-mode controllers are :

- Essentially no phase lag from the control to inductor current, practically eliminating the possibility of low-frequency oscillation of the closed loop
- Inherent pulse-by-pulse current limiting, making the power converter nearly immune to damage from overloads
- Ease of paralleling power stages, to provide increased output-current capability, with equal current-sharing among the paralleled stages
- Ease of applying output-current feedforward, to obtain super-fast correction for load transients and minimization of the deviations of output voltage
- Inherent insensitivity to static and dynamic variations of input voltage

Current control schemes can be classified broadly into three groups, namely

a) Constant Frequency Control Schemes

b) Variable Frequency Control Schemes

c) Zero-current, Zero-voltage Switching Control Schemes

1.5 THESIS OBJECTIVES

The various current control schemes for achieving nearly unity power factor and to minimize the total harmonic distortion (THD) of the input current have been proposed and their feasibility have been demonstrated [25-34]. However, to the best of the author's knowledge, a comparative study of their features is lacking in the literature. The objective of this thesis is, therefore, to examine and compare the performance characteristics of the various current control methods for power factor correction. The performance characteristics are obtained through the modelling and simulation of the different methods for the same circuit conditions.

1.6 THESIS OUTLINE

Chapter 2 focuses on the description, mathematical models and analysis of the different types of constant frequency current control methods. Operational and performance characteristics, namely total harmonic distortion, frequency spectrum and power losses have been presented for two values of switching frequency. MATLAB [36] has been used to simulate the system equations. The advantages and disadvantages of the different types of constant frequency control schemes are highlighted in the chapter.

Chapter 3 discusses the description, mathematical models and analysis of the variable frequency current control scheme and the performance for the same circuit conditions. Computer simulations of the control scheme are also provided to show the various characteristics of the scheme. The advantages and disadvantages are also

discussed.

Chapter 4 is devoted to the modelling, analysis and simulation of a zero current-zero voltage switching (ZCS-ZVS) scheme. Simulation results have been provided to show the operational features of the control scheme. The different performance characteristics such as total harmonic distortion, frequency spectrum and power loss are presented.

Finally, in Chapter 5, a summary of the thesis highlighting the contribution of the research and suggestions for further work is outlined.

Chapter 2

CONSTANT FREQUENCY CONTROL SCHEMES

INTRODUCTION

The most important feature of constant frequency control schemes is that the frequency of operation of the boost switch (S) remains constant throughout the cycle of operation. Constant frequency is desirable since it allows for the easy design of an input filter and the total harmonic distortion can be readily predicted. This chapter focuses on the description, modelling, analysis and simulation of constant frequency control schemes used in AC-DC converter systems. The modelling and analysis has been done using equivalent circuit representation of the various states of the boost switch. The analytical expressions corresponding to the equivalent circuits that describe the boost inductor current and output voltage in steady state operation are then formulated. These equations are then simulated using MATLAB to obtain the performance characteristics of the different constant frequency control methods.

Among the many control methods, the most popular constant frequency control methods which are described in this chapter are

a) Constant Frequency Continuous Current Control (CFCC)

b) Constant Frequency Discontinuous Current Control (CFDC)

2.1 CONSTANT FREQUENCY CONTINUOUS CURRENT CONTROL SCHEME

This control scheme gives a continuous non-zero boost inductor current at a fixed switching frequency. Through the action of the control scheme, the inductor current is constrained to follow the rectified waveshape of the input voltage, resulting in a nearly sinusoidal input current waveform.

In order to achieve a nearly unity power factor at the input and a constant DC output voltage, the two important circuit variables which are to be controlled are the boost inductor current and the output voltage. These variables can be used in a feedback control circuit which in turn will control the duty cycle of the boost switch. Figure 2.1 shows the control circuit diagram of the constant frequency continuous current (CFCC) control scheme [26]. The scheme uses the average value of the inductor current as an inner loop control variable to determine the ON/OFF switching of the boost switch (S). A signal proportional to the actual instantaneous inductor current is compared with a signal from the block K through the comparator (EA). The prime importance of the block K is to establish the desired average inductor current.

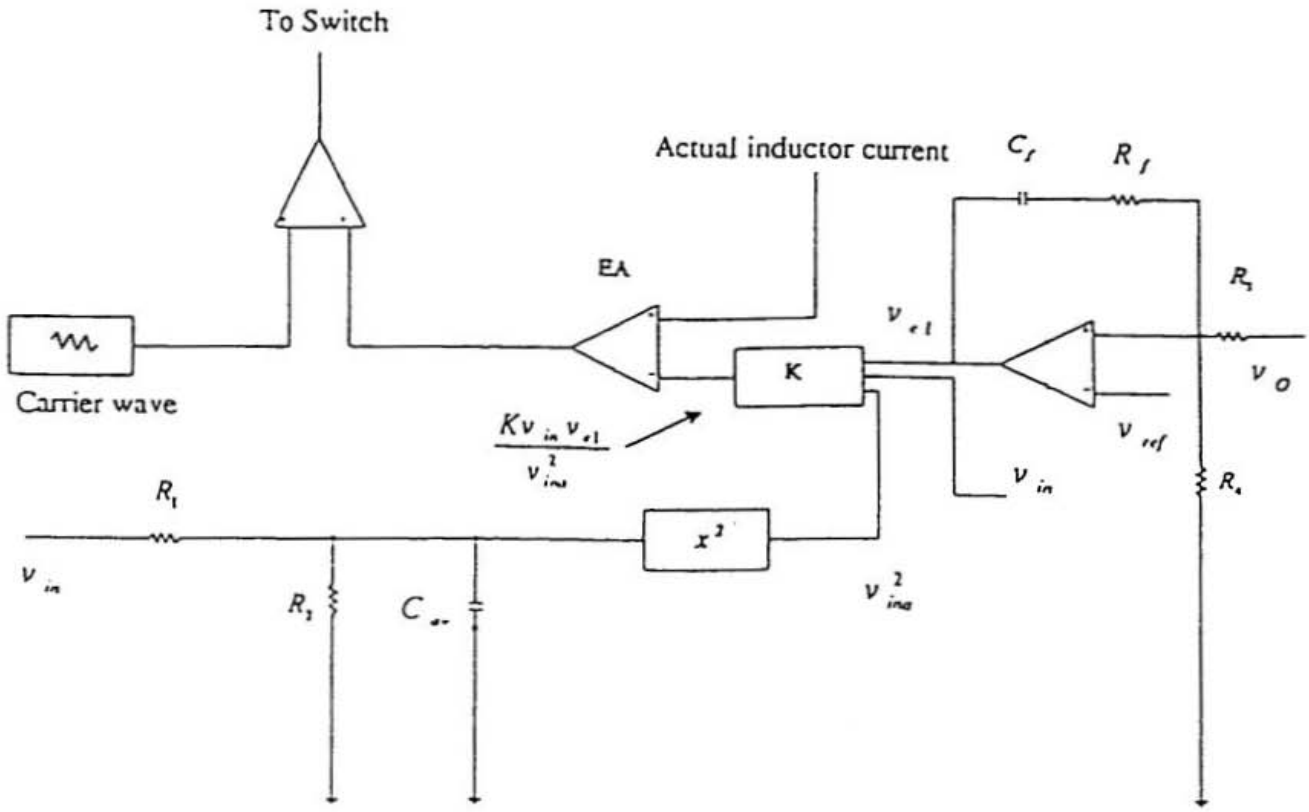


Figure 2.1: Control circuit of the CFCC scheme [26]

An outer voltage feedback loop, comprising the filtered output voltage (v_o), the rectified input voltage (v_{in}) and the square of the feedforward signal (v_{ina}), provides the regulation of the output voltage.

The average current is directly proportional to the rectified input voltage, error amplifier output voltage (v_{el}) and inversely proportional to the square of the feedforward voltage. From fig 2.1 the desired average inductor current i_{av} is obtained as

$$i_{av} = \frac{K v_{in} v_{el}}{v_{ina}^2} \tag{2.1}$$

where

v_{in} is the instantaneous voltage of the rectified sine wave from the line

v_{el} is the instantaneous output voltage of the error amplifier

v_{ina} is a signal proportional to the rms value of the line voltage which is introduced to normalize the rectified sine wave and provide feedforward.

K is the multiplying factor to achieve a desired average inductor current

For one switching interval the input voltage, error amplifier voltage and the feedforward voltage are assumed to be constant and equation 2.1 can be written as

$$I_{av} = \frac{K V_{in} V_{el}}{V_{ina}^2} \tag{2.2}$$

The output of the comparator EA is compared with a fixed frequency triangular waveform to produce a PWM signal for the ON/OF control of the boost switch. The error amplifier (EA) is designed with a very slow frequency response. This prevents the error signal from following the ripple changes in the output voltage.

2.1.1 MODELLING AND ANALYSIS OF THE POWER CIRCUIT

This section presents the modelling and analysis of the power factor correction circuit taking into account the effect of the control scheme. The converter operates in two distinct states, namely the ON and OFF states.

2.1.1.1 THE ON STATE

The equivalent circuit for the ON state of the boost switch is shown in fig 2.2. The model includes the series resistance (R_L) associated with the boost inductor, and the equivalent series resistance (R_{esr}) of the output capacitor.

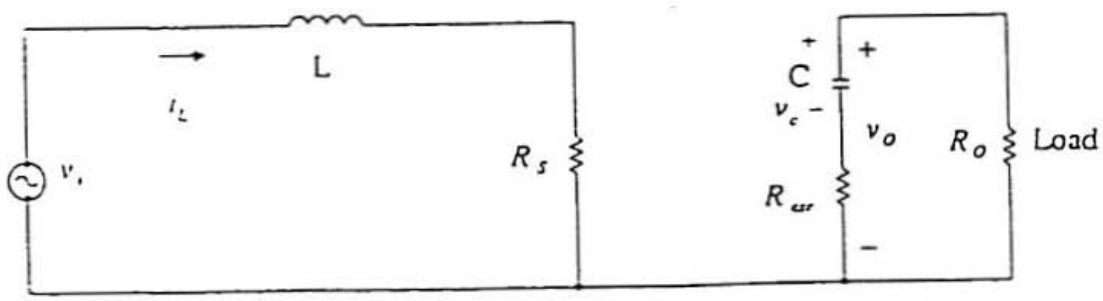


Figure 2.2 : ON state equivalent circuit

The following equations can be derived from the equivalent circuit.

$$L\frac{di_L}{dt} = v_i - i_L R_s \tag{2.3}$$

$$C\frac{dv_c}{dt} = -\frac{v_c}{R_{esr} + R_O} \tag{2.4}$$

where

i_L is the instantaneous inductor current

v_i is the instantaneous supply voltage

v_c is the instantaneous capacitor voltage

R_{esr} is the series resistance associated with the output capacitor C

R_s is the series resistance associated with the boost inductor L

R_O is the load resistance

For a small time increment Δt, the inductor current i_L, capacitor voltage v_c and the supply voltage, v_i may be assumed constant and may be represented as I_L, V_c and V_i respectively. Over the time interval Δt, equations 2.3 and 2.4 may be written as

$$L\frac{\Delta i_L}{\Delta t} = V_i - R_s I_L \tag{2.5}$$

$$C\frac{\Delta v_c}{\Delta t} = -\frac{V_c}{R_{esr} + R_O} \tag{2.6}$$

Equations (2.5) and (2.6) can be used to calculate the state variables Δi_L and Δv_c at the end of the time interval Δt. The values obtained at the end of the time interval can be used as the initial values of the next interval. This procedure, repeated for subsequent

intervals gives continuous values of i_L and v_c during the ON state of the switch. This method is only accurate if the time interval is small.

In equation (2.5) and (2.6), the inductor current I_L and capacitor voltage V_c are approximated as the average of the values at the start (i_{Ls}, v_{cs}) and end (i_{Le}, v_{ce}) of the time interval Δt, and are expressed as

$$I_L = 0.5(i_{Ls} + i_{Le}) \tag{2.7}$$

$$V_c = 0.5(v_{cs} + v_{ce}) \tag{2.8}$$

$$\Delta i_L = i_{Le} - i_{Ls} \tag{2.9}$$

$$\Delta v_c = v_{ce} - v_{cs} \tag{2.10}$$

Substituting these values into equations (2.5) and (2.6) gives

$$i_{Le} = \frac{V_i + i_{Ls}\left(\frac{L}{\Delta t} - \frac{R_s}{2}\right)}{\frac{L}{\Delta t} + \frac{R_s}{2}} \tag{2.11}$$

$$v_{ce} = \frac{\frac{C}{\Delta t} - \frac{1}{2(R_{esr} + R_O)}}{\frac{C}{\Delta t} + \frac{1}{2(R_{esr} + R_O)}} v_{cs} \tag{2.12}$$

The output voltage is given by

$$v_{oe} = v_{ce}\frac{R_O}{R_{esr} + R_O} \tag{2.13}$$

where v_{oe} is the output voltage at the end of the interval Δt. By applying these relationships to the successive time intervals the values of i_L and v_c at the end of the ON interval can be found if the duty ratio D is known. These values are used as the starting

values of the OFF state. A procedure for determining the duty ratio D is described in section 2.1.3.

Neglecting the resistances, R_{esr} and R_s in equation 2.11 to 2.13, simplified results are obtained for the inductor current and capacitor voltage, which are given as

$$i_{Le} = \frac{V_i + i_{Le}\left(\frac{L}{\Delta t}\right)}{\frac{L}{\Delta t}} \tag{2.14}$$

$$v_{ce} = \frac{\frac{C}{\Delta t} - \frac{1}{2(R_o)}}{\frac{C}{\Delta t} + \frac{1}{2(R_o)}} v_{ce} \tag{2.15}$$

During the ON state the energy is drawn from the output capacitor to the load and during the OFF state energy is supplied by the source to the load. The change in capacitor voltage (neglecting the inductor and capacitor resistances) is given by

$$\Delta V_{01} = \frac{1}{C}.I_o.T_{on} = \frac{I_o}{C}.D.T_S = \frac{V_O.D.T_S}{C.R_O} \tag{2.16}$$

where T_{on} is the ON time period

T_S is the total time period of one switching cycle

I_o is the discharging current through the output capacitor

D is the duty ratio

The power output of the converter circuit is given by

$$P_o = \frac{V_{ref}^2}{R_O} \tag{2.17}$$

where

P_o is the total power output of the circuit

V_{ref} is the reference output voltage

Substituting equation 2.17 into equation 2.16 gives

$$\Delta V_{01} = -\frac{P_o . V_o . D}{V_{ref}^2 . C . F_s} \tag{2.18}$$

The minus sign denotes the capacitor is discharging during the ON period and there will be a drop in the output voltage.

2.1.1.2 THE OFF STATE

The equivalent circuit for the OFF state is shown in fig 2.3. The governing equations of the inductor current and capacitor voltage are obtained as

$$L\frac{di_L}{dt} = v_i - i_L(R_s + \frac{R_{esr} . R_O}{R_{esr} + R_O}) - v_c \frac{R_O}{R_{esr} + R_O} \tag{2.19}$$

$$C\frac{dv_c}{dt} = \frac{i_L R_O}{R_{esr} + R_O} - \frac{v_c}{R_{esr} + R_O} \tag{2.20}$$

and the output voltage is given by

$$v_o = (v_c + i_L R_{esr}) \frac{R_o}{R_o + R_{esr}} \tag{2.21}$$

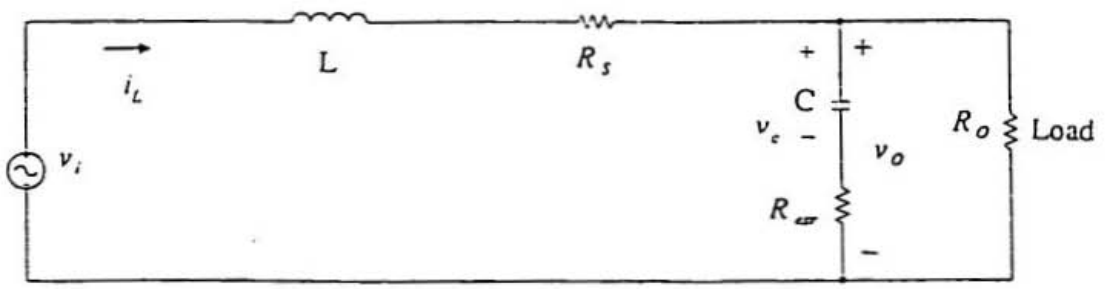


Figure 2.3 : OFF state equivalent circuit

Using the approximations introduced for the ON state (equations 2.7 to 2.10), the values of i_{Lf}, v_{cf} and v_{of} at the end of the OFF interval are derived from equations 2.19 to 2.21. Using MAPLE [37] to solve 2.19 and 2.20, the values of i_{Lf}, v_{cf} and v_{of} can be determined. The general results are given in Appendix A.

Neglecting the resistances, R_{esr} and R_s in equation A.1 and A.2, simplified results can be obtained for the inductor current and capacitor voltage, which are given as

$$i_{Le}=\left\{\frac{-2.F_1.C_1+2.B_1^2.F_1-\sqrt{A_1}.V_i.B_1^2-4.C_1.V_i.L-\sqrt{A_1}.C_1.V_i+\sqrt{A_1}.L.i_{Le}.B_1+4.B_1^2.V_i.L}{\left(L\left(\sqrt{A_1}.B_1^2-4.B_1^2.L-\sqrt{A_1}.C_1+4.C_1.L-\sqrt{A_1}.B_1\right)\right)}\right\}$$

(2.22)

$$v_{ce}=\left\{\frac{-\sqrt{A_1}.v_{cs}.B_1+2.C_1.i_{Le}.R_O.L+2.C_1.V_i.R_O-2.B_1^2.i_{Le}.R_O.L-2.B_1^2.V_i.R_O}{\sqrt{A_1}.B_1^2+2.C_1.L+\sqrt{A_1}.C_1-\sqrt{A_1}.B_1-2.B_1^2.L}\right\}$$

(2.23)

where

$$A_1=L^2+4.L.C.R_O^2 \qquad F_1=L.v_{ce}.R_O.C$$

$$B_1=e^{\left(0.5\cdot\frac{\left(-\sqrt{A_1}+2.L\right).t}{(R_O).L.C}\right)} \qquad C_1=e^{\left(-\frac{t}{(R_O).C}\right)}$$

The values at the end of the OFF state are used as the starting values for the next ON state. Since the switching frequency (F_S) is known, the OFF time period can be calculated as

$$t_{off}=(1-D)/F_S \tag{2.24}$$

This process is repeated for the full cycle of the input voltage. During the OFF state, the output voltage is determined by the discharging current from the inductor and the supply voltage as

$$\Delta V_{O2}=\frac{(I_{pk}+I_2)(1-D)}{2C.F_s} \tag{2.25}$$

where

I_{pk} is the inductor current value at the end of the ON period

I_2 is the inductor current value at the end of OFF period

Combining the equations 2.24 and 2.25, a linearised equation for the output voltage is obtained as

$$V_{O(n)} = V_{O(n-1)} + (\Delta V_{O1} + \Delta V_{O2}) \tag{2.26}$$

$$V_{O(n)} = V_{O(n-1)} + \left(-\frac{P_O V_O D}{V_{ref}^2 . C . F_s} + \frac{(I_{pk} + I_2)(1-D)}{2C . F_s} \right) \tag{2.27}$$

The resulting theoretical input current waveform of the CFCC scheme for a half-cycle is shown in fig 2.4. The waveform shows that the input current is continuous, i.e. non zero except at the zero crossings of the input voltage.

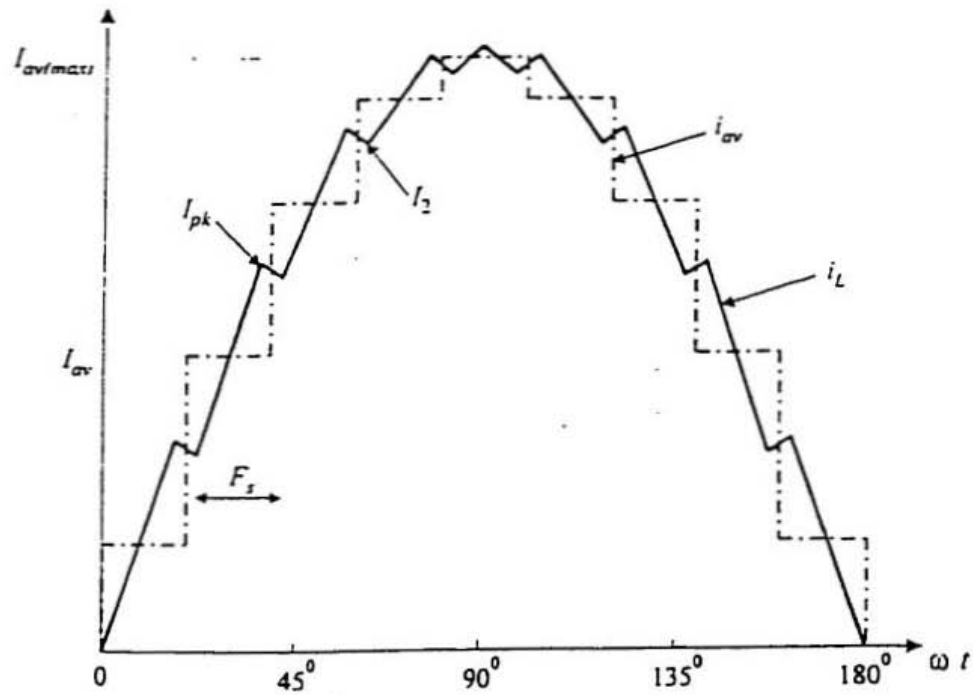


Figure 2.4: Theoretical input current waveform of the CFCC control scheme

2.1.2 MODELLING AND ANALYSIS OF THE CONTROL CIRCUIT

Referring to fig 2.1, a sample of the rectified line waveform (v_{in}) is supplied to the block K. The second input signal to the block 'K' is a DC voltage proportional to the rms value of the line voltage. This signal is used to provide low output distortion and good transient response. A passive low-pass filter ($R_1 - R_2 - C_{av}$) is used to generate this signal. The output of the filter at the start of a switching cycle is

$$V_{ina(n)} = V_{ina(n-1)} + \frac{\left(\frac{V_{in} - V_{ina(n-1)}}{R_1}\right) - \frac{V_{ina(n-1)}}{R_2}}{C_{av} F_s} \tag{2.28}$$

where:

R_1, R_2 and C_{av} are the resistances and capacitor of the low pass filter respectively

n is the number of the switching cycle

In the CFCC circuit [fig 2.1], the error amplifier which is used in the voltage feedback loop, is designed with a very slow frequency response. To achieve this slow frequency response, the corner frequency is chosen to be in the range 15-30Hz. The governing equation of the error amplifier is

$$V_{e(n)} = V_{e(n-1)} - \frac{\frac{(V_O - V_{ref})}{R_3} + \frac{(V_{e(n-1)} - V_{ref})}{R_f}}{C_f . F_s} \tag{2.29}$$

In the control circuit, an error amplifier is used in the outer voltage feedback loop. Figure 2.5 shows the error amplifier which is assumed to be a single order integrator. Assuming an ideal op-amp the feedback current can be expressed as

$$i_{FB} = \frac{v_O - v_{ref}}{R_3} - \frac{v_{ref}}{R_4} \tag{2.30}$$

$$v_{e1} = v_{ref} - v_{cf} - i_{FB} R_f \tag{2.31}$$

where

i_{FB} is the instantaneous value of the feedback current

R_3 and R_4 are the resistances at the input of the error amplifier circuit

v_{ref} is the instantaneous value of the reference output voltage

v_{e1} is the instantaneous value of the error amplifier output

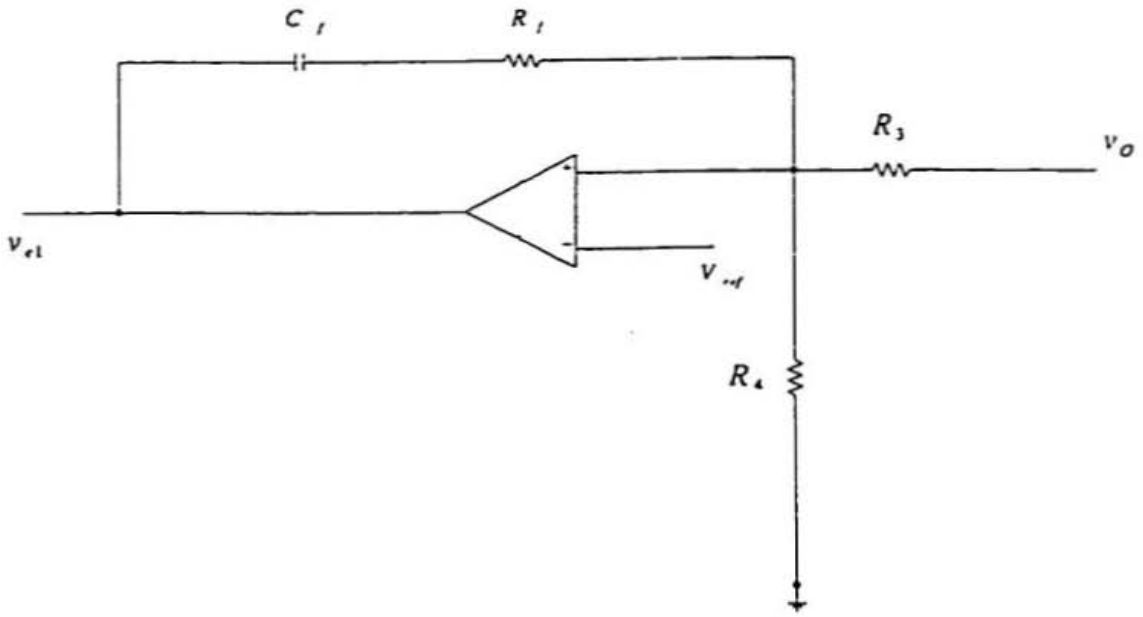


Figure 2.5: The error amplifier used in the voltage feedback loop

For a small interval, Δt, the voltage across C_f is given by

$$\frac{\Delta v_{cf}}{\Delta t} = \frac{I_{FB}}{C_f} \tag{2.32}$$

Equations 2.30 to 2.32 can be applied during the ON or OFF interval to determine the error amplifier voltage v_{e1} in each switching period. With v_{e1} determined, equation 2.2 can be used to obtain the desired average current (I_{av}).

2.1.3 DETERMINATION OF THE DUTY RATIO, D

The duty ratio, D can be determined using an iterative procedure that continuously calculates the ON/OFF times. The computation method results in an exhausting program looping run time in finding the correct duty ratio, D. In order to improve the computer run time for the simulation program, the duty ratio is calculated within each switching cycle. Fig 2.6 shows the inductor current waveform in the continuous mode of operation.

It is assumed that the switch is turned OFF so that the inductor current at the end of the OFF state cycle (I_2) is such that the required average inductor current is obtained during the next switching cycle. This is an approximation since the response of the circuit is not so precise and the desired average inductor current does not remain constant.

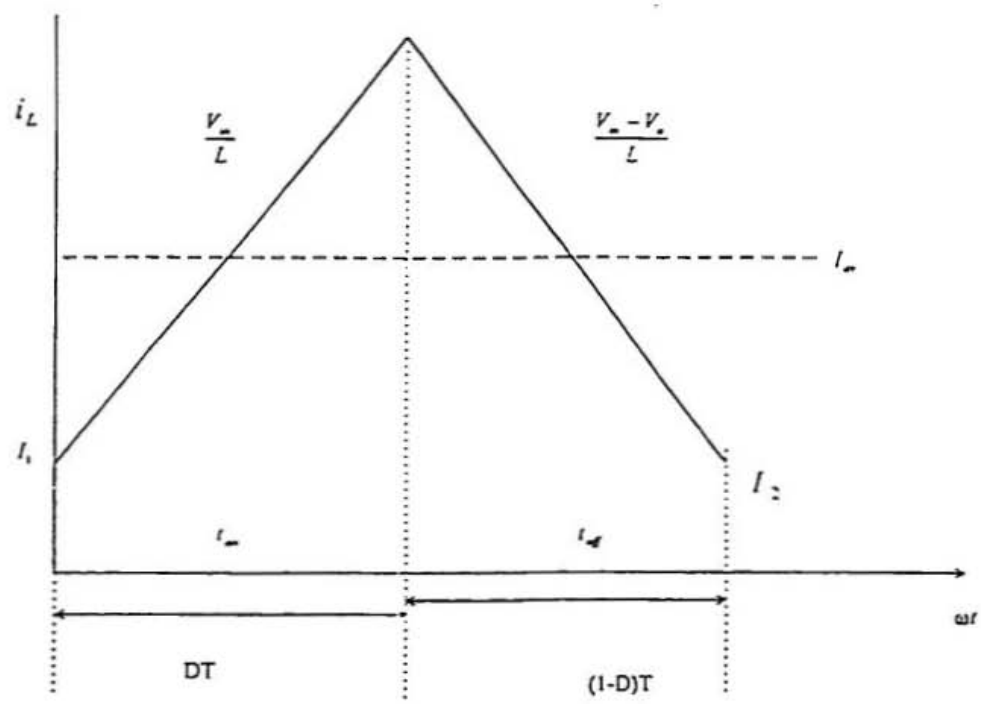


Figure 2.6: Inductor current waveform in the continuous mode of operation

In steady-state operation the duty ratio, D, taking into consideration the resistances of the boost inductor, output capacitor and the load, is given by [35]

$$\frac{V_o}{V_{in}} = \frac{1}{D'}\left[\frac{(D')^2 R_o}{R}\right] \tag{2.33}$$

where

$D' = 1\text{-}D$

$$R' = R_s + \left(\frac{R_o * R_{esr}}{R_o + R_{esr}} \right) * D' + \frac{R_o^2 * (D')^2}{R_o + R_{esr}}$$

V_O is the output voltage

V_{in} is the average rectified input voltage

Neglecting the equivalent series resistance of the output capacitor and the boost inductor equation (2.33) reduces to

$$\frac{V_O}{V_{in}} = \frac{1}{1 - D} \tag{2.34}$$

The average inductor current over one switching cycle is given by

$$I_{av} = I_2 + \frac{V_{in} D}{2LF_s} \tag{2.35}$$

From equations 2.34 and 2.35 the current I_2 is obtained as

$$I_2 = I_{av} - \frac{V_{in}(V_O - V_{in})}{2LF_s V_O} \tag{2.36}$$

From Fig 2.6 I_2 is obtained as

$$I_2 = I_1 + \frac{V_{in} D}{F_s L} - \frac{(V_O - V_{in})(1 - D)}{F_s L} \tag{2.37}$$

where, I_1 is the inductor current at the start of one switching cycle. The duty ratio D is obtained from equation 2.37 as

$$D = \frac{F_s L(I_2 - I_1) + V_O - V_{in}}{V_O} \tag{2.38}$$

Equation 2.38 gives the estimated duty ratio of an ON/OFF switching cycle. V_o and V_{in} are the respective average values of the output voltage and rectified input voltage

during the ON/OFF switching cycle. In a practical circuit the duty ratio D varies between 0.05 and 0.95. The duty ratio calculated from equation 2.38 is maintained within these limits

2.1.4 DESIGN EXAMPLE

A design example is given to illustrate the procedure for determining the control circuit constants and the power circuit parameters for the following conditions

Output power = 400 W Input voltage = $90V_{rms}$ (min) and $240V_{rms}$ (max)

Output DC voltage = 380V Switching frequency = 100 kHz

To determine the exact value of K (eqn 2.2), the desired maximum average input current ($I_{av(max)}$) is first calculated. Assuming that the stepped waveform, i_{av} (fig 2.4) follows a sinusoidal waveform, in phase with the input voltage, the desired peak average input current $I_{av(max)}$ at the minimum line voltage of $90V(rms)$, is obtained from

$$P_o = I_{av}(rms) * V_{in}(rms) = \frac{I_{av(max)}}{\sqrt{2}} * V_{in}(rms) \tag{2.39}$$

$$I_{av(max)} = \frac{P_o}{V_{in}(rms)}.\sqrt{2} = \frac{400}{90}.\sqrt{2} = 6.28A \tag{2.40}$$

Similarly the desired peak average input current $I_{av(max)}$ at the line voltage of $240V(rms)$ is obtained as

$$I_{av(max)} = \frac{400}{240}.\sqrt{2} = 2.36A \tag{2.41}$$

At an input voltage of 240 V(rms) and $I_{av(max)}$ of 2.36 A, the voltage V_{ina} is obtained from fig 2.1 as

$$V_{ina}(appr.) = \frac{2}{\pi}.V_{in}(pk).\frac{R_2}{R_2 + R_1} = \frac{2}{\pi}.240.\sqrt{2}.\frac{5.1}{5.1 + 270} = 4.01V$$

Assuming an error amplifier gain of 5 and a maximum error signal of 10, the maximum error voltage $V_{el}(\max)$ is

$$V_{el}(\max) = 5 * 10 = 50V$$

Using these values the value of the block 'K' is obtained from equation 2.2 as

$$K = \frac{I_{av(max)}V_{ina}^{\ 2}}{V_{in}(pk).V_{el}(\max)} = 2.23x10^{-3} \qquad (2.42)$$

If the average peak-to-peak ripple current (Δi) of the boost inductor for each switching cycle is assumed to be 0.3 amp and the supply voltage v_i is assumed to be constant over one switching cycle, the ON time (t_{on}) and OFF time (t_{off}) are obtained from fig 2.6 as

$$t_{on} = \frac{L\Delta i}{V_{in}} \qquad (2.43)$$

$$t_{off} = \frac{L\Delta i}{V_o - V_{in}} \qquad (2.44)$$

The switching period (T_s) is given by

$$T_s = \frac{1}{F_s} = t_{on} + t_{off} \qquad (2.45)$$

Substituting the ON and OFF time in equation (2.45) gives

$$L = \frac{V_i.(V_0 - V_i)}{F_s.\Delta i.V_0} \tag{2.46}$$

For an input voltage of 240 V(rms), output voltage at 380 V(dc), switching frequency of 100KHz and a ripple current of 0.3 amp, equation 2.46 gives

$$L = \frac{240\sqrt{2} * \left(380 - 240\sqrt{2}\right)}{100 * 10^3 * 0.3 * 380} = 1.2 \text{ mH} \tag{2.47}$$

From the above design procedure the value of the boost inductor is chosen to be 1.5 mH.

The value of the output capacitor is determined by assuming that the peak-to-peak ripple voltage of the capacitor is 1.2%, i.e. a voltage of magnitude 4.56V is expected over the steady DC output voltage of 380V. To achieve the above mentioned peak-to-peak ripple voltage, the change in voltage across the capacitor in one switching cycle (ΔV_{01}) is first calculated. As both the supply and switching frequencies are known parameters, the number of switching sections for one cycle of supply frequency can be obtained as

$$S_S = \frac{T_P}{T_S} = \frac{16.667 m\text{sec}}{10 \mu\text{sec}} \cong 1667 \tag{2.48}$$

where

T_P is the time period of the supply voltage

T_S is the switching time of the boost switch

S_S is the number of switching sections

Assuming equal change in capacitor voltage (ΔV_{01}) during each switching interval, ΔV_{01} is calculated as

$$\Delta V_{01} = \frac{4.56}{1667} = 2.74mV \tag{2.49}$$

When the switch is ON, the output capacitor supplies the load current, and the change in capacitor voltage is given by

$$\Delta V_{01} = v_c - v_c(t=0) = \frac{1}{C}\int_0^{t_{on}} I_c.dt = \frac{I_c * t_{on}}{C} \tag{2.50}$$

Equation (2.50) may be written as

$$\Delta V_{01} = \frac{I_c * D * T_s}{C} = \frac{I_c * D}{C * F_s} \tag{2.51}$$

Substituting for D (from equation 2.34) in equation 2.51, gives

$$\Delta V_{01} = \frac{I_c * (V_o - V_{in})}{V_o * C * F_s} \tag{2.52}$$

The discharging current of the capacitor during the ON time period is also the load current (I_{Load}) and can be written as

$$I_c = I_{Load} = \frac{P_o}{V_o} \tag{2.53}$$

Substituting equation (2.53) in equation (2.52) gives

$$\Delta V_{01} = \frac{P_o * (V_o - V_{in})}{V_o^2 * C * F_s} \tag{2.54}$$

From equation (2.54) the value of the output capacitor is obtained as

$$C = \frac{P_o * (V_o - V_{in})}{V_o^2 * \Delta V_{01} * F_s} = \frac{400 * (380 - 240\sqrt{2})}{380^2 * 100 * 10^3 * 2.74 * 10^{-3}} = 410\mu F \qquad (2.55)$$

A conservative value of $470\,\mu F$ for the output capacitor is chosen for the simulation of the circuit.

2.1.5 POWER LOSS CALCULATION OF THE BOOST SWITCH

Power dissipation in semiconductor power devices is fairly generic in nature; that is, the same basic factors governing power dissipation apply to all devices in the same manner. The power converter under consideration represents the commonly encountered situation; the current flowing through a switch (i_{ST}) also must flow through a series inductance. The design calculation therefore assumes an inductive load switching. Referring to fig 1.5 when the switch is ON, I_{av} flows through the switch while a voltage equal to the rectified input voltage (V_{in}) appears across the switch for a small interval (t_n). During the OFF time I_{av} flows through the diode while a voltage equal to the rectified input voltage (V_{in}) appears across the switch, assuming a zero voltage drop across the diode. Figure 2.7(a) shows the waveform for the current through the switch (i_{ST}) and the voltage across the switch (v_{ST}) when it is being operated at a repetition rate or switching frequency.

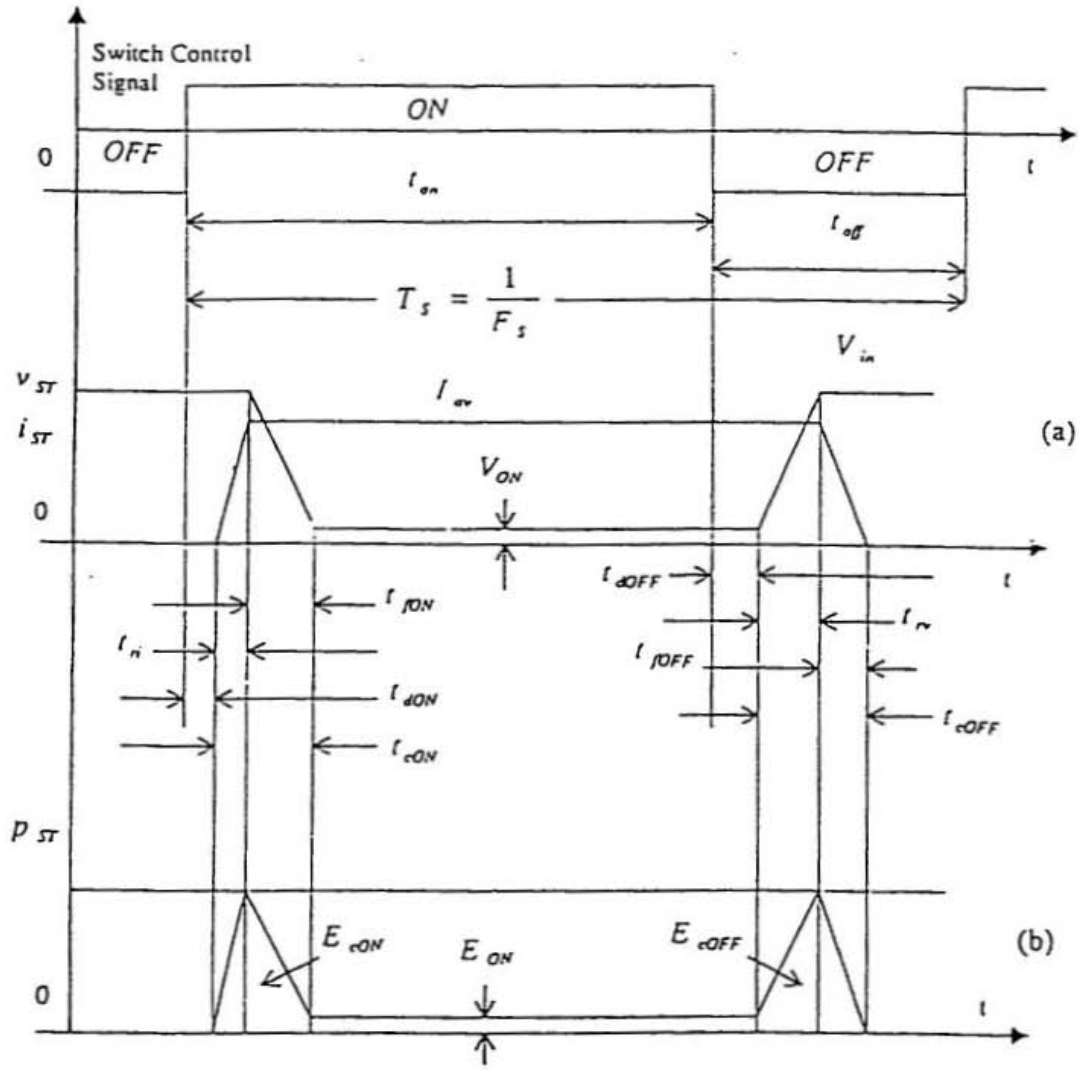


Figure 2.7 : (a) Boost switch waveforms, (b) Instantaneous boost switch power loss

The switching waveforms are represented by linear approximation to the actual waveforms in order to simplify the discussion. As seen from fig 2.7(a), during the turn-ON transition of the boost switch, the current buildup consists of a short delay time

t_{dON} followed by the current rise time t_{ri}. The boost switch voltage (v_{ST}) then falls to a small ON-state value of V_{ON} with a fall time of t_{fON}. The turn-ON crossover interval t_{cON} is given by

$$t_{cON} = t_{ri} + t_{fON} \tag{2.56}$$

The energy dissipated in the device during this turn-ON transition can be approximated from fig 2.7(b) as

$$E_{cON} = \frac{1}{2} * V_{in} * I_{av} * t_{cON} \tag{2.57}$$

The energy dissipation (E_{ON}) in the switch during this ON-state interval can be approximated as

$$E_{ON} = V_{ON} * I_{av} * t_{ON} \tag{2.58}$$

where $t_{ON} >> t_{cON}, t_{cOFF}$

During the turn-OFF transition period, the voltage buildup consists of a turn-OFF delay time t_{dOFF} and a voltage rise time t_{rv}. Once the voltage reaches its final value of v_{ST}, then the current in the switch falls to zero with a fall time t_{fOFF}. The turn-OFF crossover interval is given by

$$t_{cOFF} = t_{rv} + t_{fOFF} \tag{2.59}$$

The energy dissipated (E_{cOFF}) during turn-OFF transition can be written as

$$E_{cOFF} = \frac{1}{2} * V_{in} * I_{av} * t_{cOFF} \tag{2.60}$$

Figure 2.7(b) shows the instantaneous power dissipation ($p_{ST} = v_{ST} * i_{ST}$) across the boost switch. From equation 2.57 and 2.60 the average power loss (P_{SS}) due to these transitions for a switching frequency of (F_S) is given as

$$P_{SS} = \frac{1}{2} * V_{in} * I_{av} * F_S * \left[t_{cON} + t_{cOFF} \right] \tag{2.61}$$

The other major contribution to the power loss in the boost switch is the average power dissipated during the ON-state P_{ON}, which is given by

$$P_{ON} = V_{ON} * I_{av} * \frac{t_{on}}{T_S} \tag{2.62}$$

The leakage current during the OFF state of the boost switch is negligibly small and therefore can be neglected. Hence, the total average power dissipation (P_T) across the boost switch is given by

$$P_T = P_{SS} + P_{ON} \tag{2.63}$$

The worst case power loss across the boost switch will occur at the peak input voltage. Using the equations 2.61, 2.62 and 2.63 and assuming t_{ri}, t_{fON}, t_{rv}, t_{fOFF}, V_{ON} to be 100ns, 50ns, 100ns, 200ns and 1.5V respectively, the average power loss at the peak input voltage for a constant switching frequency of 100kHz, is obtained as

$$P_T = \left[\frac{1}{2} * 240\sqrt{2} * 2.36 * 100 * 10^3 * 450 * 10^{-9} \right] + \left[1.5 * 2.36 * \frac{1\mu s}{10\mu s} \right] = 18.37W \tag{2.64}$$

2.1.6 SIMULATION OF THE PFC CIRCUIT FOR THE CONTINUOUS CURRENT MODE CONTROL

Normally the PFC circuit is operated at higher frequencies so as to reduce the total harmonic distortion of the input current. However, the circuit has been simulated at a reduced frequency in order to show the details of the waveform. The two values of switching frequency used for the simulation are 100KHz and 5KHz. The procedure outlined in the previous section is used to determine the circuit parameters at the two frequencies, which are as follows

Line voltage, $V_i = 240\,V(rms)$	Line voltage, $V_i = 100\,V(rms)$
Line frequency, f_i = 60Hz	Line frequency, f_i = 60Hz
Output Voltage, V_o = 380V(dc)	Output Voltage, V_o = 200V(dc)
Output power, P_o = 400W	Output power, P_o = 160W
Switching frequency, F_s = 100kHz	Switching frequency, F_s = 5kHz
Boost inductor, L = 1.5mH	Boost inductor, L = 5.5mH
Output capacitor, C = 470 μF	Output capacitor, C = 1000 μF

Per-unit values

1 p.u voltage = 240V	1 p.u voltage =100V
1 p.u power = 400W	1 p.u power = 160W
1 p.u current = $\frac{400}{240}$ = 1.67 A	1 p.u current = $\frac{160}{100}$ = 1.6 A

2.1.6.1 SIMULATION PROCEDURE

The flow chart of the complete simulation procedure of the CFCC control is given in fig 2.8. MATLAB is used to simulate the design equations.

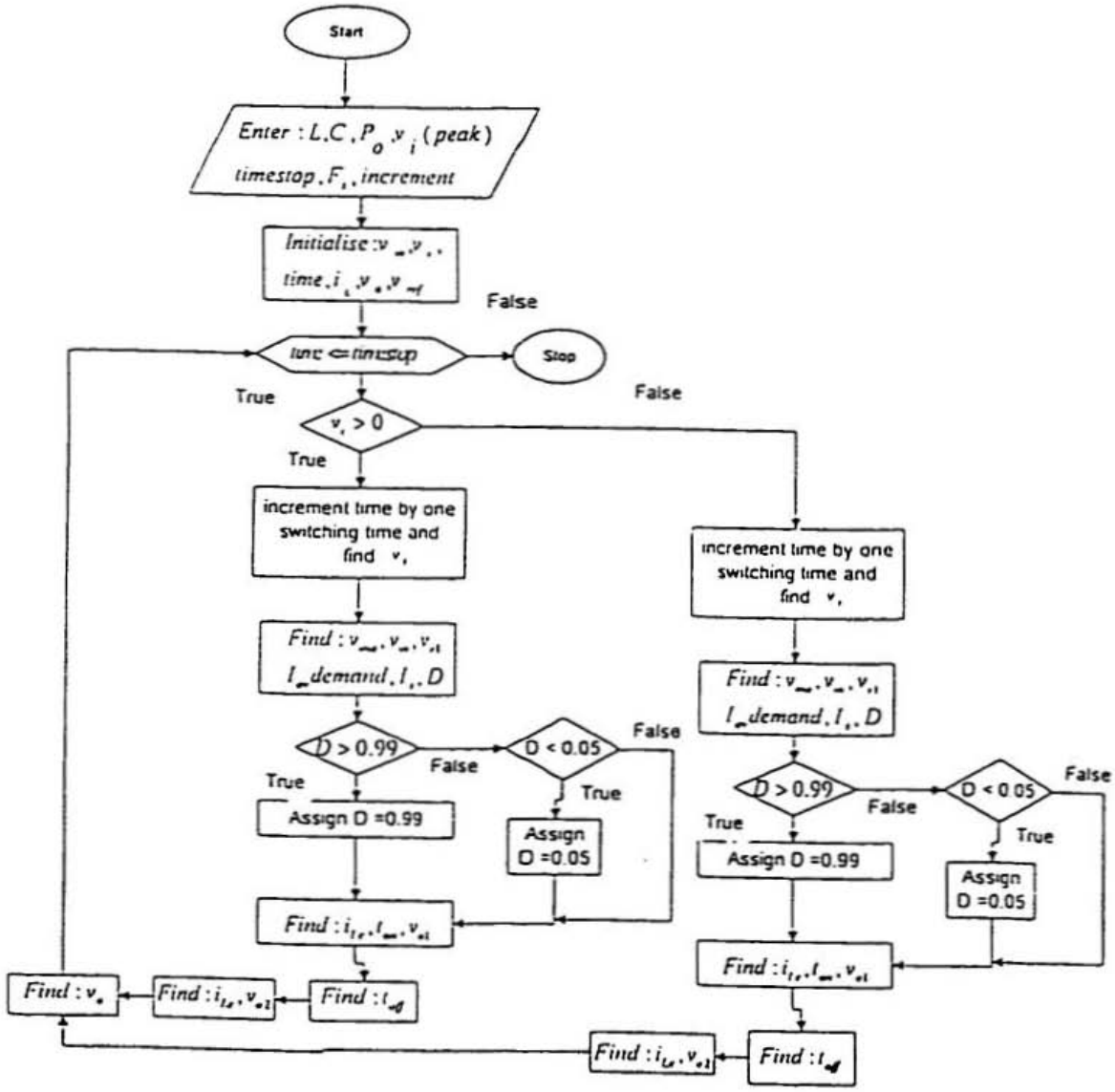


Figure 2.8 : Flow chart of the CFCC control scheme showing the simulation procedure

2.1.6.2 SIMULATION RESULTS

Figures 2.9 and 2.10 show the source current and source voltage in per unit at 100KHz and 5KHz respectively. As seen from the graphs, this control scheme is capable of producing nearly sinusoidal input current waveform.

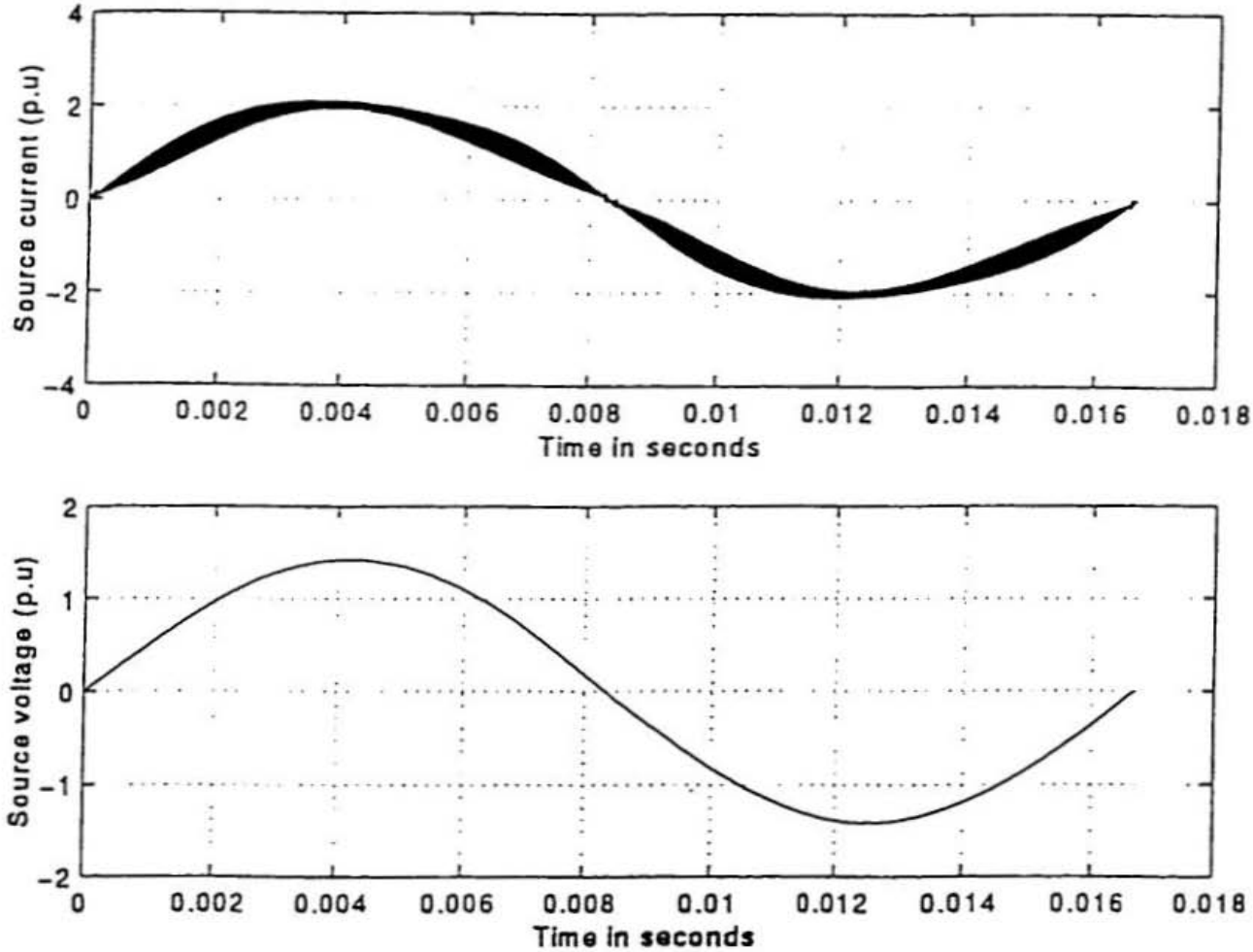


Figure 2.9 : Per-unit source current and source voltage waveforms

(L = 1.5mH, C = 470 μF , F_s = 100kHz)

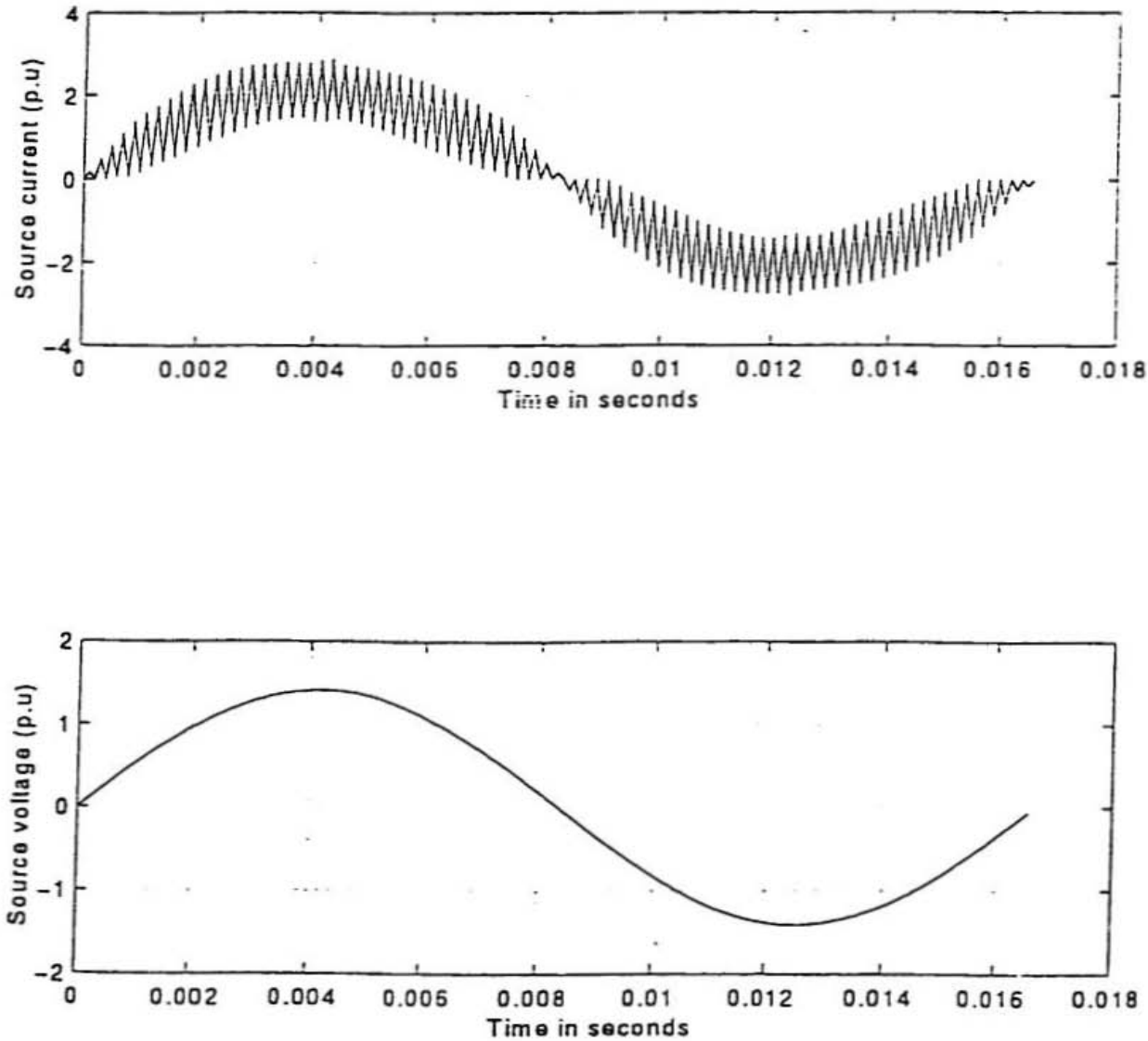


Figure 2.10 : Per unit source current and source voltage waveforms

(L = 5.5mH, C = 1000 μF , F_r = 5kHz)

The total harmonic distortion (THD) for fig 2.9 is calculated to be 4%. The performance characteristics (fig 2.11 and 2.12) show that the peak to peak ripple of the boost inductor current decreases with increase in the value of the boost inductor for a fixed output capacitor and switching frequency of 100kHz and 5kHz respectively.

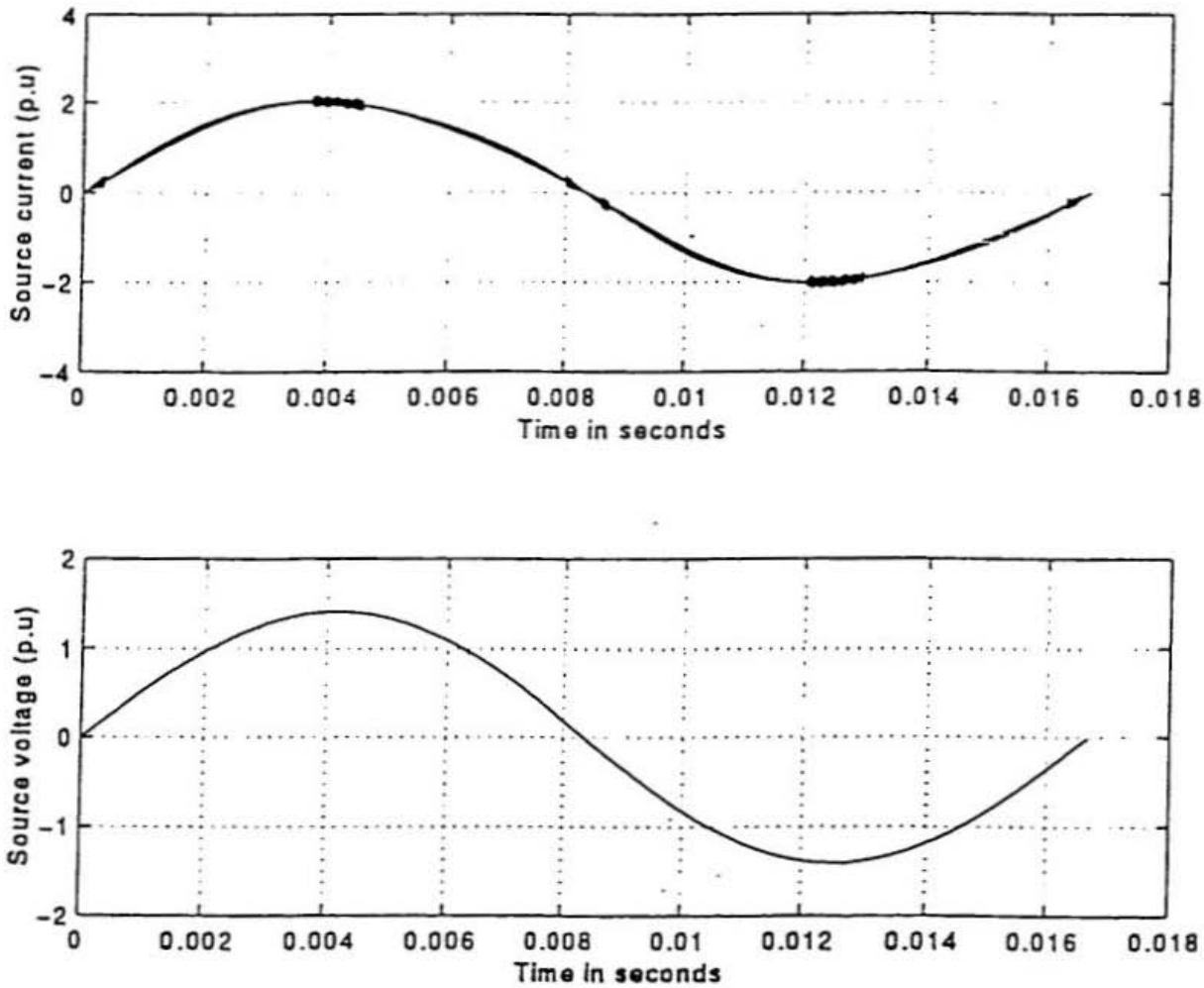


Figure 2.11 : Per unit source current and source voltage waveforms

(L = 5mH, C = 470 μF , F_s = 100kHz)

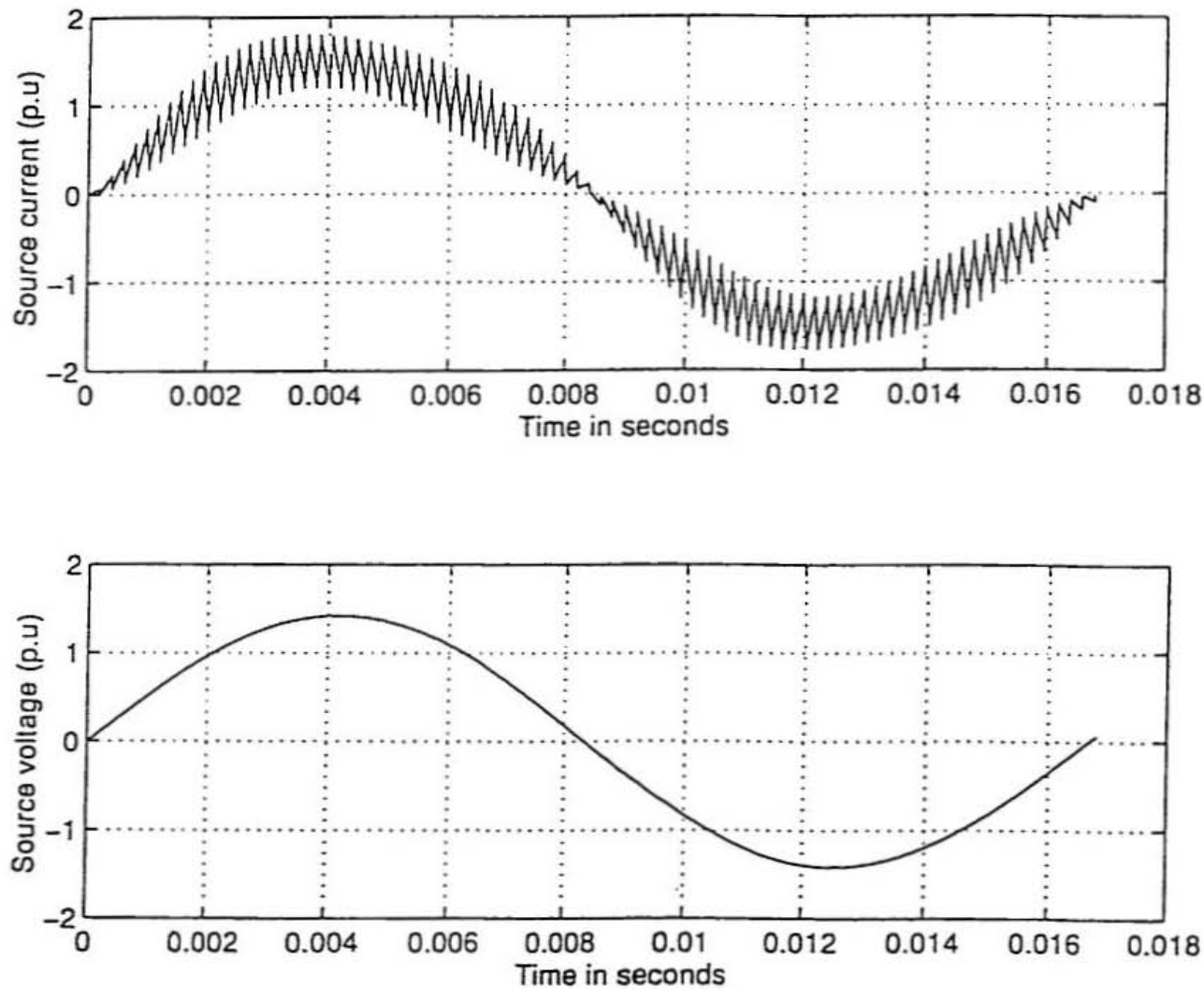


Figure 2.12 : Per unit source current and source voltage waveforms

(L = 10mH, C = 1000 μF , F_r = 5kHz)

Figure 2.13 shows the per-unit output voltage ripple waveform. The peak-to-peak ripple on the output voltage is found to be 1.4% as assumed in the design example. Figures 2.14 and 2.15 show a plot of the total harmonic distortion (THD) of the source current with respect to varying boost inductor value and switching frequency respectively.

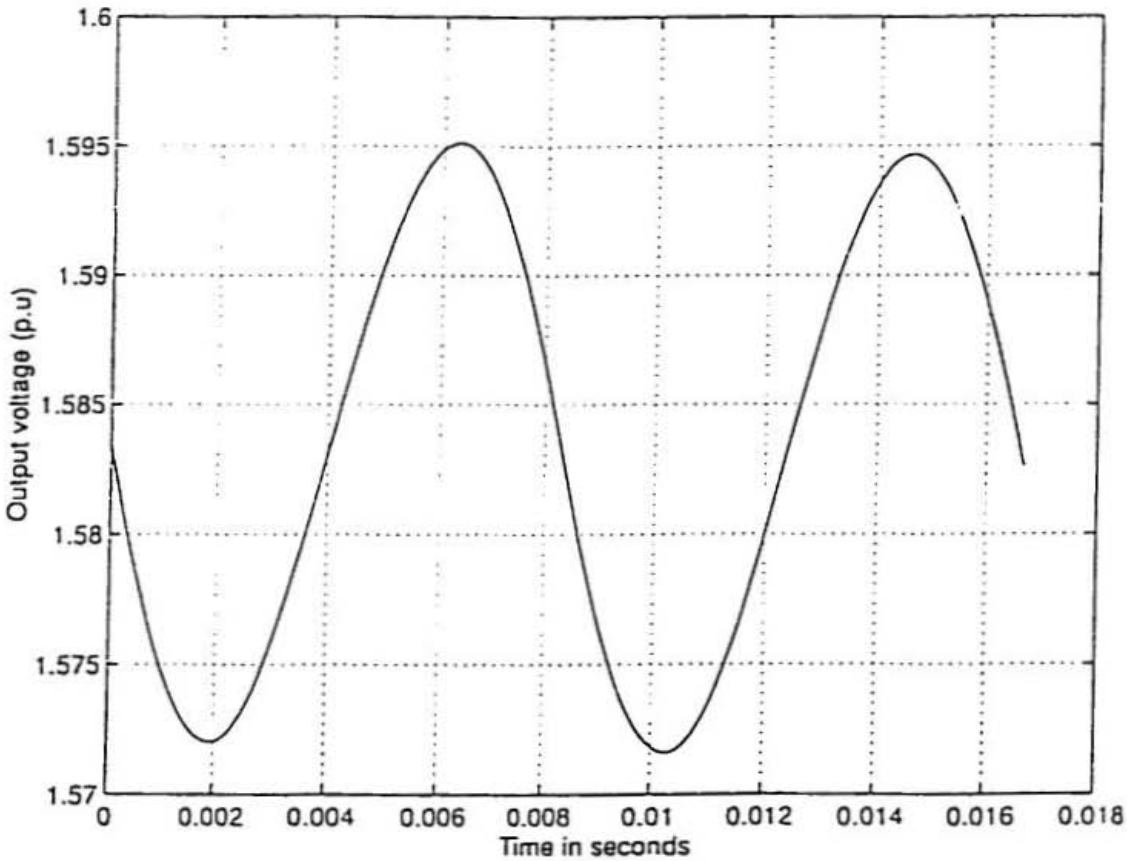


Figure 2.13 : Per-unit output voltage waveform

(L = 1.5mH, C = 470 μF , F_s = 100kHz)

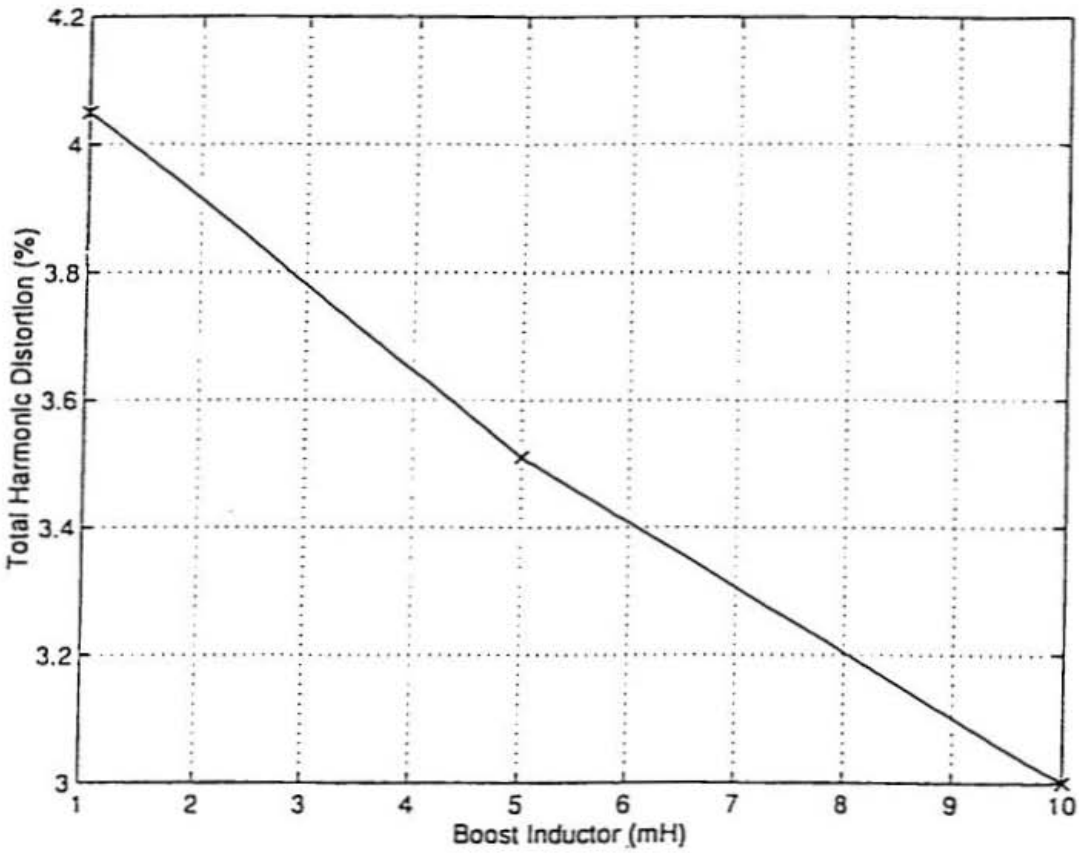


Figure 2.14 : THD of the source current versus varying boost inductor

(C = 470 μF , F_s = 100kHz)

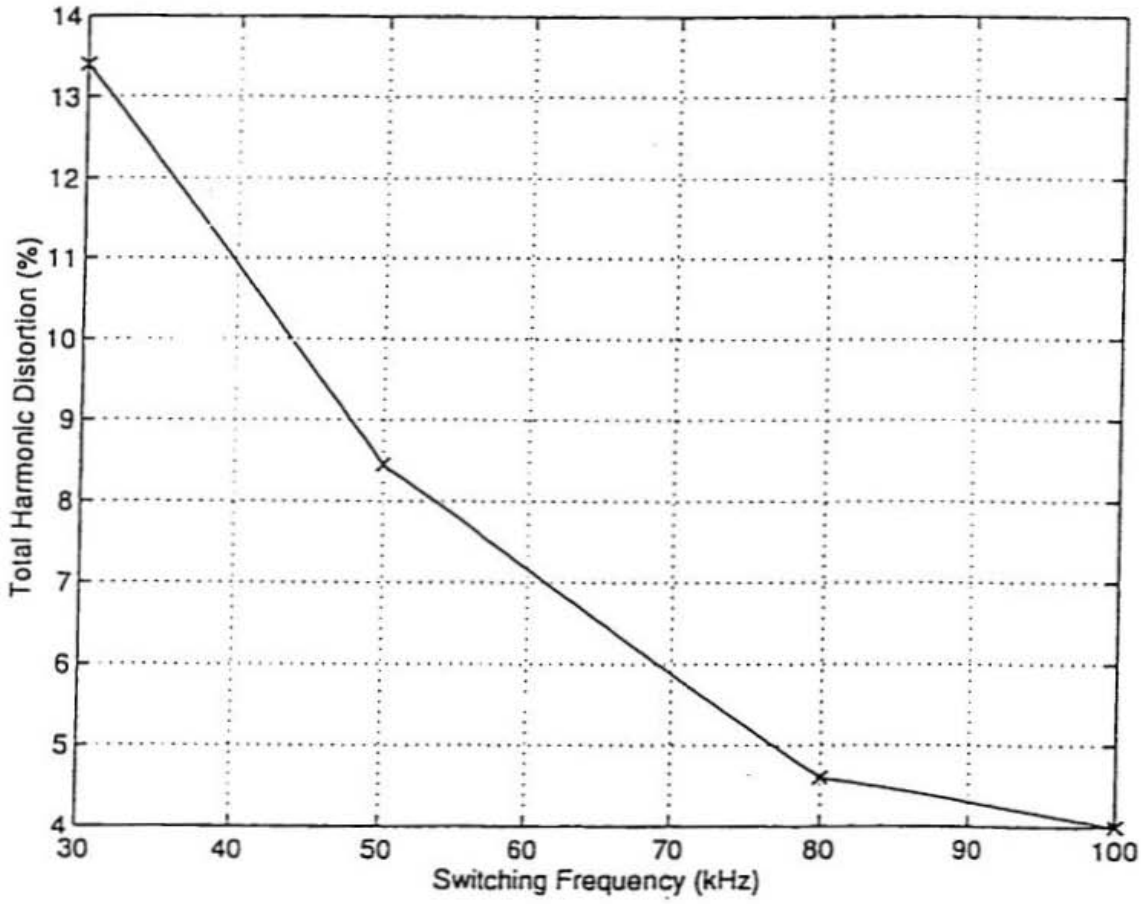


Figure 2.15 : THD of the source current versus varying switching frequency

(L = 1.5 mH, C = 470 μF)

It can be seen that at constant switching frequency the THD decreases for increasing values of the boost inductor. Increasing values of boost inductor decreases the instantaneous input current value which in turn decrease the THD. It can be seen from fig 2.15 that for a given boost inductor, the THD decreases with increasing switching frequency. The turn ON time of the boost switch decreases with the increasing switching frequency which decreases the THD of the input current. Figure 2.16 shows the harmonic component of the input current (per-unit) with respect to the order of the harmonics.

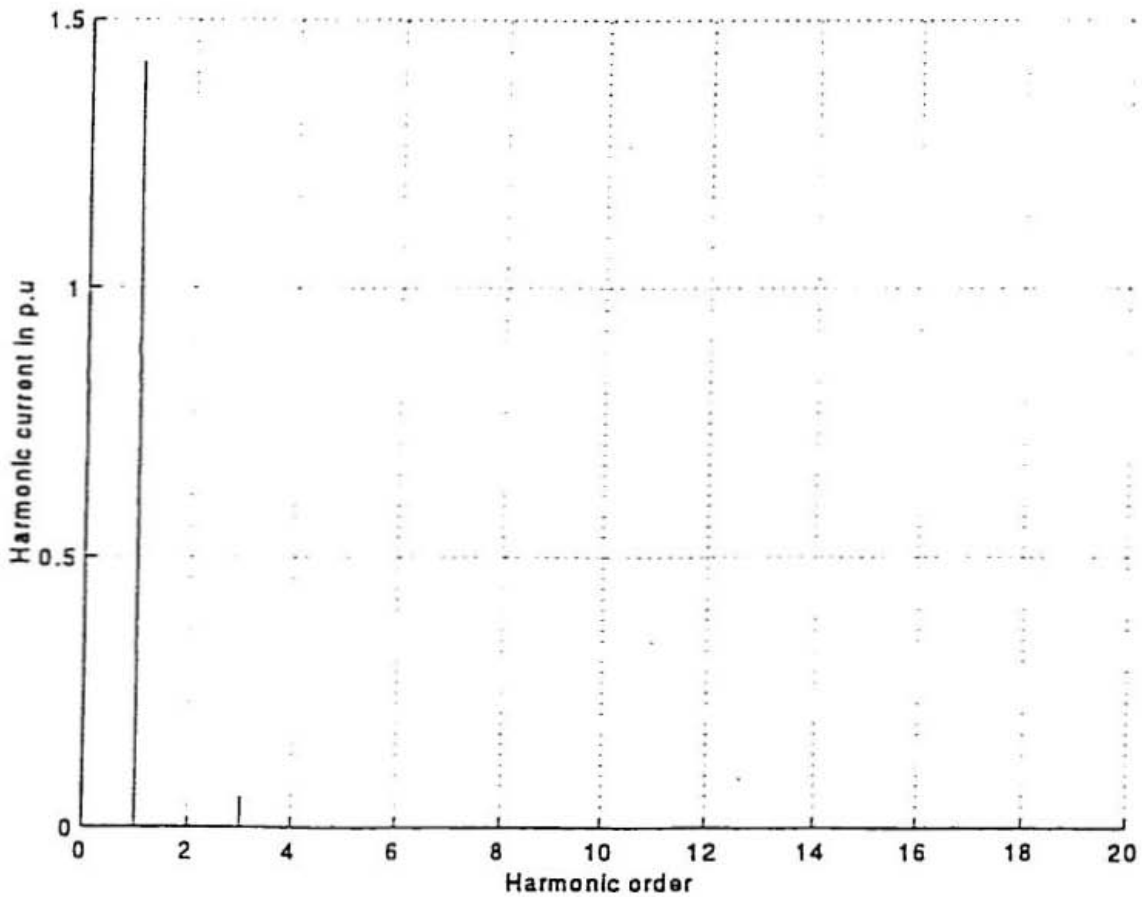


Figure 2.16 : Per-unit harmonic component of the source current versus harmonic order

(L = 1.5mH, C = 470 μF , F_s = 100kHz)

Figure 2.17 and 2.18 show the average power loss across the boost switch with respect to varying boost inductor value and switching frequency respectively. Approximate average power loss is found to be 8.31W from fig 2.17 (for L=1.5mH). It can be seen that at constant switching frequency the average power loss decreases with increasing values of the boost inductor.

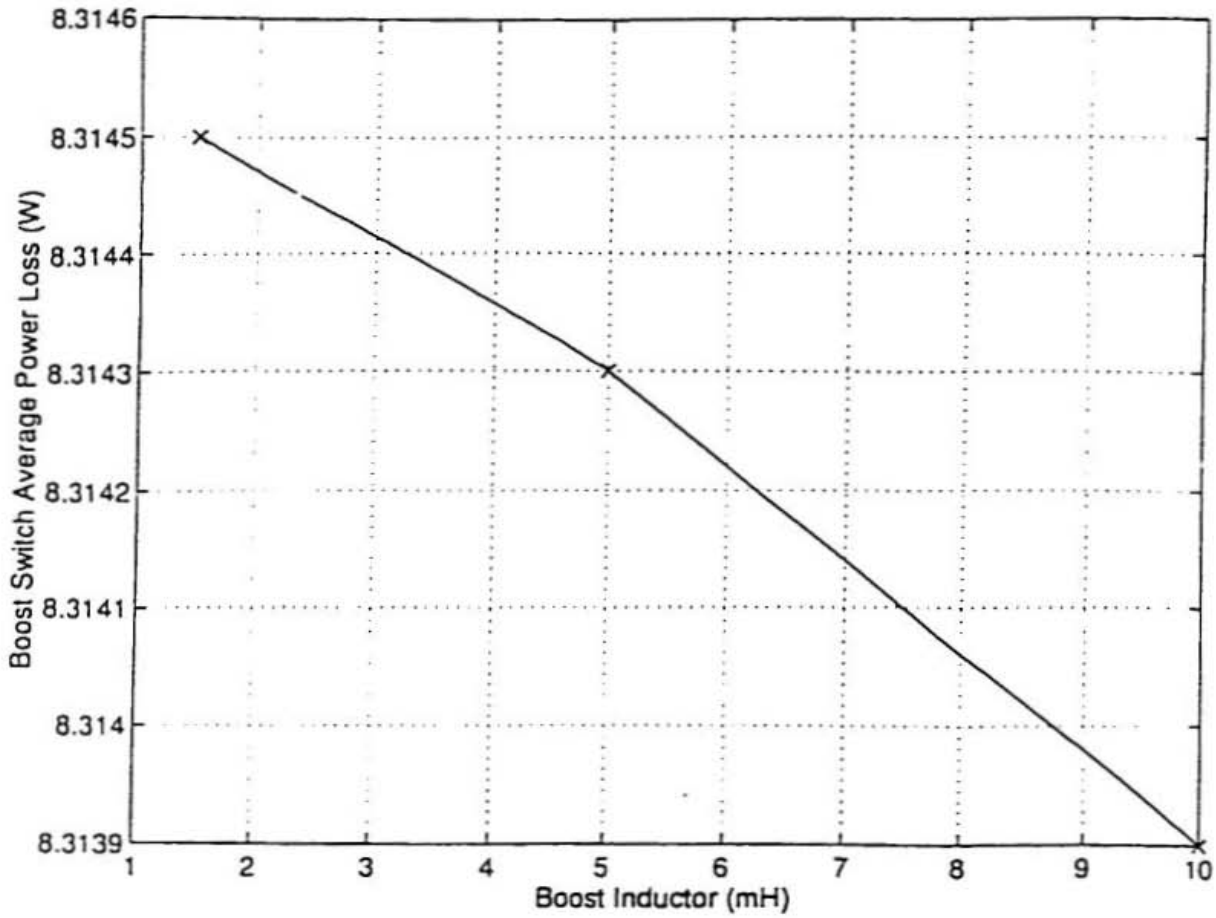


Figure 2.17: Power loss across the boost switch versus varying boost inductor

(C=470 μF , F_s=100kHz)

For a given boost inductor value the average power loss increases with increasing switching frequency. Figure 2.18 validates the equations 2.61 and 2.62, where it shows that the average power loss is proportional to the switching frequency.

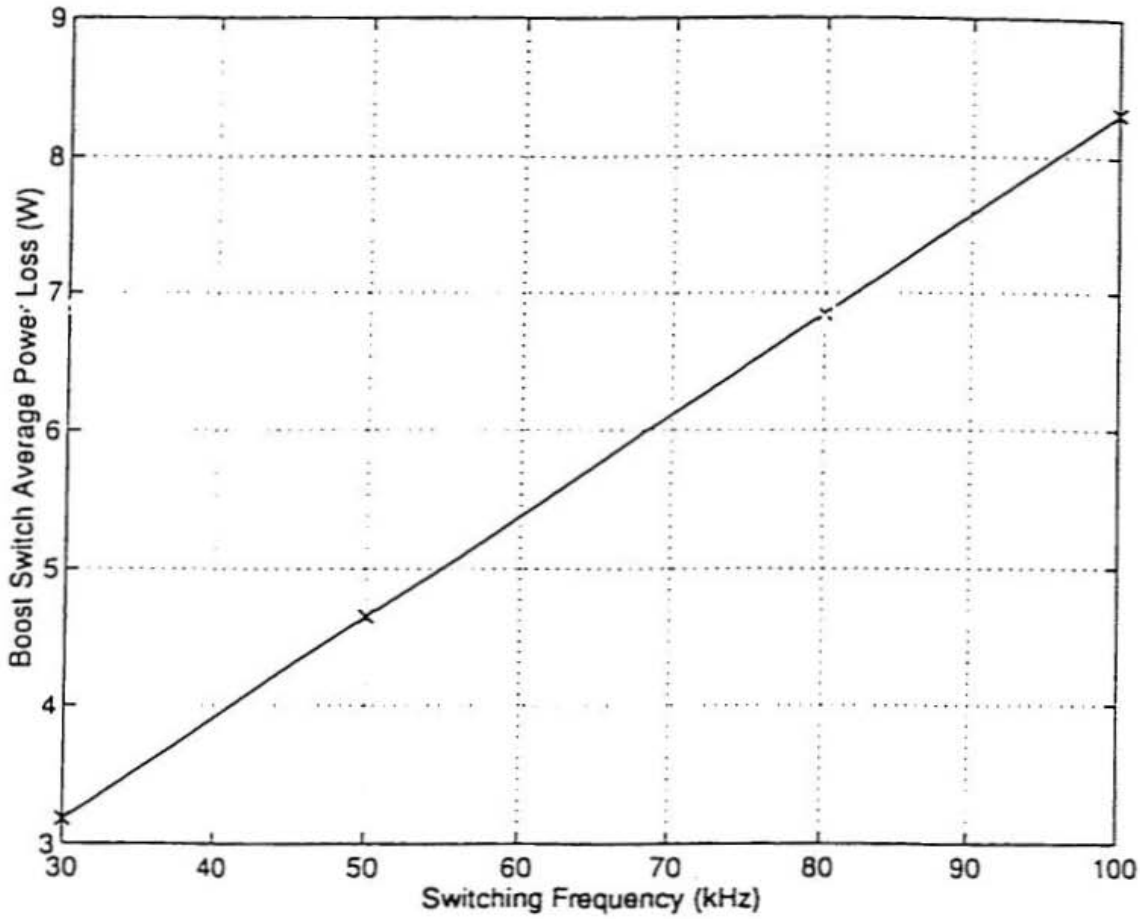


Figure 2.18: Power loss across the boost switch versus varying switching frequency (L=1.5mH, C=470 μF)

The main disadvantage of constant frequency continuous current control (CFCC) method is that there is a continuous finite value of current through and voltage across the boost switch at every switching instant. Hence, the boost switch is subjected to continuous power losses. The discontinuous current control can be implemented to minimize the continuous power losses in the switch.

2.2 CONSTANT FREQUENCY DISCONTINUOUS CURRENT CONTROL

The constant frequency discontinuous current control scheme gives a discontinuous boost inductor current at a fixed switching frequency. The inductor current is allowed to decrease to zero at the end of the OFF interval, resulting in a discontinuous inductor current. In this scheme, the duty ratio is fixed for a given output voltage and the boost switch is operated at constant frequency.

This type of current control method is also used in rectifier converter circuits to achieve a constant DC output voltage and nearly unity power factor at the input. The drawback of the constant frequency continuous current control scheme, i.e. the continuous power loss of the boost switch, can be minimized by this type of control scheme.

Fig 2.19 shows the constant frequency, discontinuous current control scheme. The actual DC output voltage is first compared with a reference through an error amplifier. The output of the error amplifier provides the reference current for the inductor current. The comparator (EA) compares the actual inductor current with the reference current.

The output of the comparator is fed to a control block, P, which performs the function of a look-up table, giving the appropriate duty cycle which corresponds to the desired minimum output capacitor voltage. The look-up table has a set of duty ratios (D), preprogrammed for varying output voltage of the error amplifier.

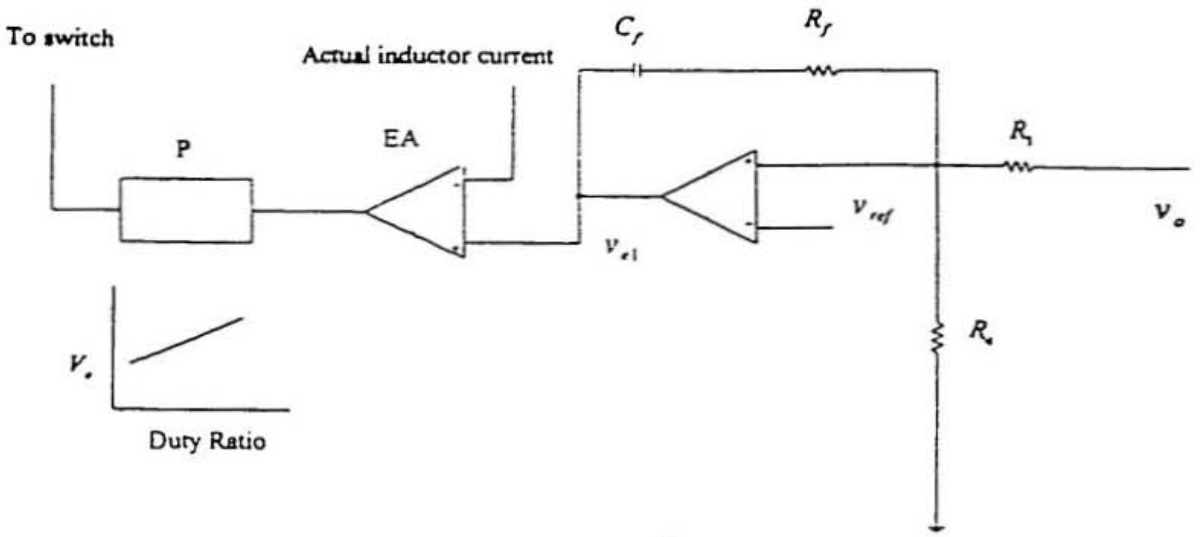


Figure 2.19: Control circuit of the CFDC control scheme

2.2.1 MODELLING AND ANALYSIS OF THE CONTROL SCHEME

This section presents the modelling and analysis of the CFDC control scheme during the ON/OFF time of the boost switch (S). The peak current value during each ON interval is proportional to the average value of the input voltage during the same ON interval. Since the average value of the input voltage varies sinusoidally, the peak value of the input current peak also varies sinusoidally. In the analysis of the control scheme, the resistances associated with the boost inductor and the output capacitor are neglected.

2.2.1.1 THE ON STATE

During the ON time of the boost switch (S) the input current (i_L) rises at the rate determined by the source voltage (v_i) and the boost inductor (L). Figure 2.20(a) shows the equivalent circuit when the boost switch is ON. The inductor current during this period ($t_0 \le t \le t_1$) is given by,

$$V_i \sin(\omega t) = L\frac{di_L}{dt} \tag{2.65}$$

On solving equation 2.65 for i_L and substituting the initial conditions, $i_L(\omega t_0) = 0$

$$i_L(\omega t) = \frac{V_i}{\omega L}\left[\cos(\omega t_0) - \cos(\omega t\ )\right] \tag{2.66}$$

where

t_0 is the instant at which the boost switch is turned ON

t_1 is the instant at which the boost switch is turned OFF

V_i is the amplitude of the input voltage

The most critical point of the design is when the switching occurs at the peak input voltage. Under this condition the current through the boost switch increases to its maximum at the end of t_1. Also under this condition the time required for the inductor current to fall to zero is maximum.

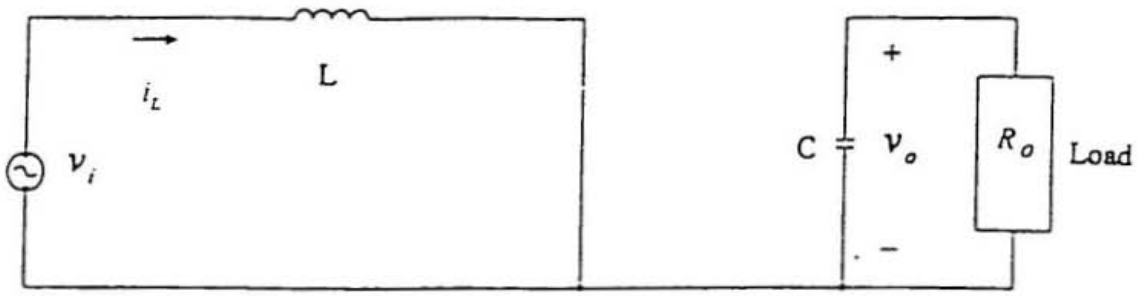


Figure 2.20(a): Equivalent circuit during the ON state

Substituting $\omega t_0 = 90^{\circ}$ and $\omega t = (90^{\circ} + \omega t)$ in equation 2.66, yields

$$i_L(\omega t) = \frac{V_i}{\omega L}\sin(\omega t) \qquad (2.67)$$

Normally the ON time period (t_1) is small in comparison with the input voltage time period. For small values of ωt, equation 2.67 reduces to

$$i_L(\omega t) = \frac{V_i}{L} t \qquad 0 \le t \le t_1 \tag{2.68}$$

At time t_1 the inductor current reaches its maximum value and the boost switch is turned OFF.

The output dc voltage depends on the average inductor current, which in turn depends on the AC input voltage and the value of the boost inductor. The desired output voltage can be maintained constant by varying the duty ratio and keeping the switching frequency constant. However, the frequency of the boost switch is a function of the AC input voltage and output DC voltage.

2.2.1.2 THE OFF STATE

During the period when the boost switch (S) is OFF the current through the inductor decreases at a rate proportional to the difference between the output voltage and the input voltage. Based on the DC voltage gain of the boost converter, the rectifier input phase voltage (v_r) is given by

$$v_r(\omega t) = \frac{1}{1-D} v_i(\omega t) \tag{2.69}$$

Figure 2.20(b) shows the equivalent circuit when the boost switch is OFF.

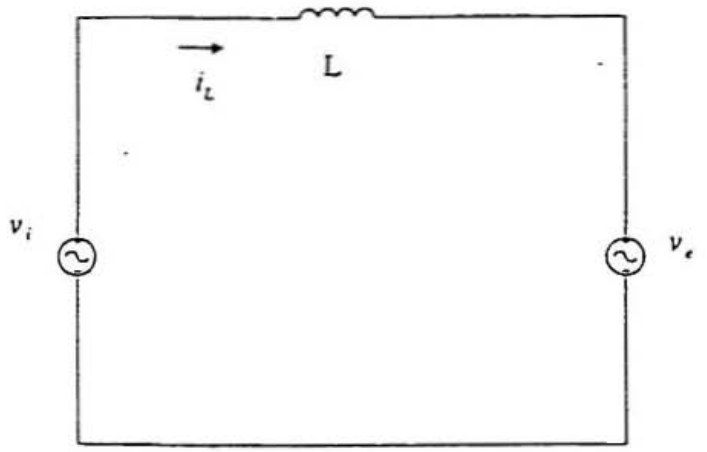


Figure 2.20(b): Equivalent circuit showing v_e during the OFF state

During the OFF period ($t_1 \le t \le t_2$), the following equation represents the current through the inductor.

$$V_i \sin(\omega t) = L\frac{di_L}{dt} + v_e \tag{2.70}$$

Solving equation 2.70 and substituting the initial condition $i_L(\omega t)\big|_{t_1} = i_L(\omega t_1)$ gives

$$i_L(\omega t) = \frac{V_i}{\omega L}\left[\cos(\omega t_1) - \cos(\omega t)\right] - \frac{v_e}{L}(t - t_1) \tag{2.71}$$

For operation at the peak of the input voltage, equation 2.71 can be written as

$$i_L(\omega t) = \frac{V_i}{\omega L}\sin(\omega t) - \frac{V_e}{L}(t - t_1) \tag{2.72}$$

For small values of ωt, equation 2.72 reduces to

$$i_L(\omega t) = \frac{V_i}{L}t - \frac{V_e}{L}(t - t_1) \qquad t_1 \le t \le t_2 \tag{2.73}$$

At $t = t_2$, the inductor current goes to zero, and substituting this condition into equation 2.73 yields

$$\frac{t_2}{t_1} = \frac{V_e}{V_e - V_i} \tag{2.74}$$

From equation 2.74 the duty ratio, D for a constant DC power output at the peak input voltage can be obtained from the following equation

$$D = \frac{V_e - V_i}{V_e} \tag{2.75}$$

For a given DC power output and input voltage, the boost inductor current can also be determined. Knowing the duty ratio, boost inductor current, input voltage and boost inductor value the ON time period can be obtained from equation 2.68 as

$$t_{on} = t_1 = \frac{i_L(\omega t_1).L}{V_i} \tag{2.76}$$

The OFF time period can then be expressed as

$$t_{off} = \frac{t_{on}.(1-D)}{D} \tag{2.77}$$

The switching frequency is then calculated as

$$F_S = \frac{1}{T_s} = \frac{1}{t_{on} + t_{off}} = \frac{1}{\left(\frac{i_L(\omega t_1).L}{V_{in}}\right) + \left(\frac{t_{on}(1-D)}{D}\right)} \tag{2.78}$$

Figure 2.21 shows the theoretical input current waveform of the discontinuous current scheme.

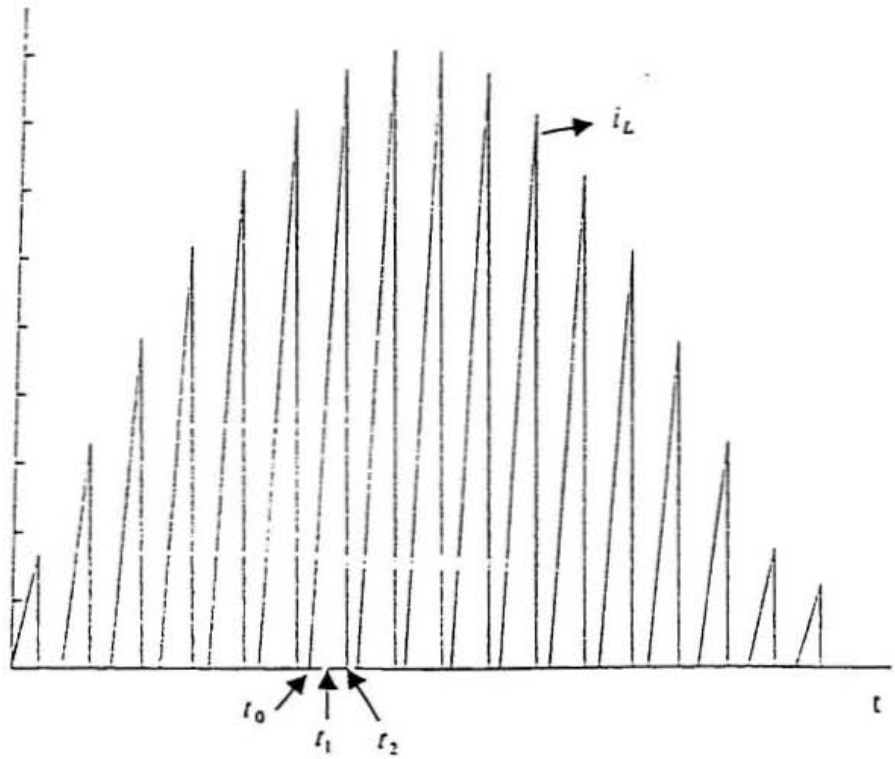


Figure 2.21: Theoretical input current waveform of the CFDC control scheme

2.2.2 DESIGN EXAMPLE

To ensure a fair comparison between the constant frequency continuous current (CFCC) and the constant frequency discontinuous current (CFDC) control methods, the source voltage, frequency of operation of the boost switch, output power and output voltage values used in the CFCC scheme are employed for the CFDC scheme. In the CFDC scheme, the duty ratio is maintained constant and the general procedure for finding the boost inductor value is as follows.

To determine the value of the boost inductor, the desired maximum (peak) average input current is first calculated. The desired fundamental peak average input I_{av}(max) at the maximum line voltage (i.e. 240 V_{rms}) is obtained as

$$I_{av}(\max) = \frac{P_o}{V_{in}(rms)}.\sqrt{2} = \frac{400}{240}.\sqrt{2} = 2.36A \tag{2.79}$$

To maintain the fundamental peak average current, $I_{av}(\max)$ of 2.36A at the line voltage of 240 V (rms), the maximum value of the instantaneous input current (i_L) flowing through the boost inductor is approximated to be 3.34A (i.e $\sqrt{2} * 2.36$). The supply voltage v_i is assumed to be constant over one switching cycle. The approximate duty ratio at the peak source voltage is calculated from equation 2.75 to be 0.1 (with $V_o = 380V$ and $V_i = 240 * \sqrt{2}$ V).

At the end of the ON period, the inductor current is given by

$$i_L(\omega t) = \frac{V_i}{L} t_{on} \tag{2.80}$$

For a switching frequency of 100 kHz, and duty ratio of 0.1, the boost inductor value is obtained from equation 2.80 as

$$L = \frac{V_i}{i_L(\omega t)} t_{on} = \frac{V_i}{i_L(\omega t)} * D * T_S = \frac{240\sqrt{2} * 0.1 * 10\mu}{3.34} = 0.101mH \tag{2.81}$$

From the above design procedure the value of the boost inductor is chosen to be 0.1 mH. The value of the output capacitor is obtained from the procedure outlined in section 2.1.4. Assuming the peak-to-peak ripple voltage of the capacitor to be 1.2%, i.e. a voltage of magnitude 4.56V is expected over the steady DC output voltage of 380V, the output capacitor is calculated to be $410\mu F$. A conservative value of $470\mu F$ for the output capacitor is chosen for the simulation of the circuit.

2.2.3 SIMULATION OF THE PFC CIRCUIT FOR THE DISCONTINUOUS CURRENT MODE CONTROL

As in the CFCC control scheme, the CFDC control scheme is simulated for two values of switching frequency (100KHz and 5KHz). The waveforms for the 5KHz operation are given to show the details of the operation of the circuit. The procedure outlined in the previous section is used to determine the circuit parameters at the two frequencies, which are as follows.

Line voltage, $V_i = 240\,V(rms)$

Line frequency, $f_i = 60$Hz

Output Voltage, $V_o = 380$V(dc)

Output power, $P_o = 400$W

Switching frequency, $F_s = 100$kHz

Boost inductor, L = 0.1mH

Output capacitor, C = 470 μF

Line voltage, $V_i = 100\,V(rms)$

Line frequency, $f_i = 60$Hz

Output Voltage, $V_o = 200$V(dc)

Output power, $P_o = 160$W

Switching frequency, $F_s = 5$kHz

Boost inductor, L = 2.2mH

Output capacitor, C = 1000 μF

Per-unit values

1 p.u voltage = 240V

1 p.u power = 400W

1 p.u current = $\frac{400}{240} = 1.67$ A

1 p.u voltage =100V

1 p.u power = 160W

1 p.u current = $\frac{160}{100} = 1.6$ A

2.2.3.1 SIMULATION PROCEDURE

The flow chart of the complete simulation procedure of the CFDC control is shown in fig 2.22. MATLAB is used to simulate the design equations.

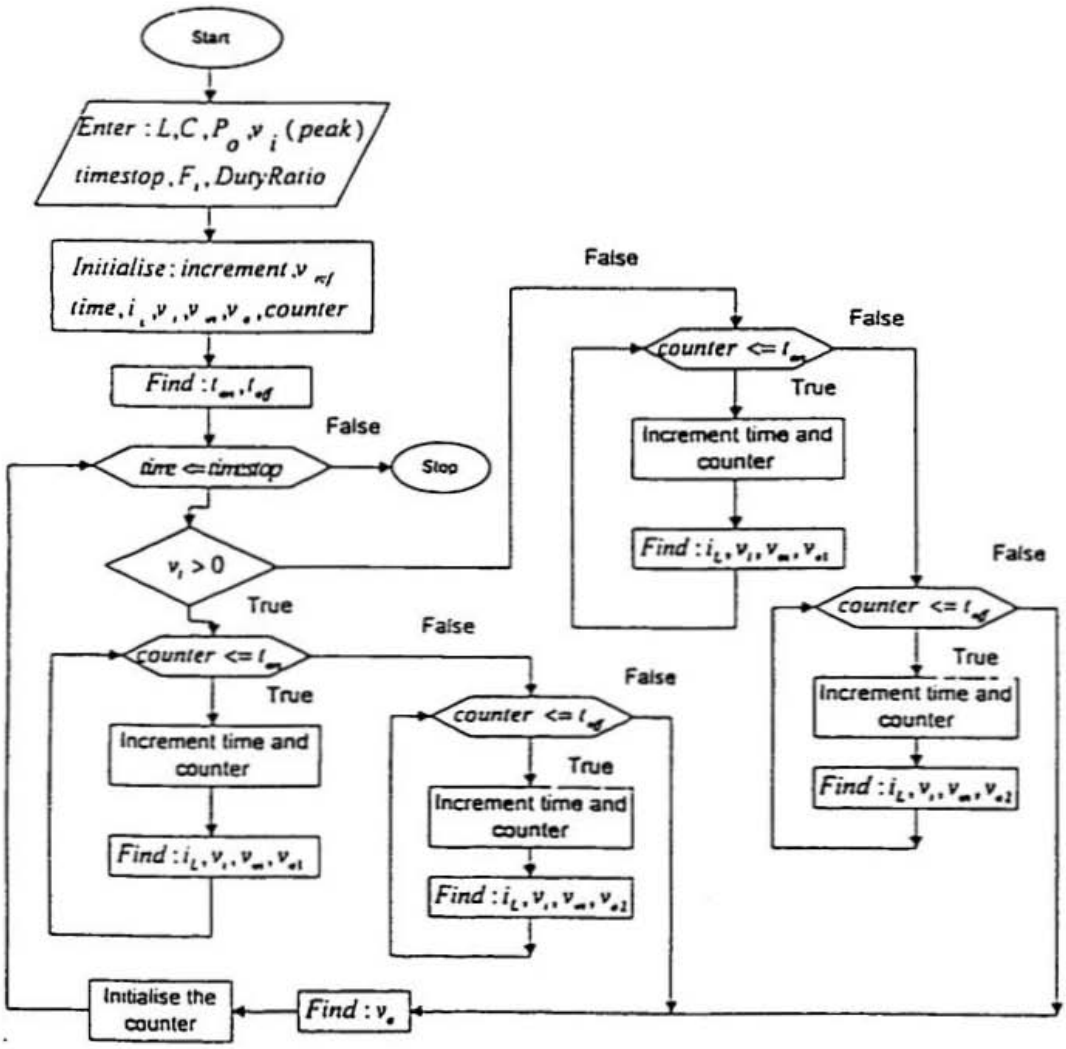


Figure 2.22 : Flow chart of the CFDC control scheme showing the simulation procedure

2.2.3.2 SIMULATION RESULTS

Figures 2.23 and 2.24 show the source current and source voltage in per unit at 100KHz and 5KHz. This control scheme is also capable of producing nearly sinusoidal input current waveform.

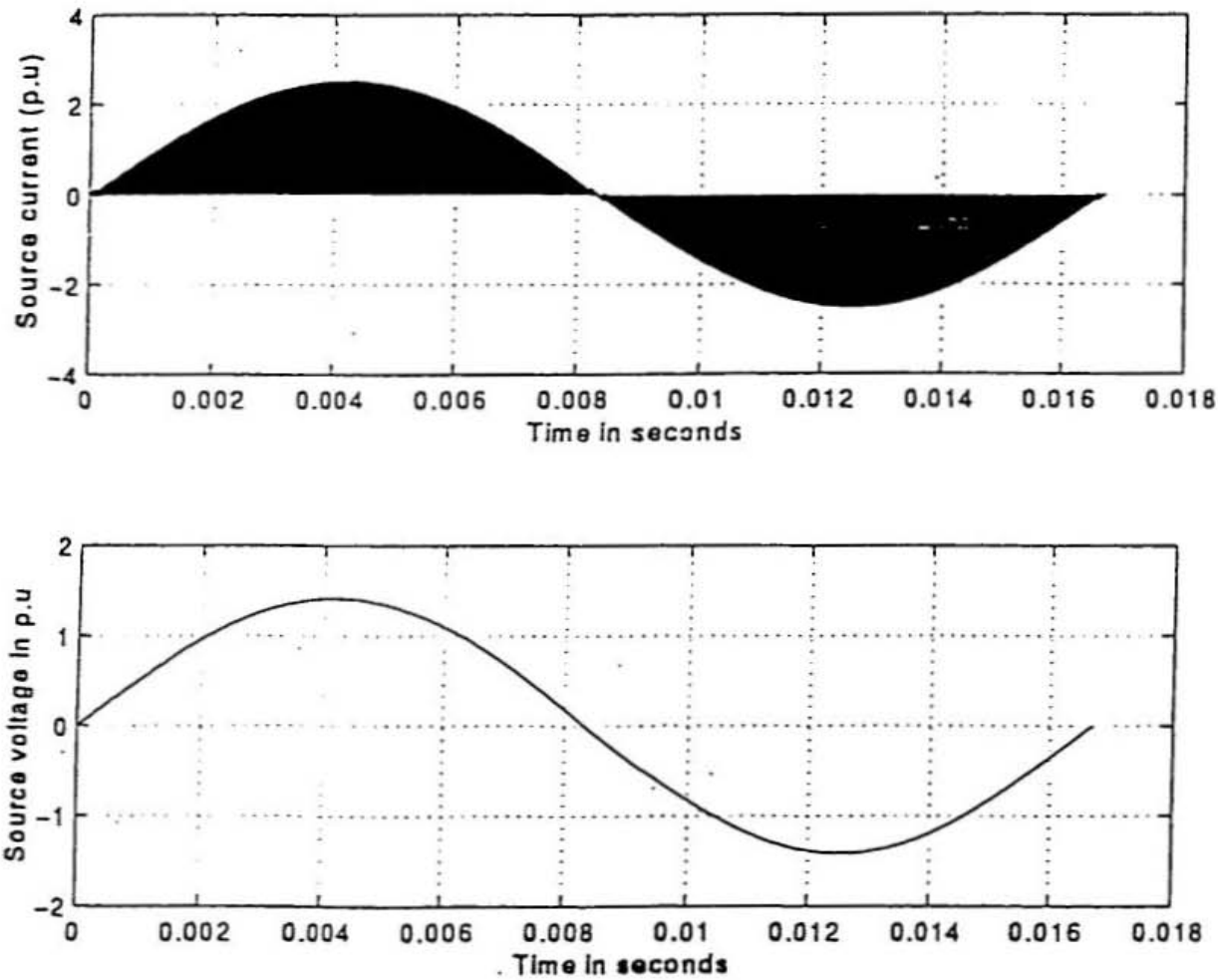
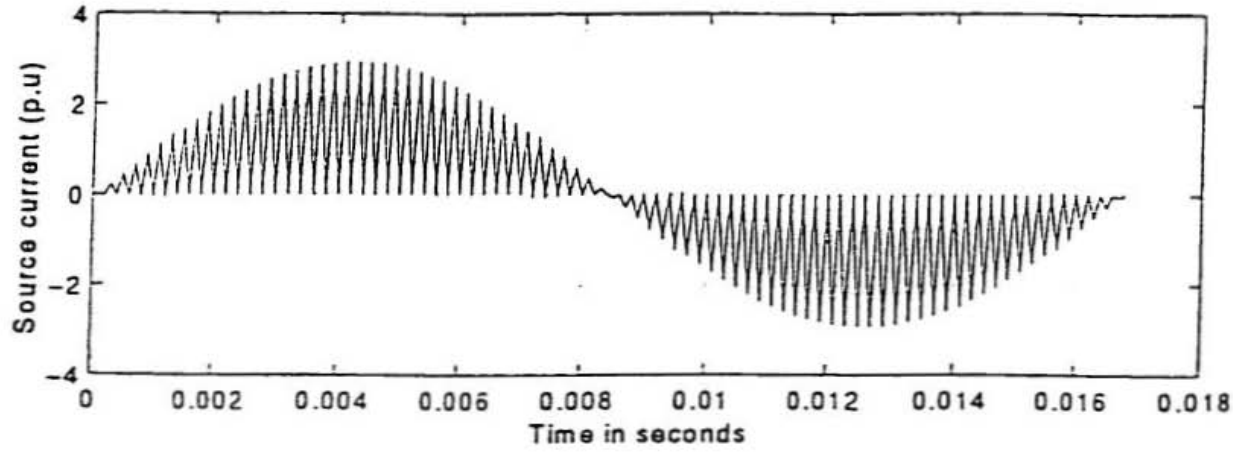


Figure 2.23 : Per-unit source current and source voltage waveforms

(L = 0.1mH, C = 470 μF , F_i = 100kHz)



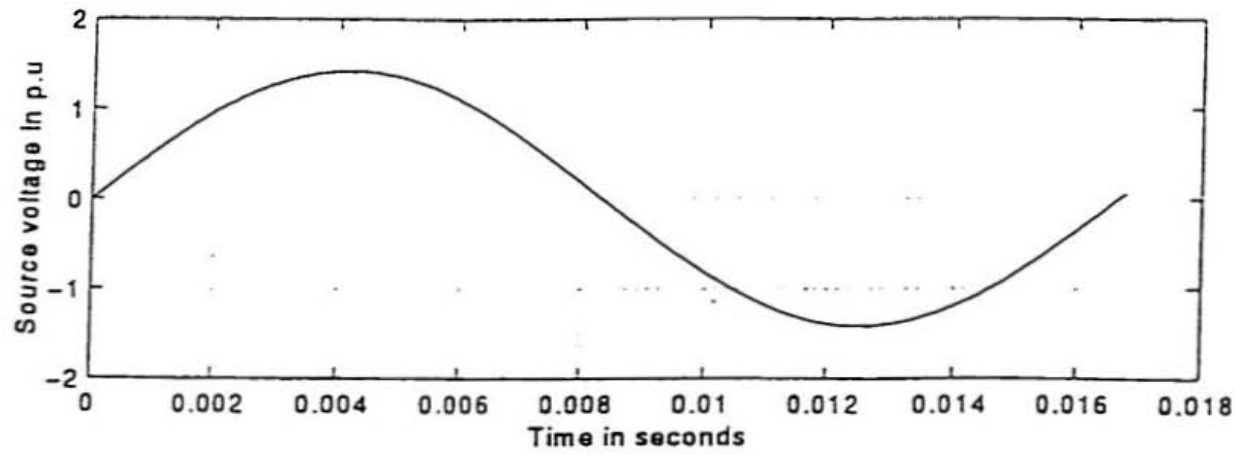


Figure 2.24 : Per unit source current and source voltage waveforms

(L = 2.2mH, C = 1000 μF , F_r = 5kHz)

The total harmonic distortion (THD) of the source current for fig 2.23 is calculated to be 5.1% and the peak-to-peak output voltage ripple for fig 2.25 is found to be 1.7%. Figure 2.25 shows the per-unit output voltage ripple of the CFDC control scheme. Figure 2.26 and 2.27 show the plots of the total harmonic distortion (THD) of the input current with respect to varying boost inductor value and switching frequency respectively.

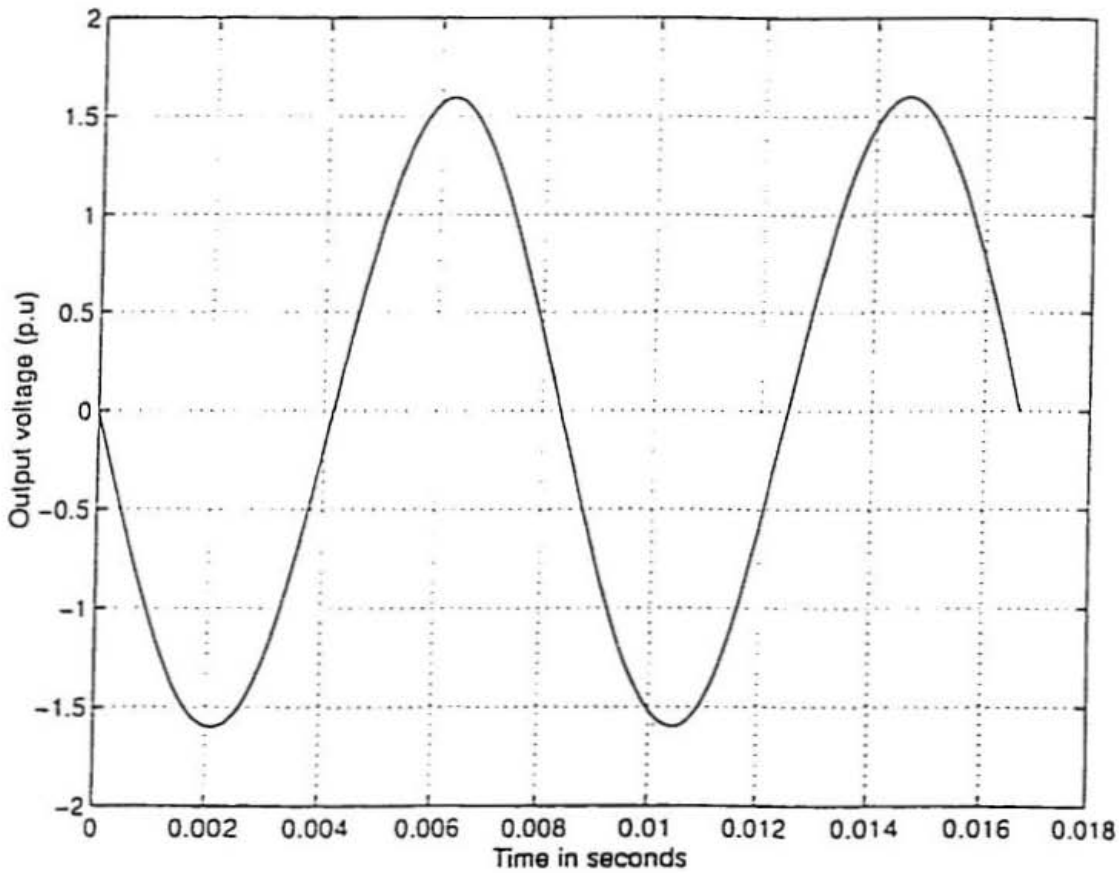


Figure 2.25 : Per-unit output voltage waveform

(L = 0.1mH, C = 470 μF , F_s = 100kHz)

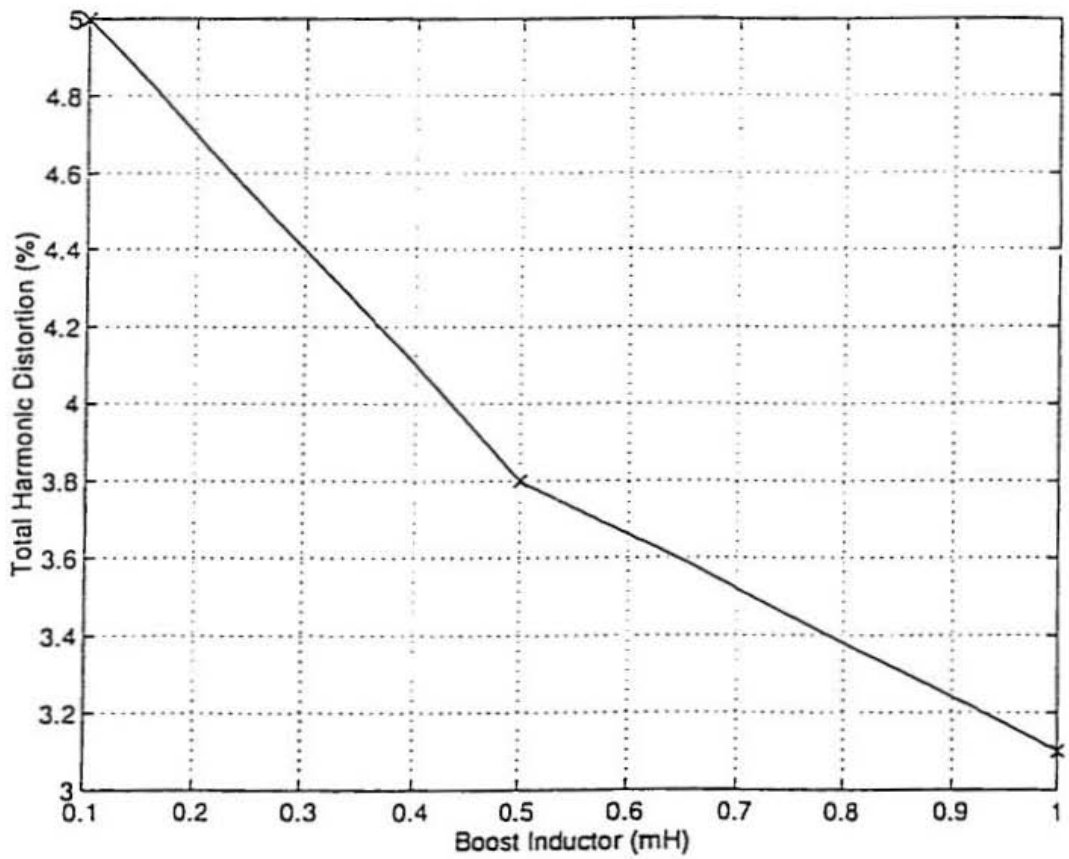


Figure 2.26 : THD of the input current versus varying boost inductor

($C = 470\,\mu F$, F_s = 100kHz)

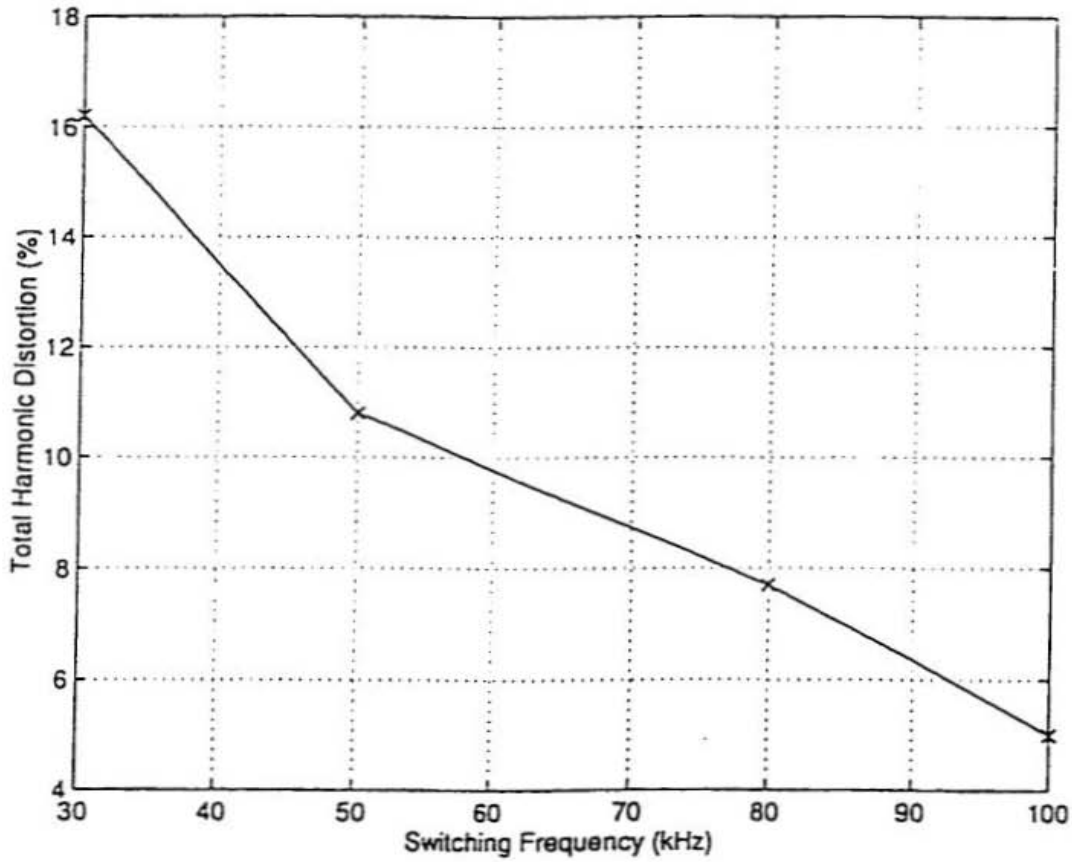


Figure 2.27: THD of the input current versus varying switching frequency

($L = 0.1\text{mH}, C = 470\,\mu F$)

It can be seen that at constant switching frequency the THD decreases for increasing values of the boost inductor. For a given boost inductor, the THD decreases with increasing switching frequency. Higher values of boost inductor and switching frequency decrease the instantaneous value of the input current and the turn ON time respectively, which decrease the total harmonic distortion. Figure 2.28 shows the harmonic component of the input current (per-unit) with respect to the order of the harmonics. The spectrum reveals that higher order harmonics are present in the input current. These harmonics occur at multiples of the switching frequency.

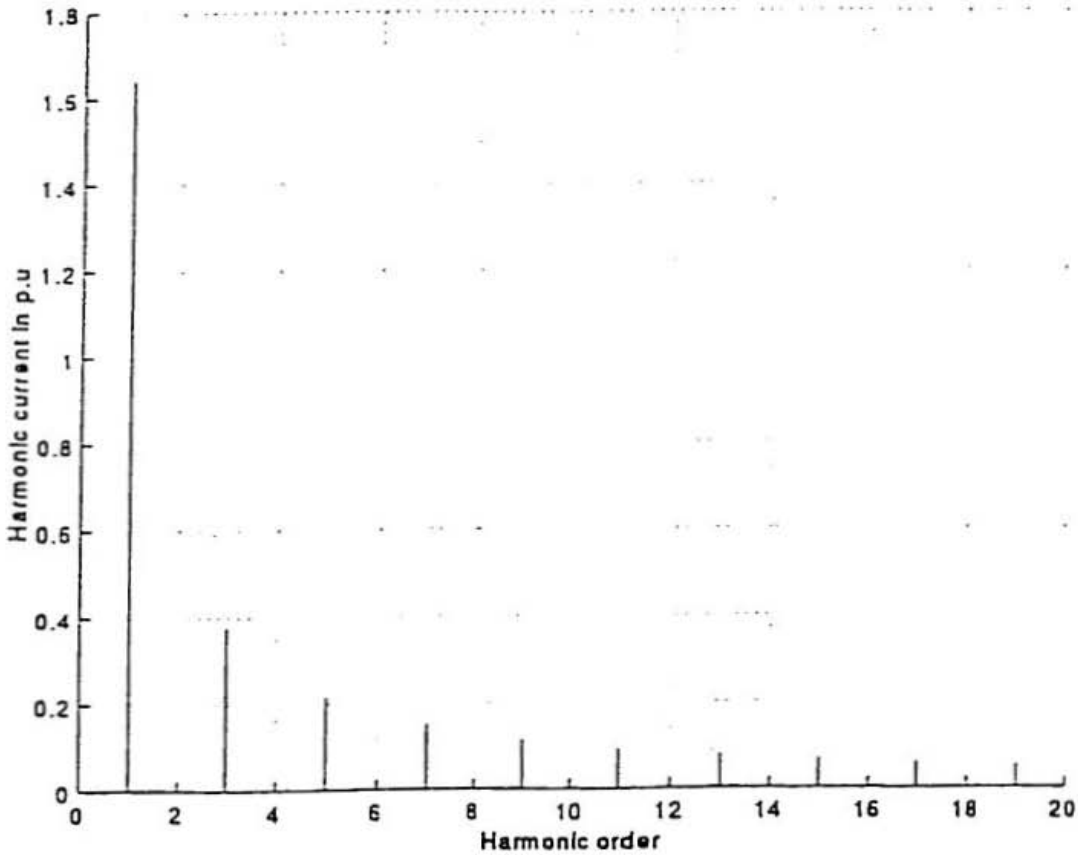


Figure 2.28 : Per-unit harmonic component of the input current versus harmonic order

($L = 0.1\text{mH}, C = 470\,\mu F$, $F_s = 100\text{kHz}$)

Figure 2.29 and 2.30 show the average power loss across the boost switch with respect to varying boost inductor value and switching frequency respectively. It can be seen from fig 2.29 that the average power loss is approximately 6.04W [for L=0.1mH]. At constant switching frequency the average power loss decreases with increasing values of the boost inductor. Figure 2.30 shows that for a given boost inductor value the average power loss increases with increasing switching frequency.

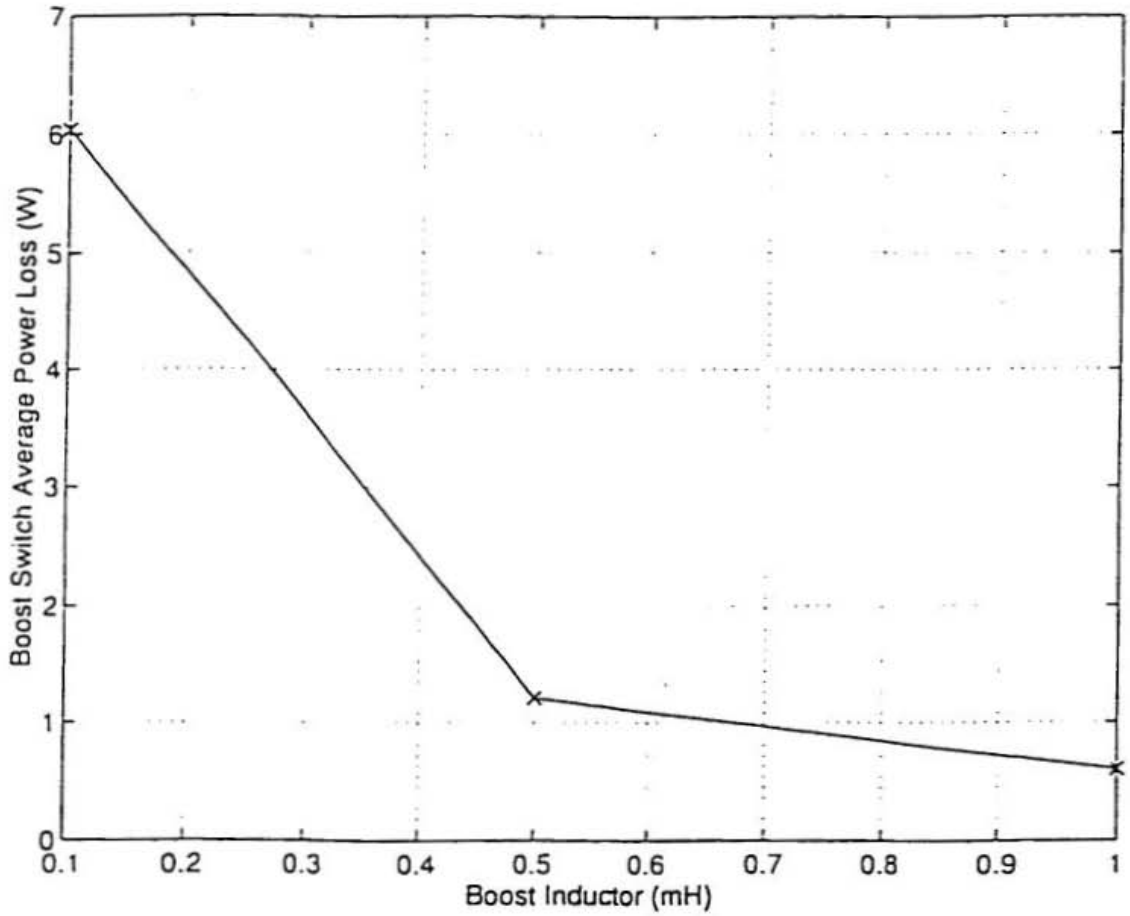


Figure 2.29: Power loss across the boost switch versus varying boost inductor

(C=470 μF , F_s=100kHz)

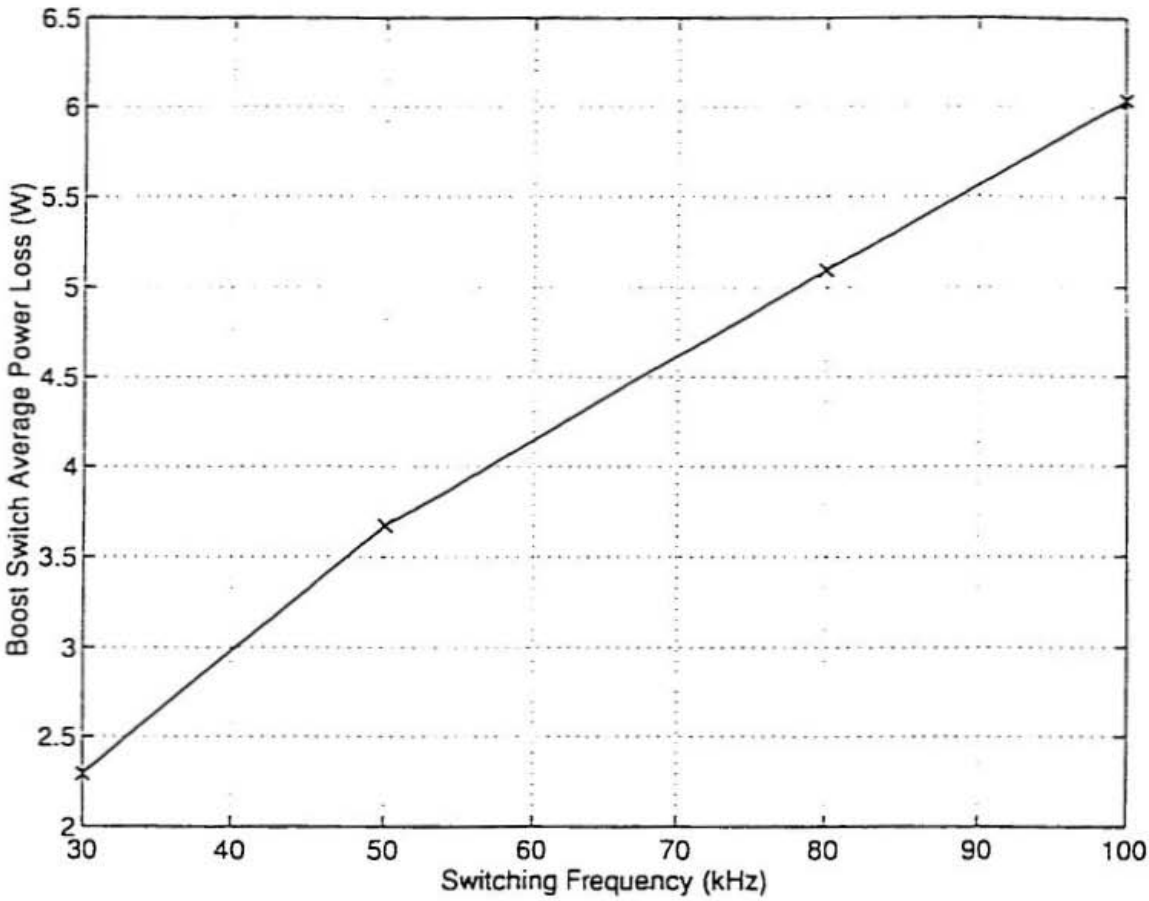


Figure 2.30: Power loss across the boost switch versus varying switching frequency

(L=0.1mH, C=470 μF)

2.3 SUMMARY

The simulation results confirm the operation of the control schemes. The simulated input current waveforms match the predicted theoretical waveforms for both control methods. The boost inductor and output capacitor values are designed for the same circuit conditions (input voltage, output voltage and output power).

The design examples show that for the same operating conditions, the boost inductor required for the Constant Frequency Discontinuous Current (CFDC) scheme is smaller compared to the inductor in the Constant Frequency Continuous Current (CFCC) scheme. Comparing the harmonic spectra of the CFCC and CFDC control methods it can be seen that the CFDC control generates higher order harmonics in the input current waveform and hence the total harmonic distortion (THD) is also higher. Keeping the boost inductor value constant for both the control schemes, simulation results show that THD tends to decrease with increasing switching frequency. Although the THDs are within established standards, additional filtering of the input current harmonics can be achieved with an input low pass filter.

The major drawback of the CFCC control is the continuous power loss of the boost switch, as the current through the boost inductor never goes to zero except at the zero crossings of the input voltage. This drawback is overcome in the CFDC control scheme where the inductor current is forced to go to zero at the end of the OFF interval of the boost switch. Simulation results show that the average power loss across the boost switch for the CFCC scheme is higher than that of the CFDC scheme. The average power

loss tends to decrease with increasing boost inductor value. An increase in the boost inductor value at fixed switching frequency, decreases the instantaneous value of the input current. However, increasing the switching frequency at fixed boost inductor value, increases the average power loss.

Although the power loss in the boost switch is minimized in the CFDC scheme there is a high current stress associated with the boost switch at the peak input voltage. The high current stresses and the high di/dt of the input current implies that a substantial size of EMI filter is required for the CFDC control scheme.

The control circuit of CFCC has three feedback loops in the outer voltage control loop and so requires additional circuitry for synchronization. In contrast, the CFDC control scheme requires only one feedback loop in the control circuitry and it does not require a synchronization logic.

Based on the characteristics presented in this chapter, the power factor correction circuit with the CFDC control scheme is likely to be smaller in size, efficient and less costly.

Chapter 3

VARIABLE FREQUENCY CONTROL SCHEME

INTRODUCTION

So far, this thesis has dealt with the modelling and analysis of constant frequency current control methods. However, the ON/OFF sequence of the boost switch can also be operated in variable frequency mode. The constant frequency control scheme, such as the CFCC control uses complex control logic circuitry to control the total harmonic distortion of the input current waveform. The control circuit complexity can be minimized by using variable frequency control method. This chapter deals with the modelling, analysis and simulation of the variable current hysteresis control (VCHC) scheme used in power factor correction circuits. The modelling and analysis has been done using equivalent circuit representation of the various states of the boost switch. Analytical expressions describing the boost inductor current and output voltage in steady state operation are then formulated from the equivalent circuits. These equations are simulated using MATLAB [36] to obtain the performance characteristics of the control scheme.

3.1 THE VARIABLE CURRENT HYSTERESIS CONTROL SCHEME FOR PFC CIRCUITS

This control scheme gives a continuous boost inductor current at a variable switching frequency. In this scheme [27] the boost inductor current magnitude is varied between an upper and lower boundary limits around the inductor current. The duty ratio of the boost switch is determined by comparing the actual inductor current between the two boundary limits, namely I_u and I_l , with a hysteresis comparator. These current limits are in phase with the source voltage. Here, the inductor current is compared with the control signal (in case of voltage-regulated converters, this is the amplified voltage-error signal, v_{el}) and the decision-making hysteresis block turns OFF the boost switch when the increasing inductor current reaches the upper boundary limit (I_u). The boost switch is turned ON when the inductor current reaches the lower boundary limit I_l. In this way the line current is confined between two sinusoidal current limits. The peak difference between the upper and lower current limits is referred to as the hysteresis band δ. Figure 3.1 shows the control circuit diagram of the variable current hysteresis control method.

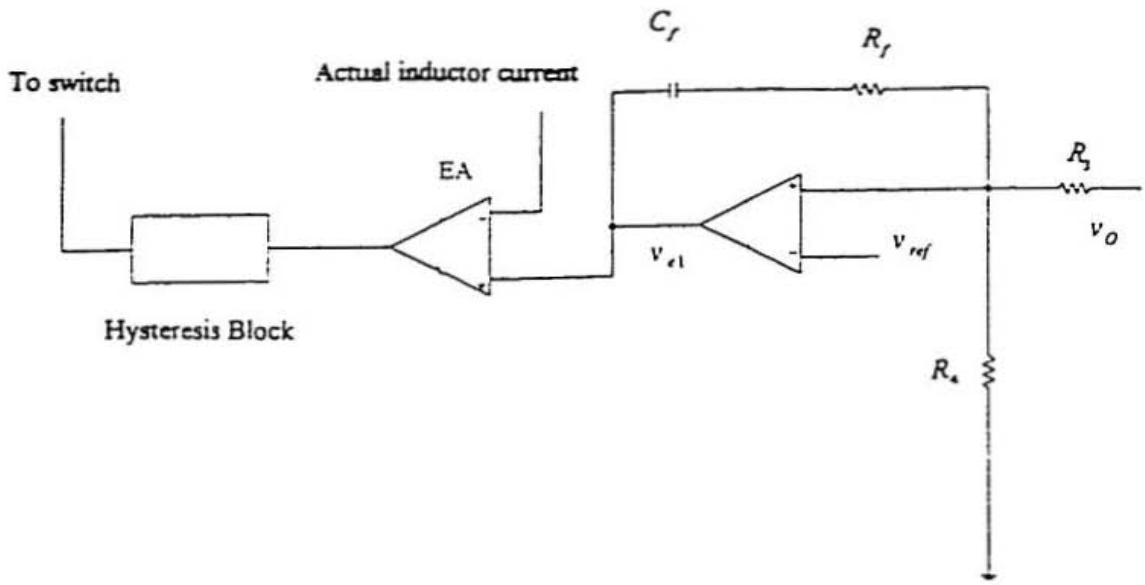


Figure 3.1: Control circuit of the VCHC scheme

3. 2 MODELLING AND ANALYSIS OF THE PFC CIRCUIT UNDER VCHC CONTROL

This section shows the modelling and analysis of the PFC under VCHC control scheme during the ON/OFF time of the boost switch (S). When the boost inductor current magnitude falls to the lower boundary the boost switch is turned ON and it remains ON till the inductor current reaches the upper limit, when the switch is turned OFF. The two limiting currents (upper and lower) are given by

$$i_U = I_{UM} \sin \omega t \text{ and } i_M = I_{MM} \sin \omega t \tag{3.1}$$

where

$$I_{UM} - I_{LM} = \delta = \text{peak difference} \tag{3.2}$$

The line current i_L is confined between I_L and I_u and centered at the reference current

$$i_{ref} = I_{refm} \sin \omega t \tag{3.3}$$

which has an amplitude

$$I_{refm} = I_{UM} - \delta / 2 = I_{LM} + \delta / 2 \tag{3.4}$$

3.2.1 THE ON STATE

During the ON state of the switch the power circuit reduces to a series network as shown in fig 3.2.

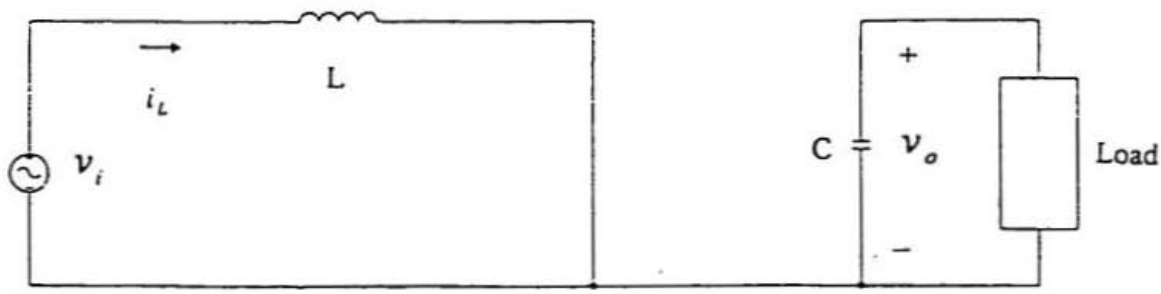


Figure 3.2 : ON state equivalent circuit

Neglecting the stray resistances of the boost inductor and the output capacitor voltage, the equations which describe the circuit are given by

$$L\frac{di_L}{dt} = v_i \tag{3.5}$$

$$C\frac{dv_c}{dt} = -\frac{v_c}{R_O} \tag{3.6}$$

where

i_L is the instantaneous inductor current

v_i is the instantaneous supply voltage

v_c is the instantaneous capacitor voltage

R_O is the load resistance

For a small time increment Δt, the inductor current i_L, capacitor voltage v_c and the supply voltage, v_i may be assumed constant and are represented as I_L, V_c and V_i respectively. Integrating equations 3.5 and 3.6 over the time increment Δt yields

$$L\frac{\Delta i_L}{\Delta t} = V_i \tag{3.7}$$

$$C\frac{\Delta v_c}{\Delta t} = -\frac{V_c}{R_O} \tag{3.8}$$

From equations 3.7 and 3.8 the inductor current and the output capacitor voltage at the end of Δt can be obtained. The time at the end of the ON state is t_{ON}.

3.2.2 THE OFF STATE

The switch is turned OFF when the inductor current reaches the upper limit of the hysteresis band. The equivalent circuit during this state is shown in fig 3.3.

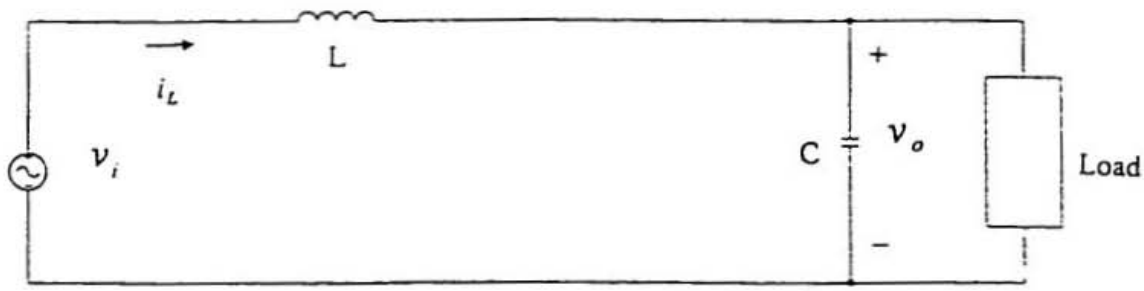


Figure 3.3 : OFF state equivalent circuit

The governing equations during this time are

$$L\frac{di_L}{dt} = v_i - v_o \tag{3.9}$$

$$C\frac{dv_c}{dt} = \frac{v_c}{R_o} \tag{3.10}$$

The inductor current and the capacitor voltage can be determined from the equations 3.9 and 3.10 for a small interval of time (Δt). The current thus obtained from equation 3.9 is then compared with the lower limit of the hysteresis band. The switch remains OFF as long as the inductor current is more than the lower boundary limit.

The time at the end of this state is the OFF time, t_{off}. The switching frequency can be calculated from the ON and OFF times as

$$F_s = \frac{1}{t_{on} + t_{off}} \tag{3.11}$$

Figure 3.4 shows the theoretical input current waveform of the VCHC control scheme. The disadvantage of the hysteresis control is that it operates at variable switching frequency (F_s). Near the zero crossing of the input voltage the ON time (t_{on}) and the OFF time (t_{off}) are very low and so the switching frequency (eqn 3.11) becomes very high, thus some means must be provided in the control circuit to limit the switching frequency near the voltage zero crossings.

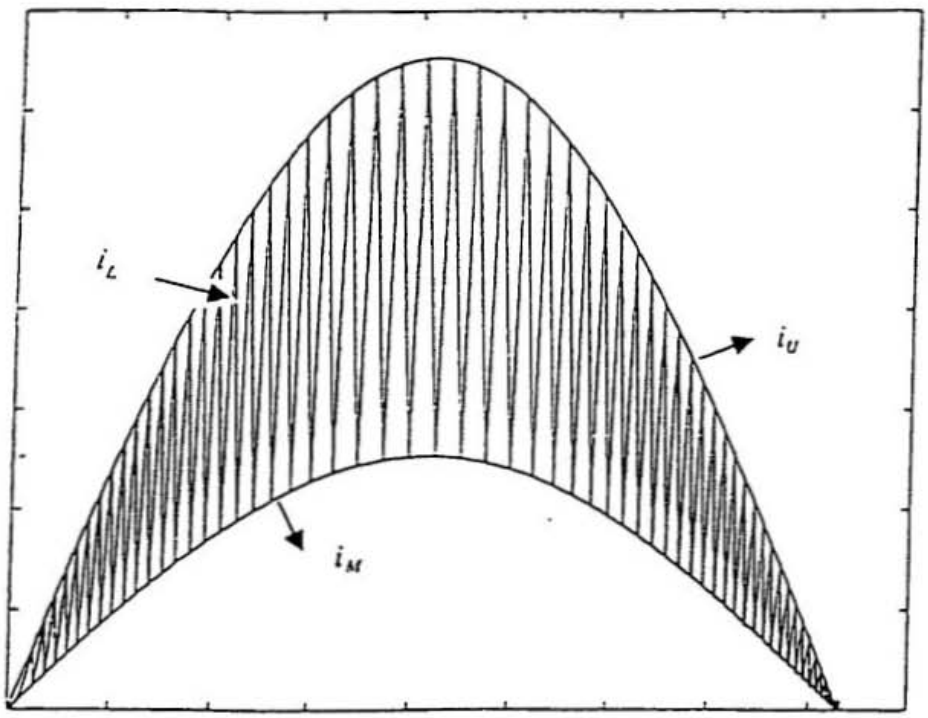


Figure 3.4 : Theoretical input current waveform of the VCHC control scheme

3.3 DESIGN EXAMPLE

For a given peak difference current (δ) of the boost inductor, if the supply voltage v_i is assumed to be constant over one switching cycle, the ON time (t_{on}) and OFF time (t_{off}) at the peak of the source voltage are obtained as

$$t_{on} = \frac{L.\delta}{V_{in}} \tag{3.12}$$

$$t_{off} = \frac{L.\delta}{V_o - V_{in}} \tag{3.13}$$

The switching time (T_s) is given by

$$T_s = \frac{1}{F_s} = t_{on} + t_{off} \tag{3.14}$$

Substituting the ON and OFF times in equation (3.14) gives

$$L = \frac{V_i.(V_0 - V_i)}{F_s.\delta.V_o} \tag{3.15}$$

The switching frequency, F_s is not constant over one cycle of operation. Equation 3.15 shows that for a fixed output voltage, given source voltage and specified peak difference current, δ , the largest value of L occurs when the switching frequency is minimum. The instantaneous switching frequency is minimum at the peak of the input voltage. Assuming a minimum instantaneous switching frequency of 17KHz at the peak input voltage and a peak difference boost inductor current of 1.4 amp, equation 3.15 gives the maximum inductance as

$$L = \frac{240\sqrt{2} * \left(380 - 240\sqrt{2}\right)}{17 * 10^{3} * 1.4 * 380} = 1.52 \text{ mH} \qquad (3.16)$$

From the above design procedure the value of the boost inductor is chosen to be 1.5mH. To obtain the value of the output capacitor the design procedure outlined in section 2.1.5 is used. The corresponding values for equations 2.48, 2.49 and 2.55 are obtained by assuming an average switching frequency, F_s of 100kHz.

3.4 SIMULATION OF THE PFC CIRCUIT FOR THE VARIABLE CURRENT HYSTERESIS CONTROL

Two values of the peak difference δ, which result in average switching frequencies of 100kHz and 5kHz are used in order to provide results and characteristics that can be compared with the constant frequency schemes. The circuit parameters chosen are as follows.

Line voltage = 240V(rms)	Line voltage =100V(rms)
Line frequency = 60Hz	Line frequency = 60Hz
Output Voltage = 380V(dc)	Output Voltage = 200V(dc)
Output power = 400W	Output power = 160W
Peak difference, δ = 1.4A	Peak difference, δ = 3A
Boost inductor = 1.5mH	Boost inductor = 5.5mH
Output capacitor = 470 μF	Output capacitor = 1000 μF

Per-unit values

1 p.u voltage = 240V	1 p.u voltage =100V
1 p.u power = 400W	1 p.u power = 160W
1 p.u current = $\frac{400}{240}$ = 1.67 A	1 p.u current = $\frac{160}{100}$ = 1.6 A

3.4.1 SIMULATION PROCEDURE

The flow chart of the complete simulation procedure of the VCHC control is given in fig 3.5. MATLAB is used to simulate the design equations.

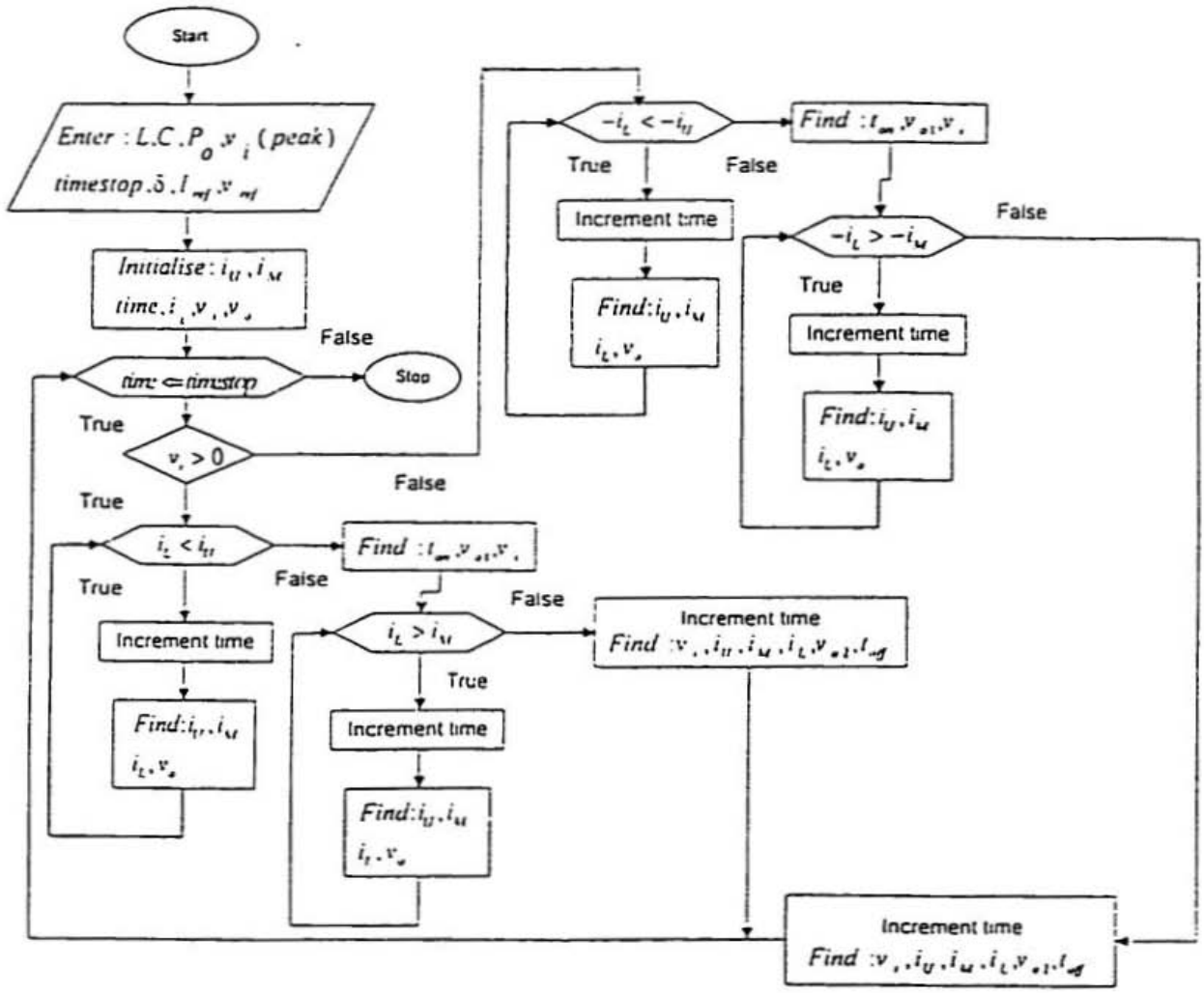


Figure 3.5 : Flow chart of the VCHC control scheme showing the simulation procedure

3.4.2 SIMULATION RESULTS

Figures 3.6 and 3.7 show the per unit source current and source voltage for two different values of boost inductor and δ respectively.

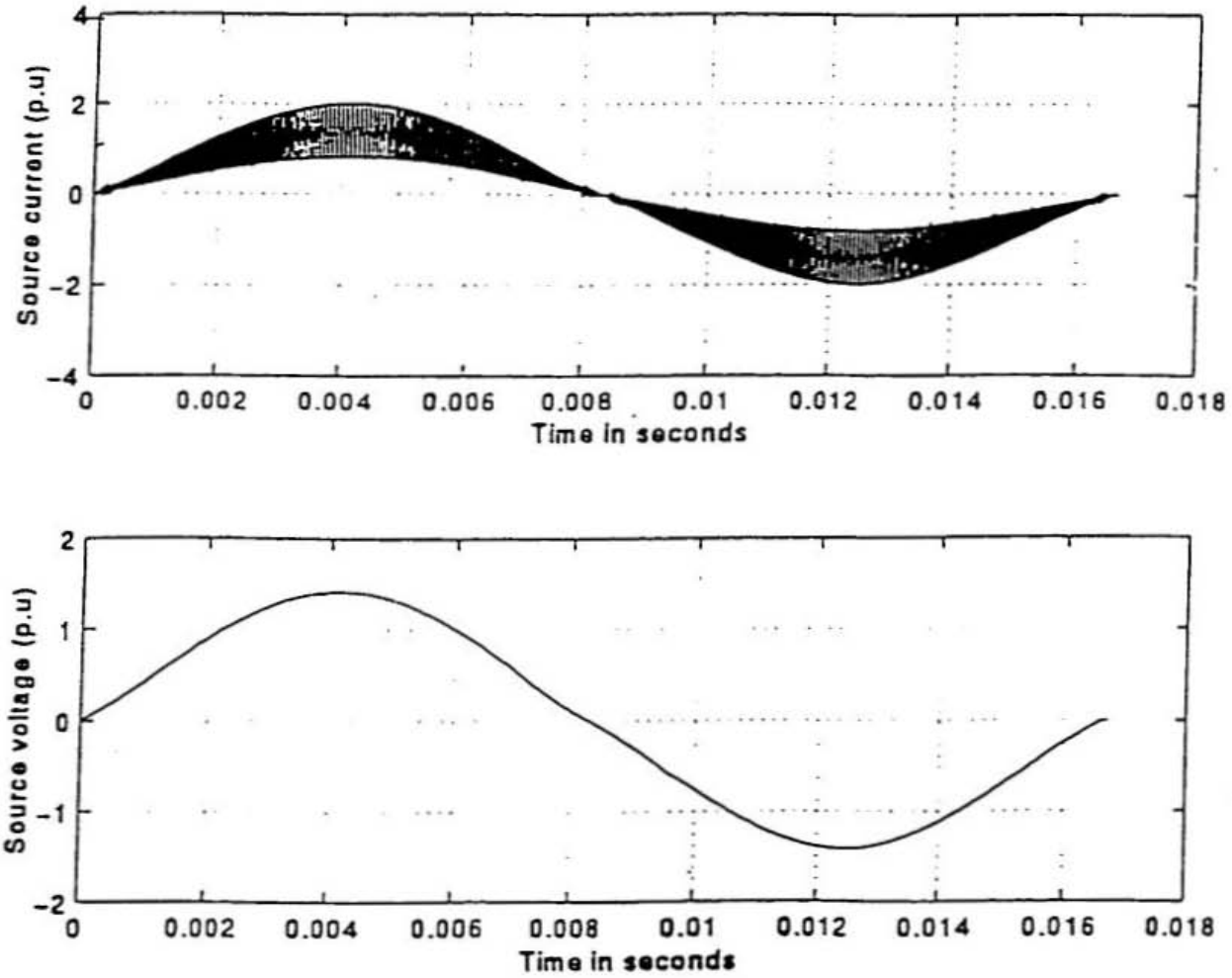


Figure 3.6 : Per-unit source current and source voltage waveforms

(L = 1.5mH, C = 470 μF , δ = 1.4 A)

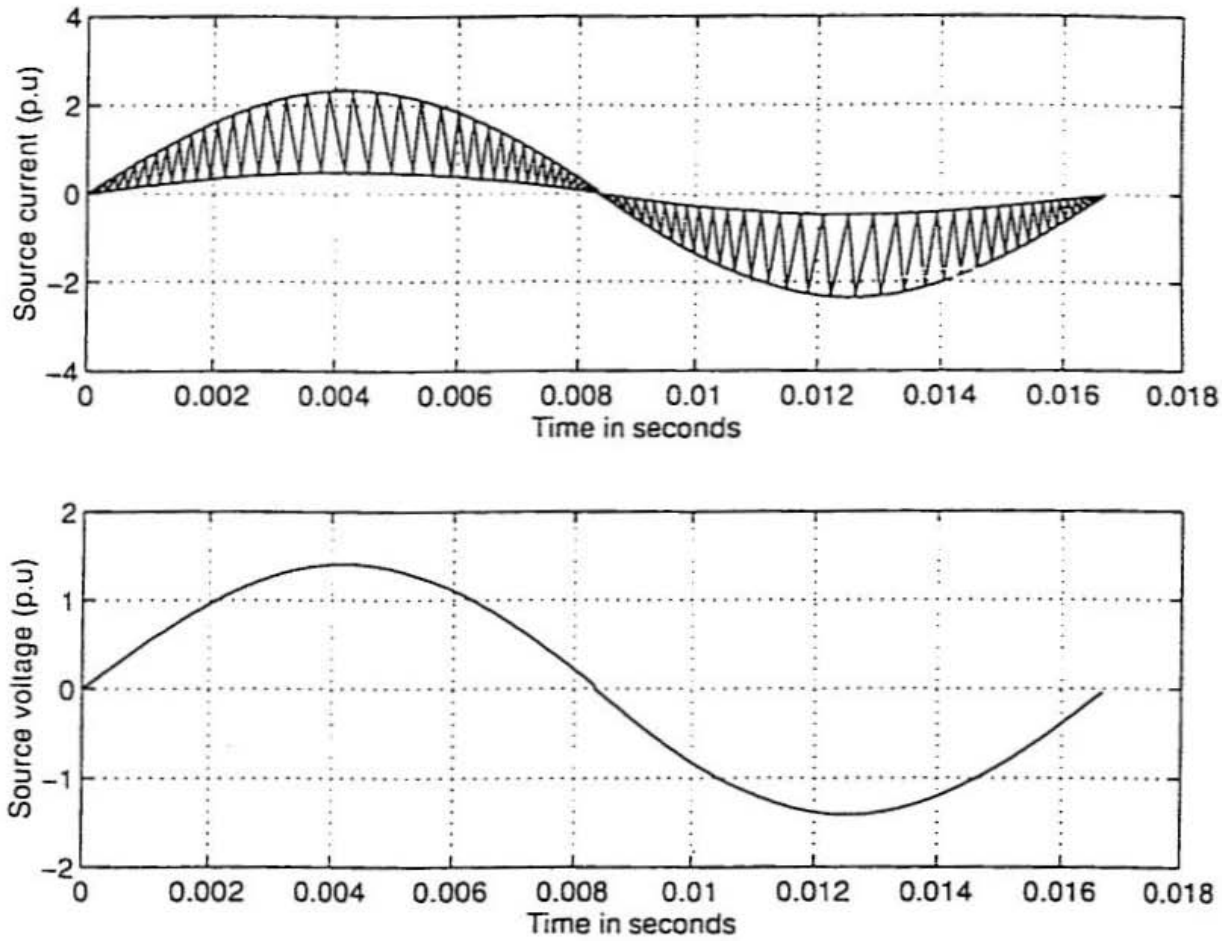


Figure 3.7 : Per-unit source current and source voltage waveforms

(L = 5.5mH, C = 1000 μF , δ = 3 A)

As seen from the graphs, this control scheme is capable of producing nearly sinusoidal input current waveform. The Total Harmonic Distortion of the source current for fig 3.6 is calculated as 2%. Fig 3.8 shows the output voltage ripple. The peak-to-peak ripple on the output voltage is 1.6%.

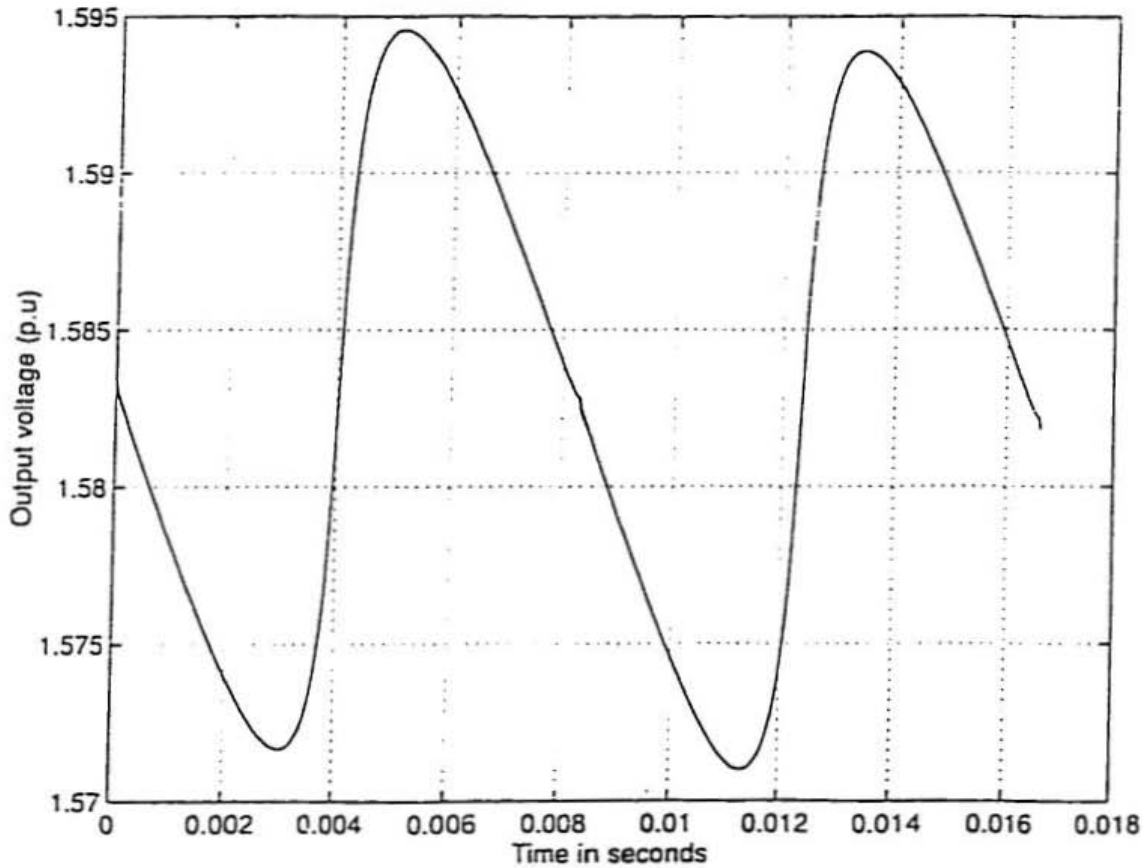


Figure 3.8: Per unit output voltage waveform

(L = 1.5mH, C = 470 μF , δ = 1.4 A)

Figure 3.9 shows the instantaneous switching frequency over one cycle of operation. It can be seen that the instantaneous switching frequency is very high at the point of zero crossing of the input voltage. The average switching frequency has been calculated to be 99.11kHz with a peak instantaneous value at zero crossing of 498.7kHz . Figure 3.10 shows the harmonic component of the input current (per-unit) with respect to the order of the harmonics.

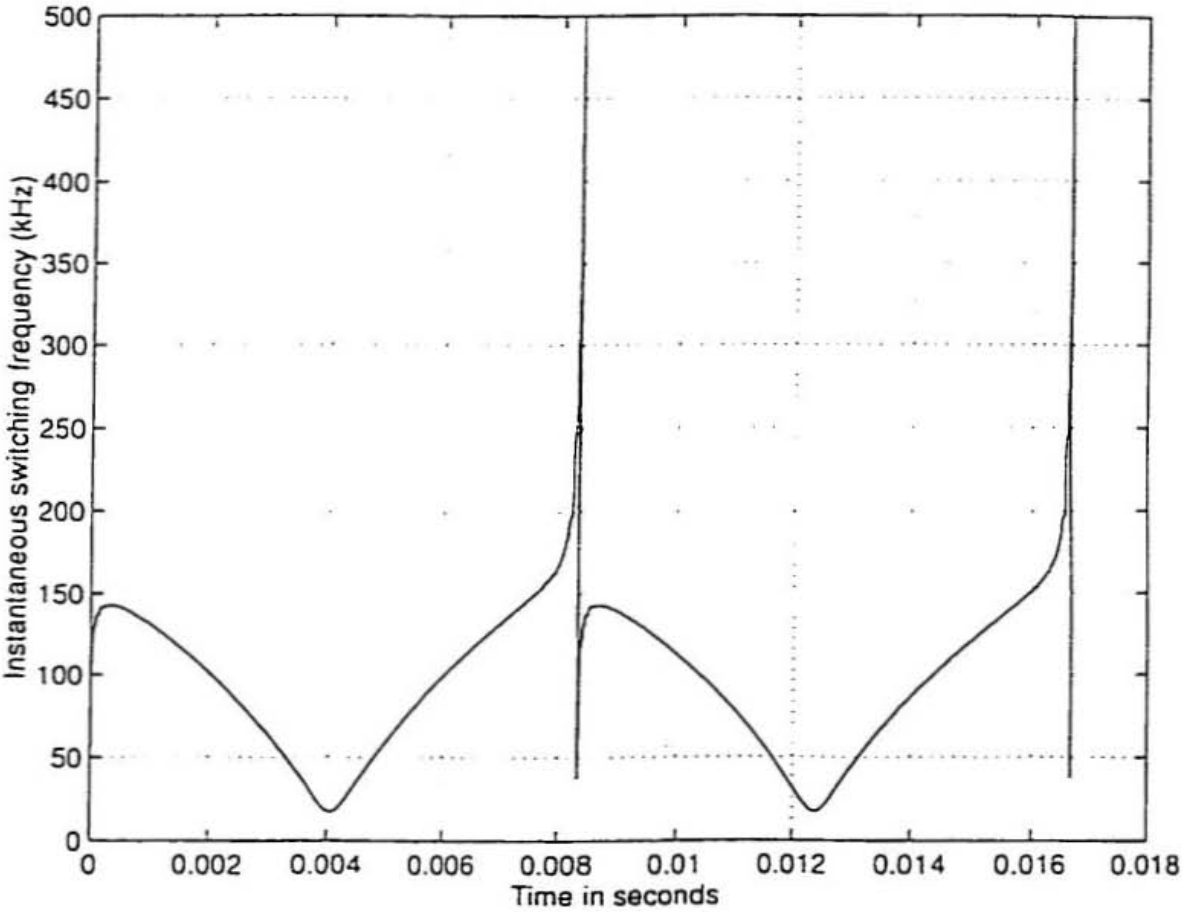


Figure 3.9 : Instantaneous switching frequency over one cycle of operation

(L = 1.5mH, C = 470 μF , δ = 1.4 A)

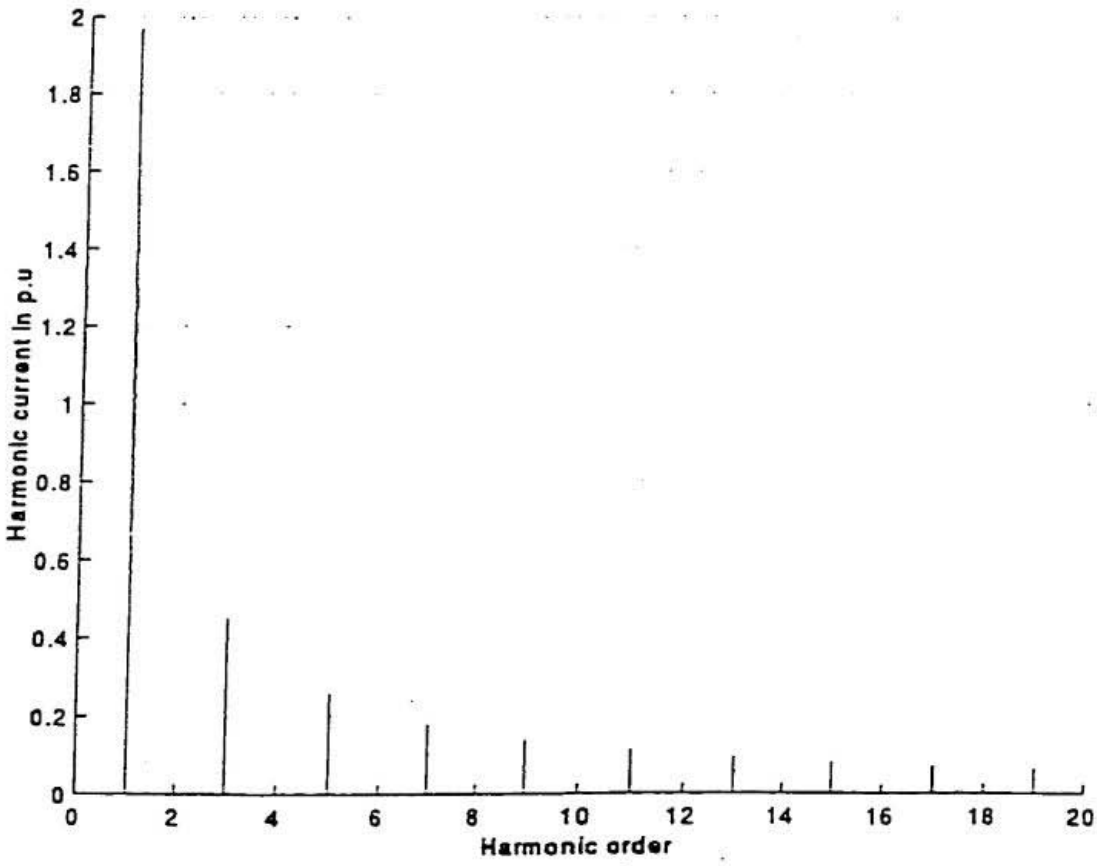


Figure 3.10 : Per-unit harmonic component of the input current versus harmonic order

(L = 1.5mH, C = 470 μF , δ = 1.4 A)

Figure 3.11 shows the frequency spectrum of the input current. The figure shows that the variable current hysteresis control produces evenly distributed frequency components in the input current.

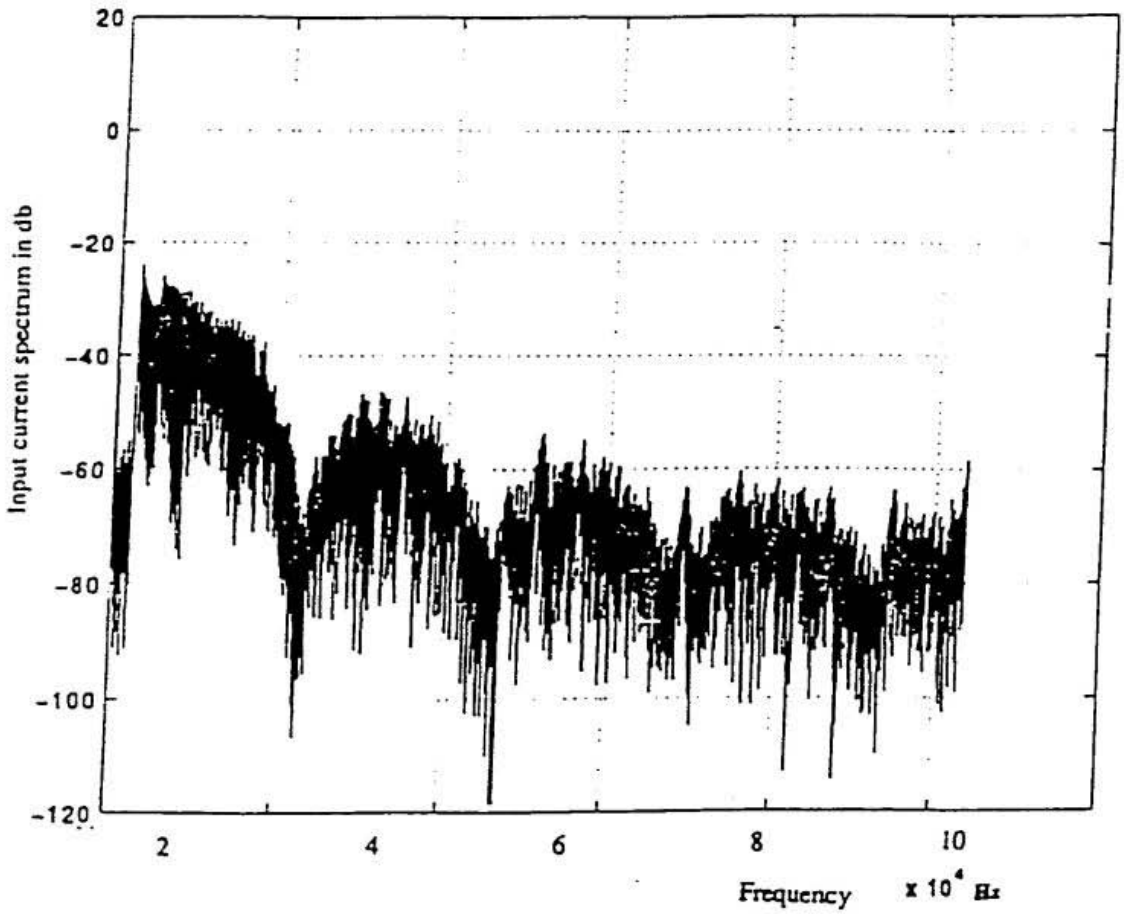


Figure 3.11: Frequency spectrum of the input current

(L = 1.5mH, C = 470 μF , δ = 1.4 A)

Keeping the boost inductor and output capacitor value constant, the variation of the peak instantaneous switching frequency and average switching frequency versus the peak difference (δ) are shown in fig 3.12 and 3.13 respectively. It is seen that both the peak instantaneous switching frequency and the average switching frequency over one cycle of operation increase with decreasing δ. The turn ON and OFF times of the boost switch decrease with decreasing δ and hence the peak instantaneous and average switching frequency increases.

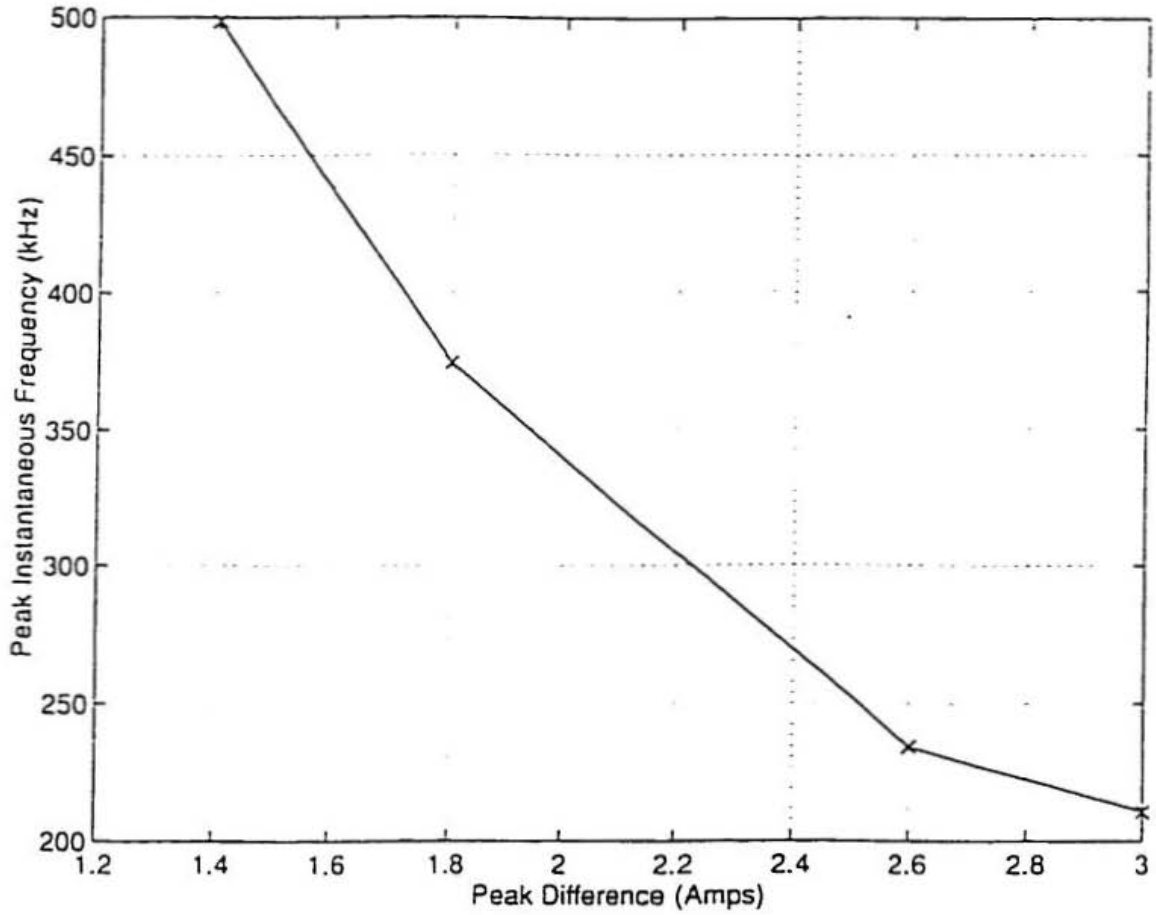


Figure 3.12 : Peak instantaneous switching frequency of the boost switch versus δ

(L = 1.5mH, C = 470 μF)

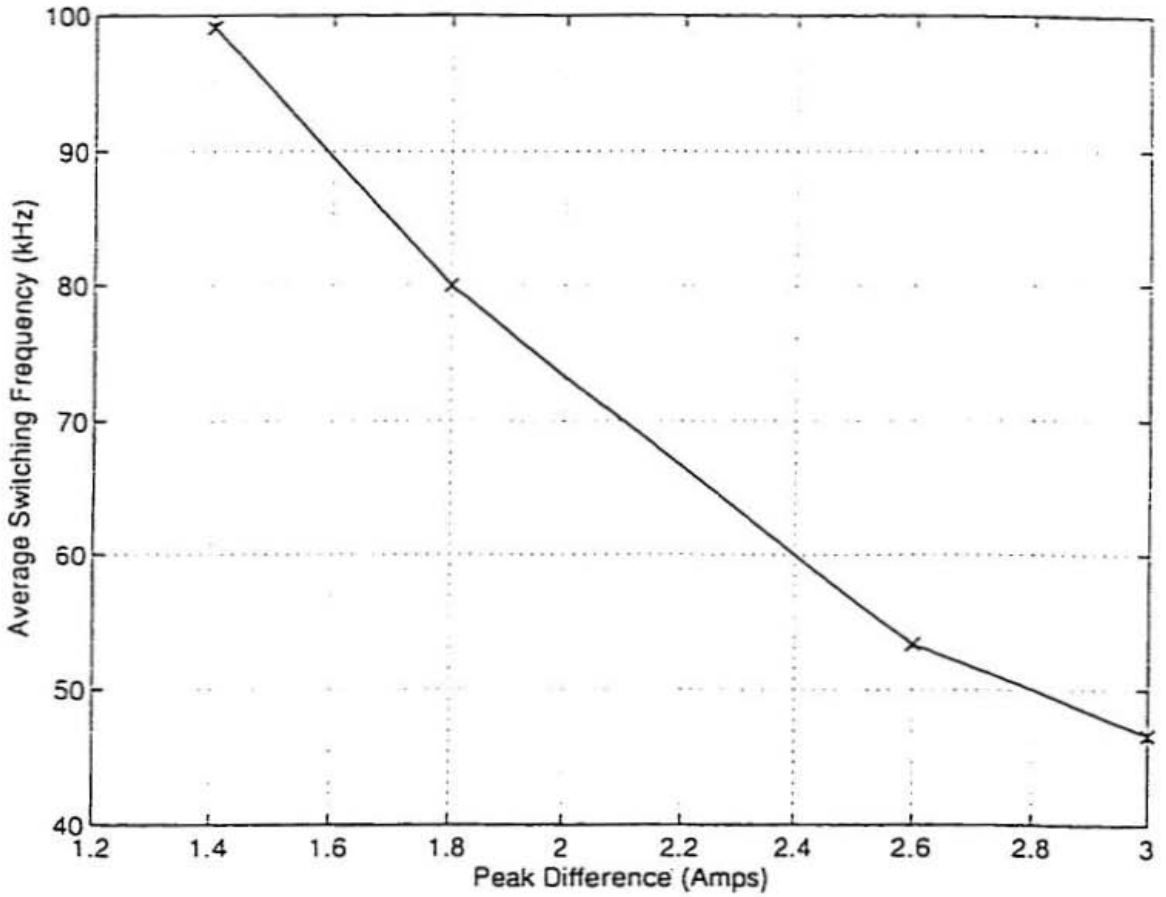


Figure 3.13 : Average switching frequency of the boost switch versus δ

(L = 1.5mH, C = 470 μF)

Figure 3.14 and 3.15 show the average power loss across the boost switch with respect to varying boost inductor value and peak difference (δ). The average power loss is found to be 8.22W with L=1.5mH and δ=1.4A. It can be seen that at constant peak difference the average power loss decreases with increasing values of the boost inductor. Increasing the boost inductor value at constant hysteresis band reduces the instantaneous value of the input current and decreases the average power loss. For a given boost inductor value the average power loss increases with decreasing peak difference.

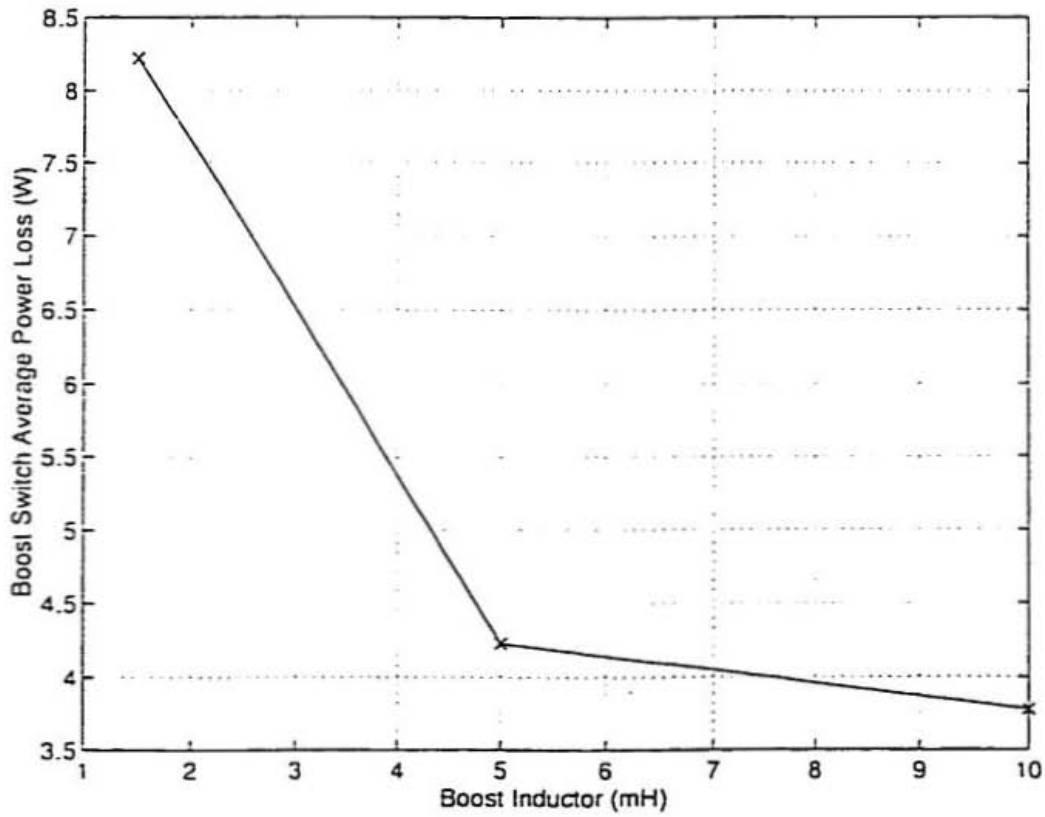


Figure 3.14: Power loss across the boost switch versus varying boost inductor

(C=470 μF , δ = 1.4 A)

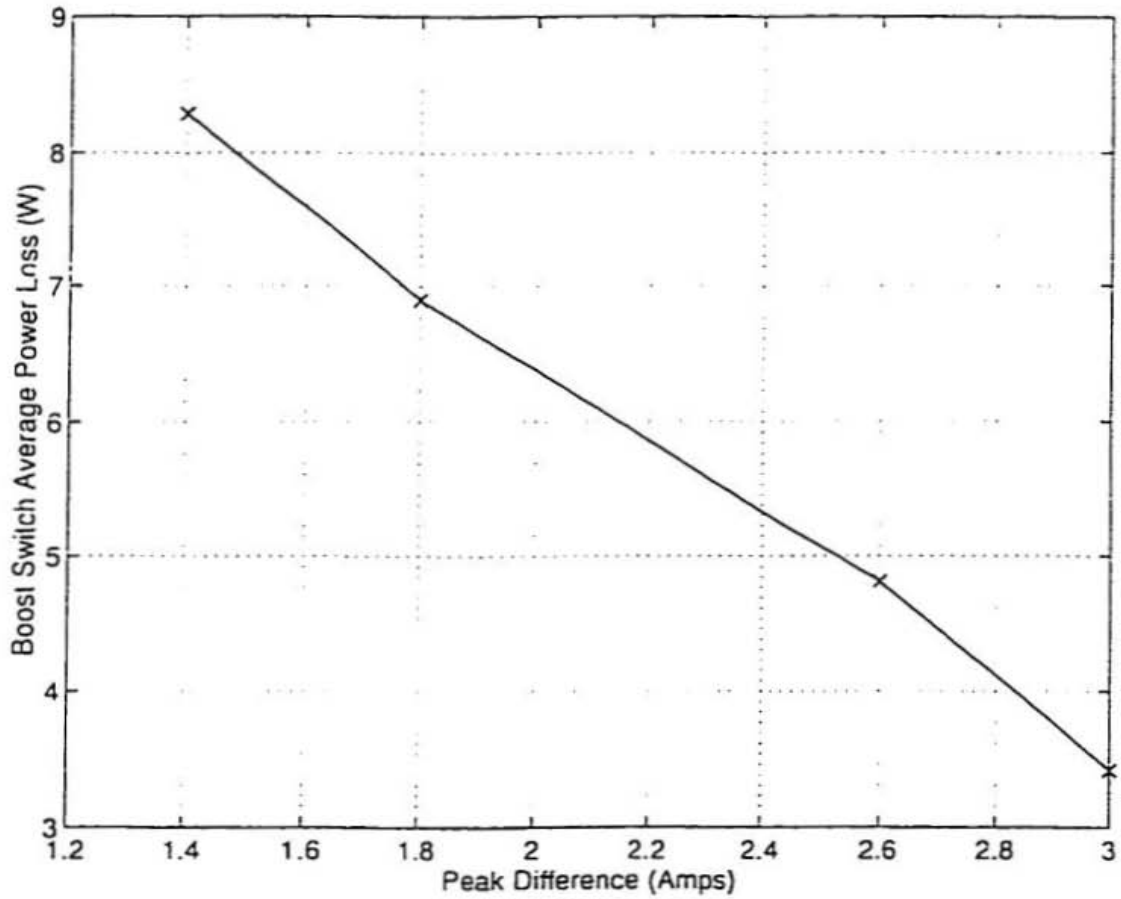


Figure 3.15: Power loss across the boost switch versus varying peak difference

(L=1.5mH, C=470 μF)

3.5 SUMMARY

The simulation results show that the inductor current is confined within the two boundary limits and is capable of producing nearly sinusoidal input current waveform. The simulated waveforms of the input current closely resemble the predicted theoretical waveforms for the variable current hysteresis control (VCHC) method.

The simulation results show that the peak instantaneous switching frequency increases with decreasing hysteresis band. The ON and OFF times of the boost switch decrease with increasing hysteresis band which in turn increase the peak switching frequency. It is seen that the average power loss across the boost switch, at fixed hysteresis band decreases with increasing values of boost inductor value. However, the average power loss increases with decrease of hysteresis band at constant boost inductor value.

The frequency spectrum shows that the variable current hysteresis control produces evenly distributed frequency components in the input current, thus, making the design of EMI filter very difficult. The control circuit design is simpler and easy to install. However, it is seen that the instantaneous switching frequency is very high at the zero crossing of the input voltage, higher than the average switching frequency, which is a serious limitation of the variable current hysteresis control scheme.

Chapter 4

ZERO-CURRENT ZERO-VOLTAGE SWITCHING SCHEME

INTRODUCTION

The constant frequency discontinuous current (CFDC) control method, described in chapter 2 has a major drawback in terms of the switching stress and power loss. In order to reduce the switching stress and power loss, the zero-current, zero-voltage switching (ZCS-ZVS) schemes have been proposed. This chapter deals with the analysis, modelling and simulation results of the ZCS-ZVS scheme. Operational characteristics such as total harmonic distortion (THD) and switch power dissipation and input current waveforms are discussed. As this scheme is an improvement over the CFDC control, this chapter provides a comparison between CFDC control scheme and ZCS-ZVS scheme in terms of total harmonic distortion (THD) and switch power dissipation. The control circuit for the ZCS-ZVS scheme are also described in this chapter.

4.1 THE ZERO-CURRENT, ZERO VOLTAGE CONTROL SCHEME FOR PFC CIRCUIT

It is seen from the CFDC control scheme that the inductor current is forced to go to zero at the end of the OFF period of the boost switch. The boost switch turns ON at zero current resulting in zero current switching. Therefore switching loss caused by ON switching is low. However, the switch is switched OFF at the maximum current and a certain level of voltage which causes a large current stress and high power loss in the switching device. In order to minimize the switching power loss, the power factor circuit (PFC) is modified as shown in Fig 4.1.

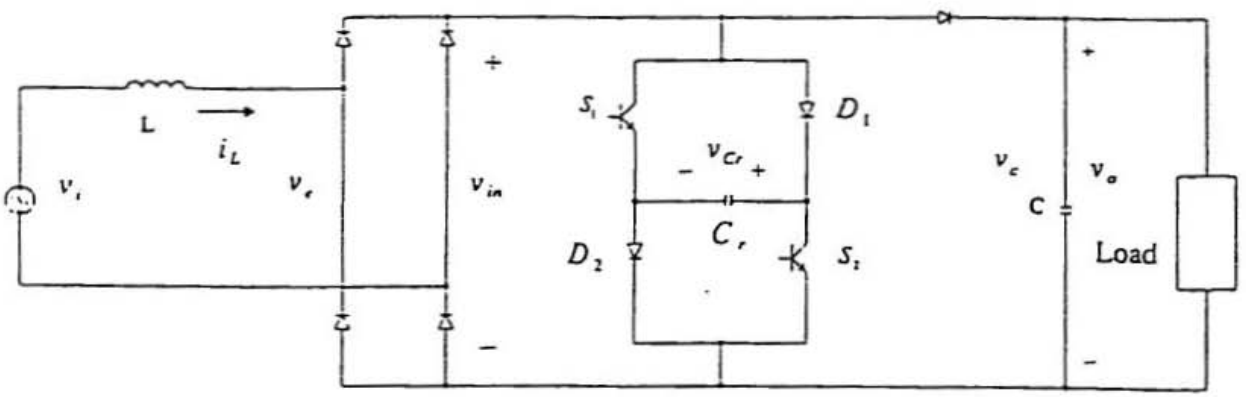


Figure 4.1: Power factor correction circuit with zero voltage switching scheme

Basically, the zero voltage switching circuit is a snubber circuit which is assumed to be lossless in this chapter. The commutating capacitor C_r is inserted in the main PFC circuit so as to realise ZVS at turn OFF operation of the switching device S_1 and S_2. The current flowing through the boost inductor (L) is controlled to be discontinuous. Hence, soft switching is achieved in the main power factor correction circuit .

4.2 MODELLING AND ANALYSIS OF THE PFC CIRCUIT UNDER ZCS - ZVS CONTROL

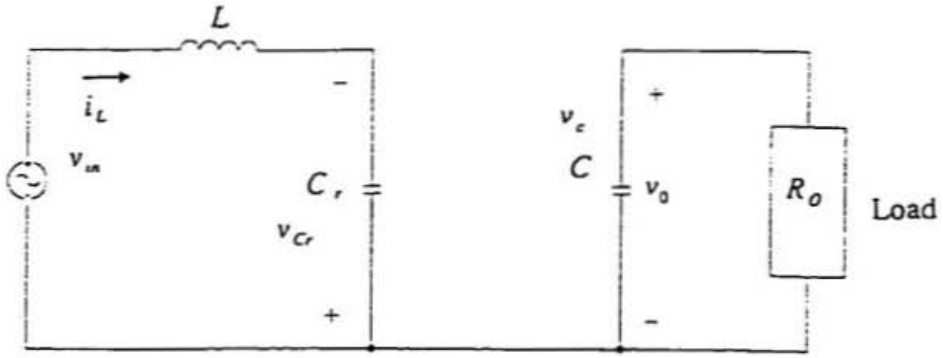
Initially, the current flowing through the boost inductor (L) is assumed to be zero. S_1 and S_2 are OFF and C_r is charged to the DC output voltage (V_o). The switching frequency is normally very high so that the supply voltage is assumed to be constant during the switching cycle.

4.2.1 ON STATE OF S_1 AND S_2

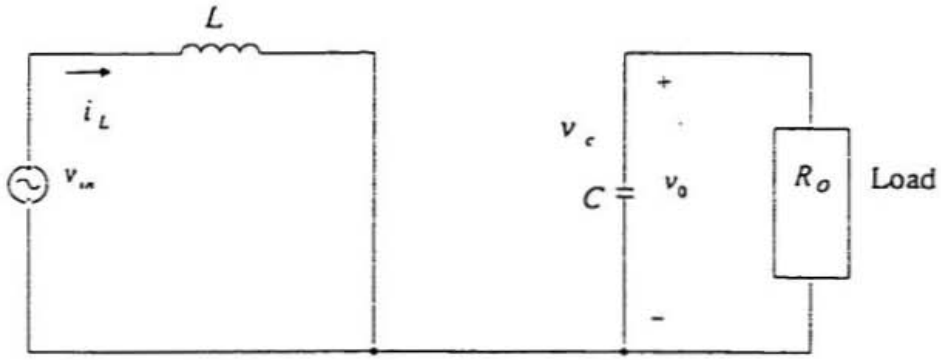
Two modes of operation result from turning on S_1 and S_2. The equivalent circuits for the two modes are shown in fig 4.2.

Mode 1

Mode 1 begins by turning ON both S_1 and S_2 at the same time. Since the voltage across the commutating capacitor is the same as the output voltage, no charging current flows through the switches (S_1 and S_2).



(a)



(b)

Figure 4.2: Equivalent circuits of the ZCS-ZVS PFC circuit ON state

(a) Mode 1 (b) Mode 2

During the interval when the switches are ON, the sum of the input voltage and the capacitor (C_r) voltage is applied to the boost inductor (L). The capacitor starts discharging through L.

The voltage across C_r is given by

$$v_{Cr} = v_L - v_{in} \tag{4.1}$$

where

v_{in} is the instantaneous rectified supply voltage

v_L is the instantaneous voltage across the boost inductor

v_{Cr} is the instantaneous voltage across the commutating capacitor

Assuming that the input voltage magnitude remains constant during the modes of operation, the voltage across C_r can be expressed as

$$v_{Cr} = (V_{in} + V_o)\cos\omega_r t - V_{in} \tag{4.2}$$

and the boost inductor current is obtained as

$$i_L = \frac{V_{in} + V_o}{X_r}\sin\omega_r t \tag{4.3}$$

where

$$\omega_r = \frac{1}{\sqrt{L\,C_r}} \qquad \text{and} \qquad X_r = \sqrt{\frac{L}{C_r}} \tag{4.4}$$

This mode ends at $t = t_1$, when $v_{Cr} = 0$. The time, t_1 is obtained from equation 4.2 as

$$t_1 = \sqrt{L\,C_r}\cos^{-1}\left(\frac{V_{in}}{V_{in} + V_o}\right) \tag{4.5}$$

and the inductor current at the end of the mode is obtained from equation 4.3 as

$$I_{L1} = \frac{1}{X_r}\sqrt{V_o^2 + 2V_{in}V_o} \tag{4.6}$$

Mode 2

Mode 2 begins when the voltage across C_r is zero. At this point the diodes D_1 and D_2 start to conduct and the DC current flows in two paths through S_1 - D_2 and $S_2 - D_1$. As a result of the short circuit across the bridge rectifier, the current in the boost inductor (L) increases. Since v_{in} is assumed constant the current increase linearly as

$$i_L = \frac{V_{in}}{L}t + I_{L1} \tag{4.7}$$

where

I_{L1} is the final value of the boost inductor current at the end of Mode 1

Mode 2 ends at the time, t_2 given by

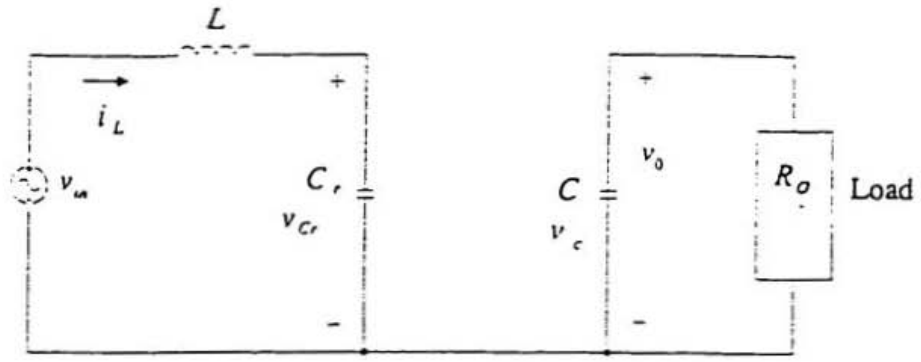
$$t_2 = t_{ON} - t_1 \tag{4.8}$$

and the inductor current at the end of this mode is given by

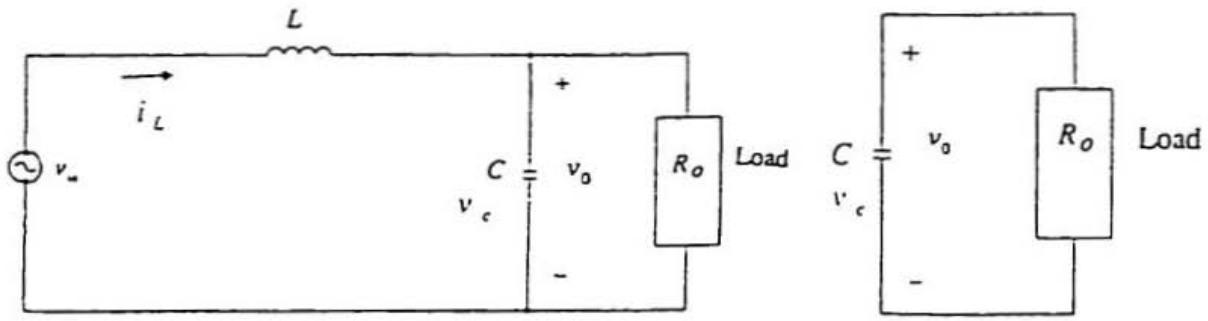
$$I_{L2} = \frac{V_{in}}{L}t_2 + I_{L1} \tag{4.9}$$

4.2.2 OFF STATE OF S_1 AND S_2

Three modes of operation result from turning OFF S_1 and S_2. The equivalent circuits for the three modes are shown in fig 4.3.



(a)



(b) (c)

Figure 4.3: Equivalent circuits of the ZCS-ZVS PFC circuit OFF state

(a) Mode 3 (b) Mode 4 (c) Mode 5

Mode 3

Mode 3 begins by turning OFF S_1 and S_2. In this mode the input current flows through L- $D_1 - C_r - D_2$. L and C_r resonate and C_r is charged. Since the capacitor was fully discharged to zero at the end of Mode 2, switching OFF of S_1 and S_2 results in zero voltage switching (ZVS). The capacitor voltage (v_{Cr}) and the inductor current, i_L are given by

$$v_{Cr} = V_{in} + X_r I_a \sin(\omega_r t + \theta) \tag{4.10}$$

$$i_L = I_a \cos(\omega_r t + \theta) \tag{4.11}$$

where

I_a is defined as

$$I_a = \sqrt{\frac{C_r}{L} V_{in}^2 + I_{L2}^2} \tag{4.12}$$

the phase angle, θ is given by

$$\theta = \sin^{-1}\left(- \frac{V_{in}}{\sqrt{V_{in}^2 + I_{L2}^2 \cdot \frac{L}{C_r}}} \right) \tag{4.13}$$

and I_{L2} is the inductor current at the end of Mode 2 (equation 4.9)

Mode 3 ends when $v_{Cr} = V_o$. Rearranging equation 4.10 the time, t_3 when mode 3 ends is solved as

$$t_3 = \frac{1}{\omega_r}\left\{\{\sin^{-1}(\frac{V_o - V_{in}}{X_r . I_a})\} - \theta\right\} \tag{4.14}$$

Substituting the value of X_r and I_a(from equation 4.12) in equation 4.14 the time duration is solved using MAPLE and given by

$$t_3 = \sqrt{L\ C_r}\left\{\sin^{-1}\left(\frac{V_o - V_{in}}{\sqrt{V_{in}^2 + \frac{L}{C_r} I_{L2}^2}}\right) - \theta\right\} \tag{4.15}$$

The inductor current at the end of the Mode 3 can be found from the following equation

$$I_{L3} = I_{L2}\cos\omega_r t_3 + \sqrt{\frac{C_r}{L}} V_{in}\sin\omega_r t_3 \tag{4.16}$$

<u>Mode 4</u>

Mode 4 begins when the voltage across C_r is equal to the output voltage (V_o). The DC current which was flowing through C_r then flows through the load. Since the output voltage is greater than the input voltage the DC current is decreased to zero at the end of Mode 4. The boost inductor (L) current for Mode 4 is given by

$$i_{L4} = -\frac{V_o - V_{in}}{L} t + I_{L3} \tag{4.17}$$

Mode 4 ends when $i_{L4} = 0$. From equation 4.17, the time t_4 when mode 4 ends is obtained as

$$t_4 = \frac{L}{V_o - V_{in}} I_{L3} \tag{4.18}$$

Mode 5

Mode 5 begins when $i_L = 0$ and ends when S_1 and S_2 are turned ON at the same time. At the end of Mode 5 the commutating capacitor C_r is charged to the output voltage V_o, and Mode 1 begins once again for the next switching cycle.

The theoretical waveforms of the boost inductor current and voltage across the commutating capacitor for various modes are shown in fig 4.4

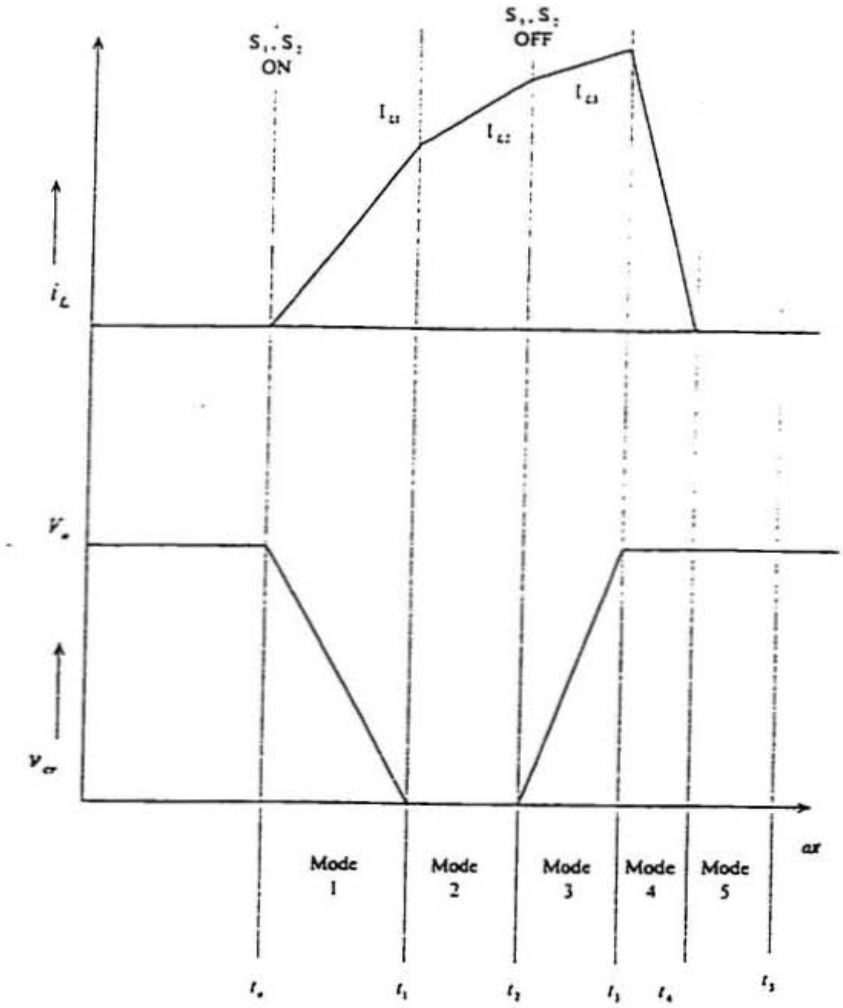


Figure 4.4 : Theoretical waveforms of input current and voltage across commutating capacitor of ZCS-ZVS control scheme

4.3 DESIGN EXAMPLE

To ensure a fair comparison between the ZCS-ZVS and constant frequency discontinuous current (CFDC) control methods, the source voltage, frequency of operation of the boost switch, output power and output voltage values used in the CFDC scheme are kept constant and are employed for the ZCS-ZVS scheme. The general procedure for finding the boost inductor value for the ZCS-ZVS scheme is as follows.

Rearranging equation 4.9 the boost inductor value is obtained as

$$L = \frac{V_{in}}{I_{L2} - I_{L1}} t_2 \tag{4.19}$$

Substituting I_{L1} and t_2 from equation 4.6 and 4.8 respectively in equation 4.21 yields

$$L = \left[\frac{V_{in}}{I_{L2} - \left(\frac{1}{X_r} \sqrt{V_o^2 + (2 * V_{in} * V_o)} \right)} \right] * (t_{ON} - t_1) \tag{4.20}$$

Substituting X_r and t_1 from equation 4.4 and 4.5 respectively in equation 4.22 gives

$$L = \frac{V_{in}}{I_{L2} - \left(\frac{1}{\sqrt{\frac{L}{C_r}}} \sqrt{V_o^2 + (2 * V_{in} * V_o)} \right)} * \left[t_{ON} - \left\{ \sqrt{LC_r} \cos^{-1} \left(\frac{V_{in}}{V_{in} + V_o} \right) \right\} \right] \tag{4.21}$$

With $C_r = 0.001 \mu F$, $V_{in} = 240V(rms)$, $V_o = 380V$, $F_s = 100kHz$, D=0.1 and $I_{L2} = 3.34A$ the value of L is approximately calculated to be 0.1mH.

4.4 SIMULATION OF THE PFC CIRCUIT FOR ZCS-ZVS SCHEME

The same circuit parameters, which were used before for CFDC, CFDC and VCHC control methods, are used for the ZCS-ZVS scheme so as to ensure that a fair comparison is made between all the control methods. For completeness, the circuit parameters are given below.

Line voltage, $V_i = 240\,V(rms)$

Line frequency, f_i = 60Hz

Output Voltage, V_o = 380V(dc)

Output power, P_o = 400W

Switching frequency, F_s = 100kHz

Boost inductor, L = 0.1mH

Output capacitor, C = 470 μF

Line voltage, V_i = 100 $V(rms)$

Line frequency, f_i = 60Hz

Output Voltage, V_o = 200V(dc)

Output power, P_o = 160W

Switching frequency, F_s = 5kHz

Boost inductor, L = 2.2mH

Output capacitor, C = 1000 μF

Per-unit values

1 p.u voltage = 240V

1 p.u power = 400W

1 p.u current = $\frac{400}{240}$ = 1.67 A

1 p.u voltage =100V

1 p.u power = 160W

1 p.u current = $\frac{160}{100}$ = 1.6 A

4.4.1 SIMULATION PROCEDURE

The flow chart of the complete simulation procedure of the ZCS-ZVS control scheme is given in fig 4.5. MATLAB is used to simulate the system equations.

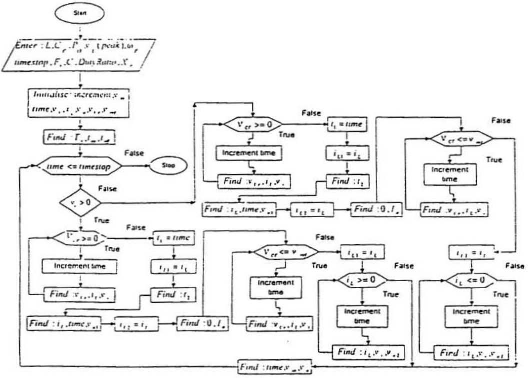


Figure 4.5 : Flow chart of the ZCS-ZVS control scheme

showing the simulation procedure

4.4.2 SIMULATION RESULTS

Figures 4.6 and 4.7 show the source current and source voltage in per unit at 100KHz and 5KHz respectively.

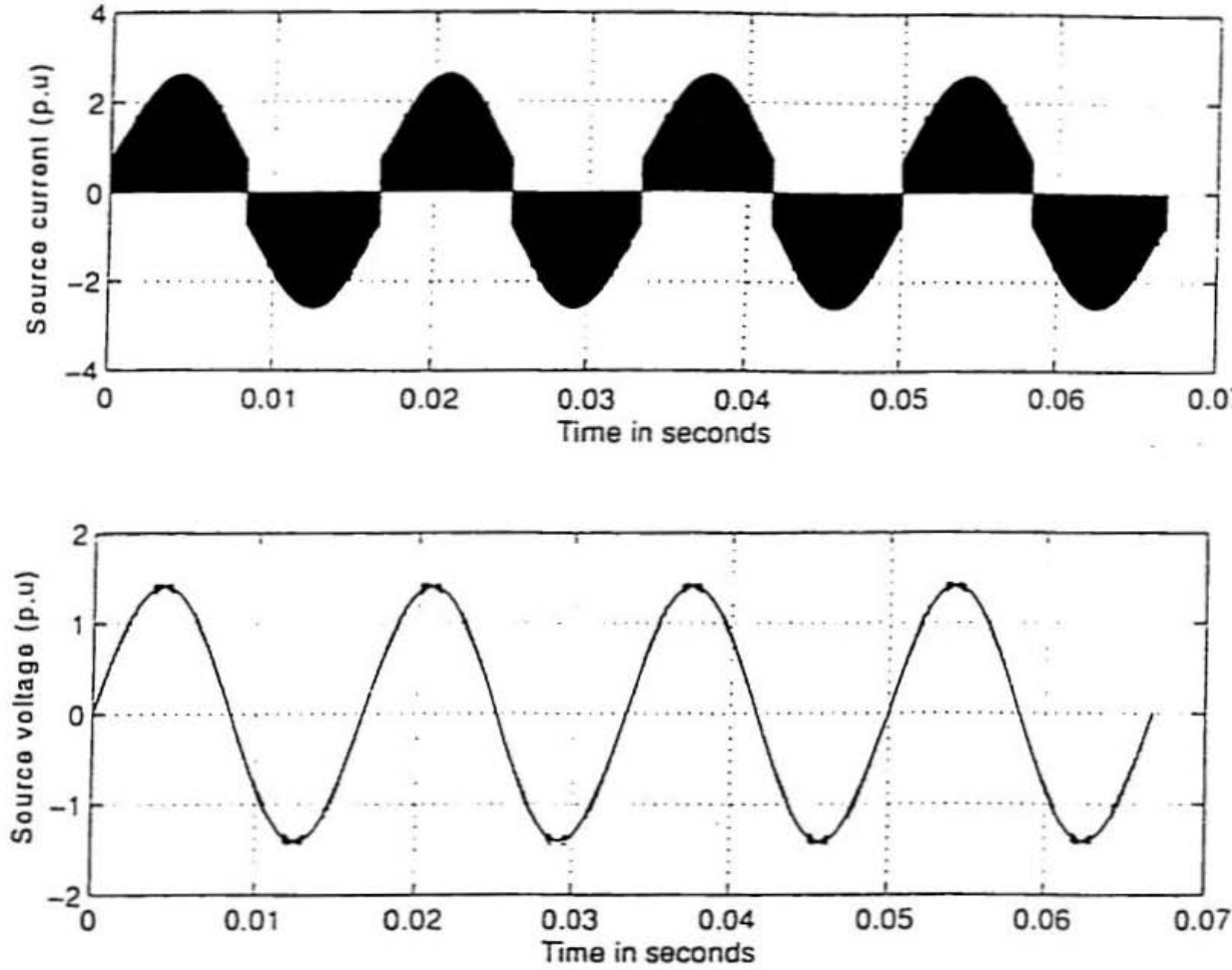


Figure 4.6 : Per-unit source current and source voltage waveforms

(L = 0.1mH, C = 470 μF , C_r = 0.001 μF , F_r = 100kHz)

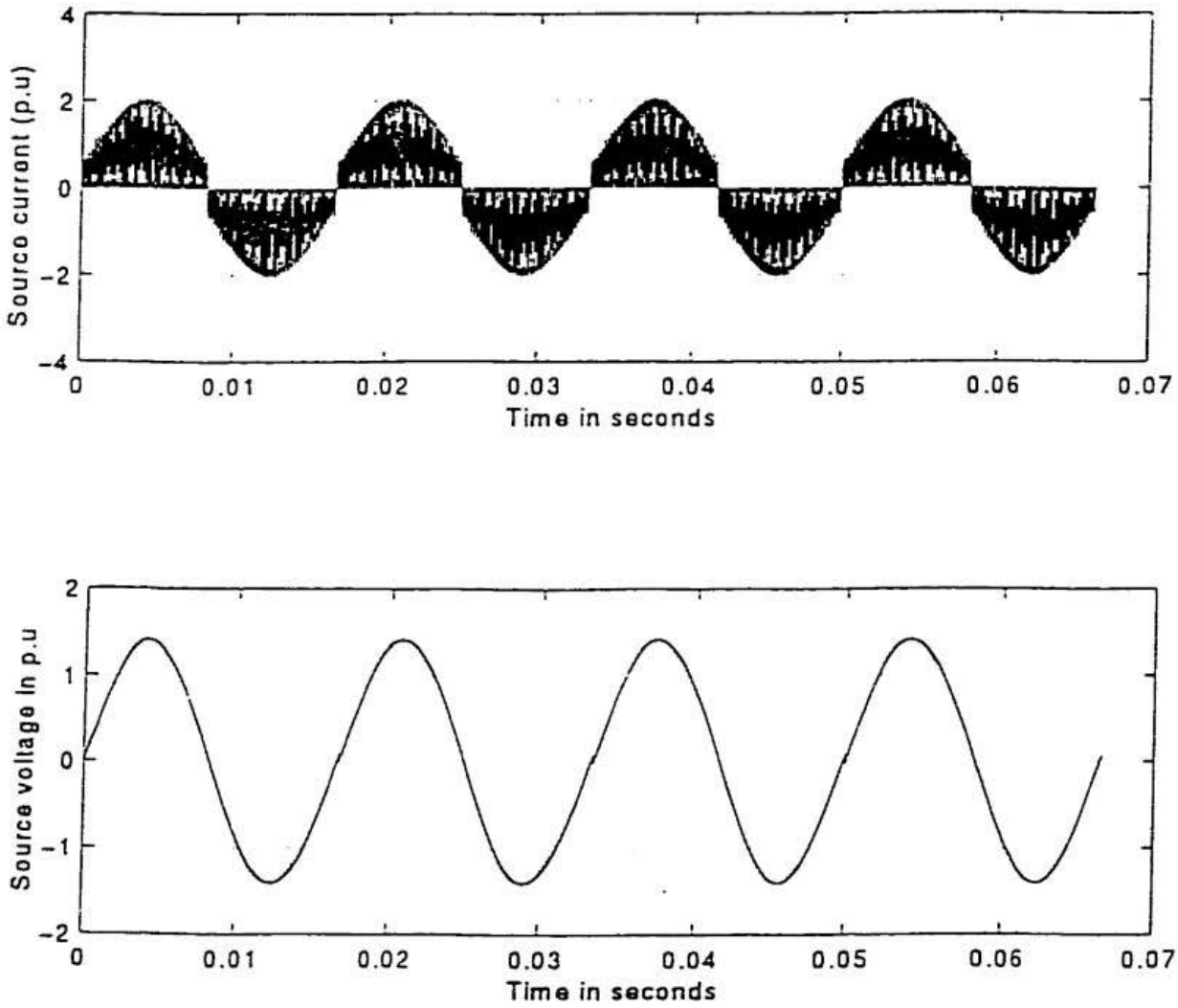


Figure 4.7 : Per unit source current and source voltage waveforms

(L = 2.2mH, C = 1000 μF , C_r = 0.001 μF , F_s = 5kHz)

As seen from the graphs the amplitude of the source current waveform is higher around the zero voltage crossing point. This is due to the fact that the electric charge of the commutation capacitor C_r is added to the total charge of the boost inductor, giving rise to an increase in the input current. However, the shape of the fundamental component of the input current is nearly similar to a sinusoidal waveform.

Figure 4.8 shows the voltage across the boost switch and the inductor current which match the expected theoretical waveforms of fig 4.4. It clearly shows that the boost switch is turned OFF at zero voltage, as predicted.

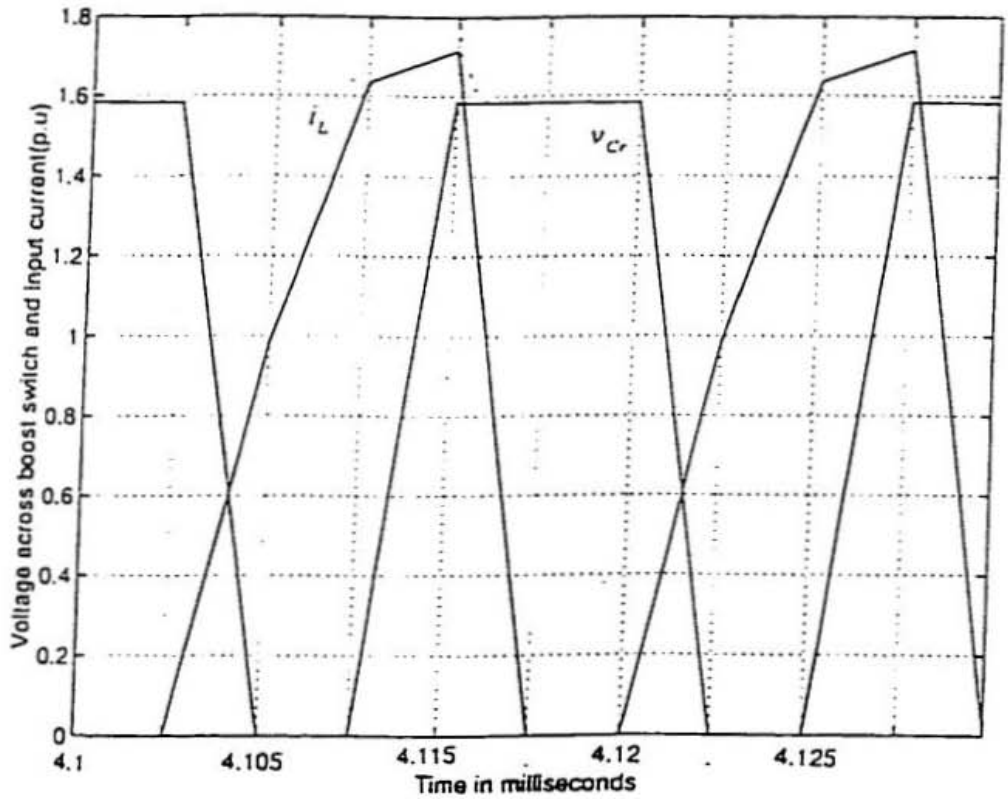


Figure 4.8: Per unit voltage across the boost switch and input current waveforms

(L = 0.1mH, C = 470 μF , C_r = 0.001 μF , F_s = 100kHz)

Figure 4.9 shows the input current spectrum over a wide range of frequency. The total harmonic distortion of the source current for fig 4.6 is found to be 3.12%. It can be seen from fig 4.9 that the spectrum is uniform and so the design of the input filter for the ZCS-ZVS scheme is easier.

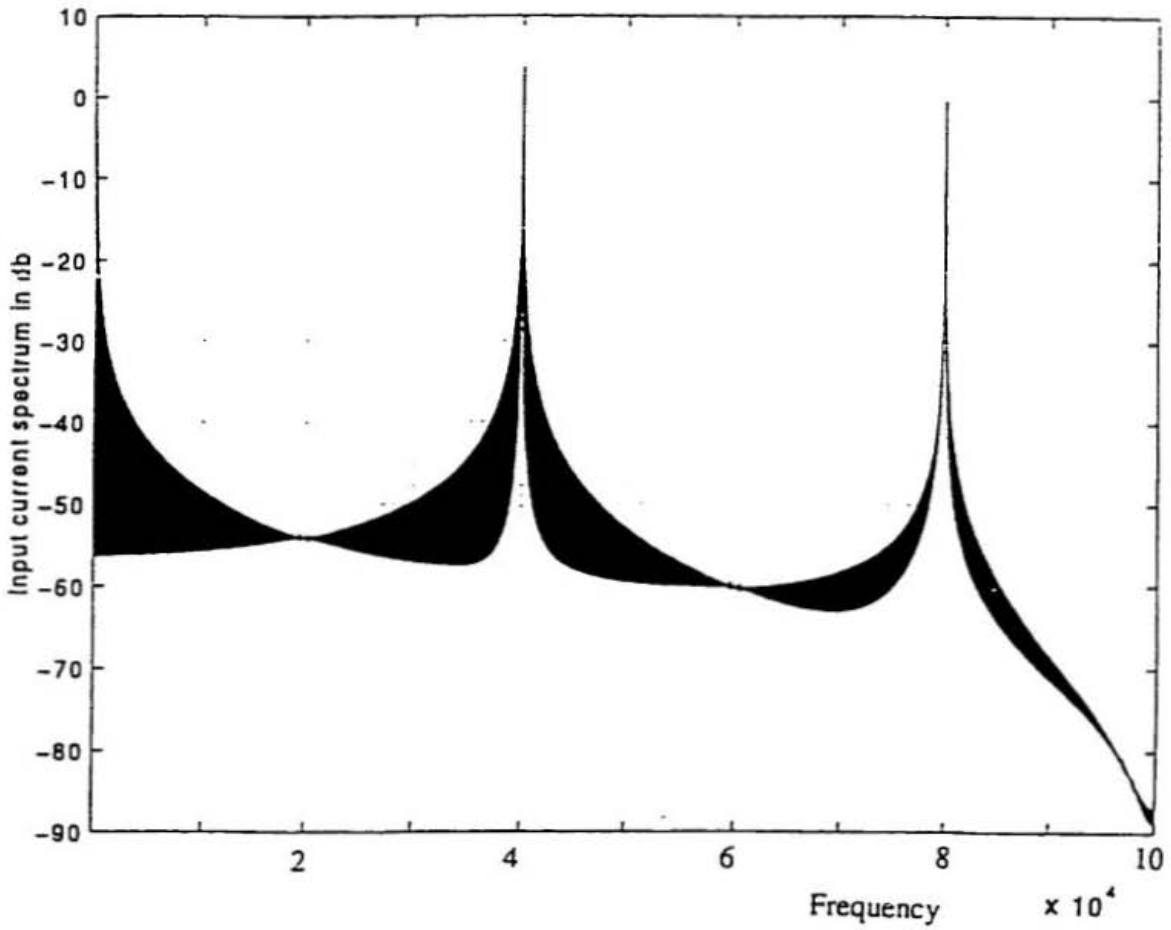


Figure 4.9: Frequency spectrum of the input current

(L = 0.1mH, C = 470 μF , C_r = 0.001 μF , F_s = 100kHz)

Figure 4.10 shows the input current harmonic spectrum in terms of the harmonic order. The figure shows that a small input filter is required to remove the higher order harmonics in the input current.

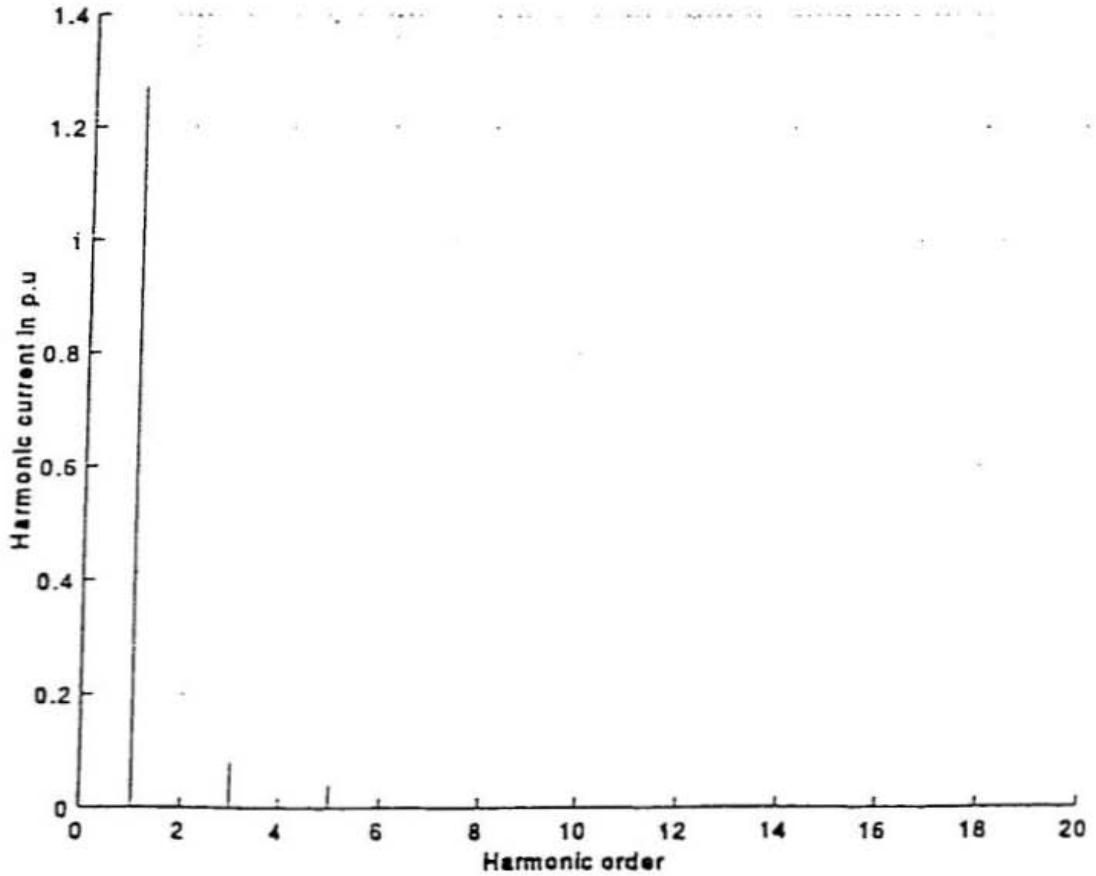


Figure 4.10 : Per-unit harmonic component of the input current versus harmonic order

(L = 0.1mH, C = 470 μF , C_r = 0.001 μF , F_s = 100kHz)

Keeping the switching frequency constant fig 4.11 shows a plot of the total harmonic distortion (THD) of the input current with varying values of the boost inductor. The THD decreases with increase of the boost inductor value for a fixed switching frequency.

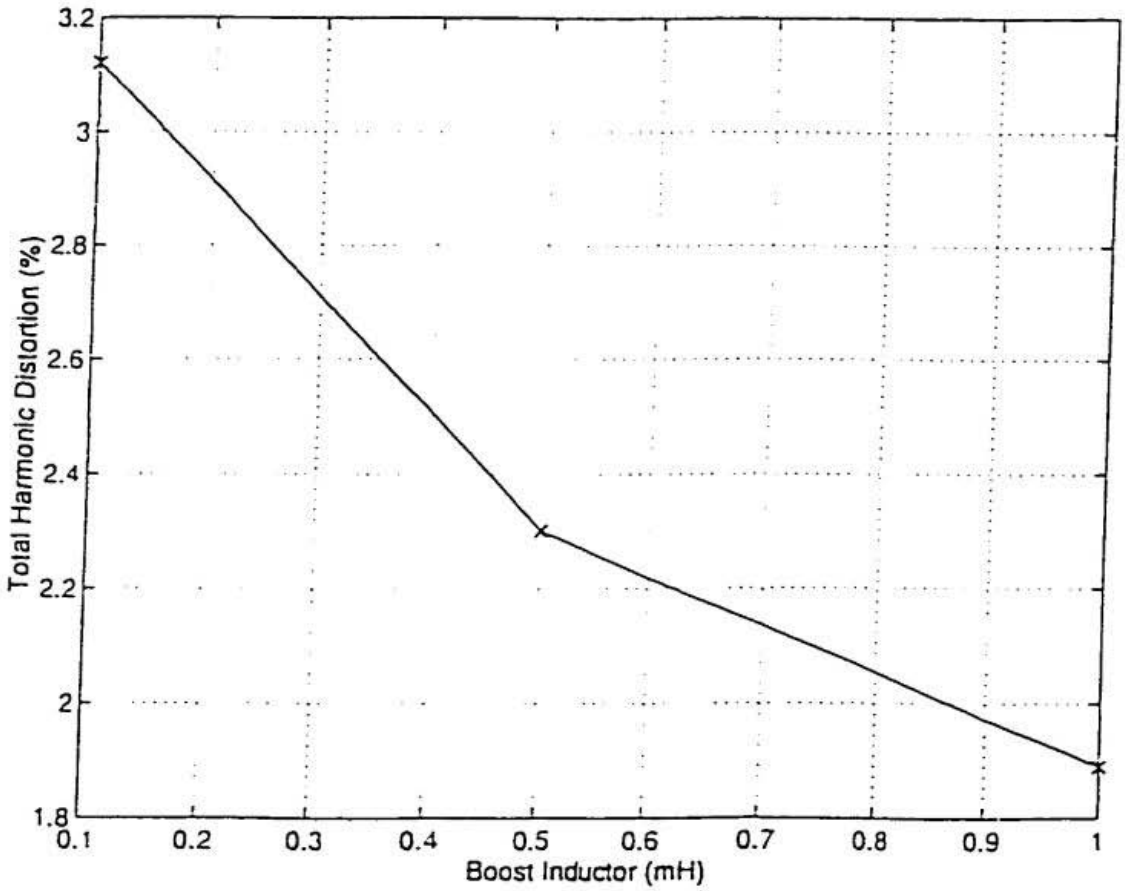


Figure 4.11: THD of the input current versus boost inductor value

($C = 470\,\mu F$, $C_f = 0.001\,\mu F$, $F_s = 100\text{kHz}$)

Figure 4.12 shows the change in THD with varying switching frequency keeping the boost inductor value constant. The figure shows that the THD of the input current decreases with increasing switching frequency.

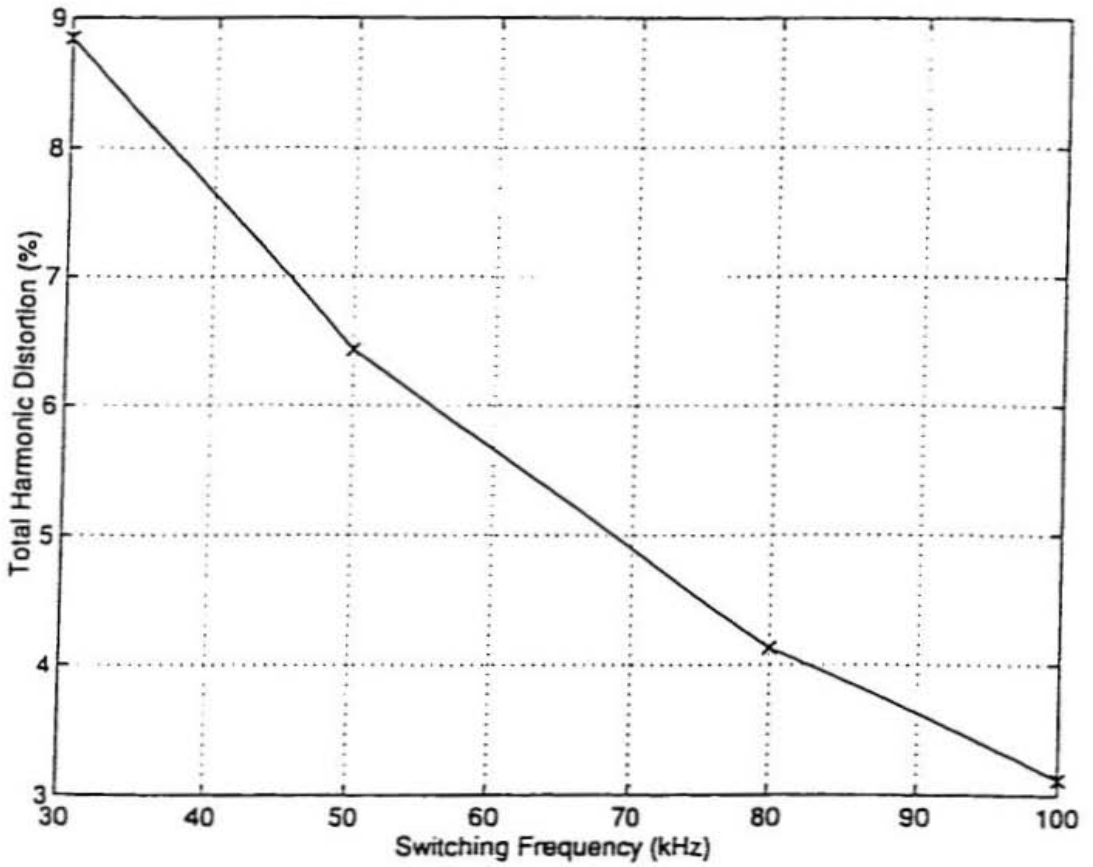


Figure 4.12: THD of the input current versus varying switching frequency

(L = 0.1mH, C = 470 μF , C_r = 0.001 μF)

Figure 4.13 and 4.14 show the average power across the boost switch with respect to varying values of boost inductor and switching frequency respectively. The average power loss is found to be 5.72W for L= 0.1mH and F_s =100kHz. From the figure 4.13 it can be seen that the average power loss decreases with increasing values of boost inductor. For a given boost inductor value the average power loss increases with increase of switching frequency.

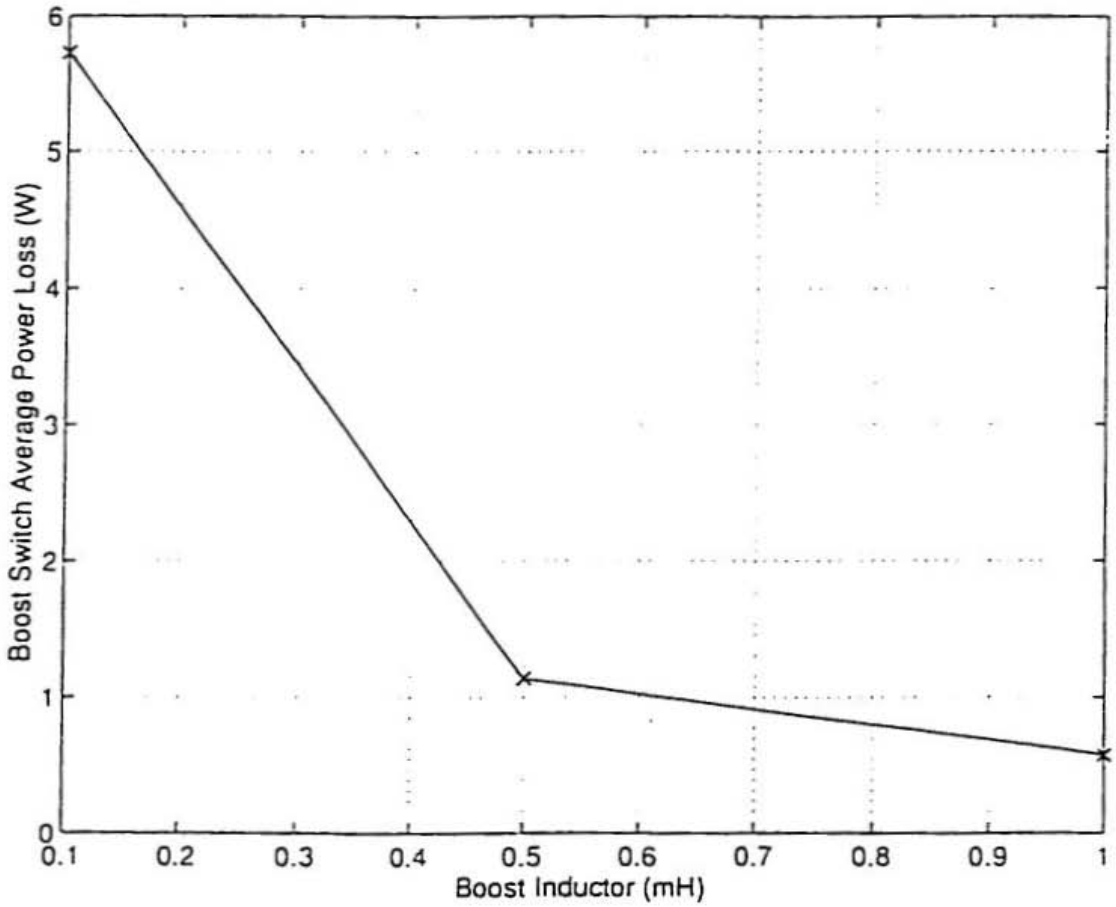


Figure 4.13: Power loss across the boost switch versus varying boost inductor

(C=470 μF , C_r = 0.001 μF , F_s=100kHz)

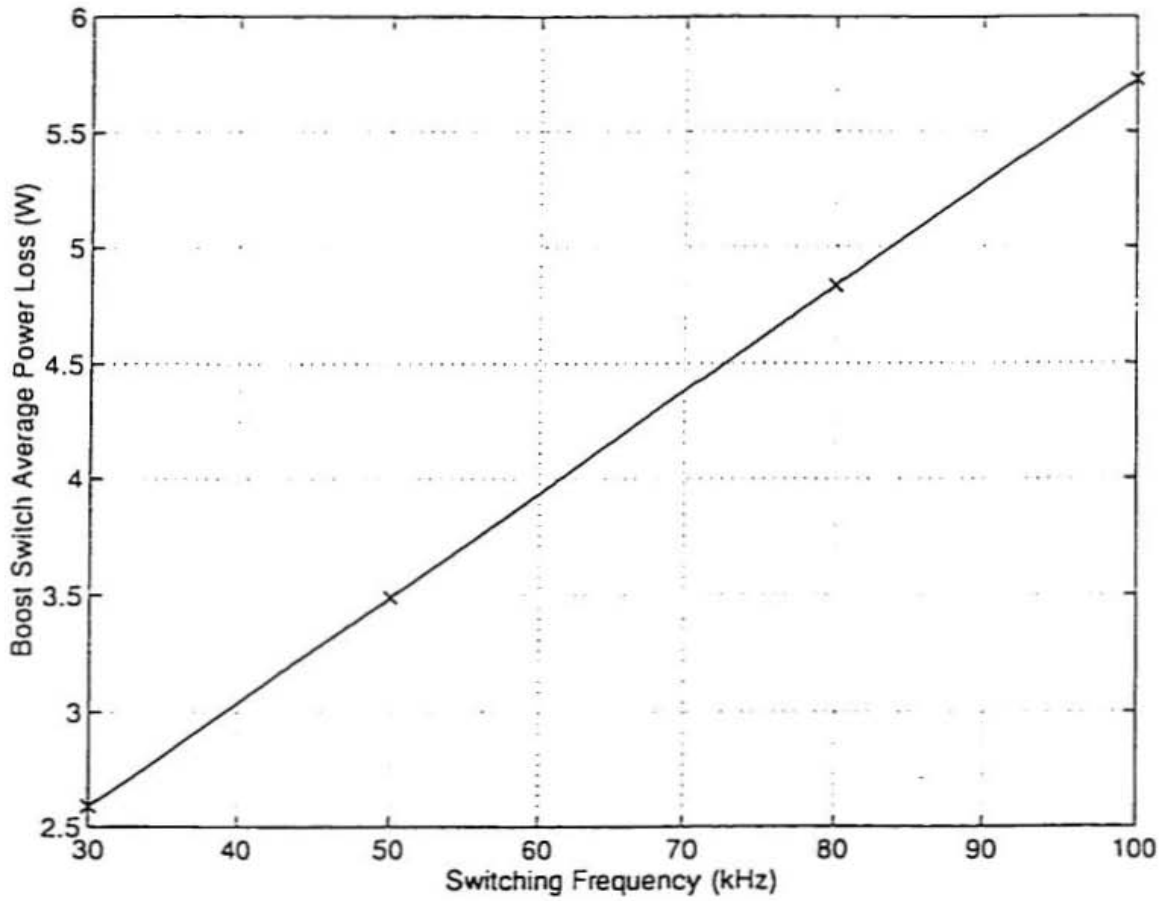


Figure 4.14: Power loss across the boost switch versus varying switching frequency

(L=0.1mH, C=470 μF , $C_r = 0.001\,\mu F$)

Keeping the switching frequency and boost inductor value constant, fig 4.15 shows the average power across the boost switch with respect to varying values of commutating capacitor. The average power tends to increase with increasing value of commutating capacitor. This is because the commutating capacitor holds more electric charge and in turn adds to the total charge of the boost inductor, giving rise to an increase in the input current.

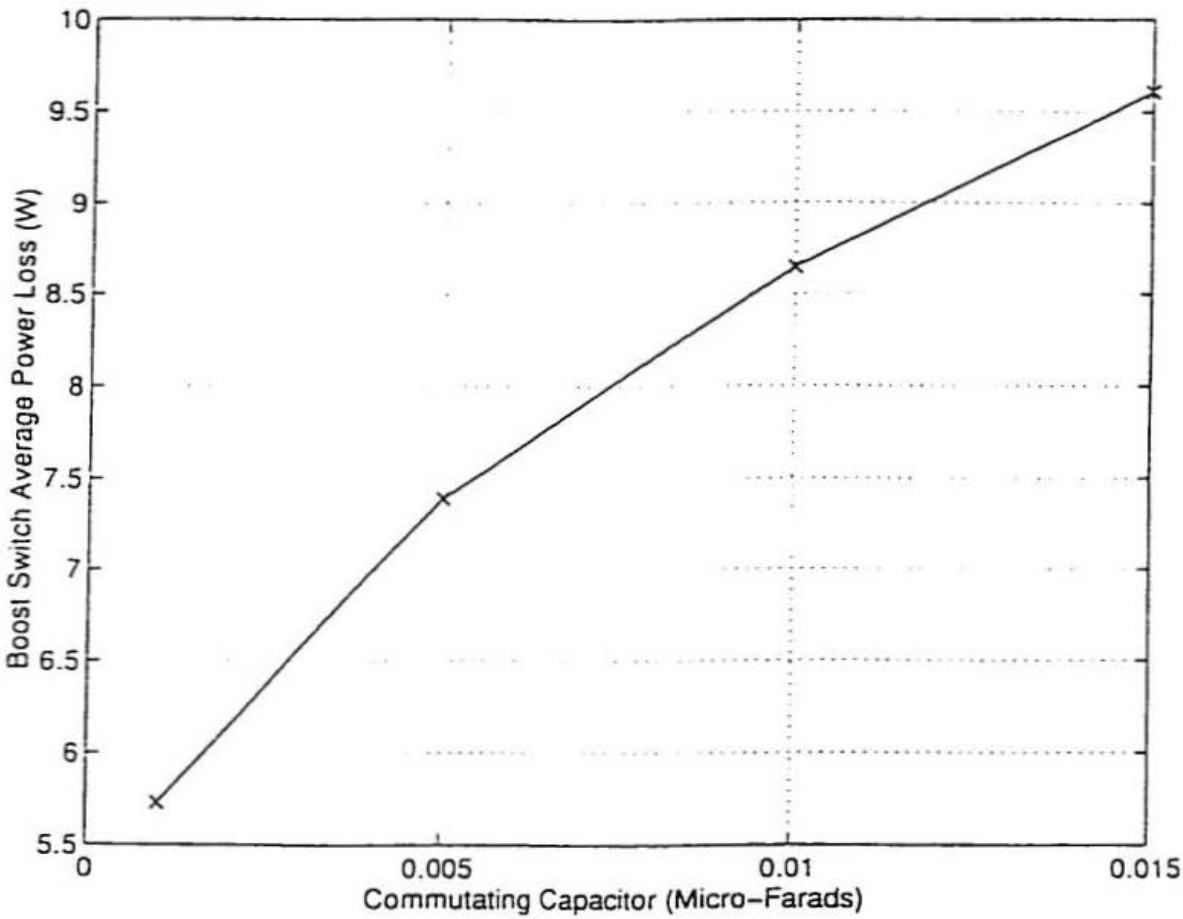


Figure 4.15: Power loss across the boost switch versus varying commutating capacitor

(L=0.1mH, C=470 μF , F_s =100kHz)

4.5 SUMMARY

The simulation results confirm the operation of the control schemes. The simulation results confirm the predicted waveform of the input current which shows that the boost switch turns ON and OFF at zero-current and zero-voltage respectively. The THD of this scheme is found to be less than that of CFDC scheme. It has been shown that the THD of the input current decreases with increasing boost inductor value and switching frequency. Keeping the switching frequency constant, the average power loss across the boost switch decreases with the increasing value of the boost inductor. However, the average power loss increases with the increasing value of switching frequency at constant boost inductor value.

The instantaneous value of the input current decreases with increasing boost inductor value. Moreover, the zero-current turn ON and zero-voltage turn OFF of the boost switch reduce the average power loss. The turn ON time decreases with increasing switching frequency which in turn reduces the THD of the input current. However, keeping the switching frequency and boost inductor value constant, the average power loss across the boost switch increases with increase of commutating capacitor value.

Although the operational characteristics show a definite improvement over the CFDC control, one drawback of the ZCS-ZVS scheme is that it is expensive as it requires more circuit components. Moreover, the ON/OFF timing of the switches have to be precise in order to obtain the full benefit of the ZCS-ZVS scheme. Generally, this requires a good synchronization logic.

Chapter 5

COMPARATIVE STUDY OF THE CONTROL SCHEMES

INTRODUCTION

So far, this thesis has dealt with the modelling and analysis of constant frequency current control, variable frequency current control methods. This chapter deals with the comparative study of all the control methods discussed before.

5.1 COMPARATIVE STUDY

Since the principle of operation of the zero-current zero-voltage (ZCS-ZVS) control and constant frequency discontinuous current (CFDC) control schemes are similar, both control methods are compared. Figure 5.1 shows a plot of the total harmonic distortion (THD) of the input current versus varying switching frequency, keeping the boost inductor value constant.

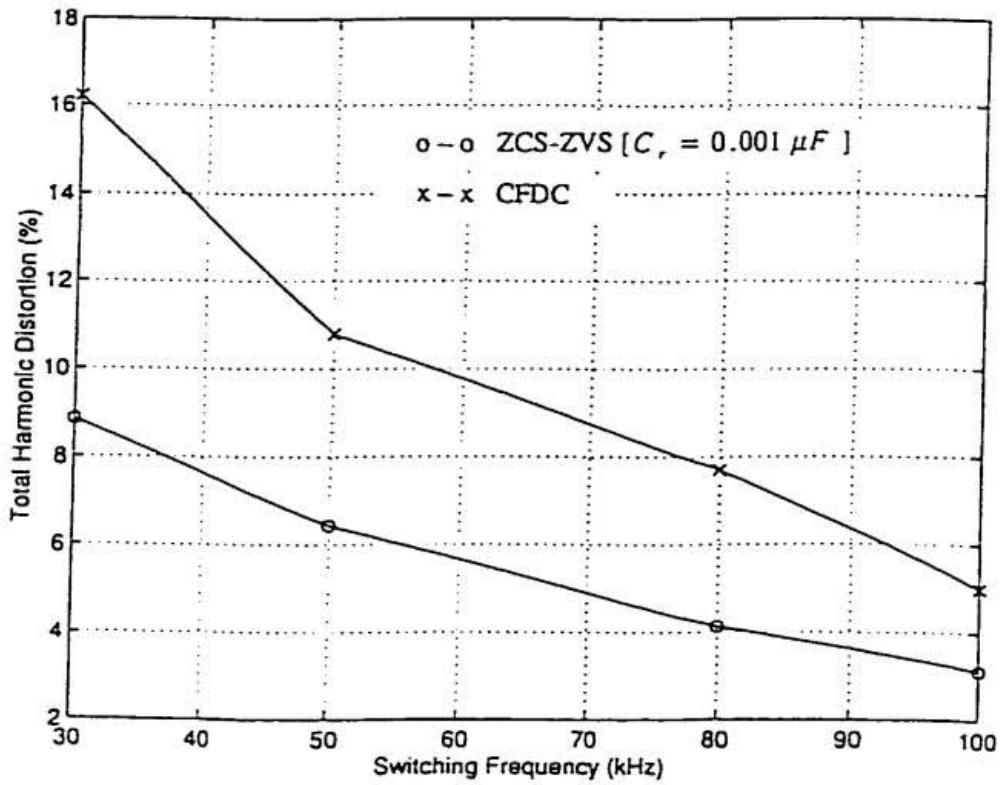


Figure 5.1: THD versus varying switching frequency

(L = 0.1mH, C = 470 μF)

Figure 5.2 shows a comparative plot of the THD of the input current versus varying boost inductor value, keeping the switching frequency constant. From figures 5.1 and 5.2 it can be seen that the ZCS-ZVS control scheme has less THD in the input current than the CFDC control.

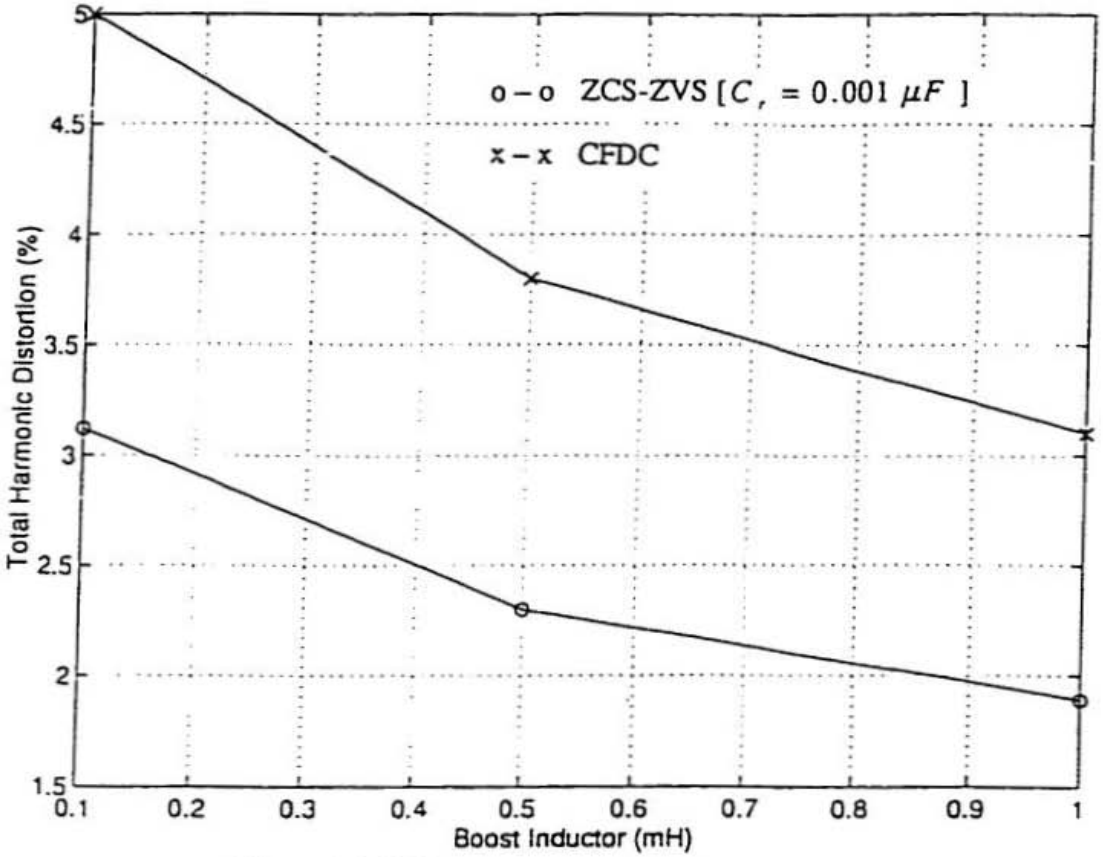


Figure 5.2: THD versus varying boost inductor value

(C=470 μF , F_s =100kHz)

Figure 5.3 shows the average power loss across the boost switch versus varying boost inductor value, keeping the switching frequency constant for the ZCS-ZVS and CFDC schemes.

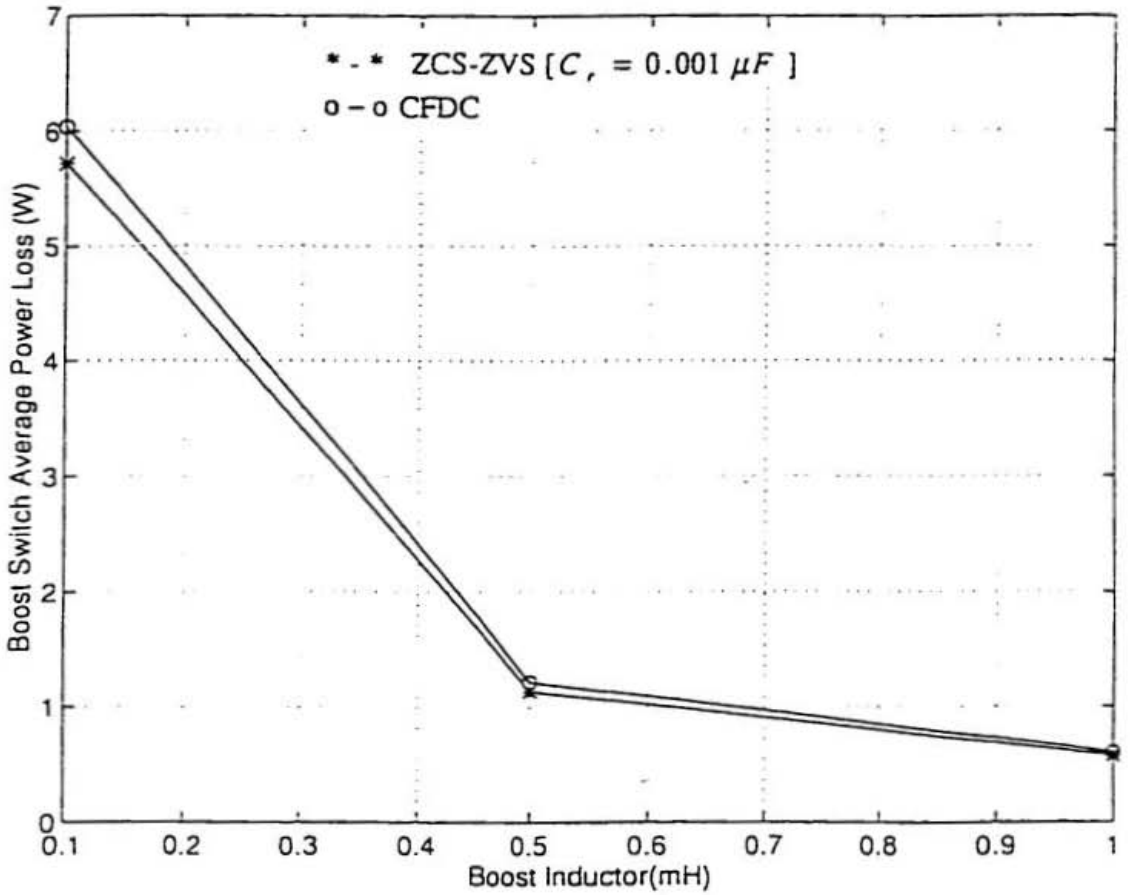


Figure 5.3: Power loss across the boost switch versus varying boost inductor

(C=470 μF , F_s =100kHz)

Keeping the boost inductor value constant, a plot of the average power loss across the boost switch versus switching frequency of ZCS-ZVS and CFDC control schemes is shown in fig 5.4. Figures 5.3 and 5.4 shows that the average power loss across the boost switch in the ZCS-ZVS scheme is lower than that of the CFDC scheme.

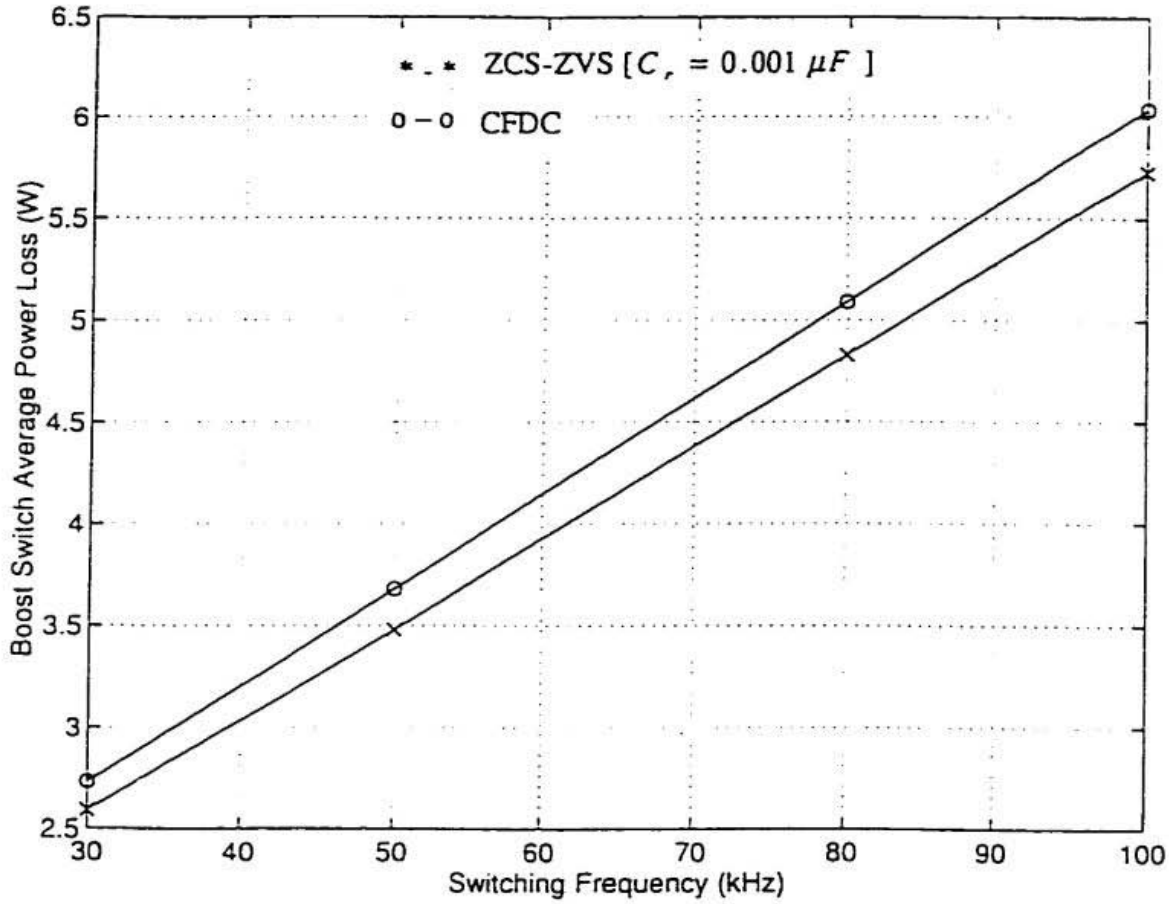


Figure 5.4: Power loss across the boost switch versus varying switching frequency

(L=0.1mH, C=470 μF)

The boost switch of the variable current hysteresis current (VCHC) scheme operates in variable switching frequency mode, whereas the switching frequency is constant for the CFCC, CFDC and ZCS-ZVS. The instantaneous switching frequency of the VCHC depends on the peak difference or the hysteresis band (δ). If the average switching frequency of the VCHC can be compared to that of the fixed switching frequency of CFCC scheme for the same circuit parameters, then the THD of the input current and power loss across the boost switch can be compared. Keeping the boost inductor value fixed, fig 5.5 shows a plot of the average power loss across the boost switch versus the switching frequency of the CFCC scheme and the average switching frequency of VCHC scheme.

It can be seen from fig 5.5 that the average power loss of the VCHC is slightly higher than that of the CFCC scheme. Fig 5.6 shows a comparative plot of average power loss across the boost switch versus switching frequency for the three constant frequency control schemes (CFCC, CFDC, ZCS-ZVS) for the same input voltage, output voltage and output power. It can be seen that the ZCS-ZVS scheme has the lowest average power loss.

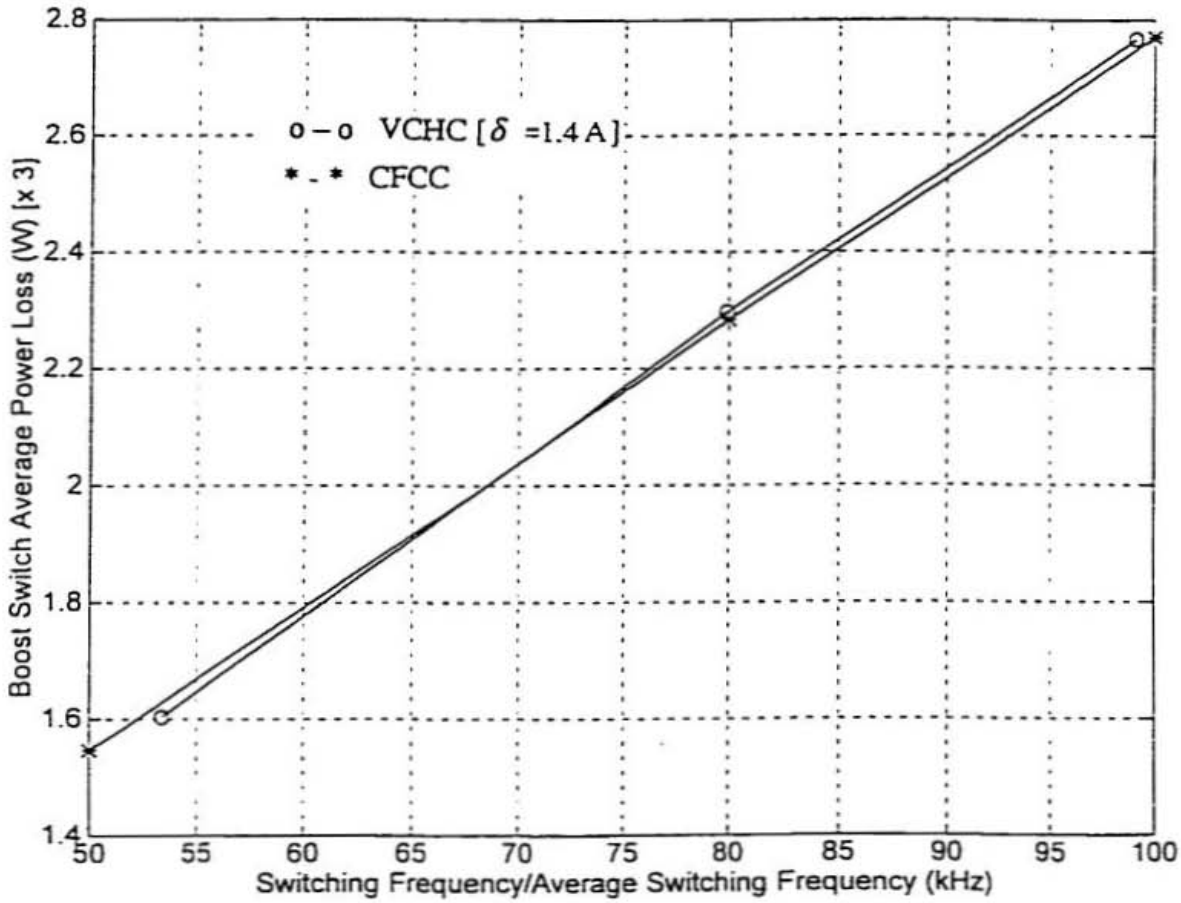


Figure 5.5: Power loss across the boost switch versus varying switching frequency

(L=1.5mH, C=470 μF)

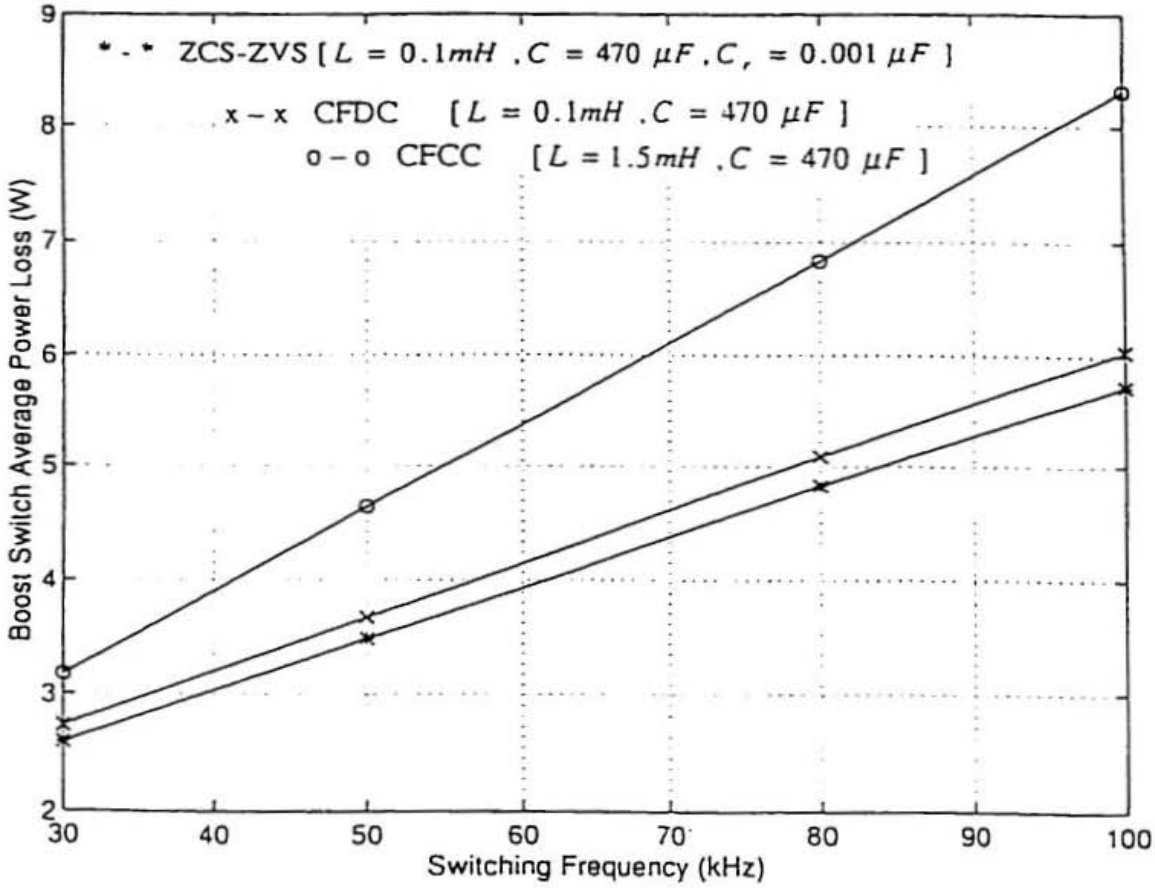


Figure 5.6: Power loss across the boost switch versus varying switching frequency

(V_s =240V (rms), V_o =380V(dc), P_o =400W)

Figure 5.7 shows a comparative plot of the THD of the input current versus switching frequency for the same input voltage, output voltage and power output for the constant frequency control methods. The THD of the input current for the ZVS-ZCS is the lowest of the three schemes. Table 5.1 shows the qualitative comparison of the four current mode control methods, namely the CFCC, CFDC, VCHC and ZVS-ZCS control schemes.

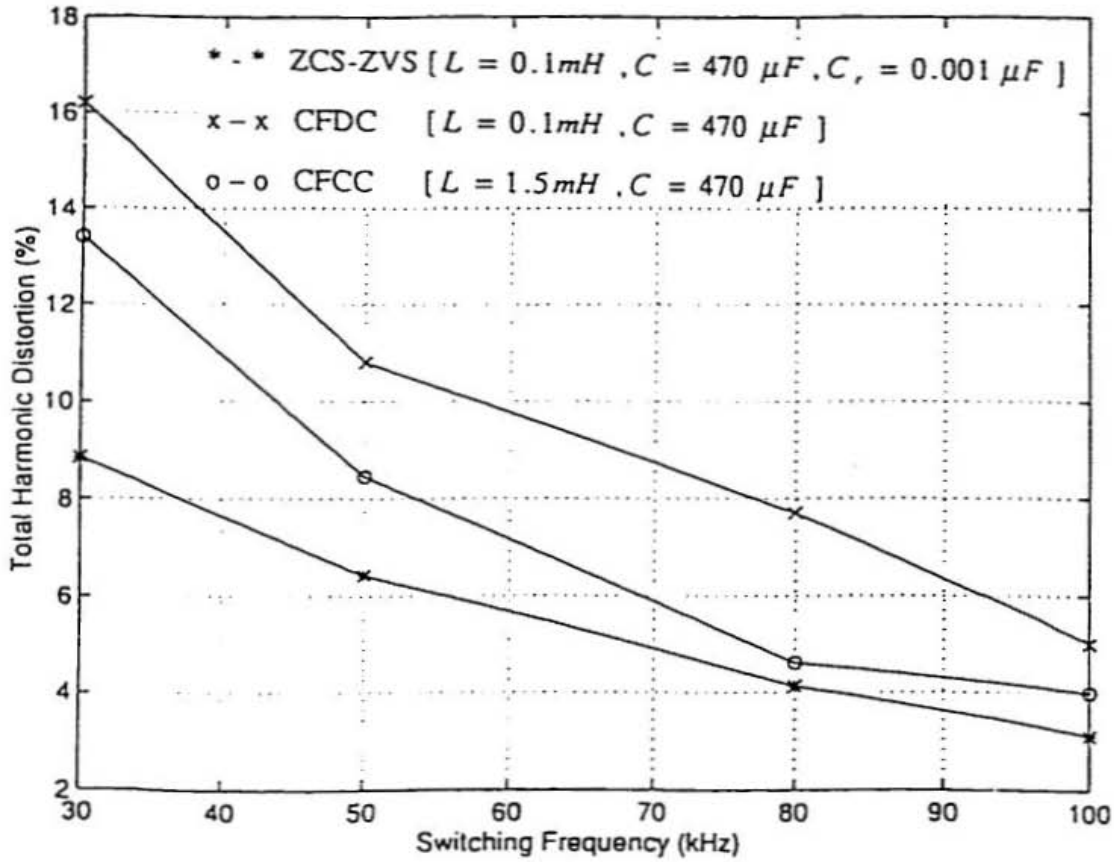


Figure 5.7: THD versus varying switching frequency

(V_s =240V (rms), V_o =380V(dc), P_o =400W)

Table 5.1: Qualitative comparison of CFCC, CFDC, VCHC & ZVS-ZCS control schemes

	CFCC	CFDC	VCHC	ZVS-ZCS
THD	MEDIUM	HIGH	LOW	LOW
Boost Switch Power Loss	HIGH	MEDIUM	HIGH	LOW
Input Filter Design	SIMPLE	SIMPLE	COMPLEX	SIMPLE

Chapter 6

CONCLUSIONS

In this thesis, the simulation of the four most popular current-mode control schemes for power factor correction, namely the Constant Frequency Continuous Current (CFCC), Constant Frequency Discontinuous Current (CFDC), Variable Current Hysteresis Control (VCHC) and the Zero-Current Zero Voltage switching (ZCS-ZVS) control has been carried out. The characteristic and performance of the schemes are presented.

From a power supply designer's standpoint, the most important objective is to choose an optimum control scheme so as to meet the design specifications. The comparative study carried out in this thesis provides a basis for selecting an optimum control scheme for a particular industrial application. The advantages and disadvantages of the schemes from the point of view of the quality of the input current waveform, input filter requirements, and the complexity of the control circuit for the same circuit conditions are discussed.

The simulation results of the CFCC control scheme show that the input current has continuous non-zero value throughout the full cycle of operation. With CFCC control the total harmonic distortion (THD) of the input current decreases with increasing

switching frequency. The THD also decreases with increasing boost inductor value at fixed switching frequency.

One drawback of the CFCC control scheme is that the response of the circuit is not precise since the desired average inductor current is not constant. Also, as the boost inductor current is continuous throughout the full cycle of operation, there is a higher power loss across the boost switch. Simulation results show that the average power loss tends to decrease with increasing boost inductor value and increases with increasing switching frequency. The control circuit of CFCC requires complex synchronization logic.

To decrease the continuous power loss across the boost switch of CFCC control scheme, the CFDC control scheme has been studied. The harmonic spectrum of the CFDC reveals the presence of higher order harmonics in the input current. The total harmonic distortion (THD) is higher and requires a substantial size of EMI filter to decrease the THD to the IEEE standards. On the other hand increasing the boost inductor value and the switching frequency decrease the THD. The CFDC control circuitry is easy to implement and requires no synchronization logic. A drawback of this scheme, however, is the high current stresses associated with the boost switch at the peak input voltage.

To further reduce the power loss of the boost switch in the constant frequency control methods, the Zero Current-Zero Voltage Switching (ZCS-ZVS) was proposed. Simulation results show that the boost switches are turned ON and OFF at zero-current and zero-voltage respectively. The THD of the input current decreases with increasing boost inductor value and switching frequency. The average power loss across the boost

switch increases with the increasing value of the switching frequency, but decreases with the increasing value of the boost inductor. However, the average power loss tends to increase with increasing value of commutating capacitor at fixed switching frequency and boost inductor. The ZCS-ZVS scheme is expensive and requires a good synchronization logic.

The switching frequency of the boost switch in variable current hysteresis control (VCHC) is not constant and it depends on the hysteresis band. The simulation results show that the inductor current is confined between the two boundary limits and is capable of producing nearly sinusoidal input current waveform. It is seen that the peak instantaneous switching frequency increases with decreasing hysteresis band. Simulation results also show that the average power loss across the boost switch, at fixed hysteresis band, decreases with increasing value of boost inductor. Moreover the average power loss increases with decreasing hysteresis band, at constant boost inductor value.

The frequency components of the input current for the VCHC scheme are evenly distributed making the design of EMI filter very difficult. The control circuit design is simpler and easy to install. However, the instantaneous switching frequency at zero crossing of the input voltage increases the switching stress of the boost switch.

Among all the control methods simulated, the constant frequency control schemes (CFCC, CFDC, ZCS-ZVS) would be the definite choice over the variable switching frequency control (VCHC) as the switching stress at zero crossing of the input voltage is less. Comparing the simulation results of the constant frequency control schemes for the same circuit conditions, it can be predicted that the zero-current zero-voltage switching (ZCS-ZVS) scheme is the best choice, in terms of average power loss across the boost

switch and total harmonic distortion (THD) of the input current. However, the synchronization logic of the boost switches of ZCS-ZVS scheme is difficult to implement, but with the development of microprocessor this can be overcome.

6.1 SUGGESTIONS FOR FUTURE WORK

The present work contains the comparative study of current-mode control schemes used in AC-DC rectifier circuits. Future work in this area may be stated as follows:

- A microprocessor implementation of the control schemes should be investigated, since a microprocessor-based system will enhance the noise immunity of the system.
- To improve the dynamic behaviour of the control methods, knowledge-based systems like Artificial Neural Network (ANN), Fuzzy logic based control methods should also be investigated.
- Though the primary aim of these control schemes is to obtain nearly unity power factor operation, it is possible to operate the circuits at leading power factor. This would allow the converter to be used as power factor correcting circuit for a utility system.
- While component sizes tend to decrease with an increase in the switching frequency, device switching losses are proportional to frequency and usually limit the maximum operating frequency attainable in a given circuit. Even with the availability of extremely fast power MOSFETs, a frequency of 100kHz seems to represent a typical maximum value. A switching frequency of 1 MHz is commonly considered the next

significant milestone for power converters rated in the hundreds of watts. Further work needs to be carried out to investigate the design and implementation of the power factor correction circuit for higher frequencies.

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APPENDIX A

The governing equations of the inductor current and capacitor voltage during the OFF state of the boost switch of the power factor correction (PFC) circuit are solved using MAPLE (version 5). The solution includes the stray resistances of the boost inductor and output capacitor. These equations are used in the thesis for the modelling of the PFC circuit.

A.1 MAPLE SOLUTION OF THE BOOST INDUCTOR CURRENT AND OUTPUT CAPACITOR VOLTAGE DURING THE OFF STATE OF THE BOOST SWITCH

The notations used in this calculation are as follows

Vin	supply voltage
L	boost inductor
C	output capacitor
Rs	series resistance associated with the boost inductor
Resr	series resistance associated with the output capacitor
Ro	load resistance
il	Instantaneous value of the inductor current
ile	Inductor current at the end of the OFF period
ils	Inductor current at the start of the OFF period

vc Instantaneous value of the output capacitor voltage

vce Voltage of the output capacitor at the end of the OFF period

vcs Voltage of the output capacitor at the start of the OFF period

v_{oe} Output voltage at the end of the OFF period

The general results at the end of the OFF period for the inductor current, capacitor voltage and output voltage are given as

$$i_{Le} = \left| \frac{2.F_1.B_1^2 - 2.C_1^2.E_2 - 2.C_1^2.E_3 - 2.F_1.C_1 + 2.B_1^2.F_1 + 2.B_1^2.E_2 - \sqrt{A_1}.V_{cs}.B_1^2 - 4.C_1^2.V_{cs}.L + 2.B_1^2.E_3 - 2.C_1^2.E_1 - \sqrt{A_1}.C_1.V_{cs} + \sqrt{A_1}.L.i_{Ls}.B_1 + 4.B_1^2.V_{cs}.L}{\left(L\left(-2.B_1^2.G_2 + 2.C_1.G_2 - 2.B_1^2.G_3 + 2.C_1.G_3 + \sqrt{A_1}.B_1^2 - 4.B_1^2.L - \sqrt{A_1}.C_1 + 4.C_1.L + 2.C_1.G_1 - \sqrt{A_1}.B_1 - 2.B_1^2.G_1\right)\right)} \right| \quad \text{A.1}$$

$$v_{oe} = \left\{ \frac{-\sqrt{A_1}.v_{cs}.B_1 + 2.C_1.i_{Ls}.R_{eq}.L + 2.C_1.V_{cs}.R_O - 2.B_1^2.i_{Ls}.R_{eq}.L - 2.B_1^2.V_{cs}.R_O}{4.C_1.G_2 - 4.B_1^2.G_2 + 4.C_1.G_3 - 4.B_1^2.G_3 + \sqrt{A_1}.B_1^2 + 2.C_1.L + \sqrt{A_1}.C_1 - 4.B_1^2.G_1 + 4.C_1.G_1 - \sqrt{A_1}.B_1 - 2.B_1^2.L} \right\} \quad \text{A.2}$$

$$v_{oe} = (v_{ce} + i_{Le} R_{esr}) \frac{R_O}{R_O + R_{esr}} \quad \text{A.3}$$

where

$$A_1 = G_3^2 + 2.C.R_{eq}^2.G_1 + 2.C.R_{eq}^2.G_2 - 2.L.G_3 + G_2^2 + 2.C.R_O^2.G_1 - 2.L.G_2 + G_1^2 - 2.G_1.L + L^2 + 4.L.C.R_O^2$$

$$B_1 = e^{\left(0.5 * \frac{\left(2.C.R_{esr}.R_{eq} + 2.C.R_O.R_{eq} - \sqrt{A_1} + 2.L + 2.C.R_O.R_{esr}\right).t}{(R_{esr} + R_{eq}).L.C} \right)}$$

$$C_1 = e^{\left(2.\frac{t.(C.R_O.R_{esr} + C.R_O.R_{eq} + C.R_{esr}.R_{eq} + L)}{(R_{esr} + R_{eq}).L.C} \right)}$$

$$E_1 = V_i.C.R_{esr}.R_O \qquad E_2 = V_i.C.R_O.R_O$$

$$E_3 = V_i.C.R_O.R_{esr} \qquad F_1 = L.v_{ce}.R_O.C$$

$$G_1 = R_{esr}.R_O.C \qquad G_2 = R_s.R_O.C$$

$$G_3 = R_s.R_{esr}.C$$