EXPERIMENTAL TESTING OF STAND-ALONE DIGITAL RELAY FOR POWER TRANSFORMERS

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Experimental Testing of Stand-Alone Digital Relay for Power Transformers

By

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A thesis submitted to the School of Graduate Studies in partial fulfillment of the requirements for the degree of Master of Engineering Faculty of Engineering and Applied Science Memorial University of Newfoundland

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Abstract

The differential protection scheme is one of the most widely used techniques in power system protection, especially for power transformers. This method extracts harmonic components from current signals via current transformers using various digital filtering algorithms to make protection decisions. Different researchers reported that they have found the best algorithms for their transformer differential protection schemes. However, since their test results are usually based on different equipment, it is difficult to compare the relative performance of the test results. For the protection of various types of transformers, both the hardware and software of the earlier protection units may have to be changed.

Presented in this thesis is a stand-alone microprocessor based digital relay
that has been designed and implemented. Only the software modification is required to accommodate the protection of different types of transformers. The
hardware portion of the design consists of seven identical scaling circuits, a sixth
order Chebyshev anti-aliasing filter, a sample-and-hold circuit, and a multiplexer
which is connected to an analog-to-digital converter on the TMS32010 boards. The
TMS32010 signal processor is used to compute the power transformer data. The
digital relay is designed in a modular form such that the hardware part is a "black
box" to the news.

The software has been written in TMS assembler language which includes second and fifth harmonic restraints with ground fault plus internal and external protection. Five digital filtering algorithms are used to extract the harmonic components. These algorithms are: Discrete Fourier Transform, Walsh Functions Algorithm, Rectangular Transform Algorithm, Finite Impulse Response filtering, and Least Squares Algorithm. The digital relay was tested extensively in the laboratory using the five algorithms. By comparing the real time performance of these algorithms. Discrete Fourier Transform (DFT) was found to be the best among the algorithms presented. As a result, a transformer protection test set-up has been developed using DFT. This test set-up can be used for the protection of any kind of three phase transformer with minor changes on the relay software.

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Chapter 1

Introduction

For the past twenty years, there has been a lot of interest in the area of digital protection of power systems. Digital relays using minicomputers were proposed in the early 1970s and were mainly tested to be used for the protection of transmission lines [1, 2]. However, this has encouraged many researchers to investigate the feasibility of designing digital relays for other power system applications.

The introduction of low-cost microprocessors has made it possible to design and implement digital protection schemes for power system and power apparatus. The capability of minicomputer based digital relays can now be demonstrated by the use of microprocessors with the improvement of reliability, speed, simplicity, performance, and with the decreasing in cost.

The protection of the three phase power transformer poses a challenging problem for relay designers. A designer has to consider the magnetizing inrush during the energisation of the transformer, the over-excitation condition resulting from dynamic over-voltage, tap changing, current transformer saturation, internal ground fault and external faults, etc.. The differential protection scheme is a popular method used by most transformer protection designers in building a microprocessor based digital relay. Description of this protection scheme is presented in this thesis. As the name suggested, a digital relay requires the sampling of signals to obtain digital data to perform analysis to operate. For differential transformer protection, three transformer current signals from the primary side, three current signals from the secondary side and one ground current signal are needed to be sampled. These sampling data are then digitally filtered by an algorithm to extract the current harmonic components. A digital filter algorithm is the heart of any microprocessor based digital relay. It uses the sampled current signals and performs some specific computations which will tell whether the transformer is faulty or not, and at the same time clear the fault if there is one.

1.1 Purpose of this thesis

Protection algorithms play the most important role in transformer protection schemes. They provide the accuracy and speed for the digital relay operations. There are various technical publications available on microprocessor based three phase transformer relay algorithms for power transformer protection. Their authors had claimed that they had achieved accuracy, speed, computational burden, etc. using these algorithms. It is really very difficult to find out the real significance of these algorithms since these were evaluated using different models either by computer simulation or by on-line/off-line tests. Analysis of different algorithms are presented in this thesis.

The purpose of this research is to find out the best algorithm for transformer protection in terms of speed, accuracy, and performance on different kinds of fault. One way to compare the accuracy of various algorithms is to find their frequency responses. However, this thesis does not consider this aspect. Instead the comparisons will be made in a more practical point of view, which is based on real time testing results using a three phase power transformer. Five algorithms were chosen for testing. They are Discrete Fourier Transform (DFT), Walsh Functions Algorithm (WFA), Rectangular Transform Algorithm (RTA), Finite Impulse Response (FIR) filtering, and Least Square Algorithm (LSA). The reasons for choosing these algorithms are that they are simple and will not need a 1-4 of computation time.

After an algorithm is selected, a transformer protection test bench will be developed with the selected algorithm. This test bench is a relay module which can be used for protection of any kind of three phase power transformers. The hardware part of this relay will be a 'black box' to a user. The only part the user has to be concerned about is the data part of the software. The user only has to change threshold values in the software to accommodate different type of power transformers.

The hardware part of this test bench consists of seven identical scaling circuits, a sixth order Chehyshev anti-aliasing filter, a sample-and-hold circuit and a multiplexer which is connected to the A/D converter on the TMS32010 boards. The TMS32010 boards consists of a digital signal processor with 4K-word program memory, 144-word data memory, and digital input/out ports. The software is written on the TMS assembler which consists of second and fifth harmonic restraints with ground fault plus internal and external protection. A program written in C has been developed for the analysis of all five algorithms using the real time data obtained from the power transformer. All tests have been done at both no load and load conditions.

1.2 Outline of this thesis

Chapter 2 gives the background information about the non-linear characteristic of a three phase power transformer. This includes the magnetizing inrush, overexcitation and the saturation of current transformer. The percentage differential with harmonic restraint transformer protection scheme is also described here. Chapter 3 reviews the various algorithms for power transformer protection which are available from various papers. These methods, equipment used and test results are briefly described.

Chapter 4 describes the hardware of the laboratory relay module.

Chapter 5 describes the software of the laboratory relay module.

Chapter 6 describes the test results of each algorithm in the laboratory, hence the best algorithm is selected.

Chapter 7 contains conclusions and comments on possible future developments.

Chapter 2

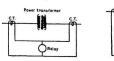
Transformer Protection Fundamentals

The differential protection scheme is one of the most widely used techniques in power system protection. It is used especially for transformers. The following sections will give some background on a differential protection technique, basic transformer protection problems and a three phase transformer protection scheme.

2.1 Principle of Differential Protection

The circulating current principle is the basis of differential protection. It involves a direct comparison of the electrical quantities entering and leaving the protected area. Current transformers having suitable ratios of transformation are used at both ends of the protection zone to accomplish the comparison. These current transformers have their secondary connected as shown in Fig 2.1(a). Ideally, the sum of currents flowing in is equal to the sum of currents flowing out during normal operation. If the net current is not zero, an internal fault exists and the difference current can operate the associated relay. This is usually called the unbiased protection scheme.

However due to various factors such as magnetizing inrush current, current transformer saturation, etc., an ideal condition may not be obtainable in trans-





- (a) Overall Differential Relay
- (b) Percentage Differential Relay

Figure 2.1: Differential protection of transformers [3]

former protection. In this case some spill or unbalanced current will flow into the differential relay and then the relay will tend to operate if some form of restraint is not provided. Thus a biased differential relay is needed. Such a relay is shown in Fig 2.1(b). The operating coil is used for the vector sum of currents in the transformer windings while the restraining coils are used for the through-current. Spill current is expressed as a percentage of the through-current in the restraining coil. In this case the relay will operate only when the spill current exceeds the relay bias setting ratio.

2.2 Basic Protection Problems

In general, the internal faults in a transformer provide significant operating current for the relay to operate. However, as mentioned earlier, a simple differential arrangement may be handicapped by difficulties such as inrush, over-excitation, and saturation, etc..

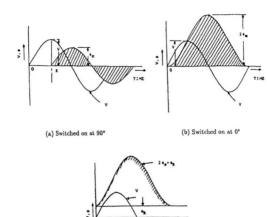
2.2.1 Magnetizing Inrush Current

When a transformer is energized, a transient magnetizing or exciting current will flow which appears as an internal fault to the differential relay. The peak value of this inrush current may exceed 8 to 30 times the full load peak [4]. To prevent relay misoperation, the identification of the inrush currents is important.

Single Phase Transformer

When a single phase power transformer is connected to the supply with its secoudary circuit open, the steady state flux waveform Φ in the core is normally in quadrature with the supply voltage waveform V, neglecting the winding resistance. Switching in the transformer at any point of the voltage waveform will cause the core flux to have a similar waveform as the voltage with a phase shift and different amplitude. Its starting point will depend upon the residual flux Φ_R in the core.

For an initially unmagnetized core, if the switch is closed at 90° of the voltage waveform them flux will start increasing from zero at that point as shown in Fig 2.2(a). Ideally, the flux will lag the voltage by 90°. In case of Fig 2.2(b), the switch is closed at a zero value of the voltage waveform with no residual flux. It is evident that the peak value attained by the flux will be $2\Phi_m$, where Φ_m is the maximum value of the steady state flux. If at the instant of closing the switch, the core has a residual flux value of Φ_n , the resultant peak value of the flux becomes



(c) Switched on at 0° with residual flux

Figure 2.2: Effect of switching on at 0° and 90° of supply voltage and residual flux [6]

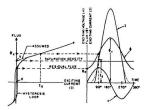


Figure 2.3: Deviation of magnetizing inrush current from excitation characteristic [7]

 $2\Phi_m + \Phi_R$ as shown in Fig 2.2(c).

A simplified excitation curve in Fig 2.3 can be used to describe the formation of the inrusl current. The curve is assumed as two straight lines from O to S and from S to P. The inrush current I can be determined graphically by extending the curve OSP with instantaneous flux values. The flux wave ϕ at 90° for example, can be used to determine the value of ϕ_x which in turn yields I_x . All other inrush current values can be found by a similar procedure. Another simple method is to use digital simulation for inrush current [5].

Three Phase Transformer

In case of a three phase transformer, the inrush phenomenon is complicated by the fact that there may be inrush currents in more than two phases when switched-on to the power supply. The instantaneous values of inrush currents in the three phases will be affected by electric connections and magnetic coupling between the phases.

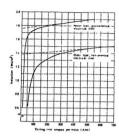


Figure 2.4: Trend in transformer steel magnetizing characteristics [8]

The energizing inrush also depends substantially upon the residual magnetization in the transformer. The maximum residual will be near the y-intercept of the magnetizing curve projection as shown in Fig 2.4. This value is approximately 1.8 T for new transformers and 1.4 T for older ones. The modern transformer tends to have more inrush current.

Since the inrush current exists only on the primary side of the transformer, the
inrush current will appear as an internal fault and operate the relay. However,
inrush and fault currents can be distinguished on the basis that the differential
current in the inrush case will have a considerable amount of second harmonic,
while in the fault case, it will have negligible second harmonic component. The
problem can be solved by using the differential relays with harmonic restraint or
harmonic blocking schemes as described in later section.

2.2.2 Over-excitation

A typical transformer containing a good quality grain oriented steel is expected to operate with a peak magnetic flux density in the steady state of 1.67 to 1.87 [9]. If the peak magnetic flux density exceeded the above range, the transformer is said to be overexcited. Over-excitation of the transformer is closely related to inrush current resulting from the opening of power supply lines, excessive applied voltage, clearing of system faults. These cause rise of voltage, load rejection, a below-normal supply frequency or misoperation of a tap-changer device etc. Although it is not generally considered as a fault, too much over-excitation may cause winding and core damage. Extreme over-excitation can destroy a transformer in seconds.

It is not possible to protect against all over-excitation by fusing. Damage or false tripping of a fuse for a transformer can be caused by a combination of overexcitation and less than optimal fuse selection. Fortunately, increase current flow around the peak produces significant third and fifth harmonics which distinguish over-excitation from load current or fault current. While the 3rd harmonic is suitable for this function, it has not been used because it may be stopped by the transformer itself or by a three phase current transformer with delta connection on the wye side [3].

As a general rule, a 40% fifth harmonic restraint is desirable to prevent tripping from normal over-excited conditions [10]. Higher than this restraint value, the overvoltage may actually damage the transformer and the relay will trip the transformer off the line. To obtain a good measurement of the fifth harmonic for a digital relay, a sampling rate of 12 to 16 samples per cycle is required.

2.2.3 Current Transformer Saturation

In general, the current transformer is the most critical part in the differential protection scheme, since it provides data for protection analysis. In contemporary power systems, saturation of the current transformer is likely to occur for heavy external and internal faults, due to the slow decaying affect current components of the fault current. The direct current component siese because the current in an inductance cannot change instantaneously and the steady state current, before and after a change, must lead or lag the voltage by a certain power factor angle [4].

Saturation causes extensive transient error which may affect the performance of the differential relay. This problem can be solved by providing a percentage bias for the relay. For the the large value of a internal fault, saturation may not be a scrious problem as long as it is not severe enough to delay relay operation. Usually an instantaneous tripping is provided in the protection scheme for the case of heavy internal fault to prevent relay misoperation.

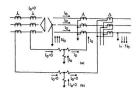
2.3 Three Phase Transformers Differential Protection

Basic differential protection can also be applied to three phase transformer protection. However, the protection scheme is more complicated because more than one phase has to be considered.

2.3.1 Current Transformer

Current transformers (CTs) play a very important role in transformer differential protection. It is the component from which current data can be obtained for analysis to decide whether or not a fault has occurred. For a single phase transformer, only two current transformers are needed. In the three phase case, at least six CTs have to be used. Three CTs are used for the primary side and another three CTs for the secondary. Their connections and characteristics have to be carefully examined to prevent relay misoperation.

As a general rule of thumb, the current transformers on the Delta side of a transformer bank have to be connected in Wye. Similarly current transformers on the Wye side have to be connected in Delta. The reason for these connections is to block the zero sequence current on external ground faults and to compensate for the 30° phase shift introduced by a Wye/Delta transformer bank. Fig 2.5 shows that zero sequence current will flow to the circuit if there is an external ground fault. If the current transformers are connected in delta, zero-sequence current can only circulate inside the current transformer and cannot trip the relay. Otherwise if connected in wye, the spilled current may operate the relay. Also if current transformers are connected in delta, their secondary rating have to be reduced by $\frac{1}{\sqrt{3}}$ times the secondary rating of Wye connected current transformers so that the current outside the Delta may balance with the current of the Wye connected



- (a) I₀ will flow in the differential circuit if current transformers were connected as were causing relay misoperation.
 - (b) No current will flow in the differential circuit if current transformers were connected as delta.

Figure 2.5: Example for Delta connected current transformers on Wye connected windings[4]

current transformers.

Current transformers should also have a primary rating to match the rated current of the three phase transformer because the rated current is usually in inverse ratio of the corresponding voltages on the primary and secondary sides. Furthermore, if the three phase transformer has a tap changing facility enabling its ratio to be varied, the differential protection system must be able to accommodate the change. It should provide a percentage bias to incorporate maximum ratio deviation to ensure a sensitive and stable system.

2.3.2 Differential Relaying with Harmonic Restraint

Inrush current always appears as unbalanced and is hardly distinguishable from internal faults. The normal bias is ineffective in differential protection under this

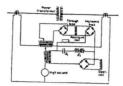


Figure 2.6: Basic circuit of harmonic restraint relay [3]

condition. In order to make differential relays insensitive to magnetic inrush current, harmonic restraint or harmonic blocking is needed. Harmonic restraint can rectify inrush currents and add them to percentage restraint as shown in Fig 2.6. This is done by inductor-capacitor filtering. This diagram shows only the protection for a single phase transformer but it can be applied to a three phase one. The relay is adjusted so that it will not operate when the restraining second harmonic exceeds a certain percentage of the operating fundamental current. The percentage is based on the type of transformer used. Owing to the fact that a direct current offset and harmonic components may also be present in fault current, an overcurrent unit is usually provided in the differential unit so that fast tripping can be assured for all heavy faults.

In harmonic blocking, a separate blocking relay whose contacts are in series with a differential relay so that the blocking relay will operate if the second harmonic is less than a certain percentage of the fundamental as shown in Fig 2.7.

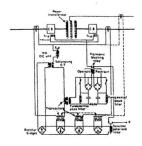


Figure 2.7: Basic circuit of harmonic blocking relay [3]

Chapter 3

Review of Work Done on Transformer Protection Algorithms

This chapter describes the research performed on transformer protection algorithm in the past years. These algorithms are actually implemented as programs of a microprocessor based relay which operate on the samples of voltage and/or current to form a basis of the relaying decision. Most of the existing algorithms can be classified into two categories. The first type is based on a model of the current or voltage waveform and the second one involves a series of R-L models of a system. Since the parameters of resistance, R and inductance, L are not important in transformer differential protection scheme, the second type of algorithms is not considered in this thesis.

3.1 Waveform Type Algorithms

The waveform type algorithms and their test results are briefly discussed in this section. Some of the tests are based on computer simulation while others are based on on-line testing for different computer hardware and software.

3.1.1 Recursive Bandpass Filter Approach

Sykes and Morrison [11] used two recursive bandpass filters (50 Hz and 100 Hz) for harmonic restraint differential protection of transformers. Fault and magnetizing inrush currents are distinguished on the basis of fundamental and second harmonic components derived from the sampled differential current through the digital bandpass filters. The digital realization of the 50Hz filter is:

$$y1_n = 0.096x_n - 0.096x_{n-1} + 1.810y_{n-1} - 0.905y_{n-2}$$
 (3.1)

and the realization of the 100Hz filter is:

$$y_{2n}^2 = 0.045x_n - 0.045x_{n-1} + 1.580y_{n-1} - 0.953y_{n-2}$$
 (3.2)

where $x_i =$ the input current sample.

 y_i = the output current sample.

The value of $y1_n$ represents the operate current signal and $y2_n$ represents the restraint signal. For the operate current greater than the restraint current, a fault is declared and a trip signal is sent. This scheme had been programmed for off-line testing. The computer used was an IBM 360/50 with the use of FORTRAN IV for program development. Programs were developed to compute simulated internal fault and inrush current waveforms for single-phase transformers only. This algorithm is quite simple but the fault response time is very slow. The relay operates adequately in the cases of inrush and internal fault. However, the results are all based on simulation and should be tested in real time.

3.1.2 Cross-Correlation Approach

Malik et al. [12] presented the harmonic differential protection approach based on a cross-correlation technique. This is very similar to the Discrete Fourier Transform algorithm. The algorithm is used for the separation of fundamental and second harmonic components of the differential current. If fundamental component exceeds the second harmonic by 15%, a trip signal is sent. The cross-correlation functions of sine and cosine are in the form:

$$\Phi_{i1} = \frac{1}{N} \sum_{k=1}^{N} i_{k-1} \sin(\frac{2j\pi}{N}(k-1)) \qquad (3.3)$$

$$\Phi_{i2} = \frac{1}{N} \sum_{k=1}^{N} i_{k-1} \cos(\frac{2j\pi}{N}(k-1))$$
(3.4)

where $i_{k-1} = (k-1)$ th sample of the differential current.

 $\Phi_{i1}, \Phi_{i2} = \text{sine and cosine, or, odd and even components}$

of differential current, respectively.

j = j-th harmonic.

N = number of samples per window.

The magnitude of the nth harmonic component of the differential current I_n is as follows:

$$I_n = \frac{2}{N} \sqrt{\Phi_{i1}^2 + \Phi_{i2}^2}$$
(3.5)

In order to make this algorithm more practical, the arithmetic operation required has to be speeded up. The differential current can correlate with even and odd square wave references. In this case, all data manipulations can be done by simple addition and subtractions. However, since a square wave contains odd and even harmonics itself, the results obtained are not quite accurate.

The cross-correlation algorithm was tested using off-line simulation on a CDC 6400 computer. The detection and tripping of the internal fault were done approximately within $\frac{1}{2}$ to $\frac{3}{4}$ cycle of a 60 Hz waveform using sine and cosine functions and $12 \, ms$ to $15 \, ms$ for even and odd waveforms. The algorithm should also be tested in real time for verification.

3.1.3 Finite Impulse Response Approach

Schweitzer et al. [13] presented an inrush current-detection algorithm which does not require multiplication or division by using simple digital filters. The filters used in this algorithm are Finite Impulse Response Filters having values of either plus or minus at any instant during the period of one cycle. Using the time discrete current samples i_m the algorithm basically consists of determining the following four coefficients:

$$S_1 = \sum_{m=0}^{k-N/2} (i_m - i_{m+\frac{N}{2}})$$
(3.6)

$$C_1 = \sum_{m=k-N+1}^{k-3N/4} (i_m - i_{m+\frac{N}{4}} - i_{m+\frac{N}{2}} + i_{m+\frac{2N}{4}})$$
 (3.7)

$$S_2 = \sum_{m=k-N+1}^{k-3N/4} (i_m - i_{m+\frac{N}{4}} + i_{m+\frac{N}{2}} - i_{m+\frac{2N}{4}})$$
 (3.8)

$$C_2 = \sum_{\substack{m=k-N+1\\ i_{m+\frac{N}{2}} - i_{m+\frac{N}{2}} - i_{m+\frac{N}{2}} + i_{m+\frac{N}{2}} + i_{m+\frac{N}{2}} + i_{m+\frac{N}{2}} + i_{m+\frac{N}{2}} - i_{m+\frac{N}{2}} - i_{m+\frac{N}{2}} + i_{m+\frac{N}{2}})$$
(3.9)

where N = Number of samples per data window.

k = kth sample period.

In order to check for an inrush condition, the following additional algorithms are used:

$$F_1 = max(|S_1|, |C_1|)$$
 (3.10)

$$F_2 = max(|S_2|, |C_2|)$$
 (3.11)

If both F_1 and F_2 are equal to zero, then an inrush condition does not exist and if F_2 was greater than $\xi_0 F_1$, where ξ_0 is the selected threshold value, then an inrush condition exists. The threshold value was chosen to be 15%.

The algorithm was tested in a FORTRAN program using simulated fault and inrush current data with a sampling rate of 8 samples per cycle. The performance of this algorithm is good only at low sampling rate and the detection of inrush current is done approximately in one cycle. Also this algorithm can only be used to detect even harmonics. The detection of fifth harmonic in the transformer over-excitation case cannot be done by this method.

3.1.4 Fourier Transform Approach

Ramamoorty [14] was the first to propose that fundamental current or voltage be extracted from the fault transients by correlating one cycle of data samples with reference sine and cosine stored samples.

Thorp and Phadke [15] presented the Discrete Fourier Transform algorithm (DFT) for digital protection of power transformer as followirer Transform algorithm (DFT) for digital protection of power transformer as follows:

$$I_n = \frac{1}{N} \sum_{k=0}^{N-1} I_k c^{j(\frac{2kn}{N})}$$
(3.12)

where $I_n = n$ -th harmonic component of the differential current.

 $I_k = k$ -th sample of differential current.

N = number of samples per cycle.

The algorithm was tested on data obtained from a model transformer off-line using a sampling rate of 12 samples per cycle. The response of the DFT algorithm was about one cycle for internal fault.

3.1.5 Rectangular Transform Approach

Rahman and Dash [16] presented the rectangular transform technique to extract the fundamental and harmonic components from the digital samples. If any waveform is sampled at time t_J , spaced Δt apart, so that there are $N=\frac{T}{\Delta t}$ samples, then the Fourier Transform coefficients S_k and C_k can be written as:

$$S_k = \frac{2}{N} \sum_{i=0}^{N-1} X(t_j) \sin(\frac{2\pi k j}{N})$$

$$C_k = \frac{2}{N} \sum_{i=0}^{N-1} X(t_i) \cos(\frac{2\pi k j}{N})$$
 (3.13)

where $X(t_i)$ = the discrete sampled current signal.

The sine and cosine terms in Eqn (3.13) are then replaced with the equivalent rectangular functions:

$$\sin \gamma t(x) = sgn(\sin x)$$

 $\cos \gamma t(x) = sgn(\sin x)$ (3.14)

where

$$sgn(y) = \frac{y}{|y|}, for y \neq 0$$

= 0, $for y = 0$ (3.15)

Using this method for transformer differential protection, the Fourier coefficients can be obtained as:

$$S_1 = S_1 - \frac{1}{3}S_3 - \frac{1}{5}S_5$$

 $C_1 = C_1 - \frac{1}{3}C_3 - \frac{1}{5}C_5$
 $S_2 = S_2$
 $C_2 = C_2$
 $C_3 = S_5$
 $C_5 = C_5$ (3.16)

where $\hat{S}_1, \hat{C}_1...\hat{S}_5, \hat{C}_8$ are the rectangular coefficients obtained from sampled differential current.

The fundamental and harmonic contents of the differential current can then be determined as:

$$I_n = \frac{2}{N} \sqrt{S_n^2 + C_n^2}$$
(3.17)

where $I_n = n$ -th harmonic component of the differential current.

N = number of samples per cycle.

The algorithm was tested by simulating transformer data programmed on a PDP-11/60 computer. The response was approximately one cycle for internal fault. The protection scheme was then implemented online using an Intel 8085 microprocessor with other peripherals and the algorithm was tested on data obtained from a 3-phase 400V 50Hz laboratory transformer using a sampling rate of 12 samples per cycle. The preliminary testing result had shown good performance on the algorithm. However, a complete set of testing has not been carried out.

3.1.6 Walsh Functions

Horton [17] proposed a special method for impedance distance relaying for faultprotection of a high-voltage power lines. The method is for computing impedance from data samples and employed mainly computer operations of add, subtract, and shift. This method is based on the use of Walsh functions. The performance of Walsh functions is tested first by a Fourier analysis and then by a Walsh analysis on impedance using IBM System/7.

For Fourier analysis, the impedance by definition is:

$$|Z| \equiv \frac{(\sqrt{F_1^2 + F_2^2})_{voltage}}{(\sqrt{F_1^2 + F_2^2})_{current}}$$
(3.18)

where F_1 and F_2 are the components of Fourier coefficients.

For Walsh Functions analysis, the impedance can be found as:

$$|Z| = \frac{\{1.0822(|W_1| + |W_2|) - 0.414||W_2| - |W_1||\}_{voltage}}{\{1.0822(|W_1| + |W_2|) - 0.414||W_2| - |W_1||\}_{urrent}}$$
(3.19)

where F_1 and F_2 are the components of Walsh coefficients.

The impedance calculation for Fourier takes 211.2 μ s and for Walsh takes 170.4 μ s. Both methods were competitive and the Walsh function was faster. However, the accuracy of the Walsh Function analysis was less than the Fourier method. Jeyasurya and Rahman [18] applied Walsh functions for digital differential protection of power transformers. Walsh functions are a squared up version of sine and cosine functions. They take only values of ± 1 and ± 1 and change sign only when time t is a power of $\frac{1}{2}$.

In terms of these functions, the Walsh expansion of x(t) with finite energy and a finite number of discontinuities in the interval (0, T) can be defined as:

$$x(t) = \sum_{k=0}^{\infty} W_k wal(k, \frac{t}{T}) \qquad (3.20)$$

where

$$W_k = \frac{1}{T} \int_0^T x(t)wal(k, \frac{t}{T})dt \qquad (3.21)$$

Also x(t) is expressed in this interval as a Fourier series:

$$\gamma(t) = F_0 + \sqrt{2}F_1 \sin \frac{2\pi t}{T} + +\sqrt{2}F_2 \cos \frac{2\pi t}{T} + +\sqrt{2}F_3 \sin \frac{4\pi t}{T} + ...$$
 (3.22)

By substituting Eqn (3.21) into Eqn (3.21), it is found that the Walsh coefficients of Eqn (3.21) forms a vector in Hilbert space like the Fourier coefficients F_k . This relationship can be expressed in matrix form as:

$$W = AF (3.23)$$

where any element A_{kk} of the matrix A is the result of substituting the k-th sinusoid that appears in Eqn (3.22) for x(t) in Eqn (3.21). Since $F = A^TW$, the Fourier coefficients F_1 , F_2 , F_3 and F_4 can easily be determined as:

$$F_1 = 0.9W_1 - 0.373W_5 - 0.074W_9$$

 $F_2 = 0.9W_2 + 0.373W_6 - 0.074W_{10}$
 $F_3 = 0.9W_3 - 0.373W_{11}$
 $F_4 = 0.9W_4 + 0.373W_{12}$ (3.24)

The fundamental and second harmonic content of the differential current can be determined using:

Fundamental =
$$\sqrt{F_1^2 + F_2^2}$$

2nd Harmonic = $\sqrt{F_3^2 + F_4^2}$ (3.25)

The Walsh algorithm was tested with digitally samulated inrush current and short circuit faults of a single-phase transformer. Data provided by computer simulation was transferred to an INTEL 8088 personal computer. Software was written to simulate the on-line digital relay and to use the simulated data to determine the operating (fundamental component) and restraining (second harmonic) signals. The sampling frequency used was 960 Hz. In case of an internal fault, the circuit breaker had cleared the fault in 9 — 14 ms, which was less than one cycle period. In this paper, the authors dealt with only internal faults and inrush current, other features required for complete protection of power transformer are omitted.

3.1.7 Haar Function

Fakruddin et al. [19] developed an algorithm based on Haar functions for extracting frequency components from power system relaying signals. The Haar functions [20] form an orthogonal function of periodic square wave and assume a set of values $0, \pm 1, \pm \sqrt{2}, \pm 2, \pm 2\sqrt{2}$, etc.. They can be expressed as HAR(n,t). The first 16 Haar functions are shown in Fig 3.1.

For a given continuous function f(t) within the interval $0 \le t \le 1$ and repeats periodically outside this interval can be synthesized from a Haar series as:

$$f(t) = \sum_{n=0}^{\infty} C_n H AR(n, t)$$
 (3.26)

and

$$C_n = \int_{-\infty}^{1} f(t) II AR(n,t) dt \qquad (3.27)$$

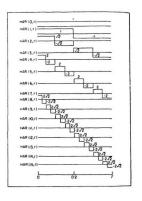


Figure 3.1: First sixteen Haar functions.

The sine and cosine components of any harmonic can be calculated from Haar coefficients C_n using Haar-Fourier relations. By using the combined second and fifth harmonic magnitude of the differential current and then comparing the result with the fundamental component, a trip decision can be made for power transformer differential protection. This protection scheme is based on Haar functions as follows:

$$K_1 = \frac{\sqrt{F_3^2 + F_4^2} + \sqrt{F_9^2 + F_{10}^2}}{\sqrt{F_1^2 + F_2^2}}$$
(3.28)

and

$$K_2 = \frac{max(F_3, F_4) + max(F_9, F_{10})}{max(F_1, F_2)}$$
(3.29)

where F_1 , F_2 , F_3 , F_4 , F_9 and F_{10} are the Fourier components obtained from Haar functions.

A trip signal is issued if K_1 or K_2 falls below certain threshold level of 0.01. The Haar algorithm was tested using a variety of simulated inrush and internal fault signals. In case of an internal fault, the circuit breaker would have cleared the fault in around 20 ms. Due to the complication of Haar function, the time taken to process data signals is usually longer compared to other algorithms. As a result it is not a attractive method unless a powerful microprocessor is used.

3.1.8 Kalman Filtering

Murty and Smolinski [21] presented a digital relay for a three phase power transformer protection based on a five-state Kalman filter. The Kalman filter equation used to recursively estimate the new values of the state variable is:

$$\hat{x}_{k+1}^{-} = \Phi(\hat{x}_{k}^{-} + K_{k}(z_{k} - H_{k}\hat{x}_{k}^{-}))$$
 (3.30)

where $\hat{x}_{k+1}^- = \text{the updated estimate of } n \times 1 \text{ process state vector at time } t_k$. $\hat{x}_k^- = \text{the estimate of } n \times 1 \text{ process state vector at time } t_k$. $K_k = \text{Kalman gains at time } t_k$.

 z_k = the $m \times 1$ vector measurement at t_k .

 $H_k =$ the $m \times n$ matrix given the noiseless connection between the measurement and state vector.

 Φ_k = the $n \times n$ state transition matrix.

The inrush and fault conditions are distinguished by the fundamental and second harmonic components of the differential current $I1_k$ and $I2_k$ respectively as follows:

$$I1_k^2 = \hat{x}1_k^2 + \hat{x}2_k^2$$
 (3.31)

$$I_{2k}^2 = \hat{x}_{3k}^2 + \hat{x}_{4k}^2$$
 (3.32)

where $\hat{x}1_k^2$, $\hat{x}2_k^2$, $\hat{x}3_k^2$, $\hat{x}2_k^2$ are the estimated state variables at time t_k .

Then the combined fundamental and second harmonic components $F1_k^2$ and $F1_k^2$ respectively can be calculated as follows:

$$F1_k^2 = I1a_k^2 + I1b_k^2 + I1c_k^2$$
 (3.33)

$$F2_k^2 = I2a_k^2 + I2b_k^2 + I2c_k^2$$
 (3.34)

where $I1a_k^2$, $I1b_k^2$, $I1c_k^2$, and, $I2a_k^2$, $I2b_k^2$, $I2c_k^2$, are the combined fundamental and second harmonic components for phases a, b, c respectively.

The relay was implemented on a TMS320 digital signal processor and tested on a three phase transformer. The sampling frequency used was 960Hz. The relay operation time for internal faults was reported to be around half a cycle [21]. However this response will occur only when the fault has occurred on the first sample. The response will be slower if a fault occurs at 12th or 13th samples. So, in fact, the relay response time should be around one cycle. Also the fivestate Kalman filter has no provision for higher order harmonics and error in the estimation can be caused by high frequency components. Murty and Smolinski [22] extended their previous work by including the percentage differential characteristic and over-excitation restraint for the relay. They also include the ground fault protection for primary and secondary windings of power transformers. The fifth-state Kalman filter is increased to eleventh-state to accommodate up to fifth barmonic components of current signal.

The relay operation time for internal fault was around one cycle and it also took about one cycle to send a trip signal for other faults. However, this algorithm performs only for the case where the fault occurred on the first current sample. If the fault occurred on the 13th or 14th samples, the relay operation time will take much longer. Also a 25% even harmonic threshold level was chosen in the experiments. For modern transformers with amorphous metal, the threshold level can go down to 5% or even lower. By using the Kalman filtering method, the relay operating time will increase with a decrease in threshold level. Moreover, the authors did not consider the anti-aliasing filters in their hardware design. The presence of high frequency components in the inputs can corrupt the estimates due to aliasing. If additional anti-aliasing filters are used, they will introduce extra time delay to the relay response time. The parameters for Kalman filters used were based on a model transformer. If these parameters are very different from the chosen values for another chosen transformer, they have to be recalculated. Accordingly, this algorithm is not quite convenient.

3.1.9 Least Square Approach

Sachdev and Baribeau [23] presented a new algorithm calculating impedances from sampled voltages and currents. The output during a fault is assumed to be composed of a decaying dc component as well as the fundamental and harmonic frequencies as follows:

$$x(t_1) = k_1 e^{-(t_1/\tau)} + \sum_{n=1}^{N} k_{2n} \sin(n\omega_0 t_1 + \theta_n)$$
 (3.35)

where $x(t_1) = \text{instantaneous voltage or current at time } t_1$.

 $\tau = \text{time constant of the decaying dc component.}$

N = highest order of the harmonic component present in the signal.

 ω_0 = fundamental frequency of the system.

 $k_1 = \text{magnitude of the dc offset at } t=0.$

 $k_{2n} = \text{peak}$ value of the n-th harmonic component.

 θ_n = phase angle of the n-th harmonic component.

Parameters determined by the least square approach were then used to compute the real and imaginary components of the voltage and current. Impedances were then calculated using the following equations:

$$R = Re\{\frac{V}{I}\} = \frac{(V_p \cos \theta_v)(I_p \cos \theta_i) + (V_p \sin \theta_v)(I_p \sin \theta_i)}{(I_p \cos \theta_i)^2 + (I_p \sin \theta_i)^2}$$
(3.36)

$$X = Im\{\frac{V}{I}\} = \frac{(V_p \sin \theta_v)(I_p \cos \theta_i) - (V_p \cos \theta_v)(I_p \sin \theta_i)}{(I_p \cos \theta_i)^2 + (I_p \sin \theta_i)^2}$$
(3.37)

Two types of data were used in testing the algorithm. The first type was generated from a digital model of a transmission line and the second type was obtained from the Saskatchewan Power Corporation at Regina South switching station. The results implied that the algorithm can calculate the impedance from the off-line fault data from a power system. Although all the tests were based on an impedance relay, the authors stated that the proposed algorithm would provide information on harmonic components for use in transformer differential relays if the harmonics in transformer inrush currents were included in the equations.

Degens [24] used the least squares curve-fitting technique to find the ratio between the fundamental and second harmonic components of the differential current for inrush detection. The time constant of the decaying dc is considered unknown.

If it is assumed that the inrush current does not contain more than five harmonics,
then in a certain time interval, the inrush current can be approximated by:

$$i(t) = p_0 e^{-\lambda t} + \sum_{k=1}^{5} p_k \sin(k\omega_0 t + \theta_k)$$
 (3.38)

where i(t) = instantaneous differential current sample at time t.

 $p_0 = dc$ component.

 λ = inverse decay time constant of the dc component.

 $p_k = \text{peak component of the k-th harmonic differential current.}$

 $\omega_0 = \text{fundamental frequency.}$

 θ_k = phaser angle of the k-th harmonic component.

Using Taylor expansion of the decaying dc current of two terms, Eqn (3.38) can be rewritten in the form:

$$i(t) = p_0 - p_0\lambda t + \sum_{k=1}^{5} p_k \cos \theta_k \sin(k\omega_0 t) + \sum_{k=1}^{5} p_k \sin \theta_k \cos(k\omega_0 t)$$
 (3.39)

If N samples are considered at time t_1 to t_N , then the sampling current process resulted in the following set of equations:

$$\begin{bmatrix} i(t_1) \\ i(t_2) \\ \vdots \\ i(t_N) \end{bmatrix} = \begin{bmatrix} 1 & t_1 & \sin \omega_0 t_1 & \cos \omega_0 t_1 & \cdots & \sin 5\omega_0 t_1 & \cos 5\omega_0 t_1 \\ 1 & t_2 & \sin \omega_0 t_2 & \cos \omega_0 t_2 & \cdots & \sin 5\omega_0 t_2 & \cos 5\omega_0 t_2 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ 1 & t_N & \sin \omega_0 t_N & \cos \omega_0 t_N & \cdots & \sin 5\omega_0 t_N & \cos 5\omega_0 t_N \end{bmatrix} \begin{bmatrix} p_0 \\ -p_0 \lambda \\ p_1 \cos \theta_1 \\ p_2 \sin \theta_1 \\ p_3 \sin \theta_5 \end{bmatrix}$$

$$\begin{bmatrix} i(t_1) \\ 1 \\ t_2 & \sin \omega_0 t_N & \cos \omega_0 t_N & \cdots & \sin 5\omega_0 t_N & \cos 5\omega_0 t_N \end{bmatrix} \begin{bmatrix} p_0 \\ -p_0 \lambda \\ p_1 \cos \theta_1 \\ p_2 \sin \theta_3 \\ p_3 \sin \theta_5 \end{bmatrix}$$

$$\begin{bmatrix} 3.40 \end{bmatrix}$$

If the above equations are written in matrix form as:

$$I = AX (3.41)$$

then the least square solution becomes:

$$\mathbf{X} = [(\mathbf{A}^{\mathrm{T}}\mathbf{A})^{-1}\mathbf{A}^{\mathrm{T}}]\mathbf{I} = \mathbf{B}\mathbf{I}$$
(3.42)

Since matrix **B** contains known elements, it can be used to calculate the vector of unknown **X** from the sampled differential current as follows:

$$p \cos 1 = p_1 \cos \theta_1(t_N) = \sum_{i=1}^{N} b(3, n)i(t_n)$$
 (3.13)

$$p \sin 1 = p_1 \sin \theta_1(t_N) = \sum_{n=1}^{N} b(1, n)i(t_n)$$
 (3.44)

$$p \cos 2 = p_2 \cos \theta_2(t_N) = \sum_{n=1}^{N} b(5, n)i(t_n)$$
 (3.45)

$$p \sin 2 = p_2 \sin \theta_2(t_N) = \sum_{n=1}^{N} b(6, n)i(t_n)$$
 (3.46)

Finally P_1 and P_2 can be calculated by:

$$P_i = \sqrt{p_i^2 \cos^2 \theta_i + p_i^2 \sin^2 \theta_i}, \text{ where } i = 1, 2$$
 (3.47)

The algorithm was designed so that if $\frac{p_1}{p_2}$ was smaller than a 12.5% threshold value, a trip command would be given. This algorithm was tested with digitally simulated inrush and short circuit faults of a single phase transformer. Only four test cases had been done. In case of a fault current, a trip command was given around two cycles of the power frequency.

Degens [25] continued the work of the digital inrush current detection based on the least-squares curve fitting of sampled differential current by a decaying dc and five harmonic components. The author implemented the digital filter by means of a microprocessor. The microprocessor was built around an AlM 65 microcomputer with a 6502 CPU. The algorithm was being tested on-line via a single phase 2.2 kVA transformer with sampling frequency of 600 Hz. The author had incorporated a fast tripping option in the protection scheme. In case of a severe short fault, the tripping time would be between 5 to 10 ms. However, for other faults such as winding faults, the tripping time would be again around two cycles.

Rahman et al. [26] presented a weighted least-square scheme for differential protection of power transformer similar to Degens [24, 25]. The only difference is that they added a Root Mean Square Error (RMSE) criterion technique to select proper harmonic orders, data window, weighting matrix and sampling rate. The RMSE is obtained as follows:

$$RMSE = \sqrt{\frac{(x_m(t) - x(t))^T Q(x_m(t) - x(t))}{N}}$$
 (3.48)

where $x_m(t)$ = the measured instantaneous sample of the differential current at time t.

x(t) = instantaneous differential current sample at time t.

Q = weighting matrix.

N = number of samples (data window) used for performing computation.

The power transformer fault or inrush current model is dependent on the type of transformer and the operating conditions. The lowest RMSE gives the correct model for the fitted data. The proposed method was programmed on a PDP 11/60 computer for off-line simulation with sampling rate of 720 Hz. The performance of the filter for internal fault current was around one cycle. However, the authors have not done any real time testing.

The weighting matrix Q of this proposed method requires the fault and inrush data for a number of case studies to obtain the best weight factors. This involves a lot of computational overhead and cannot be done on-line. Furthermore, large weights on the fundamental and second harmonic coefficients can produce computational orund off errors. Small weights can also result in computational problems. As a result the weighted least-squares algorithm is not optimum.

3.1.10 Voltage Restraint Algorithm

Thorp and Phadke [27] presented a voltage restraint algorithm for transformer protection. The restraint technique is as follows:

$$V_p = \frac{2}{N} \sum_{k=0}^{\frac{N}{2}-1} V_k e^{-\frac{2\pi j k}{N}}$$
(3.49)

where V_p = the primary voltage.

 V_k = the k-th sample of the primary voltage.

N is the number of samples per window.

If the calculated voltage, V_p is lower than a predefined threshold voltage, then a fault is declared and a trip signal is sent. It is obvious that the restraint samplesignal is obtained from voltage. However, most of the transformers used in industry today give rise to a current signal. So this voltage restraint algorithm is not so useful in practical application.

3.1.11 Flux Restraint Algorithm

Thorp and Phadke [28] used flux-current relationship to obtain the restraint function for transformer protection. The mutual flux linkage Λ of a transformer can be calculated from its past with measured voltage and current as follows:

$$\Lambda_k = \Lambda_{k-1} + \frac{\Delta t}{2} (e_k + e_{k-1}) - L(i_k - i_{k-1})$$
(3.50)

where Λ_k = the k-th sample of the flux linkage.

 e_k = the k-th sample of the primary voltage.

 i_k = the k-th sample of the primary current.

This equation is an approximation to the solution of the differential equation:

$$\frac{d\Lambda}{dt} = c - L(\frac{di}{dt}) \tag{3.51}$$



Figure 3.2: Fault and no fault region in flux vs different current plane [28]

The transformer is found to be in a fault condition or not is based on the position of the point of flux and current (A₈, i₈) in the flux-differential current plane as shown in Fig 3.2. The tests were carried out in the American Electric Power Service Corporation Power System Simulator Laboratory on a model transformer. The sampled data of all current and voltages were collected onto a microcomputer and were used in off-line FORTRAN program to study the performance of the algorithm "he relay response time was around one and one - and - a - half cycles. This method needs both voltage and current for sampling in order to get the flux restraint. That is why it was not found to be an attractive method.

3.2 Research on Comparison of Algorithms

Rahman and Jeyasurya [29] presented a comparative study of six algorithms for digital differential protection of power transformers. The six algorithms are Fourier Analysis, Rectangular Transform, Walsh Functions, Haar Functions, Finite Impulse Response, and Least-squares Curve Fitting. All algorithms were tested on a simulated three phase transformer using a VAX-11/785 mainframe computer. The sampling frequency was 960 Hz and the results are given in Table 3.1.

Algorithm	Sampling Interval (µs)	Number of Arithmetic Operation			Time for Arithmetic Computation	Percentage of Sampling Interval
		+/-	×/÷	\sqrt{x}	(10) (µs)	
Fourier	1024	51	14	2	380	36 %
Rectangular	1042	106	8	2	110	39 %
Walsh	1042	116	14	2	526	50 %
Haar	1042	96	16	2	512	49 %
Finite	1042	81	-1	2	298	29 %
Curve	1389	46	19	2	447	32 %

Table 3.1: Computational requirements for transformer protection algorithms [29]

The simulation results have shown that all algorithms provided a trip signal around a cycle for an internal fault. However, the algorithms have not been tested on marginal operating conditions such as during loads. Also tests are done only to distinguish between an inrush and internal fault. Other features required for complete protection of power transformer are omitted.

Habib and Marin [30] presented a survey and a comparative analysis of various algorithms for the differential protection of three phase transformers. These algorithms were analyzed based on the problem of differential protection and exciting-current detection problem. They were defined by two performance indices based on time and frequency. As a result, the harmonic restraint Discrete Fourier Transform algorithm was found to be the best algorithm for the implementation of a digital relay for the differential protection of transformers.

Chapter 4

Design of a Microprocessor Based Relay Hardware Module for Transformer Protection

Conventional relays designed for the protection of power systems use electromechanical technology. Not until recently, researchers are beginning to develop microprocessor relays since in most cases microprocessor relays are faster and more reliable in operation. In the case of transformer protection, researchers use different algorithms based on simulation or hardware and software to find the best way to protect transformers from faults and to distinguish between the inrush and fault currents as discussed in the last chapter. The researchers usually state that they have found the best algorithms for the transformer protection scheme. However, since their test results are usually based on different equipment, it is difficult to compare their test results. Also their protection methods may not be applicable to all types of transformers. The hardware part of their protection schemes as well as the software portion may have to change to accommodate different transformers.

The main purpose of the present design is to make a digital relay for the protection of transformers of different types. The design changes can be made by changing the software only. This means that the hardware part of the design is a "black box" to users because they do not have to know much about it. The final product will be a user friendly testing tool for laboratory and a real time transformer protection instrument for industry.

4.1 Hardware Design

The functional blocks of the microprocessor based relay are shown in Fig. 4.1. The current signal of the power transformer is obtained via the current transformers. This signal is then scaled down to the acceptable computer input level by the scaling circuit and fed to the anti-aliasing filter to filter out unwanted frequencies. The sample and hold will perform desired sampling and hold a signal until the next signal pulse comes in. The multiplexer can channel the analog signal to the analog-to-digital converter to change the signal to a number which can be read by the microprocessor. The microprocessor used in this design belongs to the TMS32010 family. It consists of two boards, namely TMS32010 Evaluation Module (EVM) which contains the processor itself and the Analog Interface Board (AIB). It can process digital signals to determine a trip or no trip decision defined by a software program residing in memory. The detail of each functional block will be discussed in the next few subsections.

4.1.1 Relay Control Circuit and The Solid State Relay

The relay control circuit is used to control the opening and closing of the solid state relay. It consists of two resistors and two npn transistors as shown in Fig.4.2. The left side of the circuit is hooked up to the analog output of the microprocessor through the AIB and the right side is connected to the relay. If a signal of zero voltage is given out by the microprocessor, the +3 and -4 terminals will go 'high'. Otherwise if a voltage of 10V is ap₁ ied, the terminals will go 'low' to open the relay for tripping.

The Potter and Brumfield solid state relay with paired SCR output are used in

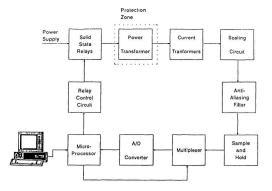


Figure 4.1: Function blocks of microprocessor relay

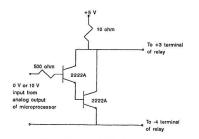


Figure 4.2: Relay control circuit

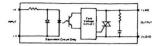


Figure 4.3: Solid state relay equivalent circuit [31]

this part of the design. The equivalent circuit schematic of the relay is shown in Fig 4.3. This relay has the features of zero voltage turn on, optical isolation, and open within one half cycle.

There are totally three sets of control circuits and relays to accommodate the three phases of the power supply. An extra set is also included in the design for backup.

4.1.2 Power Transformer

The transformer used for testing was a $5 \, kVA \, 230/550 - 575 - 600 \, V$, Delta/Wye connected three phase power transformer given by Newfoundland and Labrador Hydro. This test transformer can be replaced by other transformers and the hardware setup does not have to be changed.

4.1.3 Current Transformers

The current transformers with ratings of 120/5 A are used to obtain signals from the power transformer. There are totally seven current transformers used in the laboratory setup. Three for the primary side, another three for the secondary side and one for the ground of the secondary. Current transformers on the primary side are connected in Wye whereas on the secondary side they are connected in Delta to eliminate the zero-sequence current. Also the primary and secondary sides shunt resistances are 0.5 ohm and 0.7 ohm respectively.

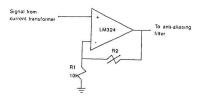


Figure 4.4: One set of scaling circuit

4.1.4 Scaling Circuit

The scaling circuit is used to convert the output signal obtained from the current transformer to the appropriate voltage for the analog-to-digital converter to be compatible and to fine tune the anti-aliasing filter that will be discussed later. It can also be used to compensate for the errors caused by current transformer shunt resistor mismatch. Fig 4.4 shows the diagram of one scaling circuit.

The operational amplifier employed here is operated as non-inverting dc gain amplifier as follows:

$$GAIN = 1 + \frac{R2}{R1} \tag{4.1}$$

As can be seen from Fig. 4.4, R2 is a variable resistor and the gain can be adjusted by varying R2. The LM324AN amplifier which is used in this design consists of four internally frequency compensated operational amplifiers. Seven amplifiers are needed to construct seven scaling circuits. Three scaling circuits for each of primary and secondary phases as well as one for the ground current. Also since three amplifiers will be used for building each of the seven anti-aliasing filters, one LM324AN chip is suitable for constructing one scaling circuit and one filter. As a result only seven LM324AN chips are needed.

4.1.5 Anti-Aliasing Filter

The phenomenon of downward frequency translation occurs whenever a frequency component is under-sampled so that the sampling frequency is less than twice the cutoff frequency and is given the name aliasing. The aliasing effect is serious because the frequency characteristic of a continuous signal and its sampled sequence are no longer linearly related. Hence the data obtained from the sampled signal may contain errors. In order to lower or even climinate the aliasing effect, the continuous signal has to be filtered as much as possible before sampling.

In the case of transformer differential protection, the design must detect inrush current by checking the presence of second harmonic component and also able to detect over-excitation by fifth harmonic component. To preserve these components, the low-pass anti-aliasing filter must preserve the 60, 120 and 300 Hz components. A cutoff frequency of about 400 Hz is practical. Now, in order firstly to guarantee the selection of the fundamental, second and fifth harmonic data, secondly to avoid aliasing, and thirdly to accommodate different transformer differential protection algorithms, a sampling rate of 900 Hz was chosen.

The chebyshev filter was used in the design as the anti-aliasing filter, because of its steep roll-off characteristics near the cutoff frequency. Referring to the filter specifications shown in Fig 4.5 and the predefined parameters $A_{max} = 3 dB$, $A_{min} =$ 30 dB, $f_c \approx 400 Hz$ and $f_s = 500 Hz$, the order n of this chebyshev filter is obtained as:

$$n = \frac{\cosh^{-1}[(10^{0.1A_{min}} - 1)/(10^{0.1A_{max}} - 1)]^{\frac{1}{2}}}{\cosh^{-1}(\omega_{*}/\omega_{*})} = 5.985$$
(4.2)

With this value, n must be selected as the next highest integer 6 and a sixthorder chebyshev filter is needed. For the purpose of comparison, the value of n for a Butterworth response that is necessary to meet same parameter specification of

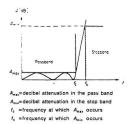


Figure 4.5: Chebyshev low-pass filters specifications [32]

the sixth-order chebyshev filter is calculated as:

$$n = \frac{\log[(10^{0.1A_{min}} - 1)/(10^{0.1A_{max}} - 1)]}{2 * \log(\omega_*/\omega_c)} = 15.487$$
(4.3)

Hence a sixteenth-order Butterworth filter is required to meet the predefined parameters that led to a sixth-order chebyshev. For low order response, less complicated analog circuits are needed to be built. Fig 4.6 shows the design of the sixth-order low-pass chebyshev anti-aliasing filter. The transfer function of this filter is:

$$H(s) = (3.2634 * 10^{-20}s^6 + 1.2850 * 10^{-16}s^5 + 5.1185 * 10^{-13}s^4 + 1.1020 * 10^{-9}s^3 + 1.8691 * 10^{-6}s^2 + 1.8929 * 10^{-3}s + 1)^{-1}$$
 (4.4)

Using the above transfer function, the frequency and phase response are found by simulation. The results of the simulation are shown in Fig 4.7. From the diagram of Fig 4.7, it can be seen that the cut-off frequency is approximately 350 Hz which ensures all frequencies lower than and including fifth harmonic pass through and other higher harmonics will be eliminated. The phase response of

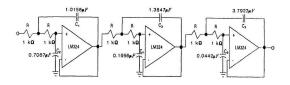


Figure 4.6: Design of the low-pass anti-aliasing filter

this filter is also linear for the passband. The program to find the filter response is given in Appendix A. The detailed calculation of the resistors and capacitors of the filter can be found in Appendix B.

4.1.6 Sample and Hold (S/H)

The filtered analog signals must be sampled at time instants determined by a sampling clock. The analog-to-digital conversion process requires that the analog signal presented to the analog-to-digital converter must be held steady during the conversion time. A laboratory function generator, which is set to give out a square wave of 15.36 kHz, is used as a clock generator. It is connected to a 7493AN four bit binary counter to divide the frequency by sixteen to produce a sampling clock rate of 960 Hz. An oscillator which generates the same clock frequency can also be used instead of the function generator.

Fig 4.8 shows the LF398 sample and hold chip used in the design. It has a less than 10μs acquisition time. The hold capacitor is 0.001μF. When the clock is 'high', S/H is in the 'track' state and the input will appear at its output. However when the clock is 'low', S/H switches to the 'hold' state and the output remains steady independent of the input value. The input and output signals of the S/II

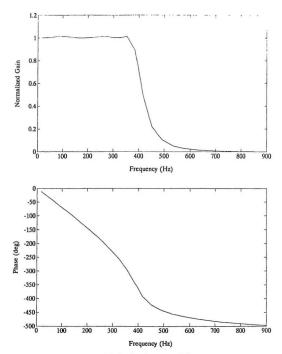


Figure 4.7: Anti-aliasing filter frequency and phase responses



Figure 4.8: Sample and hold [33]

are shown in Fig 4.9.

There are totally seven S/H circuits to accommodate seven current signals. In order to avoid any differential phase shift between the signals, all S/H have to be controlled by the same sampling clock.

4.1.7 Multiplexer

Multiplexing means transmitting a large number of information units over a smaller number of channels or lines. A multiplexer is a circuit that selects information from one of many input lines and directs it to a single output line. Fig 4.10 shows an analog CMOS multiplexer IIS-508 applied in the design to select one S/II output at a time for subsequent analog-to-digital (A/D) conversion.

This unit is an eight-to-one line multiplexer with an access time of 500ns. It can withstand a continuous input up to 10V which is greater than the supply voltage and that lowers the possibility of damage when the power supplies are off but the input signals are present. Also it can withstand brief input transient spikes of several hundred volts. It has a break-before-make switch to prevent channel corruption.

This multiplexer has an ENABLE (EN) line input for the external control of the operation of the unit. When EN input is in 'low' (L) state, the output is

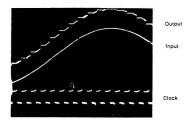


Figure 4.9: Input and output of the sample and hold



Figure 4.10: Multiplexer used in the design [34]

Channel	EN	A_0	A_1	A ₂ X L
none	L	X	X	
1	11	L	L	
2	11	H	L	L
3	H	L	11	L
-1	H	H	Н	1.
5	H	L	L	11
6	11	H	L	H
7	H	L	II	11
8	11	H	H	11

Table 4.1: Truth table of the multiplexer

disabled. If EN is in 'high' (II) state, the circuit functions as a normal multiplexer. The channels selections are based on EN and A_0 , A_1 , A_2 lines. The truth table is shown in Table 4.1. All A_0 , A_1 and A_2 are connected to the Analog Interface Board (AIB). They are controlled by the microprocessor software.

4.1.8 Analog-To-Digital (A/D) Converter

The scaled, filtered, sampled, and selected transformer analog signal has to be presented to the analog-to-digital converter for conversion from a signal to form a number which can be read by the microprocessor. Fig. 4.11 shows the Analog Interface Board (AIB) schematic including the detailed operation of the 12-bit ADC80-Z A/D converter used in the design. This Λ /D operates on a 12 V power supply with a 25 μ s conversion time. It is configured for bipolar analog inputs between +10 and -10 V. Variable resistors R2 and R3 on the AIB are used for the offset and gain adjustment of the A/D respectively. This Λ /D output is in offset binary form with two's complement representation.

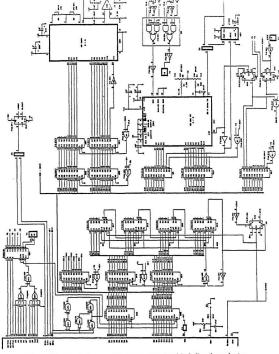


Figure 4.11: Circuit diagram of Analog Interface Board including the analog-to-digital converter [35]



Figure 4.12: TMS32010 Microprocessor [36]

4.1.9 Microprocessor

The microprocessor performs the transformer protection functions and other tasks defined in the software. Fig 4.12 shows the TMS32010 chip and Table 4.2 shows the function of its pins. This microprocessor is located on the Evaluation Module (EVM) board which is connected to the Analog Interface Board (AIB). It comes with 4 k words of program memory and 144 words of data memory. Only 200 ns is needed for it to execute one program instruction or one multiplication.

Six data buses of the microprocessor are used in the design. D1, D2 and D3 are tied to the pins 31, 30 and 24 of the A1B to provide the means of selection of channels for the multiplexer. D5 is joined to pin 22 of A1B to clear the interrupt whereas D6 is attached to pin E5-3 to control the A/D converter operation. Finally D8 is used to send a trip signal to the solid state relay if a fault occurs.

The EVM has a 25 pin D type connector which is hooked up to a computer terminal for software download and reset. The complete circuit diagram of the

Pin(s)	Description		
V.c	+5 V supply voltage		
V.,	Ground		
X2/CLKIN, X1, CLKOUT	Internal clocks		
WE	Write enable		
DEN	Data enable		
MEN	Memory enable		
RS	Reset		
INT	Interrupt		
B10	I/O branch control		
MC/MP	Microcomputer/microprocessor mode		
D0 to D15	Bidirectional data bus		
A3 to A11	Program memory address bus		
A0/PA0, A1/PA1, A2/PA2	Program memory and port address bu		

Table 4.2: TMS32010 microprocessor pin descriptions

EVM is given in Appendix C.

4.1.10 Computer Terminal

As mentioned before, a computer terminal is connected to the microprocessor via a RS232 cable. The main function of this terminal is to down load different transformer protection software from a floppy disk or the hard disk. Moreover, in the case of a fault and when the relay is tripped, the software has to be manually reset through the computer. An IBM 8088 was used as the terminal in the laboratory setup.

4.2 Hardware Operation

At any time instant, seven current signals will arrive at the analog scaling circuit and the anti-aliasing filter through the current transformer. These signals are then passed to the S/H circuit. When sampling clock changes to 'low' state, the S/H will also be in 'low' state and hold the signal steady to pass to the multiplexer. The complete circuit is shown in Fig 4.13.

At this time the microprocessor is being interrupted by the \overline{INP} line. The software in memory will send a signal to A_0 , A_1 , A_3 lines to select the first multiplexer channel of the current signal for the A/D to convert the analog signal to a digital signal. A conversion is now initiated by the rising edge of the convert start (SOC) line of the A/D converter. During the conversion SOC will go 'low' and stay there but the status output (EOC) line will go 'high'. Approximately 25 μ s later, the conversion is completed. The EOC will now go low and trigger the \overline{HIO} line of the microprocessor for the software to jump out of the first signal input loop and put the data in memory. The software will send another pulse to A_0 , A_1 , A_2 lines again to select a multiplexer channel for another current signal input.

After all seven signals have been put in memory, the microprocessor will process
the data. If there is no fault, the software will go back to the beginning and
start inputing another set of data at the next falling edge of the sampling clock.
However, if a fault is found, a trip signal will be sent to the relay control circuit by
the microprocessor to open the solid state relay and to cut off the power supply of
the power transformer. In this case after the fault has been cleared, the software
has to be reset manually via the computer terminal to close the relay and to start
the protection operation again.

4.3 Hardware in Module Form

The hardware part of the microprocessor based relay is designed to be a "black box" type. For the protection of different types of transformers, the only change that has to be made is to initialize the data defined in the software.

All the hardware including the relay control circuits, scaling circuits, antialiasing filters, sample and hold circuits, multiplexer, TMS Analog Interface Board

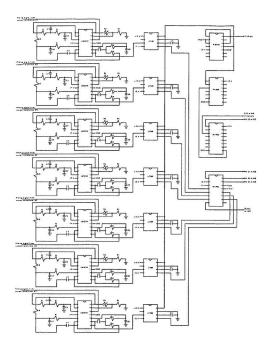


Figure 4.13: Detail Hardware circuit

with A/D converter and the Evaluation Module board with TMST2010 microprocessor are put in a $36 \times 50 \times 36$ cm² box or module as shown in Fig 4.14. The top, two sides and the end part of the box is attached together as one piece which can be removed to get access to the hardware if needed.

Fig 4.15 shows the front panel of the box. There are eight binding posts on the top side of the panel. They are connected to the four sets of relay control circuits inside the box. Three sets of binding posts are for the connection to the three solid state relays and one extra set for the ground relay if necessary.

On the top left side of the front panel there are another eight binding posts. The first four are for the connection to the +12V, -12V, +5V power supplies and to ground (GND) for the AIB and EVM boards. The other four are +15V, -15V, +5V and GND for the supplies of the rest of the hardware.

Near the bottom of the front panel, there are nine BNC front mount receptacles.

The single BNC jack that is closest to the left is for the external clock. A square
wave of 15.36 kHz should be input through this jack to a 4 bit counter to obtain
a 960 Hz sampling frequency. The remaining eight BNC jacks are used as follows:

- Three for primary phase currents (d1, d2, d3).
- Three for secondary phase currents (t1, t2, t3).
- Two for ground (g1, g2).

Usually only one ground is needed. The second ground is just for backup purpose.

The last component on the front panel is a 25 pin D type connector. It is joined to the EVM board inside the box. This should be connected to a computer terminal via a RS232 cable for downloading and to reset the transformer protection software of the TMS32010 microprocessor.

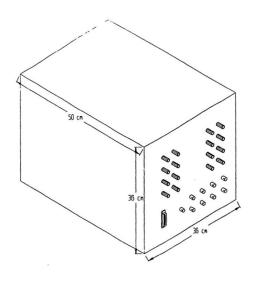


Figure 4.14: The hardware module

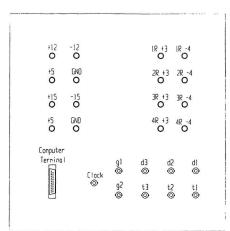


Figure 4.15: Front panel of the hardware module

Chapter 5

Development of Relay Software for Selected Algorithms

This chapter gives a detail description of the software design of the microprocessor relay completed with detailed flow chart diagram. The software occupies approximately 1 k word of program memory.

5.1 Data Conversion

 Λ 5kVA 230/550 - 575 - 600 V, Delta/Wye connected three phase power transformer was used in the laboratory testing. The rated primary current is calculated as:

$$I_{rated} = \frac{5000}{230\sqrt{3}} = 12.55 A = 1 P.U.$$
 (5.1)

Each data or program memory of TMS32010 is 16-bit. The maximum value of data that can be stored in one memory location is $2^{15} - 1 = 32767$. In order to get a standard conversion, the value of $(1 P.U.)^2 = 32767 = 7FFF$ Hex is selected. Hence 1 P.U. is approximately equal to 181 (B5 Hex).

5.2 Detailed Software Design

The following subsections describe the detailed design of the relay software on selected algorithms. The general data initialization, current signals inputs, dif-

Variable Name	Data in Hex	Channel Selected
M0	F0	1
MI	FI	2
M2	F2	3
M3	F3	-1
M4	F4	5
M5	F5	6
M6	F6	7

Table 5.1: Software data for multiplexer channel selection

ferential current and through current calculations, and the protection decision subroutines are the same for all algorithms. Only the coefficients initialization and harmonic components extraction subroutines are dependent on the algorithm used for laboratory testing. A flow chart for the software is shown in Fig 5.1.

5.2.1 Data Initialization

The first step for writing the transformer protection software is to define all variables. Then all data have to be initialized to zero.

The data initialization part of the software is to put down predefined data according to the power transformer specifications, the hardware and the chosen protection algorithms. The first important data variable named MODE is used to set the Analog Interface Board to asynchronous receive mode. It tells the Λ/D converter that an external sampling clock is provided and the auto sampling clock is to be ignored. This mode is enabled by the data F6 Hex stored in variable MODE. The next set of data are provided for selecting the multiplexer channel. Table 5.1 shows the variable names corresponding to the data for channel selection.

As mention before, TMS32010 microprocessor comes only with 144 data memory. There are not enough memory for all 16 samples for each of the seven current

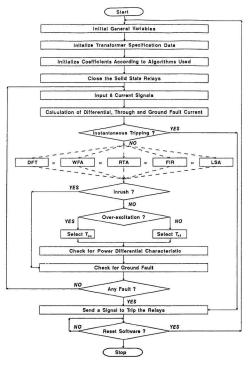


Figure 5.1: Flow chart for the differential relay software

Program Memory Addresses in Hex	Reserved for
800-80F	Differential current phase a
810-81F	Differential current phase b
820-82F	Differential current phase c
830-83F	Through current phase a
840-84F	Through current phase b
850-85F	Through current phase c
860-86F	Primary ground fault current
870-87f	Secondary ground fault current

Table 5.2: Program memory locations for current signals storage

signals (3 for the differential currents, 3 for the through currents, 2 for the primary and secondary ground fault currents) with some processing variables. All current sample signals have to be stored in program memory and then retrieved one by one into a temporary data memory buffer for calculation. The reserved program memory locations are shown in Table 5.2.

In order for the digital relay to work properly, the following data have to be defined for the protection of different types of transformer:

- Threshold for normal loading of transformer (T_{nl}) = 0.05 p.u..
- Threshold for the over-excitation case to prevent relay misoperation $(T_{ov}) = 0.075 \, p.u.$.
- The slope of the Percentage Differential Characteristics (PDC) for the relay to be insensitive to transformer tap-changing, current transformer saturation and ratio mismatch during through fault conditions as shown in Fig 5.2 (T_{pdc}) = 0.25.
- Threshold for instantaneous tripping $(T_{it}) = 10 p.u.$
- Second harmonic restraint percentage for inrush condition (T_{2r}) = 17.7%.

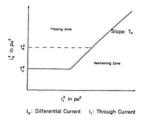


Figure 5.2: Power Differential Characteristic

- Fifth harmonic restraint percentage for over-excitation (T_{5r}) = 6.5%.
- Second harmonic restraint percentage for ground relay (T_{2rg}) = 11.25%.
- Threshold for ground fault (T_{gf}) = 0.05 p.u..

The final data set to put in the software are the coefficients needed for different algorithms. The values of all coefficients and the total number of coefficients needed are unique for each individual algorithm. Coefficient values are all ranged from -1 to +1 for the algorithms chosen for testing in this thesis. Since the program is written using TMS Assembly language, the minimum and maximum 16-bit data values have to be $-(2^{18}-1)$ and $+(2^{15}-1)$, respectively. To obtain a high precision for data manipulation the data range -32767 to +32767 is used to represent coefficients -1 to +1 respectively, in the software.

5.2.2 Current Signals Input

At the falling edge of the sampling clock, current signal will be held by the sample and hold while the microprocessor is being interrupted. An address is then sent by the software to the digital output port of the Analog Interface Board to select the proper multiplexer channel to send the data to the Analog-ta-Digital (A/\mathbb{D}) converter. After data conversion, the input/output control $(\overline{B}\overline{B}O)$ line of the microprocessor will go 'low' and read in the converted data. The data is then stored in data memory. This is repeated until all seven current signals are read. The flow chart for the input data subroutine is shown in Fig 5.3. It is important to note that the last four steps are carried out for all primary three phase currents, secondary three phase currents and the ground current.

As mentioned in the above section, the asynchronous receive mode is used for input data. Because a delay is involved in the conversion by the Λ/D converter, the first data read will be invalid. The program has to read one dummy and then seven more current signals before a set of data acquisition is completed.

5.2.3 Calculation of Differential, Through and Ground Fault Currents

Fig 5.4 shows the protection scheme designed and tested in the laboratory. The differential protection is based on the difference between primary and secondary currents. It is required to compute first the fundamental up to the fifth harmonic components of the differential current and then the fundamental component of the through current with all phases. The equations to calculate the differential currents are given as follows [37]:

$$i_{d_a} = i_{1_a}(t) + [i_{2_a}(t) - i_{2_c}(t)] \frac{N_2}{N_1}$$

 $i_{d_b} = i_{1_b}(t) + [i_{2_b}(t) - i_{2_c}(t)] \frac{N_2}{N_1}$
 $i_{d_c} = i_{1_c}(t) + [i_{2_c}(t) - i_{2_b}(t)] \frac{N_2}{N_1}$
(5.2)

and the equations for the through current are:

$$i_{t_a} = i_{1_n}(t) - [i_{2_n}(t) - i_{2_r}(t)] \frac{N_2}{N_1/2}$$

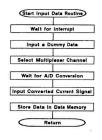


Figure 5.3: Flow chart for the input data subroutine

5 kVA 230/550-575-600 V Three Phase Transformer Delta/Wye

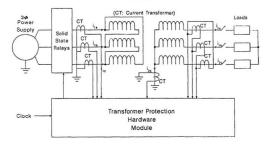


Figure 5.4: Power Transformer Protection Laboratory Setup

$$i_{t_k} = i_{1_k}(t) - [i_{2_k}(t) - i_{2_k}(t)] \frac{N_2}{N_1/2}$$

 $i_{t_\ell} = i_{1_\ell}(t) - [i_{2_\ell}(t) - i_{2_k}(t)] \frac{N_2}{N_1/2}$
(5.3)

where $i_{1a}, i_{1b}, i_{1c} = \text{currents}$ of the three phases for the primary side.

 $i_{2a}, i_{2b}, i_{2c} = currents$ of the three phases for the secondary side.

 N_1 and $N_2 = turn$ ratio for the primary and secondary side respectively.

The sensitivity of differential protection is limited for ground fault due to the magnitude of ground fault impedance. The primary ground fault current is determined by the following equation:

$$i_{1_{qf}} = i_{1a}(t) + i_{1b}(t) + i_{1c}(t)$$
 (5.4)

and the secondary ground fault current equation is given by:

$$i_{2} = i_{2}(t) + i_{2}(t) + i_{2}(t) + i_{2}(t)$$
 (5.5)

When all current data have been calculated, they are stored in program memory for later use to find the necessary harmonic components.

5.2.4 Extraction of Fundamental, Second and Fifth Harmonic Components

After all the current signals have been taken as input, the most important part of the software which is to extract harmonics from these signals has to be done. This part determines the accuracy of the transformer protection software. In the laboratory testing, five algorithms were selected for implementation. These are Discrete Fourier Transform (DFT) Algorithm, Walsh Functions Algorithm (WFA), Rectangular Transform Algorithm (RTA), Finite Impulse Response (FIR) Filtering Algorithm and Least Square Algorithm (LSA).

DFT was chosen because several authors [10, 29, 30] claimed that it is a suitable method to use for transformer protection. Although WFA and RTA are related to DFT, they are simpler with fewer multiplications. FIR filtering is the simplest algorithm. However, it cannot extract fifth harmonic. As a result, the RTA was used in combination with FIR algorithm to extract fifth harmonic. Finally, LSA is the most complicated one out of the five algorithms chosen. It needs lots of calculation overhead before implementation. It was chosen to see if its complexity will improve protection performance. The detail description of these five algorithms are given in Appendix D.

The remainder of this section will provide the method of numerical calculation for each algorithm implemented in the software. Each algorithm has it own data set for its coefficients.

Discrete Fourier Transform (DFT) Algorithm

Let $\ell(I)$ be the current sampled at 16 samples per cycle which are denoted by $I_1, I_{s+1}, Also let S_1, C_1, S_2, C_2, S_5, C_5$ be the sine and cosine of the fundamental, second and fifth harmonic components respectively. The letter S stands for Sine term and the letter C stands for Cosine term. The suffix 1, 2 and 5 represent fundamental, second and fifth harmonic components respectively. The sine and cosine terms are calculated as follows:

```
S_1 = 0.382683I_1 + 0.707107I_{-1} + 0.923880I_{-1} + 1.000000I_{-2} +
         0.923880L_{+4} + 0.707107L_{+5} + 0.382683L_{+6} + 0.000000L_{+7} =
         0.382683I_{i+8} - 0.707107I_{i+9} - 0.923880I_{i+10} - 1.000000I_{i+11} -
         0.923880I_{i+12} - 0.707107I_{i+13} - 0.382683I_{i+14} - 0.000000I_{i+15}
C_1 = 0.923880I_i + 0.707107I_{i+1} + 0.382683I_{i+2} + 0.000000I_{i+3} -
         0.382683I_{i+4} - 0.707107I_{i+5} - 0.923880I_{i+6} - 1.000000I_{i+7} -
         0.923880I_{i+8} - 0.707107I_{i+9} - 0.382683I_{i+10} + 0.000000I_{i+11} +
         0.382683I_{i+12} + 0.707107I_{i+13} + 0.923880I_{i+14} + 1.000000I_{i+15}
S_2 = 0.707107I_1 + 1.000000I_{1+1} + 0.707107I_{1+2} + 0.000000I_{1+2} -
         0.707107I_{i+4} - 1.000000I_{i+5} - 0.707107I_{i+6} \sim 0.000000I_{i+7} +
         0.707107I_{i+8} + 1.000000I_{i+9} + 0.707107I_{i+10} + 0.000000I_{i+11} -
         0.707107I_{i+12} - 1.000000I_{i+13} - 0.707107I_{i+14} - 0.000000I_{i+15}
C_2 = 0.707107I_i + 0.000000I_{i+1} - 0.707107I_{i+2} - 1.000000I_{i+3} -
         0.707107I_{i+1} - 0.000000I_{i+5} + 0.707107I_{i+6} + 1.000000I_{i+7} +
         0.707107I_{i+8} + 0.000000I_{i+9} - 0.707107I_{i+19} - 1.000000I_{i+9} -
         0.707107I_{i+12} - 0.000000I_{i+13} + 0.707107I_{i+14} + 1.000000I_{i+15}
S_5 = 0.923880I_1 - 0.707107I_{i+1} - 0.382683I_{i+2} + 1.000000I_{i+3} -
```

$$\begin{aligned} 0.382683I_{t+4} &- 0.707107I_{t+5} + 0.923880I_{t+6} + 0.000000I_{t+7} - \\ &- 0.923880I_{t+8} + 0.707107I_{t+9} + 0.382683I_{t+10} - 1.000000I_{t+11} + \\ &- 0.382683I_{t+12} + 0.707107I_{t+13} - 0.923880I_{t+14} - 0.000000I_{t+15} - \\ &- 0.382683I_t - 0.707107I_{t+1} + 0.923880I_{t+2} + 0.000000I_{t+5} - \\ &- 0.923880I_{t+4} + 0.707107I_{t+5} + 0.382683I_{t+6} - 1.000000I_{t+7} + \\ &- 0.382683I_{t+8} + 0.707107I_{t+9} - 0.923880I_{t+30} - 0.000000I_{t+15} - \\ &- 0.923880I_{t+12} - 0.707107I_{t+3} - 0.382683I_{t+14} + 1.000000I_{t+15} - \\ &- 0.923880I_{t+12} - 0.707107I_{t+13} - 0.382683I_{t+14} + 1.000000I_{t+15} - \\ &- 0.923880I_{t+12} - 0.707107I_{t+13} - 0.382683I_{t+14} + 1.000000I_{t+15} - \\ &- 0.923880I_{t+12} - 0.707107I_{t+13} - 0.382683I_{t+14} + 1.000000I_{t+15} - \\ &- 0.923880I_{t+15} - 0.707107I_{t+15} - 0.923880I_{t+15} + 1.000000I_{t+15} - \\ &- 0.923880I_{t+15} - 0.707107I_{t+15} - 0.382683I_{t+15} + 1.000000I_{t+15} - \\ &- 0.923880I_{t+15} - 0.707107I_{t+15} - 0.382683I_{t+15} + 1.000000I_{t+15} - \\ &- 0.923880I_{t+15} - 0.707107I_{t+15} - 0.382683I_{t+15} + 1.000000I_{t+15} - \\ &- 0.923880I_{t+15} - 0.707107I_{t+15} - 0.382683I_{t+15} + 1.000000I_{t+15} - \\ &- 0.923880I_{t+15} - 0.707107I_{t+15} - 0.382683I_{t+15} + 1.000000I_{t+15} - \\ &- 0.923880I_{t+15} - 0.707107I_{t+15} - 0.9382683I_{t+15} + 1.000000I_{t+15} - \\ &- 0.923880I_{t+15} - 0.923880I_{t+15} -$$

The squared magnitude of the k-th harmonic component at any instant is given by:

$$h_k^2 = S_k^2 + C_k^2$$
 where $k = 1, 2, 5$ (5.7)

and squared combined harmonic components for the differential current of all phases are:

$$(Fundamental)^2 = S_{1s}^2 + C_{1s}^2 + S_{1s}^2 + C_{1s}^2 + S_{1s}^2 + C_{1s}^2$$

 $(2nd Harmonic)^2 = S_{2s}^2 + C_{2s}^2 + S_{2s}^2 + C_{2s}^2 + S_{2s}^2 + C_{2s}^2$
 $(5th Harmonic)^2 = S_{2s}^2 + C_{2s}^2 + S_{2s}^2 + C_{2s}^2 + S_{2s}^2 + C_{2s}^2 + S_{2s}^2 + C_{2s}^2$ (5.8)

The flow chart of the subroutine for this algorithm is shown in Fig 5.5. This subroutine is used to extract the fundamental, second and fifth harmonic components. From Eqn (5.6), it can be seen that the 16 Fourier coefficients repeat themselves for the sine and cosine of all harmonic components. As a result, only a maximum 16 coefficients are needed to be stored in data memory for DFT.

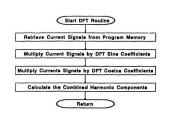


Figure 5.5: Flow chart for Discrete Fourier Transform

Walsh Functions Algorithm (WFA)

In order to find all harmonic components by Walsh Functions, the magnitude of necessary Walsh coefficients have to be computed first as follows:

$$\begin{aligned} W_1 &= I_i + I_{i+1} + I_{i+2} + I_{i+3} + I_{i+4} + I_{i+5} + I_{i+6} + I_{i+7} - I_{i+3} - I_{i+9} - I_{i+10} - I_{i+11} - I_{i+12} - I_{i+33} - I_{i+14} - I_{i+15} \\ W_2 &= I_i + I_{i+1} + I_{i+2} + I_{i+3} - I_{i+4} - I_{i+5} - I_{i+6} - I_{i+7} - I_{i+8} - I_{i+9} - I_{i+9} - I_{i+10} - I_{i+11} + I_{i+12} + I_{i+33} + I_{i+14} + I_{i+15} \\ W_3 &= I_i + I_{i+1} + I_{i+2} + I_{i+3} - I_{i+4} - I_{i+5} - I_{i+6} - I_{i+7} + I_{i+8} + I_{i+9} + I_{i+10} + I_{i+11} - I_{i+12} - I_{i+33} - I_{i+11} - I_{i+15} \\ W_4 &= I_i + I_{i+1} - I_{i+2} - I_{i+3} - I_{i+4} - I_{i+5} + I_{i+6} + I_{i+7} + I_{i+8} + I_{i+9} - I_{i+10} - I_{i+11} - I_{i+12} - I_{i+33} - I_{i+14} + I_{i+15} \\ W_5 &= I_i + I_{i+1} - I_{i+2} - I_{i+3} - I_{i+4} - I_{i+5} + I_{i+6} + I_{i+7} - I_{i+8} - I_{i+9} + I_{i+10} + I_{i+11} + I_{i+12} + I_{i+33} - I_{i+41} - I_{i+15} \\ W_6 &= I_i + I_{i+1} - I_{i+2} - I_{i+3} + I_{i+4} + I_{i+5} - I_{i+6} - I_{i+7} - I_{i+8} - I_{i+9} + I_{i+10} - I_{i+11} - I_{i+12} - I_{i+33} + I_{i+44} + I_{i+15} \\ W_9 &= I_i - I_{i+1} - I_{i+2} + I_{i+3} + I_{i+4} - I_{i+5} - I_{i+6} - I_{i+7} - I_{i+8} + I_{i+9} + I_{i+10} - I_{i+11} - I_{i+12} + I_{i+33} - I_{i+44} - I_{i+5} \\ W_{10} &= I_i - I_{i+1} - I_{i+2} + I_{i+3} - I_{i+4} + I_{i+5} - I_{i+7} - I_{i+8} + I_{i+9} - I_{i+10} - I_{i+11} - I_{i+12} + I_{i+33} - I_{i+44} + I_{i+15} \\ W_{11} &= I_i - I_{i+1} - I_{i+2} + I_{i+3} - I_{i+4} + I_{i+5} - I_{i+7} + I_{i+8} - I_{i+7} - I_{i+9} - I_{i+10} - I_{i+11} - I_{i+12} + I_{i+33} - I_{i+44} + I_{i+15} \\ W_{12} &= I_i - I_{i+1} - I_{i+2} - I_{i+3} - I_{i+4} + I_{i+5} - I_{i+7} + I_{i+9} - I_{i+7} - I_{i+9} -$$

 $I_{i+8} - I_{i+9} + I_{i+10} - I_{i+11} - I_{i+12} + I_{i+13} - I_{i+14} + I_{i+15}$

(5.9)

To relate Walsh coefficients with the sine and cosine terms of DFT, the following equations are used: $S_{1} = 0.900W_{1} - 0.373W_{n} - 0.074W_{n}$

$$\begin{split} C_1 &= 0.900W_2 + 0.473W_4 - 0.074W_{10} \\ S_2 &= 0.900W_3 - 0.373W_{11} \\ C_2 &= 0.900W_4 + 0.373W_{12} \\ S_5 &= 0.180W_1 + 0.435W_5 + 0.650W_9 \end{split}$$

(5.10)

After all the Fourier coefficients are calculated, Eqn (5.8) can be used to find the combined harmonic components of the differential current. The flow chart for this Walsh algorithm is shown in Fig 5.6. From Eqn (5.10) it can be seen that for WFA only six coefficients are needed to be stored in data memory. The predefined coefficient stored are 0.9, 0.373, 0.074, 0.18, 0.435 and 0.65.

 $C_{*} = 0.180W_{2} - 0.435W_{0} + 0.650W_{10}$

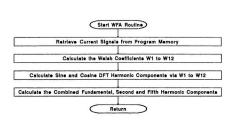


Figure 5.6: Flow chart for Walsh Functions Algorithm

Rectangular Transform Algorithm (RTA)

Rectangular Transform Algorithm is very similar to Discrete Fourier Transform Algorithm. However, it needs the extra third harmonic component to compute the fundamental component. Let $\hat{S}_1, \hat{C}_1, \hat{S}_2, \hat{C}_2, \hat{S}_3, \hat{C}_3, \hat{S}_5, \hat{C}_5$ be the sine and cosine terms of the fundamental, second, third and fifth harmonic components respectively. These are implemented as follows in the software:

$$\begin{split} \dot{S}_1 &= I_i + I_{i+1} + I_{i+2} + I_{i+3} + I_{i+4} + I_{i+3} + I_{i+6} + 0.0 * I_{i+7} - \\ I_{i+8} - I_{i+9} - I_{i+10} - I_{i+11} - I_{i+12} - I_{i+13} - I_{i+40} - 0.0 * I_{i+15} \\ \dot{C}_1 &= I_i + I_{i+1} + I_{i+2} + 0.0 * I_{i+3} - I_{i+4} - I_{i+3} - I_{i+4} - I_{i+7} - \\ I_{i+8} - I_{i+9} - I_{i+10} + 0.0 * I_{i+11} + I_{i+2} - I_{i+3} + I_{i+3} + I_{i+3} + I_{i+15} \\ \dot{S}_2 &= I_i + I_{i+1} + I_{i+2} + 0.0 * I_{i+3} - I_{i+4} - I_{i+3} - I_{i+4} - 0.0 * I_{i+7} + \\ I_{i+8} + I_{i+9} + I_{i+10} + 0.0 * I_{i+11} - I_{i+12} - I_{i+33} - I_{i+3} - 0.0 * I_{i+7} + \\ I_{i+8} + I_{i+9} + I_{i+10} + 0.0 * I_{i+11} - I_{i+12} - I_{i+33} - I_{i+3} + I_{i+4} + I_{i+15} \\ \dot{C}_2 &= I_i + 0.0 * I_{i+1} - I_{i+2} - I_{i+3} - I_{i+1} - 0.0 * I_{i+3} + I_{i+4} + I_{i+15} \\ \dot{S}_3 &= I_i + I_{i+1} - I_{i+2} - I_{i+3} - I_{i+4} - I_{i+3} + I_{i+44} + I_{i+15} \\ \dot{S}_3 &= I_i + I_{i+1} - I_{i+2} - I_{i+3} - I_{i+4} - I_{i+6} - I_{i+7} - \\ I_{i+8} - I_{i+9} + I_{i+10} + I_{i+11} + I_{i+12} - I_{i+13} - I_{i+3} - I_{i+4} - 0.0 * I_{i+15} \\ \dot{C}_3 &= I_i - I_{i+1} - I_{i+2} - 0.0 * I_{i+3} + I_{i+4} + I_{i+5} - I_{i+6} - I_{i+7} - \\ I_{i+8} + I_{i+9} + I_{i+10} + 0.0 * I_{i+11} - I_{i+12} - I_{i+13} + I_{i+14} + I_{i+15} \\ \dot{S}_5 &= I_i - I_{i+1} - I_{i+2} + I_{i+3} - I_{i+4} - I_{i+5} + I_{i+6} - 0.0 * I_{i+7} - \\ I_{i+8} + I_{i+9} + I_{i+10} - I_{i+11} + I_{i+12} + I_{i+3} - I_{i+4} - 0.0 * I_{i+7} - \\ I_{i+8} + I_{i+9} + I_{i+10} - I_{i+11} + I_{i+12} + I_{i+3} - I_{i+4} - 0.0 * I_{i+7} + \\ I_{i+8} + I_{i+9} - I_{i+10} - 0.0 * I_{i+3} + I_{i+4} + I_{i+5} - I_{i+43} - I_{i+4} + I_{i+5} \end{split}$$

The sine and cosine of the above Rectangular coefficients are related to the

Fourier coefficients as follows:

$$S_{1} = \tilde{S}_{1} - \frac{1}{3}\tilde{S}_{3} - \frac{1}{5}\tilde{S}_{5}$$

$$C_{1} = \tilde{C}_{1} + \frac{1}{3}\tilde{C}_{3} - \frac{1}{5}\tilde{C}_{5}$$

$$S_{2} = \tilde{S}_{2}$$

$$C_{2} = \tilde{C}_{2}$$

$$S_{5} = \tilde{S}_{5}$$

$$C_{5} = \tilde{C}_{5}$$
(5.12)

The predefined coefficients to be put in data memory for this algorithm are $0, \frac{1}{3}$ and $\frac{1}{\delta}$ only. The combined harmonic components of the differential current can be calculated by Eqn (5.8). The flow chart for this algorithm is shown in Fig 5.7.

Considering the above discussions, it seems that the computations of this algorithm can be further simplified by omitting the multiplications of some samples by '0' as well as saving a data memory space for storing this '0' coefficient. The reason for putting in the '0' here is to make this algorithm complete as compared to the other algorithms. In the actual program, the '0' is omitted in the calculation.

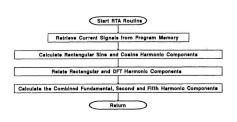


Figure 5.7: Flow chart for Rectangular Transform Algorithm

Finite Impulse Response (FIR) Filtering Algorithm

Using differential sample I_i , sampled 16 times per cycle, the FIR filter outputs are calculated as follows:

$$S_1 = \sum_{i=1}^{8} [l_i - l_{i+8}]$$

$$C_1 = \sum_{i=1}^{4} [l_i - (l_{i+4} + l_{i+8}) + l_{i+12}]$$

$$S_2 = \sum_{i=1}^{4} [l_i - l_{i+4} + l_{i+8} - l_{i+12}]$$

$$C_2 = \sum_{i=1}^{2} [l_i - (l_{i+2} + l_{i+4}) + l_{i+6} + l_{i+8} - (l_{i+10} + l_{i+12}) + l_{i+11}] \quad (5.13)$$

The FIR approach can only accommodate fundamental and second harmonic components. In the software, the fifth harmonic sine and cosine components are found by using the Rectangular Transform Algorithm given in Eqn (5.11). The flow chart is shown in Fig 5.8. For this algorithm, no coefficient has to be stored in data memory for calculation.

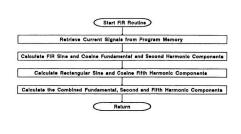


Figure 5.8: Flow chart for Finite Impulse Response filtering

Least Square Algorithm (LSA)

In order to find the coefficients for LSA, a 16x12 matrix has to be solved. Then the sine and cosine harmonic components of the differential current can be found by the following terms:

$$\begin{split} S_1 &= -0.579477l_i + 0.156244l_{i+1} - 0.062795l_{i+2} + 0.045696l_{i+3} + \\ &- 0.287002l_{i+4} + 0.004070l_{i+5} + 0.072985l_{i+6} + 0.163731l_{i+7} - \\ &- 0.115895l_{i+8} - 0.032432l_{i+9} + 0.023026l_{i+10} - 0.277486l_{i+11} - \\ &- 0.055211l_{i+12} + 0.035699l_{i+13} - 0.496798l_{i+14} + 0.531612l_{i+15} \\ &- 0.099735l_i + 0.196723l_{i+1} + 0.058316l_{i+2} + 0.033953l_{i+3} + \\ &- 0.032224l_{i+4} - 0.069997l_{i+5} - 0.091452l_{i+6} - 0.092432l_{i+7} - \\ &- 0.148053l_{i+8} - 0.112421l_{i+9} - 0.066227l_{i+10} - 0.080060l_{i+11} + \\ &- 0.013882l_{i+12} + 0.077908l_{i+13} + 0.007151l_{i+11} + 0.230750l_{i+15} \\ S_2 &= -0.278275l_i + 0.284513l_{i+1} + 0.052399l_{i+2} + 0.054874l_{i+3} + \\ &- 0.077796l_{i+4} - 0.141891l_{i+5} - 0.132397l_{i+6} - 0.032733l_{i+7} - \\ &- 0.055655l_{i+8} + 0.095785l_{i+9} + 0.178503l_{i+10} + 0.010592l_{i+11} + \\ &- 0.033514l_{i+12} - 0.015787l_{i+13} - 0.321125l_{i+14} + 0.189886l_{i+15} \\ C_2 &= 0.009735l_i + 0.169626l_{i+1} - 0.030072l_{i+2} - 0.102270l_{i+3} - \\ &- 0.092776l_{i+4} - 0.110550l_{i+5} - 0.003661l_{i+6} + 0.111441l_{i+7} + \\ &- 0.111118l_{i+12} - 0.058316l_{i+13} - 0.081238l_{i+14} + 0.203654l_{i+15} \\ S_5 &= -0.077018l_i + 0.1696261l_{i+1} - 0.18182l_{i+2} - 0.057111l_{i+3} + \\ &= 0.146531l_{i+4} - 0.062643l_{i+5} - 0.090436l_{i+6} + 0.130888l_{i+7} - \\ &= 0.015404l_{i+8} - 0.113438l_{i+9} + 0.103196l_{i+0} + 0.026304l_{i+11} - \\ &= 0.115728l_{i+1} - 0.067929l_{i+3} + 0.031197l_{i+14} - 0.0388467l_{i+15} \\ \end{aligned}$$

```
 \begin{split} C_5 &= & 0.009735I_i + 0.033402I_{i+1} - 0.118461I_{i+2} + 0.101603I_{i+3} + \\ &= & 0.032224I_{i+1} - 0.137647I_{i+5} + 0.085324I_{i+6} + 0.070888I_{i+7} - \\ &= & 0.148053I_{i+8} + 0.050899I_{i+9} + 0.110550I_{i+10} - 0.147799I_{i+11} + \\ &= & 0.013882I_{i+12} + 0.145557I_{i+13} - 0.169626I_{i+14} + 0.067430I_{i+15}(5.14) \end{split}
```

The flow chart of the subroutine is shown in Fig 5.9. This subroutine is used to extract the fundamental, second and fifth harmonic components. The combined harmonic components can be calculated using Eqn (5.8). This algorithm requires the largest data memory to store the coefficients.

All the above mentioned algorithms are basically a process of non-recursive digital filtering. Each algorithm is to determine the peak of fundamental, second and fifth harmonic components as each new current sample is taken. The output depends on the present and the immediate past input signals. Only the filter coefficients are unique to each algorithm.

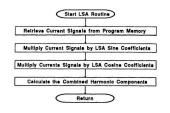


Figure 5.9: Flow chart for Least Square Algorithm

5.2.5 Protection Scheme

After all combined harmonic components are calculated and stored in memory, the second harmonic restraint is checked by the software. If the second harmonic component of the differential current is higher than the predefined harmonic restraint percentage T_{2r} compared with the fundamental component, an inrush condition is declared and the program will go to the subroutine that checks for the ground fault. Otherwise it will go to the over-excitation subroutine to test for the fifth harmonic components.

In the over-excitation subroutine, the fifth harmonic restraint for transformer over-excitation is checked. The over-excitation threshold value T_{aa} is for tossen instead of the normal one T_{ad} if the fifth harmonic component of the differential exceed the restraint percentage T_{3c} . Using the fundamental component of differential and through current, the percentage differential characteristic is then checked for all phases as shown in the flow chart of Fig 5.10. If a fault is found in any phase, the fault counter of that particular phase in the software is incremented. Otherwise, it is reset to zero. Then the program will proceed to the subroutine that checks for ground fault.

From the laboratory setup shown in Fig 5.4 it can be seen that the neutral current will normally be equal to the sum of currents in the three phases. The ground solid state relay should not trip unless there is a ground fault to upset the balance. However, in a heavy through fault (external fault) condition, the ground current transformer will be saturated due to fault current asymmetry that may trip the relay. Fortunately, during through fault condition, larger second harmonics are found in the ground current compared with the ground fault case. Hence in the ground subroutine of the software a second harmonic ground restraint. They is implemented. If the second harmonic to fundamental component ratio of

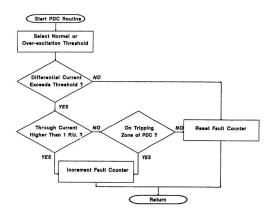


Figure 5.10: Flow chart for the percentage differential characteristic subroutine

the ground fault current is below the ground restraint ratio T_{xy} and the ground fault current also exceeds the ground fault threshold T_{yf} , a ground fault is declared. As a result the ground fault counter in the software is incremented, otherwise it is reset back to zero. However, if the second harmonic ratio stays above the ground fault restraint threshold level, an external fault is declared and the ground fault counter is again reset to zero. The flow chart for this ground subroutine is shown in Fig 5.11.

If any fault counter exceeds its threshold which is 1 for differential fault and 5 for ground fault, a trip signal is sent to trip all solid state relays that are connected to the power transformer to cut off the power supplies. After this the software will wait in a loop until it is restarted via the computer terminal by a user. If no fault is found, the software will wait for the next interrupt to start input of the next set of current signals to continue the protection analysis.

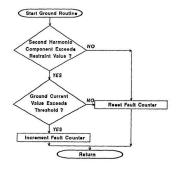


Figure 5.11: Flow chart for the ground subroutine

Chapter 6

Laboratory Testing of the Digital Relay

This chapter presents the experimental testing results and analysis of the microprocessor based digital relay for the following five algorithms: Discrete Fourier
Transform (DFT), Walsh Functions Algorithm (WFA), Rectangular Transform
Algorithm (RTA), Finite Impulse Response (FIR) filtering, and Least Square Algorithm (LSA). The real time testing results have been recorded via a digital
oscilloscope with a plotter to obtain high precision. Due to the limitation of the
oscilloscope with only two channels, only one phase of the current signal with the
trip signal can be shown at one time. To make sure that all phases were covered,
the phase current recorded for each test with each algorithm has been chosen at
random. The hard copies of some of the real time testing results can be found in
Appendix E. A computer program, written in C, has been developed for each algorithm for analysis using the real time data obtained from the power transformer.
The program has been verified via simulation data.

Each test case has been done with both no load and with load conditions. In the case of tests with load, the power transformer has been connected to a three phase resistive load with a rating of 1 kilovolt at 40 kilowatt. The testing setup is shown on Fig 6.1. All test cases, such as inrush test, internal and external faults

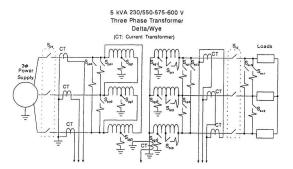


Figure 6.1: Testing procedure setup

tests etc., can be performed by simultaneously closing one or more of the switches on the testing setup. For example, a primary phase - to - phase fault can be carried out by closing switch S_{201} while switch S_{20} is in the closed position.

6.1 Inrush Tests

The magnetizing inrush test was carried out by closing the switch S_{ps} (Fig 6.1) while the digital relay was on. It can also be done with the switch S_{ps} closed at the beginning and then turning on the digital relay. In the case of the no load inrush test, the switch S_{tt} should be left open, whereas for the test with load, the switch S_{tt} should be closed before the test is performed.

Fig 6.2(a) shows the calculated inrush differential currents of a real time no load inrush test. It can be seen that in this case the amplitude of the differential currents go above 3 P.U. which is much higher than the threshold value of 0.05

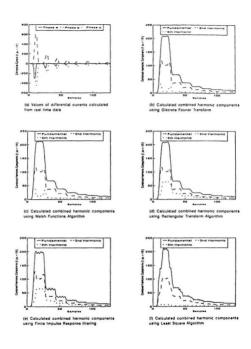


Figure 6.2: Calculated differential currents and combined harmonic components of the no load inrush test

P.U.. This may be recognized as a fault if the digital relay is not working properly. Figs 6.2(b) to (f) show the combined fundamental, second, and fifth harmonics produced by the five algorithms. The results show that the amplitude of the fundamental and second harmonics are both high during inrush condition. Also, the harmonic waveforms generated by Finite Impulse Response filtering (FIR) and Least Square Algorithms (LSA) are not as smooth as the other three algorithms.

Fig 6.3 shows the ratio of second harmonic to fundamental components of the five algorithms. The harmonic ratios are found to be around 0.5 which is above the 0.177 second harmonic restraint threshold value and the digital relay is restrained from tripping for all algorithms. Notice that the ratio value of FIR and LSA are fluctuating. If the threshold value is increased, these two algorithms may not give the proper results.

The plot of combined harmonic components of the inrush test with load is shown in Fig 6.4 and the ratio of second harmonic to fundamental components is shown in Fig 6.5. Similar to the no load case, the digital relay is restrained from tripping due to the presence of a strong second harmonic component. Many tests have been done for the inrush test for both no load and load cases. No fault tripping of the digital relay occurred for the five algorithms in all inrush tests.

6.2 Internal Fault Tests

Various types of internal faults tests were conducted on the digital relay in the laboratory. The tests may not cover all the existing transformer internal fault cases, however, they should show the general performance of all the algorithms during an internal fault. Some of the tests that were carried out in this category are:

· Fault occurred between primary phases and between secondary phases.

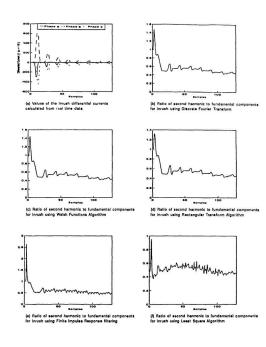


Figure 6.3: Calculated differential currents and ratio of second harmonic to fundamental components of the no load inrush test

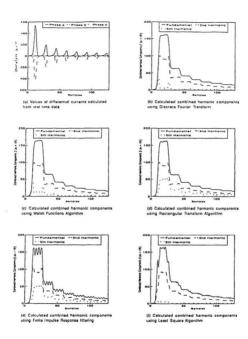


Figure 6.4: Calculated differential currents and combined harmonic components of the inrush test with load

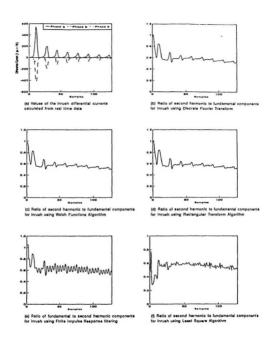


Figure 6.5: Calculated differential currents and ratio of second harmonic to fundamental components of the inrush test with load

- · Inrush followed by a phase to phase fault.
- · Switching on a phase to phase fault.
- · Fault occurred between secondary taps.

A power resistor of approximately 7.5 ohms was used for all the internal fault tests. No test was done for a fault current higher than 10 P.U.. such a heavy fault can trip the main circuit breaker of the laboratory.

6.2.1 Phase - to - phase fault tests

Primary phase \cdot to \cdot phase fault tests can be performed by closing switch S_{pp1} , S_{pp2} , S_{pp3} , or a combination of the above switches with switch S_{ps} closed (Fig. 6.1) while the digital relay is on. The secondary phase \cdot to \cdot phase fault tests can be carried out by closing either switch S_{pp} , S_{pp3} , S_{pp3} , or a combination of these witches with switch S_{ps} closed. Due to the shortage of testing equipment in the laboratory, only single phase fault tests have been done. The multi \cdot phase fault tests should have similar results as the single phase ones.

Fig. 6.6(a) shows the plot of the calculated differential currents of a no load real time primary phase a - b fault test. Fig. 6.8(a) shows the waveform of the differential currents of a secondary no load real time phase a - b fault test. It can be seen that the amplitude of the differential currents for the primary fault case is above 1.5 P.U. and for the secondary fault case is higher than 5 P.U. which will undoubtly exceed the threshold value of 0.05 P.U.

Figs 6.6(b) to (f) and Figs 6.8(b) to (f) show the combined fundamental, second, and fifth harmonic components plot for the five algorithms of the primary and secondary phase - to - phase fault tests, respectively. In both cases, the amplitude of the fundamental component of all algorithms increases and stays high whereas the second harmonic component decreases during the fault. This leads to the

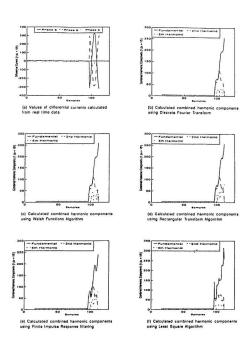


Figure 6.6: Calculated differential currents and combined harmonic components of the no load primary phase a - b fault test

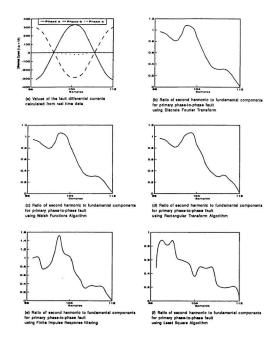


Figure 6.7: Calculated fault differential currents and ratio of second harmonic to fundamental components of the no load primary phase a - b fault test

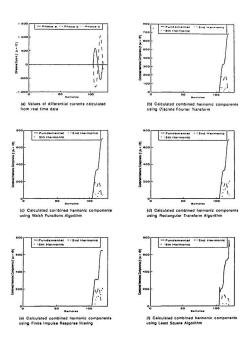


Figure 6.8: Calculated differential currents and combined harmonic components of the no load secondary phase a - b fault test

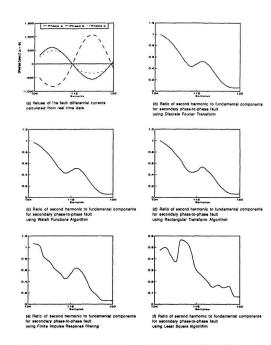


Figure 6.9: Calculated fault differential currents and ratio of second harmonic to fundamental components of the no load secondary phase a - b fault test

decrement of the second harmonic to fundamental ratio as shown in Fig 6.7 and Fig 6.9 for the primary and secondary phase - to - phase faults, respectively. The digital relay has been tripped when the ratio has gone below the 0.177 threshold level for all algorithms in both tests.

The diagrams of combined harmonic components of the primary and secondary phase a - b fault with load are shown in Fig 6.10 and Fig 6.12, respectively. Also the ratio of second harmonic to fundamental components with load are shown in Fig 6.11 and Fig 6.13 for the primary and secondary fault tests respectively. Similar to the no load case, the digital relay was tripped with all algorithms due to high differential faulty currents and the second harmonic to fundamental ratio below a 0.177 threshold.

Numerous tests has been done for these primary and secondary phase - to phase faults. The digital relay has been tripped every time this type of fault has
occurred, regardless of the algorithm.

6.2.2 Inrush followed by an internal fault tests

This test was done by closing switch S_{pg} and then switch S_{pg1} , S_{pg2} , or S_{pp3} (Fig 6.1) with the digital relay running. The internal fault created here was actually a primary phase - to - phase fault.

Fig 6.14(a) shows the plot of the calculated differential currents of a no load real time inrush followed by a primary phase a - b fault test. In this case, the fault occurs at the 41st sample. Although the amplitudes of both the inrush currents and the faulty currents exceed the 0.05 P.U. normal working threshold level, the maximum amplitude of the inrush differential currents is higher than the fault curents. Figs 6.14(b) to (f) show the waveforms of the calculated combined harmonic components of all algorithms. The displayed waveform from the first sample to the 40th sample is similar to the inrush test case with the high fundamental and sec-

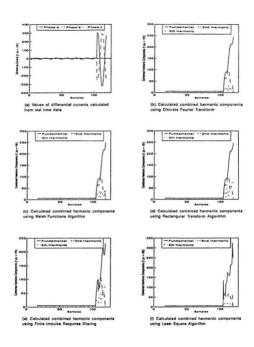


Figure 6.10: Calculated differential currents and combined harmonic components of the primary phase a - b fault test with load

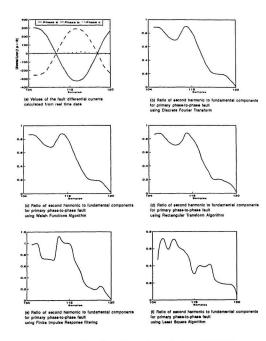


Figure 6.11: Calculated fault differential currents and ratio of second harmonic to fundamental components of the primary phase a - b fault test with load

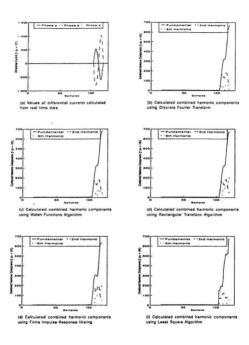


Figure 6.12: Calculated differential currents and combined harmonic components of the secondary phase a - b fault test with load

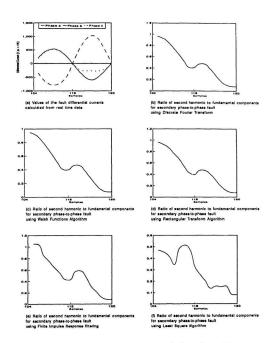


Figure 6.13: Calculated fault differential currents and ratio of second harmonic to fundamental components of the secondary phase a - b fault test with load

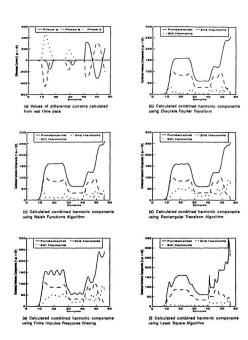


Figure 6.14: Calculated differential currents and combined harmonic components of a no load inrush followed by a primary phase a - b fault test

ond harmonic amplitudes. After sample 41, the waveform behaves exactly like the primary phase - to - phase fault that has been mentioned previously with fundamental component increases and second harmonic component decreases. Also the combined harmonic waveforms of the Finite Impulse Response filtering and Least Square Algorithm are not as smooth as compared with other three algorithms.

Fig 6.15 shows the ratio of the second harmonic to fundamental components of the no load test with the five algorithms. The second harmonic ratios before sample 41 are above 0.3. Afterwards, the ratios drop to below 0.177 threshold value to trip the digital relay.

The plot of combined harmonic components of the inrush followed by a primary phase a - b fault with load is shown on Fig 6.16. The fault starts at the 33rd sample. Fig 6.17 shows the ratio of fundamental to second harmonic components of the load test with the five algorithms. Similar to the no load test, the digital relay is restrained from tripping due to the presence of strong second harmonic component. During the fault period, the faulty differential currents are high and the second harmonic ratio drops below 0.177 threshold to trip the digital relay.

Of all the load and the no load tests that have been done, the digital relay performed accurately with the use of any of the five algorithms.

6.2.3 Switching on with an internal fault tests

This test was done by closing switch S_{ps} with S_{sp1} , S_{sp2} , or S_{sp3} closed (Fig 6.1) while the digital relay is running.

Fig 6.18 and Fig 6.20 show the plots of the calculated combined harmonic components of the no load and the load tests, respectively. Similar to other internal fault tests, the fundamental component stays high whereas the second harmonic component decreases during a fault.

Fig 6.19 and Fig 6.21 show the combined harmonic to fundamental component

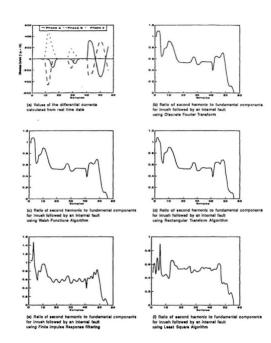


Figure 6.15: Calculated differential currents and ratio of second harmonic to fundamental components of a no load inrush followed by a primary phase a - b fault test

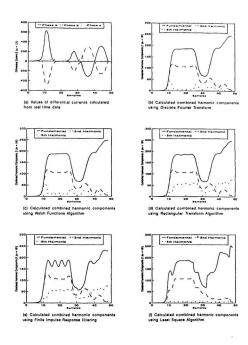


Figure 6.16: Calculated differential currents and combined harmonic components of an inrush followed by a primary phase a - b fault test with load

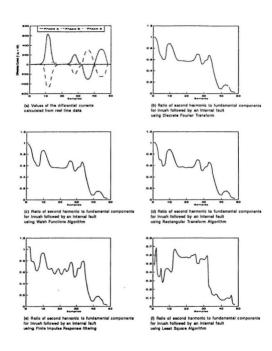


Figure 6.17: Calculated differential currents and ratio of second harmonic to fundamental components of an inrush followed by a primary phase a - b fault test with load 106

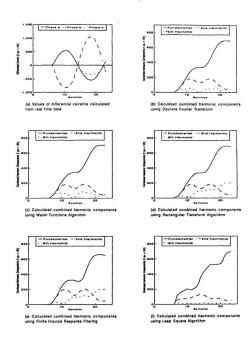


Figure 6.18: Calculated differential currents and combined harmonic components of a switching on with a secondary phase a - b fault test without the load

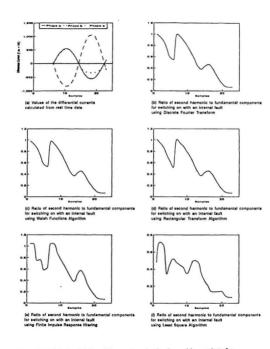


Figure 6.19: Calculated differential currents and ratio of second harmonic to fundamental components of a switching on with a secondary phase a - b fault test without load 108

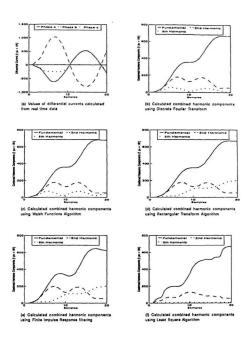


Figure 6.20: Calculated differential currents and combined harmonic components of a switching on with a secondary phase a - b fault test with load

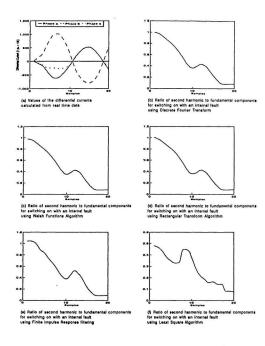


Figure 6.21: Calculated differential currents and ratio of second harmonic to fundamental components of a switching on with a secondary phase a - b fault test with load

waveform of all algorithms without and with load respectively. It can be seen that
the second harmonic ratio goes below 0.177 threshold at the 22nd sample for the no
load test and at the 17th sample for the load test. For this particular case, the no
load test takes longer for the digital relay to trip than in the load test. Generally,
an internal fault will take only 16 samples interval for the second harmonic ratio to
go below threshold value to make a trip decision. However, due to the presence of
inrush currents when the power transformer is being switched on, a strong second
harmonic component is introduced. The second harmonic ratio will not decrease
as long as the inrush remains. Obviously, in this case, the no load test has more
inrushes than the load test when the transformer is turned on. Although this test
show that the inrush disappears after several samples, in some cases, the inrush
can remain as long as several cycles before it is gone. As a result, it will take longer
for the digital relay to make a trip decision.

All algorithms have performed correctly for all the tests that have been done so far for the switching on with an internal fault tests.

6.2.4 Between taps fault tests

This test was done by closing switch S_{k1} , S_{k2} , or S_{k3} with switch S_{ps} (Fig 6.1) remained in the closed position while the digital relay is on. The fault has occurred between 550 - 600 V taps on the secondary side of the power transformer.

Fig 6.22(a) shows the waveform of the no load differential currents calculated from real time data for the between secondary phase c 550 - 600 V taps fault. During the fault, the fault differential currents increased to around 0.3 P.U.. Figs 6.22(b) to (f) show the combined harmonic components plot for all five algorithms. Similar to other internal faults, the fundamental component stays high whereas the second harmonic goes low. Fig 6.23 displays the no load second harmonic to fundamental components ratio of all algorithms. The second harmonic

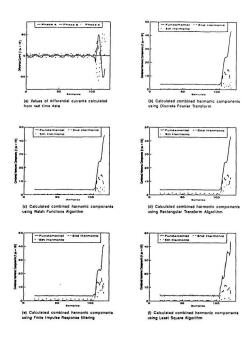


Figure 6.22: Calculated differential currents and combined harmonic components of a between secondary phase c 550 - 600 V taps fault test without load

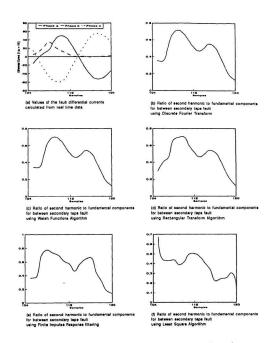


Figure 6.23: Calculated differential fault currents and ratio of second harmonic to fundamental components of a between secondary phase c 550 -600 V fault test without load

ratio decreases down to below 0.177 threshold value during the fault period to trip the digital relay.

Fig 6.24 and Fig 6.25 show the plot of combined harmonic components and the second harmonic to fundamental ratio of all algorithms respectively for the load test. Identical to the no load test, the relay will trip as soon as the second harmonic ratio has dropped to below threshold level.

All five algorithms have performed accurately with all the load and no load tests that had been done. The digital relay is tripped every time when a differential current is above 0.05 P.U. threshold with second harmonic ratio under 0.177 threshold.

6.3 Ground fault tests

The primary ground fault test was carried out by closing switch S_{pg1} , S_{pg2} , or S_{pj3} with switch S_{ps} closed (Fig 6.1) and the relay running. Switch S_{sg1} , S_{sg2} , or S_{sg3} was closed instead for the secondary ground fault test. A high impedance power resistor of approximately 100 ohms was used for the ground fault tests.

Fig 6.26(a) shows the differential currents and primary ground fault current plot calculated from the real time data for a no load primary phase a - ground g fault test. Figs 6.26(b) to (f) display the fundamental and second harmonic components of the primary ground fault current of all five algorithms. When a fault occurs, the fundamental goes high whereas the second harmonic component decreases.

Fig 6.27 shows the ratio of second harmonic to fundamental components for the primary ground fault current for all algorithms. When this ratio drops below 0.1225 threshold value, the digital relay will check the amplitude of the primary ground current. If the amplitude exceeds the threshold value of 0.05 P.U., the ground counter in the digital relay software will be incremented by 1. After the

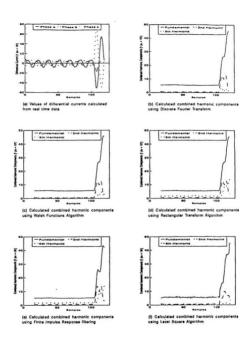


Figure 6.24: Calculated differential currents and combined harmonic components of a between secondary phase c 550 - 600 V taps fault test with the load

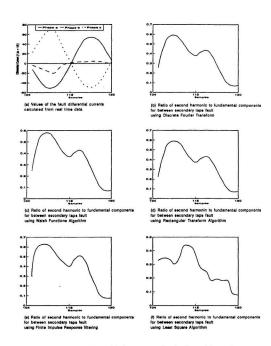


Figure 6.25: Calculated differential fault currents and ratio of second harmonic to fundamental components of a between secondary phase c 550 -600 V fault test with load

116

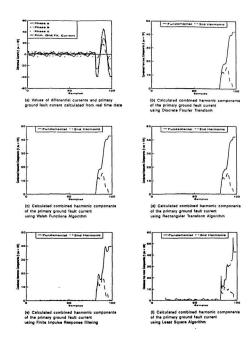


Figure 6.26: Calculated differential currents and primary ground fault current and combined harmonic components of a primary a - g ground fault test without load

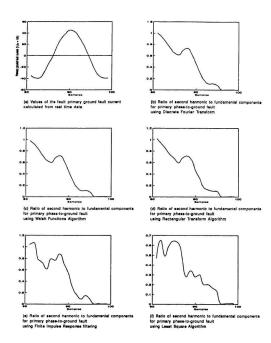


Figure 6.27: Calculated fault primary ground fault current and ratio of second harmonic to fundamental components of a primary a - g ground fault test without load

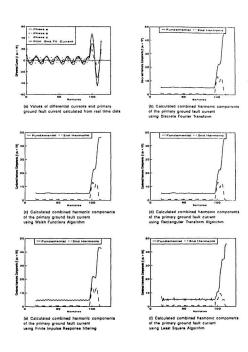


Figure 6.28: Calculated differential currents and primary ground fault current and combined harmonic components of a primary a - g ground fault test with load

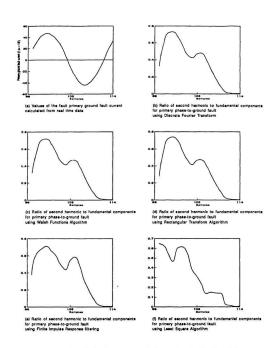


Figure 6.29: Calculated fault primary ground fault current and ratio of second harmonic to fundamental components of a primary a - g ground fault test with load

counter exceeds the threshold of 5, a trip signal is sent by the software to trip the digital relay. Fig 6.28 displays the amplitude of fundamental and second harmonic components of the primary ground fault current with load and Fig 6.29 shows the second harmonic ratio of the load test. The waveform of the load test may have some differences in magnitude with the no load case, however, the second harmonic ratio still decreases below the threshold value and the digital relay is tripped when the ground fault counter exceeds 5.

Fig 6.30 to Fig 6.33 show the performance of the five algorithms for a secondary a - g ground fault no load and load test. Although at this time, the ground fault is on the secondary side, the results are basically the same as the primary ground fault tests. The only difference in this case is that the second harmonic ratio of the secondary ground fault current is checked instead of the primary one for the inc.ment of the fault counter.

The digital relay has executed accurately for the entire primary and secondary ground fault tests that have been done with all five algorithms.

6.4 Steady state over-excitation tests

The over-excitation test was done by increasing the phase voltage from 120 V to around 170 V with switch S_{ps} closed (Fig 6.1) while the digital relay is running. The increment of the voltage was set to approximately 40% because too much over-excitation would damage the power transformer. Since the laboratory could not provide a power supply that could be used for this test, an extra step up power transformer was used to give the necessary voltage.

Fig 6.34(a) shows the amplitude of a no load over-excitation differential currents calculated from a real time test result and Figs 6.34(b) to (f) display the combined harmonic components by all algorithms. It can be seen that, in gen-

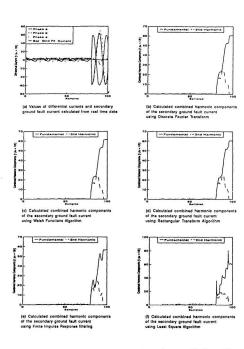


Figure 6.30: Calculated differential currents and secondary ground fault current and combined harmonic components of a secondary a - g ground fault test without load 122

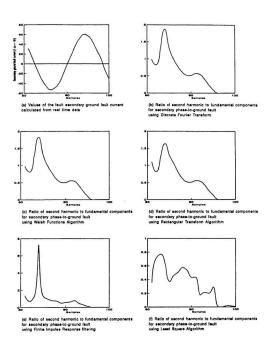


Figure 6.31: Calculated fault secondary ground fault current and ratio of second harmonic to fundamental components of a secondary a - g ground fault test without load 123

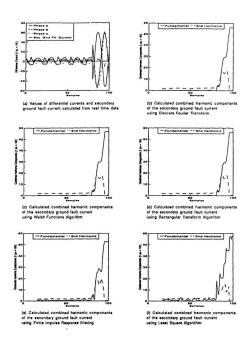


Figure 6.32: Calculated differential currents and secondary ground fault current and combined harmonic components of a secondary a - g ground fault test with load 124

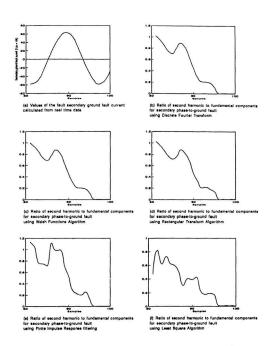


Figure 6.33: Calculated fault secondary ground fault current and ratio of second harmonic to fundamental components of a secondary a - g ground fault test with load

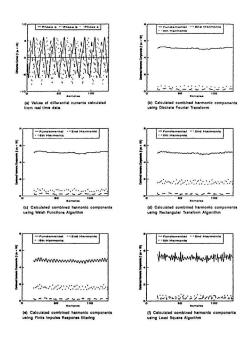


Figure 6.34: Calculated differential currents and combined harmonic components of the no load over-excitation test

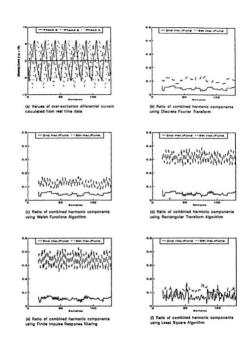


Figure 6.35: Calculated differential currents and ratio of second harmonic to fundamental components of the no load over-excitation test

eral, the fifth harmonic component is higher than the second harmonic due to the over-excitation condition. Fig 6.35 shows the combined harmonic ratio produced by the five algorithms. Although the second harmonic ratio goes below the 0.177 threshold level, the digital relay is restrained from tripping by the fifth harmonic component. The fifth harmonic ratio is set to above the 0.065 threshold for all algorithms.

Fig 6.36 and Fig 6.37 display the waveforms of calculated over-excitation combined harmonic components and the combined harmonic ratio, respectively, with load. This test has similar results to the no load one with the fifth harmonic ratio above the threshold level to prevent the digital relay from tripping.

Although all algorithms performed correctly with numerous load and no load over-excitation tests that have been carried out, the fifth harmonic restraint ratio threshold of Rectangular Transform Algorithm (RTA) and Finite Impulse Response filtering (FIR) should be increased to obtain more accuracy. Also, the harmonic ratios calculated from all algorithms except Discrete Fourier Transform (DFT) are fluctuating. This implies that DFT is more precise than the other four algorithms based on the experience from this particular experimental results.

6.5 External fault tests

The external fault test was carried out by closing switch S_{ex1} , S_{ex2} , or S_{ex3} with switch S_{ps} in the closed position (Fig 6.1) while the digital relay is on. Switch S_{td} was also closed for the tests with load.

Fig 6.38(a) shows the plot of the differential currents and primary ground fault current of a real time no load test. The external fault starts at the 65th sample. Figs 6.38(b) to (f) display the fundamental and second harmonic components of the primary ground fault current of all algorithms. It can be seen that during an

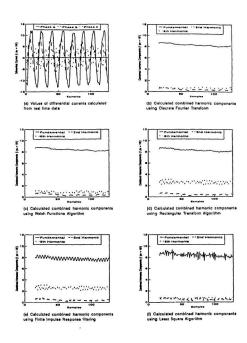


Figure 6.36: Calculated differential currents and combined harmonic components of the over-excitation test with load

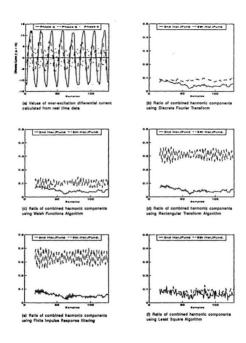


Figure 6.37: Calculated differential currents and ratio of second harmonic to fundamental components of the over-excitation test with load

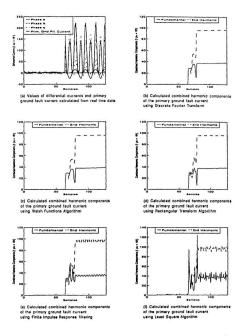
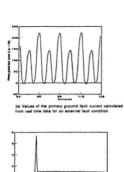
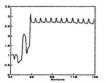


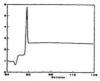
Figure 6.38: Calculated differential currents and primary ground fault current and the combined harmonic components for a no load external fault test



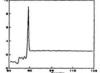
(c) Ratio of second harmonic to fundamental components for an ext ' 'fault condition using Walsh', 'critions Algorithm



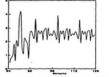
(e) Ratio of second harmonic to fundamental components for an external fault condition using Finite impulse Response filtering



(b) Ratio of second harmonic to fundamental components for an external fault condition using Discrete Fourier Transform



(d) Railo of second harmonic to fundamental components for an external fault condition using Rectangular Transform Algorithm



(f) Ratio of second harmonic to fundamental components for an external fault condition using Least Square Algorithm

Figure 6.39: Calculated primary ground fault current and ratio of second harmonic to fundamental components for a no load external fault test

external fault, both fundamental and second harmonic components increase and then stay at constant high values. Fig 6.39 shows the graphs of second harmonic to fundamental components ratio of the no load external fault test. The ratio of second harmonic to fundamental of all algorithms increase and then decrease to around 2.75. Although the primary ground fault current exceeds the threshold value of 0.05 heavily, the relay will not trip because the second harmonic ratio never falls below the ground restraint threshold value of 0.1225.

Fig 6.40 and Fig 6.41 show the plot of combined fundamental and second harmonic components, and the second harmonic ratio of the primary ground fault current, respectively, of an external fault test with load. Similar to the no load test, the relay is restrained from tripping because the second harmonic ratio is always above the ground restraint threshold value, irrespective of the algorithm.

The digital relay has executed accurately for all the external fault tests that has been carried out with all five algorithms.

6.6 Summary

All five algorithms have performed accurately for all the tests that have been done so far. The digital relay has never misoperated. However, if the calculated combined harmonic ratio of all tests have been examined carefully, it can be seen that the ratio fluctuation is generally high when using Rectangular Transform Algorithm, Finite Impulse Response filtering, and Least Square Algorithm compared with the other two algorithms. The ratio fluctuation for the Walsh Functions Algorithm is also high in the external fault tests. This harmonic ratio is often used for making digital relay trip decision. The fluctuation may affect the decision if another power transformer or a different set of threshold values are used. Using this information, the algorithms are rated as shown in Table 6.1. The table also

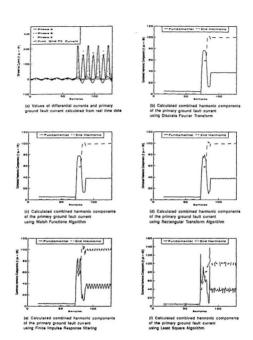


Figure 6.40: Calculated differential currents and primary ground fault current and combined harmonic components for an external fault test with load

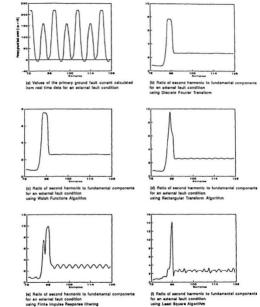


Figure 6.41: Calculated primary ground fault current and ratio of second harmonic to fundamental components for an external fault test with load

Algorithm	Approx. Time for Arithmetic Computation (ns)	Extra Data Memory Needed (Word)	Accuracy
Discrete Fourier Transform	280	16	Excellent
Walsh Functions Algorithm	330	6	Very good
Rectangular Transform Algorithm	220	3	Very good
Finite Impulse Response filtering	140	0	Very good
Least Square Algorithm	280	96	Very good

Table 6.1: Comparison for transformer digital relay algorithms

includes the number of extra data memory needed to store the coefficients of differential algorithms and the approximate time for one call to each algorithm in the relay software.

Among all the five algorithms, if the speed (arithmetic computation) and the size of extra data memory needed are the only criteria for picking a suitable algorithm to use for the digital relay, the Finite Impulse Response filtering should be the one. However, nowadays memory chips and extremely fast microprocessors can be obtained easily with a very low price. Accordingly, the software operation time and memory storage space are not the important factors anymore. The main criterion for transformer protection is accuracy. Although the digital relay has never misoperated on all the tests that have been done, Discrete Fourier is the algorithm that has the least fluctuation in the harmonic ratio values which are used for making trip decision. Based on the experimental results, Discrete Fourier Transform is likely to be the 'best' algorithm because of its accuracy and speed compared with the other four algorithms for real time digital relay implementation using a microprocessor.

Chapter 7

Conclusions and Future Works

7.1 Conclusions

A stand-alone microprocessor based digital relay has been developed and tested. The hardware of the digital relay has been designed to be a "black hox". For the protection of different types of transformers, the only item that has to be modified is the software. The hardware has been put in a 36 × 50 × 36 cm³ box. The external connections to the box include power supplies to power up the hardware, solid state relays to turn on/off the supply to the power transformer, current transformers to obtain phase currents and ground current signals, an external clock for sampling, and a computer terminal for downloading the software.

The software has been developed in the TMS assembly language. Subroutines have been written for differential protection with second harmonic restraint of inrush currents, the fifth harmonic restraint of over-excitation, and the primary and secondary ground faults protection. The second harmonic restraint was also incorporated in the software for external fault conditions. Five algorithms have been tested for harmonic extraction. They are Discrete Fourier Transform (DFT), Walsh Function Algorithm (WFA), Rectangular Transform Algorithm (RTA), Finite Impulse Response (FIR) filtering, and Least Square Algorithm (LSA). Among all five algorithms. FIR filtering required the least number of data memory and

needed the least time for execution. Extensive tests have been done and there are no misoperations of the digital relay in any of the tests. However, Discrete Fourier Transform is the algorithm that has the least fluctuations in the harmonic ratio values that are used for making a trip decision. Based on the experimental results, DFT is chosen because of its accuracy and speed. As a result, a transformer test set-up is developed. The test set-up is a relay module which can be used for protection of any kind of three phase transformer. It has the potential to be used in industrial transformer protection applications.

7.2 Future Works

The TMS32010 boards introduce high electromagnetic interference. So far they do not affect the digital relay performance in the laboratory. However, the results may be different when used in a more harsh environment. A higher model of TMS signal processing board may be used to replace the old ones to prevent the interference.

In order to use this digital relay for industrial application, it has to be tested extensively in real life environment and modified to meet the IEEE standard.

The present digital relay is used only to clear a fault when it occurs. If an artificial intelligence software can be incorporated into this digital relay, to predict when a fault will occur and clear it before it happens, the performance of the relay will be further improved.

Finally, research in the area of remote transformer protection is needed. The cost for using one set of hardware to protect one power transformer is high. If a central protection unit with multiple processors can be built for protection of transformers from different locations, the cost should be decreased. The transformer data can be obtained via telephone lines or microwave with minimum data

acquisition hardware in each site.

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Appendices

Appendix A

MATLAB Program to Find Frequency and Phase Response of the Anti-Aliasing Filter

```
format short e

% Resister R = 1k ohm

% r=1000;

% Calculate scaling factor

% s=1/(2*pi*400*r);

% Find all capacitors value

% c1=2.553*s;
c2=1.776*s;
c3=3.487*s;
c4=0.4917*s;
```

```
c5=9.531*s:
c6=0.111's:
%
% Coefficients of first 2nd order transfer function
%
b12=c1*c2*r*r;
b11=2*c2*r:
b10=1;
%
% Coefficients of second 2nd order transfer function
%
b22=c3*c4*r*r;
b21=2*c4*r;
b20=1:
%
% Coefficients of third 2nd order transfer function
%
b32=c5*c6*r*r;
b31=2*c6*r;
b30=1:
1%
% Find the coefficients of 6th order transfer function
%
x1=[b12 b11 b10];
x2=[b22 b21 b20];
x3=[b32 b31 b30];
v1 = conv(x1,x2);
```

```
y = conv(y1.x3);
%
% Find the six filter poles
%
roots(v);
z=1:
%
% Get the magnitude and phase response
%
[mag, phase, w] = bode(z, y);
%
% Create plot file for printing
% v1=[0,900,0,1.2];
axis(v1)
subplot(211),plot(w/(2*pi),mag)
xlabel('Frequency (Hz)'),ylabel('Normalized Gain')
grid
v2=[0,900,-500,0];
axis(v2)
subplot(212),plot(w/(2*pi),phase)
xlabel('Frequency (Hz)'),ylabel('Phase (deg)')
grid
meta alifil
!gpp/diet/ot alifil
```

Appendix B

Detail Calculation of the Anti-Aliasing Filter

The filter circuit used in the design is one of a class of circuits that was described in 1955 by Sallen and Key [38] as shown in Fig B.I. This is the circuit for a two pole filter. For a sixth-order chebyshev filter, three sets of cascade circuits are needed. These circuits can be routinely analyzed using Kirchhoff's current law. At node aof Fig B.I the currents directed out of the node must sum to zero as:

$$\frac{V_2 - V_b}{R_2} + V_2 C_2 s = 0 \tag{B.1}$$

Similarly, the sum of current leaving node b is:

$$\frac{V_b - V_2}{R_2} + C_1(V_b - V_2)s + \frac{V_b - V_1}{R_1} = 0$$
(B.2)

Next this equation is rearranged as:

$$(\frac{1}{R_1} + \frac{1}{R_2} + C_1 s)V_b = \frac{V_1}{R_1} + (\frac{1}{R_2} + C_1 s)V_2$$
 (B.3)

and Eqn (B.1) is rearranged as:

$$\frac{1}{R_2}V_k = (\frac{1}{R_2} + C_2s)V_2 \tag{B.4}$$

The voltage V_b can now be eliminated and solved for the ratio $\frac{V_b}{V_b} = H_1$. After some algebraic simplification, the resulting transfer function is given as.

$$H_1(s) = \frac{V_2}{V_1} = \frac{\frac{1}{B_1B_1C_1C_2}}{s^2 + (\frac{1}{B_1C_1} + \frac{1}{B_2C_1})s + \frac{1}{B_1B_2C_1C_2}}$$
 (B.5)

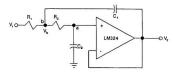


Figure B.1: Filter circuit

or

$$H_1(s) = \frac{V_2}{V_1} = \frac{1}{R_1 R_2 C_1 C_2 s^2 + C_2 (R_1 + R_2) s + 1}$$
(B.6)

The objective here is to find the value of four circuit elements R_1 , R_2 , C_1 , and C_2 . One way to do this is to use an iterative computer program to find the best solution. Fortunately, the capacitor values of the sixth order chebyshev active filter are already given [39]. The values are:

$$\begin{array}{lll} C_{1uncated} = 2.5530 & C_{2uncated} = 1.7760 \\ C_{3uncated} = 3.4870 & C_{4uncated} = 0.4917 \\ C_{5uncated} = 9.5310 & C_{6uncated} = 0.1110 \end{array}$$

The values of the two resistors are chosen as $R_1=R_2=1$ $k\Omega=R.$ Then the scale factor can be calculated as:

Scale factor =
$$\frac{1}{2\pi f_c R} = \frac{1}{2\pi (400)(1000)} = 3.9787 * 10^{-7}$$
 (B.7)

This yields capacitors of value:

$$\begin{array}{lll} C_1 = 1.0158 \mu F & C_2 = 0.70665 \mu F \\ C_3 = 1.3847 \mu F & C_4 = 0.19564 \mu F \\ C_5 = 3.7923 \mu F & C_6 = 0.04417 \mu F \end{array}$$

It is difficult to find the exact capacitors to suit the values found above. As a result, when doing the actual hardware implementation, the values are chosen either by selecting the closest capacitors or by forming a capacitor network. The circuit diagram of the sixth-order chebyshev anti-aliasing filter can be found in Fig 4.6. The transfer function of this filter is:

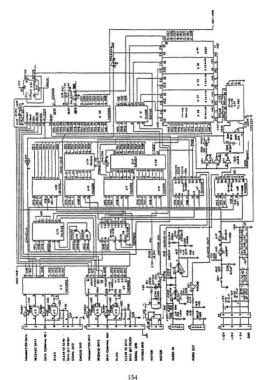
$$H(s) = \frac{1}{(7.1782 * 10^{-7}s^{2} + 1.4133 * 10^{-3}s + 1)} * \frac{1}{(2.7144 * 10^{-7}s^{2} + 3.9128 * 10^{-4}s + 1)} * \frac{1}{(1.6749 * 10^{-7}s^{2} + 3.9328 * 10^{-4}s + 1)} * \frac{1}{(1.6749 * 10^{-7}s^{2} + 8.8331 * 10^{-5}s + 1)} H(s) = (3.2634 * 10^{-20}s^{6} + 1.2850 * 10^{-16}s^{5} + 5.1185 * 10^{-13}s^{4} + 1.1020 * 10^{-9}s^{3} + 1.8691 * 10^{-6}s^{2} + 1.8929 * 10^{-3}s + 1)^{-1} \text{ (B.8)}$$

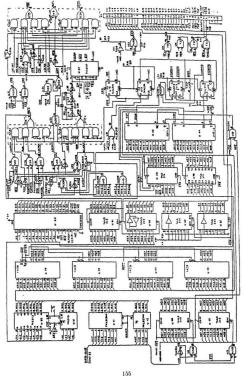
From the above transfer function of Eqn (B.8), the six complex roots of this filter are found to be:

Since all roots are on the left hand side of the complex plane, the filter is stable.

Appendix C

Evaluation Module (EVM) Circuit Diagram [40]





Appendix D

Detailed Description of Algorithms Used in this Thesis

Five algorithms are used in the software part of the microprocessor relay. These algorithms are Discrete Fourier Transform, Walsh Functions, Rectangular Transform, Finite Impulse Response Filtering and Least Square Method. A brief description of these algorithms is in the next few sections.

D.1 Discrete Fourier Transform (DFT) Algorithm

It is known that any continuous waveform f(t), having a finite energy in the interval (0,T) can be represented in the interval as a Fourier Series:

$$f(t) = \frac{a_0}{2} + \sum_{k=1}^{\infty} (C_k \cos(k\omega t) + S_k \sin(k\omega t))$$
 (D.1)

with coefficients:

$$\begin{array}{ll} \frac{a_0}{2} &=& \frac{1}{T} \int_0^T f(t)dt \\ S_k &=& \frac{2}{T} \int_0^T f(t)\sin(k\omega t)dt \\ C_k &=& \frac{2}{T} \int_0^T f(t)\cos(k\omega t)dt \end{array} \tag{D.2}$$

where a_0 is the dc component (average value) and S_k , C_k are the sine and cosine components respectively of the Fourier coefficients. If the waveform is sampled at time t_J , space Δt apart, so that there are $N = \frac{T_d}{\Delta t}$ samples, then for samples 1 to N, the coefficients S_k and C_k in Eqn (D.2) can be rewritten as:

$$S_k = \frac{2}{N} \sum_{j=1}^{N} X(t_j) \sin(\frac{2\pi k j}{N})$$

 $C_k = \frac{2}{N} \sum_{i=1}^{N} X(t_i) \cos(\frac{2\pi k j}{N})$ (D.3)

where $I(t_j)$ are the discrete sampled current signals and j = 1, 2, ..., N.

Hence, for a 16 samples per data window, 16 Fourier coefficients will have an array of 16 x 1. Both sine and cosine terms will have an array of 16 x 16. The system matrices are shown in Eqn (D.4) and Eqn (D.5).

The differential current is analyzed in terms of its Fourier series and the am-

plitude of each harmonic can be found from the system matrix as follows:

$$F_k^2 = S_k^2 + C_k^2$$
 (D.6)

where F_k = Fourier coefficients and k = 1, 2, N

For power transformers protection, F_1 , F_2 and F_3 represent the Fourier coefficients of fundamental, second harmonic and fifth harmonic components respectively of current waveform. F_2 is higher than F_1 for inrush current and F_2 is also higher than F_1 by a certain percentage in the over-excitation case. For a three phase transformer the combined harmonic components of the differential current are:

$$F_{k_{ann,burst}}^2 = S_{k_a}^2 + C_{k_a}^2 + S_{k_b}^2 + C_{k_b}^2 + S_{k_c}^2 + C_{k_c}^2$$
 (D.7)

where k = 1, 2 and 5.

D.2 Walsh Functions Algorithm (WFA)

The Walsh functions were defined in 1923 by J. L. Walsh [41]. These functions form a complete orthogonal set and are denoted by wal(k, t):

$$wal(k, t) = \prod_{j=0}^{m} sgn(\cos(2^{j}k_{j}\pi t))$$
 (D.8)

where k_i is the digit 0 or 1 of the binary numeral of k.

Walsh functions appear to be a squared up version of sine and cosine functions. They take only values +1 and -1 and change sign only when t is a power of $\frac{1}{2}$. The first sixteen Walsh Functions are shown in Fig D.1. In terms of these functions, the Walsh expansion of x(t) with finite energy and a finite number of discontinuities in the interval (0,T) can be defined as:

$$x(t) = \sum_{k=0}^{\infty} W_k wal(k, \frac{t}{T})$$
 (D.9)

```
wal(2,t) + + + + - - - - - - + + + +
wal(3,t) + + + + - - - - + + + + - - - -
wal(4,t) ++---++
wal(5.t) + + - - - + + - - + + + + - -
wal(6,t) ++--++---++
wal(7.t) + + - - + + - - + + - - + + - -
wal(8,t) + --++--++--+
wal(9.t) + - - + + - - + - + + - - + + -
wal(10,t) + - - + - + + - - + + - + - +
wal(11,t) + - - + - + + - + - - + - + + -
wal(12,t) + - + - - + - + + - + - + - + - +
wal(13,t) + - + - - + - + - + - + - + - + -
wal(14.t) + - + - + - + - + - + - + - + - +
wal(15,t) + - + - + - + - + - + - + - + -
```

Figure D.1: First 16 Walsh Functions

where

$$W_k = \frac{1}{T} \int_0^T x(t)wal(k, \frac{t}{T})dt$$
 (D.10)

The Walsh coefficients of Eqn (D.10) form a vector in Hilbert space like the Fourier coefficients F_k . This relationship can be expressed as:

$$W = AF (D.11)$$

Since A represents an orthogonal transformation, its inverse A^{-1} is the same as its transpose A^{1} and so:

$$F = A^t W (D.12)$$

Then the matrix A has been found in part as [42]:

1	0	0	0	0	0	0	0	0	0	0]
0	.900	0	0	0	.300	0	0	0	.180	0	
0	0	.900	0	0	0	300	0	0	0	.180	
0	0	0	.900	0	0	0	0	0	0	0	***
0	0	0	0	.900	0	0	0	0	0	0	***
0	373	0	0	0	.724	0	0	0	.435	0	
0	0	.373	0	0	0	.724	0	0	0	435	
0	0	0	0	0	0	0	.900	0	0	0	
0	0	0	0	0	0	0	0	.900	0	0	
0	074	0	0	0	484	0	0	0	.650	0	
0	0	074	0	0	0	.484	0	0	0	.650	
0	0	0	373	0	0	0	0	0	0	0	
0	0	0	0	.373	0	0	0	0	0	0	
	0.00	50			0.50			18		*	222
4	0.40	(*)		0.00	100		*	2	2.		
8	100	32.0		0.00	285			151.7		51	200

Since $F = A^tW$, the sine and cosine Fourier coefficients in Eqn (D.3) can easily be determined as:

$$S_1 = 0.990W_1 - 0.373W_2 - 0.074W_2$$

 $C_1 = 0.990W_3 + 0.373W_2 - 0.074W_10$
 $S_2 = 0.990W_3 - 0.373W_{11}$
 $C_2 = 0.990W_4 + 0.373W_{12}$
 $S_8 = 0.189W_4 + 0.435W_4 + 0.650W_9$
(D.14)

 $C_5 = 0.180W_2 - 0.435W_6 + 0.650W_{10}$ Finally the combined fundamental, second and fifth harmonic contents of the differential current can be determined using Eqn (D.7).

D.3 Rectangular Transform Algorithm (RTA)

If the sine and cosine terms of Eqn (D.3) are replaced with the equivalent rectangular functions:

$$\sin \gamma t(x) = sgn(\sin x)$$

 $\cos \gamma t(x) = sgn(\cos x)$ (D.15)

where

$$sgn(y) = \frac{y}{|y|}, \text{ for } y \neq 0$$

= 0, for $y = 0$ (D.16)

Then the corresponding rectangular transform coefficients can be denoted as \hat{S}_k and \hat{C}_k which are defined as:

$$\hat{S}_k = \sum_{j=0}^{N-1} I(t_j) sgn(\sin(\frac{2\pi kj}{N}))$$

 $\hat{C}_k = \sum_{i=0}^{N-1} I(t_j) sgn(\cos(\frac{2\pi kj}{N}))$
(D.17)

Again for 16 samples per cycle, 16 Rectangular coefficients will have an array of 16 x 1. Both the sine and cosine terms will have an array of 16 x 16. The system matrices are shown in Eqn (D.18) and Eqn (D.19).

$$\begin{bmatrix} \hat{C}_1 \\ \hat{C}_2 \\ \vdots \\ \hat{C}_{15} \\ \hat{C}_{16} \end{bmatrix} = \begin{bmatrix} sgn[\cos(\frac{2s-s+1}{16})] & ... & sgn[\cos(\frac{2s-s+1+16}{16})] \\ sgn[\cos(\frac{2s-s+1}{16})] & ... & sgn[\cos(\frac{2s-s+1+16}{16})] \\ \vdots \\ \vdots \\ \vdots \\ sgn[\cos(\frac{2s-s+1}{16})] & ... & sgn[\cos(\frac{2s-s+1+16}{16})] \\ sgn[\cos(\frac{2s-s+1}{16})] & ... & sgn[\cos(\frac{2s-s+1+16}{16})] \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{15} \\ I_{16} \end{bmatrix}$$

$$\begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{15} \\ I_{16} \end{bmatrix}$$

$$\vdots \\ I_{16} \end{bmatrix}$$

$$\begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{16} \end{bmatrix}$$

$$\vdots \\ I_{16} \end{bmatrix}$$

$$\begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{16} \end{bmatrix}$$

$$\vdots \\ I_{16} \end{bmatrix}$$

$$\begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{16} \end{bmatrix}$$

$$\vdots \\ I_{16} \end{bmatrix}$$

$$\begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{16} \end{bmatrix}$$

$$\begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{16} \end{bmatrix}$$

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$$\begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{16} \end{bmatrix}$$

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$$\begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{16} \end{bmatrix}$$

$$\begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{16} \end{bmatrix}$$

$$\begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{16} \end{bmatrix}$$

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$$\begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{16} \end{bmatrix}$$

$$\begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{16} \end{bmatrix}$$

$$\begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{16} \end{bmatrix}$$

$$\begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{16} \end{bmatrix}$$

$$\begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{16} \end{bmatrix}$$

$$\begin{bmatrix} \hat{S}_1 \\ \hat{S}_2 \\ \vdots \\ \hat{S}_{16} \end{bmatrix} = \begin{bmatrix} sgn[\sin(\frac{2\pi\pi+1}{2})] & sgn[\sin(\frac{2\pi\pi+1+16}{2})] \\ sgn[\sin(\frac{2\pi\pi+1}{2})] & sgn[\sin(\frac{2\pi\pi+1+16}{2})] \\ \vdots & \vdots \\ sgn[\sin(\frac{2\pi\pi+1}{2})] & sgn[\sin(\frac{2\pi\pi+1+16}{2})] \\ sgn[\sin(\frac{2\pi\pi+1+16}{2})] & sgn[\sin(\frac{2\pi\pi+1+16}{2})] \\ sgn[\sin(\frac{2\pi\pi+1+16}{2})] & sgn[\sin(\frac{2\pi\pi+1+16}{2})] \\ t_{16} \end{bmatrix} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{16} \end{bmatrix}$$

$$(D.19)$$

The Rectangular coefficients are related to the Fourier sine and cosine coefficients as:

$$[S_k] = [A^{-1}][\hat{S}_k]$$

 $[C_k] = [B^{-1}][\hat{C}_k]$
(D.20)

where $[S_k]$, $[C_k]$ are the vector of Fourier sine, cosine coefficient and $[\hat{S}_k]$, $[\hat{C}_k]$ are the vector of corresponding rectangular coefficients.

The matrices $[A^{-1}]$ and $[B^{-1}]$ are given by:

The minus sign in the above matrix is for the $[A^{-1}]$ matrix and the plus sign is for the $[B^{-1}]$ matrix. Since an analog low-pass filter is used in the hardware, frequencies higher than fifth harmonic are filtered out. As a result the Fourier coefficients can be obtained using the above matrix relationship of Eqn (D.21) with the $\frac{1}{4}$, $\frac{1}{4}$ terms only as follows:

$$S_1 = \hat{S}_1 - \frac{1}{3}\hat{S}_3 - \frac{1}{3}\hat{S}_5$$

 $C_1 = \hat{C}_1 + \frac{1}{3}\hat{C}_3 - \frac{1}{3}\hat{C}_5$
 $S_2 = \hat{S}_2$
 $C_2 = \hat{C}_1$
 $S_5 = \hat{S}_5$
 $S_5 = \hat{S}_5$
 $S_6 = \hat{S}_5$
 $S_7 = \hat{S}_7$
(D.22)

The fundamental, second and fifth harmonic components of the differential current can now be determined by Eqn (D.7).

D.4 Finite Impulse Response (FIR) Filtering Algorithm

FIR filters have values of either plus or minus one at any time instant. Four filters are used for the fundamental and second harmonic components with this algorithm and their impulse response $S_1(x)$, $C_1(x)$, $S_2(x)$ and $C_2(x)$ are:

$$\begin{array}{llll} S_1(x) &=& 1 & 0 \le x \le 1/2 \\ 1/2 < x \le 1 & 1/2 < x \le 1 \\ C_1(x) &=& 1 & 0 \le x \le 1/4, \ 3/4 < x \le 1 \\ &=& -1 & 1/4 < x \le 3/4 \\ S_2(x) &=& 1 & 0 \le x \le 1/4, \ 1/2 < x \le 3/4 \\ &=& -1 & 1/4 < x \le 3/8, \ 3/4 < x \le 1 \\ C_2(x) &=& 1 & 0 \le x \le 1/8, \ 3/8 < x \le 5/8, \ 7/8 < x \le 1/8 \end{array} \tag{D.23}$$

Since this algorithm is to be implemented in a microprocessor, the filter outputs must be found from the samples of the time continuous input. Let the current input be sampled at N times per cycle at time $t = k\Delta t$ where $\Delta t = \frac{3r}{N_{min}}$. In this case, Nis equal to 16. If the time discrete sample is denoted by I_{tr} , the impulse responses are found to be:

$$\begin{array}{ll} S_1 &=& \sum_{i=1}^{N/2} [l_i - l_{i+\frac{N}{2}}] \\ C_1 &=& \sum_{i=1}^{l-2} [l_i - (l_{i+\frac{N}{4}} + l_{i+\frac{N}{2}}) + l_{i+\frac{N}{2}}] \\ S_2 &=& \sum_{i=1}^{N/4} [l_i - l_{i+\frac{N}{4}} + l_{i+\frac{N}{2}} - l_{i+\frac{N}{2}}] \\ C_2 &=& \sum_{i=1}^{N/2} [l_i - (l_{i+\frac{N}{4}} + l_{i+\frac{N}{2}} + l_{i+\frac{N}{2}} - (l_{i+\frac{N}{4}} + l_{i+\frac{N}{2}}) + l_{i+\frac{N}{2}}] \end{array}$$

$$(D.24)$$

This FIR filtering algorithm cannot accommodate fifth harmonic component for the over-excitation case. So the Rectangular Transform which is most similar to FIR was chosen for fifth harmonic implementation. Again the combined fundamental, second and fifth harmonic contents of the differential current can be determined by Eqn (D.7).

D.5 Least Square Algorithm (LSA)

For this algorithm it is assumed that the inrush current contains a decay dc current and no more than five harmonics, then in a certain time interval, the inrush current can be approximated by:

$$i(t) = p_0 e^{-\lambda t} + \sum_{k=1}^{5} p_k \sin(k\omega_0 t + \theta_k)$$
 (D.25)

where i(t) = instantaneous differential current sampled at time t.

 $p_0 = dc$ component.

 λ = inverse decay time constant of the dc component.

 $p_k = \text{peak component of the k-th harmonic differential current.}$

 ω_0 = fundamental frequency.

 θ_k = phase angle of the k-th harmonic component.

If the time interval is small compared to the time constant $\frac{1}{\lambda}$, the dc component of the above equation can be approximated as:

$$p_0e^{-\lambda t} \approx p_0 - P_0\lambda t$$
 (D.26)

and then by Taylor expansion of the decaying dc current of two terms, Eqn (D.25) can be simplified to the form:

$$i(t) = p_0 - p_0\lambda t + \sum_{k=1}^{5} p_k \cos \theta_k \sin(k\omega_0 t) + \sum_{k=1}^{5} p_k \sin \theta_k \cos(k\omega_0 t)$$
 (D.27)

If 16 samples are considered at time t_1 to t_{16} , then the sampling current process results in the following set of equations:

$$\begin{bmatrix} i(t_1) \\ i(t_2) \\ \vdots \\ i(t_{16}) \end{bmatrix} = \begin{bmatrix} 1 & t_1 & \sin \omega_0 t_1 & \cos \omega_0 t_1 & \dots & \sin 5\omega_0 t_1 & \cos 5\omega_0 t_1 \\ 1 & t_2 & \sin \omega_0 t_2 & \cos \omega_0 t_2 & \dots & \sin 5\omega_0 t_2 & \cos 5\omega_0 t_2 \\ \vdots & \vdots & \ddots & \ddots & \ddots & \ddots & \vdots \\ 1 & t_{16} & \sin \omega_0 t_{16} & \cos \omega_0 t_{16} & \dots & \sin 5\omega_0 t_{16} & \cos 5\omega_0 t_{16} \end{bmatrix} \begin{bmatrix} p_0 \\ -p_0 \lambda \\ p_1 \cos \theta_1 \\ p_2 \sin \theta_1 \\ p_5 \sin \theta_5 \end{bmatrix}$$

$$(D.28)$$

If the above equations are written in matrix form as:

$$I = AX (D.29)$$

then the least square solution becomes:

$$\mathbf{X} = [(\mathbf{A}^{T}\mathbf{A})^{-1}\mathbf{A}^{T}]\mathbf{I} = \mathbf{B}\mathbf{I}$$
 (D.30)

From Eqn (D.30) it can be shown that:

$$\mathbf{B} = (\mathbf{A}^{\mathrm{T}}\mathbf{A})^{-1}\mathbf{A}^{\mathrm{T}} \tag{D.31}$$

and since matrix A contains known elements, matrix B can be calculated using MATLAB as follows:

$$\mathbf{B} = \begin{bmatrix} 0.926980 & -0.516782 & 0.671782 & -0.8011981 \\ -116.654602 & 77.981552 & -7.7981512 & 116.654602 \\ -0.579477 & 0.456245 & -0.496798 & 0.531642 \\ -0.09735 & 0.196723 & 0.007151 & 0.230750 \\ -0.278275 & 0.2354513 & -0.321125 & 0.188886 \\ 0.099735 & 0.169626 & -0.081238 & 0.203654 \\ -0.172907 & 0.237066 & -0.299969 & 0.657022 \\ 0.099735 & 0.129073 & -0.169626 & 0.163101 \\ -0.115265 & 0.266238 & -0.081238 & -0.09735 \\ -0.077018 & 0.169766 & 0.034107 & -0.083467 \\ -0.077018 & 0.169766 & 0.034107 & -0.083467 \\ 0.009735 & 0.033402 & -0.169626 & 0.067430 \end{bmatrix}$$

A 12X16 Matrix

Matrix B can be used to calculate the vector of unknown X from the sampled differential current. The Fourier sine and cosine components of the fundamental, second and fifth harmonic contents can by found by:

$$\begin{array}{lll} C_1 &=& p_1 \cos \theta_1(t_N) &=& \sum_{n=1}^{16} B(3,n)i(t_n) \\ S_1 &=& p_1 \sin \theta_1(t_N) &=& \sum_{n=1}^{16} B(4,n)pi(t_n) \\ C_2 &=& p_2 \cos \theta_2(t_N) &=& \sum_{n=1}^{16} B(5,n)pi(t_n) \\ S_2 &=& p_2 \sin \theta_1(t_N) &=& \sum_{n=1}^{16} B(6,n)pi(t_n) \\ C_1 &=& p_1 \cos \theta_2(t_N) &=& \sum_{n=1}^{16} B(6,n)pi(t_n) \\ S_1 &=& p_1 \sin \theta_2(t_N) &=& \sum_{n=1}^{16} B(12,n)pi(t_n) \end{array} \tag{1D.33}$$

Finally Eqn (D.7) is used to calculate the combined fundamental, second and fifth harmonic contents of the differential.

Appendix E

Some Real Time Testing Diagrams from a Digital Oscilloscope

This appendix gives some real time testing results that were recorded via a digital oscilloscope. Due to the limitation of the oscilloscope with only two channels, only one phase of the current signal with the trip signal can be shown at one time. The upper waveform represents the phase current and the lower waveform represents the trip signal. The digital relay is tripped when the trip signal waveform goes low. To make sure that all phases were covered, the phase current recorded for each test with each algorithm was chosen at random.

It can be seen that all algorithms perform accurately during the inrush (Figs. E.1 and E.2) tests. All faults are cleared within a cycle for the phase-to-phase fault (Figs. E.3 to E.6) tests. No error have occurred for the tests on inrush followed by an internal fault (Figs. E.7 and E.8) or switching on the transformer with an internal fault (Figs. E.9 and E.10), with the use of any algorithms. However, the amount of time to clear a switching on with an internal fault case depends on the amount of inrush current presented at switching on time. All algorithms have performed correctly for the between taps fault (Figs. E.11 and E.12) tests or the ground fault (Figs. E.13 and E.14) tests. Finally the digital relay never trips when

running with any algorithms during the 40% over-excitation (Figs. E.15 and E.16) tests or when applying an external fault (Fig. E.17).

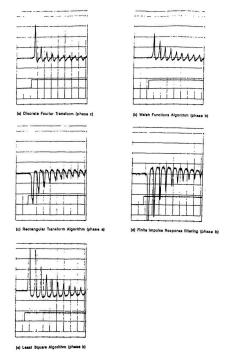


Figure E.1: No load inrush condition

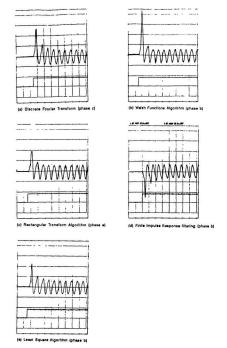


Figure E.2: Inrush condition with load

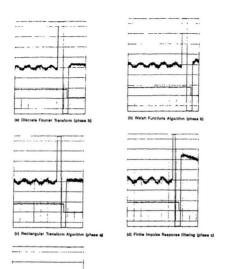


Figure E.3: No load primary phase - to - phase fault

(e) Least Square Algorithm (phase c)

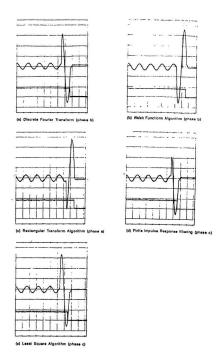
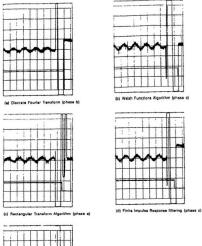
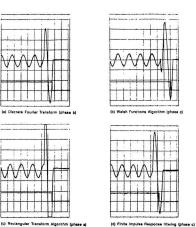


Figure E.4: Primary phase - to - phase fault with load



(a) Least Square Algorithm (phase to

Figure E.5: No load secondary phase - to - phase fauit



(c) Rectangular Transform Algorithm (phase a)

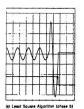


Figure E.6: Secondary phase - to - phase fault with load

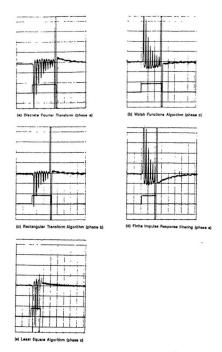


Figure E.7: Inrush followed by an internal fault without load

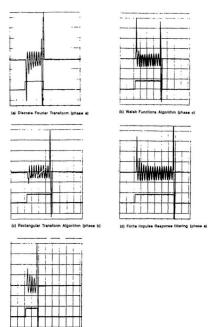


Figure E.8: Inrush followed by an internal fault with load

(e) Least Square Algorithm (phase c)

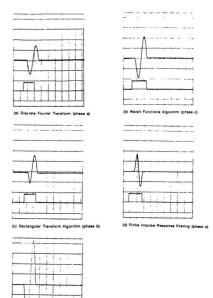
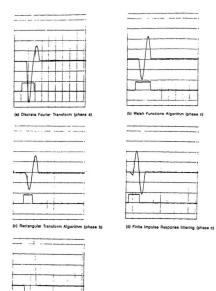


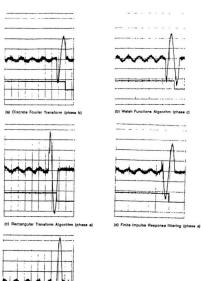
Figure E.9: Switching on with an internal fault without load

(e) Least Square Algorithm (phase a)



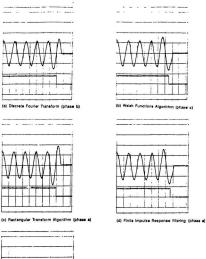
(e) Least Square Algorithm (phase a)

Figure E.10: Switching on with an internal fault with load



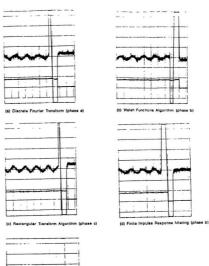
(e) Least Square Algorithm (phase s)

Figure E.11: No load between taps fault



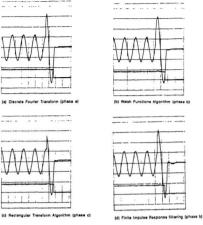
(o) Lessi Square Algorithm (phase s)

Figure E.12: Between taps fault with load



(I) Less Squar Algorith (phase d

Figure E.13: No load primary ground fault







(e) Least Square Algorithm (phase c)

Figure E.14: Primary ground fault with load

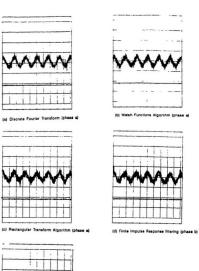




Figure E.15: No load over-excitation condition

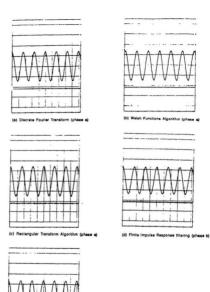


Figure E.16: Over-excitation condition with load

(e) Least Square Algorithm (phase c)

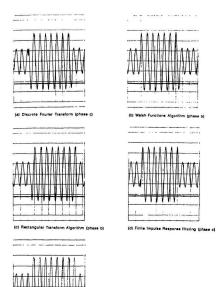


Figure E.17: External fault with load

(e) Least Square Algorithm (phase a)







