SINGLE PHASE DELTA MODULATED INVERTER
FOR
UNINTERRUPTIBLE POWER SUPPLY APPLICATIONS

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FOR
UNINTERRUPTIBLE POWER SUPPLY APPLICATIONS

by

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Abstract

This thesis examines in detail the suitability of Rectangular Wave Delta Modulation (RWDM) for Uninterruptible Power Supply (UPS) applications.

Various types of Delta Modulation schemes commonly used in communication systems are presented with a view to selecting the appropriate modulation scheme for UPS applications. It is shown that RWDM posseses many attractive features which make it suitable for UPS applications: simple control circuitry, ease of control of the frequency spectrum of the modulator output through the variation of modulator parameters.

An analytical model of the rectangular wave delta modulator is developed to qualitatively describe the effect of various modulator parameters on the modulator performance. A numerical approach based on Discrete Fourier Transform and harmonic analysis technique is proposed to quantitatively investigate the performance of the modulator.

The effect of various modulator parameters on the single phase delta modulated UPS inverter with two commonly used load filters, namely L-C and tank circuit filter, is studied for various types of load. It is shown that RWDM provides significant improved performance in single phase delta modulated UPS inverter. It offers improved voltage utilization ratio, suppressed amplitudes of low order harmonics at the inverter output and hence a small filter size.

Analytical expressions and computer simulation of voltages and currents in the load filter are provided. The predicted results are substantiated by corresponding experimental results.

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Chapter 1

INTRODUCTION

The increased number of critical loads, such as medical instrumentation, process controllers, monitoring circuits and data processing systems (computers, communication systems, protection systems, etc..), requires continuity of energy power supply, high quality load voltage, and high rate of availability (high reliability). The above requirements dictate that a source of supply other than from the local electric utility, which is disturbance free is mandatory. This demand has been met recently by the Uninterruptible Power Supply (UPS).

The UPS system has to provide electric power within precise specifications. The high rate of availability implies the use of very reliable elements with very little or no maintenance. The total loss of power of the utility and the UPS system should be kept within specified limits, usually one complete cycle based on the utility frequency. Until recently, these requirements were met by the rotary type UPS system. However, the solid state UPS system has gained more prominence.

Modern static UPS systems employ various pulse width modulation schemes to improve the quality of the load voltage (i.e., to provide load voltage with minimum distortion). Several harmonic elimination techniques have been used to reduce or eliminate the lower order harmonics (associated with the modulation scheme). This has led directly to a reduction in the size, weight and cost of the UPS system. This thesis investigates the use of the delta modulation technique for UPS applications.

In this chapter, a review of different types of UPS systems and various modulation techniques often used to control the switching inverter is presented. A brief outline of various types of delta modulators, namely linear, sigma, adaptive and asynchronous delta modulator is presented along with their main characteristics with a view to selecting a suitable delta modulation scheme for UPS applications. Finally, the thesis objectives and outline are presented.

1.1 UPS System Specifications

The objective of the UPS system is to ensure continuous flow of a specified quality of ac power to critical loads when the main ac power supply malfunctions. There are two basic methods of producing this ac power; the rotary generator type and the solid state converter type. The rotary generator type is a complete mini-generating station which produces a 'precise' power (uninterruptible) to the load [1]. However, The rotary generator type can be only economically considered for large power requirements. The system suffers from high noise levels because of its mechanically rotating parts, and the need for large installation space. The solid state converter type, on the other hand, is compact, generates less acoustic noise and hence ideally suited for medical, communication and computer environments. This work investigates the suitability of delta modulation technique for solid state uninterruptible power supply. Thus, the study of the performance of the rotary generator type is not discussed in this work.

The performance characteristics that distinguish solid state UPS systems from other static ac power supplies such as variable speed ac drives, are the 'clean' and well regulated ac output power. To achieve these performance characteristics, the UPS system should meet the following specifications [1,2,3]:

1. The amplitude of the load voltage should be kept constant irrespective of the variations in the dc supply voltage level (within $\pm 10\%$) or the load changes (magnitude or power factor). Fluctuation of the critical load voltage could result in permanent damage to the load equipment.

2. The frequency of the load voltage should be kept constant. This condition is essential for critical loads with an ac-dc adaptor. The load adaptor is usually provided with a dc filter whose components are optimally chosen to minimize its size for nominal supply frequency and amplitude. When the supply frequency deviates from its nominal value, the load filter components become ineffective in producing a well regulated and 'clean' dc output voltage. This could lead to a system failure.

3. High quality of the load voltage, i.e., the total harmonic distortion of the load voltage (THD) should be less than 5 %. The concept of high quality of the load voltage expresses the relative harmonic content in the load voltage and a stable output voltage independent of the pollution on the utility network.

4. The UPS system should have fast transient response. Systems with sluggish response to either load changes or supply variations could result in

deteriorating the load performance or malfunctioning of the critical load.

5. The system should have high availability and reliability. Typically, the maximum permissible duration of total loss of load voltage for computer applications is 16 ms, after which loss of memory of data takes place. The system batteries should have sufficient ampere-hour rating to maintain the UPS output for a specified time (usually 30 min.) to allow for data saving and proper shut down procedures of the computer system.

6. The inverter output filter should provide the least possible attenuation for the fundamental component of the inverter output voltage.

The above specifications have been met in the solid state UPS system through improvements in system topology and modulation techniques.

1.2 UPS System Configurations

Since its introduction in 1965, the solid state UPS system has undergone several topological evolution. Presently, solid state uninterruptible power supplies can be categorized into five main configurations, namely:

- The voltage-fed UPS configuration.
- The current-fed UPS configuration.
- The high frequency link UPS configuration.
- The triport UPS configuration.
- The hybrid UPS system

1.2.1 The Voltage-Fed UPS Configuration [4,5,6]

Figure 1.1a shows the block diagram of the voltage-fed (or the conventional) UPS system. It consists of a controlled bridge rectifier, a low pass input filter, a battery bank, a switching inverter, an isolation transformer, a low pass output filter and a static bypass switch.

The function of the controlled bridge rectifier is to convert the ac supply voltage into dc voltage at different levels. The level of the dc voltage at the output of the controlled bridge rectifier is controlled using conventional control schemes such as phase angle control [4]. The output of the bridge rectifier is smoothed out using the input filter. The dc voltage at the output of the input filter charges a bank of batteries as well as feeds the switching inverter. The battery bank is kept floating and is used when the ac line malfunctions. During ac line power failure, the battery bank feeds the load through the switching inverter. When the utility line recovers, the controlled bridge rectifier recharges the batteries and supplies the load through the switching inverter. The switching inverter converts the dc voltage into ac using a conventional pulse width modulation scheme (PWM).

Although the pulse width modulated inverter output waveform contains switching harmonics, its fundamental frequency is the same as the supply frequency. The switching harmonics are filtered out by the load filter to produce a load voltage whose harmonic content is within the THD specification.

In the event of a UPS system failure, the load is fed directly from the utility line through the static bypass switch. Supplying the load directly from the utility line is meant only for emergency cases and is not recommended for long duration of load operation.

From the principle of operation of the conventional UPS system, it can be seen that the UPS system interfaces the critical load with the utility power supply. This feature has the advantage of protecting the load from any events (such as voltage and frequency fluctuation, brownouts, transients) that take place in the utility network. In other words, in normal operation, the load is disturbance free [6].

One of the drawbacks of the voltage-fed UPS system is that, the system output voltage is prone to have a dc component due to the ripple on the dc link voltage [7]. Significant level of the dc component at the inverter output could result in saturating the load transformer. This drawback can be overcome by using a relatively large filter at the inverter input.

1.2.2 The Current-Fed UPS Configuration [7]

Figure 1.1b shows the current-fed UPS system. It consists of a controlled bridge rectifier, a low pass input filter, a battery bank, a dc chopper, a smoothing reactor, a current source inverter, a load filter, an isolation transformer and static bypass switch.

The main feature of the controlled bridge rectifier and the input filter is the same as that for the voltage-fed UPS system. The current source reactor (CSR) converts the voltage source into a current source, while the dc chopper allows control of the current level to ensure constant output voltage irrespective of the load or supply changes.

The function of the current source inverter is to convert the input dc current into an ac current. Since the load filter is fed from a train of current pulses,

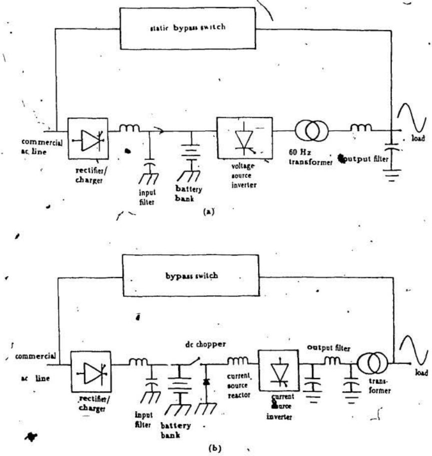


Figure 1.1: UPS system configurations: (a) Voltage-Fed UPS system (b) Current-Fed UPS system

its input component has to be capacitive. The filter input capacitor reduces the voltage spikes associated with the current source inverter switching and hence the stresses on the switching devices [7].

Since the current source reactor converts the dc link voltage into a current source, the current-fed UPS system is immune to dc components in its output voltage. However, it requires an extra power conversion stage (the CSR and the dc chopper), to create a regulated current source. The system efficiency is therefore reduced and its response is expected to be slower than its voltage-fed UPS system counterpart.

1.2.3 The High Frequency Link UPS Configuration [8]

Figure 1.2a shows the block diagram of the high frequency link UPS system. It consists of a controlled bridge rectifier, a low pass input filter, a dc battery bank, a high frequency inverter, an isolation transformer, a cycloconverter, a low pass output filter and a static bypass switch.

The functions of the bridge rectifier, the low pass input filter and the battery bank are the same as those described for the previous UPS systems.

The output of the high frequency inverter is a pulse-width-modulated ac voltage switched at a very high frequency. A sinusoidal output voltage of the UPS system whose frequency is the same as the supply frequency is synthesized from the inverter output voltage using a cycloconverter. The undesired harmonics at the cycloconverter output are suppressed by the low pass filter at the load terminals.

The high frequency UPS scheme offers several improved performance features over the voltage-fed and the current-fed UPS systems. Since the inverter is switched at a very high frequency, the size of the isolation transformer and the output filter are significantly reduced. Moreover, The level of audible noise produced by the isolation transformer is also reduced especially if the inverter is switched at frequencies higher than 20 KHz. However, these desirable features are achieved at the expense of increased number of switching devices, complex control circuitry and hence, a reduction in the system reliability. A major problem with the system is the commutation of the cycloconverter which is load dependent and is not effective under all load conditions[8].

1.2.4 The Triport UPS Configuration [2,9]

Figure 1.2b shows the block diagram of the triport system. In this scheme, the load is constantly supplied by the commercial ac line through a voltage regulator. The voltage regulator is normally a transformer with two primary windings: one winding is fed by the ac line while the other is fed by the inverter. The output transformer regulates the ac line voltage while the inverter is in a hot standby condition. When the ac line fails, the inverter provides the critical load with the required power. In some versions, the inverter is in OFF standby condition. This design is justified since the energy stored in the transformer core will supply the load until the inverter is brought on-line [2]

As opposed to the conventional UPS system, the triport configuration does not buffer the load from the utility network transients. The output transformer is also larger because of the multiple primary windings. Furthermore, an additional voltage regulation at the secondary of the output transformer is required

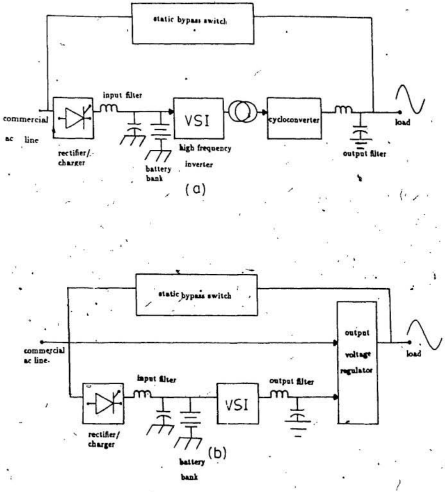


Figure 1.2: UPS system configurations: (a) The High Frequency Link UPS system (b) The Triport UPS system

to maintain a constant supply voltage to the load [9].

1.2.5 The Hybrid UPS Configuration [10]

The hybrid UPS system comprises of both static and rotary type UPS configurations. Figure 1.3 shows the block diagram of the hybrid UPS system. It consists of a synchronous motor-generator set, a static UPS system, and a bypass switch. Under normal operating conditions, the critical load is supplied by the utility supply through the motor- generator set via a static switch. The utility supplies the major part of the load (normally 95 %). The conventional UPS system is connected in parallel with the static switch and feeds the critical load through the motor-generator set with the rest of the load power (5 %). Such power flow arrangement is justified because it ensures that the static inverter path remains operational and ready to deliver full power instantaneously when needed.

If the utility supply deviates from its specified limits for a certain duration of time (normally 20 ms), the static switch of the motor-generator set is switched OFF and full load power is supplied by the dc batteries through the static inverter. When the utility supply regains its normal conditions, the power arrangement of the power flow reverts to its normal operation. In the event of failure in the static inverter and motor generator set, the critical load is supplied directly by the utility line through the bypass switch. In some cases, the system bypass switch is chosen to be a non-static switch. This prevents the critical load from being subjected to high voltage transients that can pass through a static switch.

The hybrid configuration offers high reliability and efficiency. However, the system requires complex control circuitry. For example, to adjust the level of

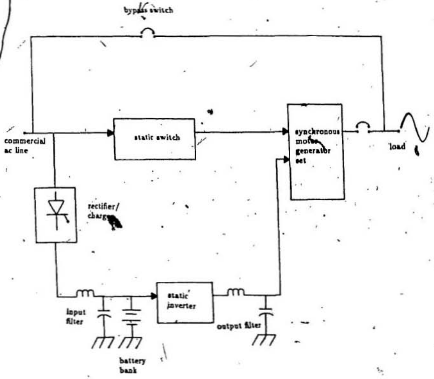


Figure 1.3: The Hybrid UPS system configuration

power flow in the system buses, a special synchronization circuit is required. Moreover, it is very expensive and can only be economically considered for large loads. The system size is large and its noise level is higher than the conventional static UPS system.

1.2.6 Stand-by and On-line UPS Systems

The configurations described above may be further classified as stand-by and on-line UPS systems. In the stand-by system, of which the triport configuration is an example, the load is supplied by the raw ac line and the UPS inverter may be either working in an idle or OFF condition. When the loss of the utility line voltage is detected, the inverter is brought on-line via a transfer switch. The stand-by system is a redundant system, and hence it provides higher reliability and efficiency. However, it requires a finite time for the stand-by equipment to be brought on-line to supply the critical load.

On-line systems, such as the conventional UPS system, the current- fed UPS and the high frequency link UPS, provide the load with 'clean' and well regulated ac power. The load is constantly supplied by the utility through the UPS system. In other words the UPS system interfaces the ac line voltage to the critical load and when the ac input is lost, the battery bank provides the dc voltage which is converted to ac by the inverter. On-line systems have the advantage of protecting the load from utility disturbances in normal operation [6].

1.3 Control Schemes for Uninterruptible Power Supplies

The evolution in UPS system configurations has resulted in improved system efficiency and reliability. However, improvement in the system performance in terms of the system providing constant load voltage and frequency, high quality of load voltage, fast transient response and reduced component size has been achieved through various modulation schemes for the inverter of the UPS system. In this section, a review of various pulse width modulation schemes, often used in controlling the inverter switching devices is presented.

Pulse width modulation (PWM) is a process by which a sinusoidal waveform can be synthesized from a train of positive and negative pulses with their widths varying according to a certain modulation technique. The purpose of using modulation technique for UPS system is to control the amplitude of the load voltage and minimize the low order harmonic contents of the output voltage.

The earliest PWM technique applied to UPS systems is the single PWM scheme [3]. This technique is capable of load voltage variations and minimization of few selected harmonics in the inverter output. However, significant improvement in UPS system performance and quality of load voltage have been achieved through the use of one of the following schemes:

- The sine pulse width modulation.
- The harmonic elimination technique.

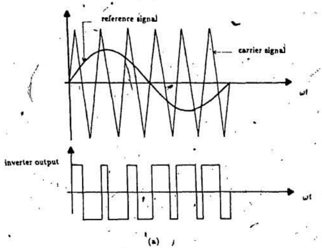
Sinusoidal pulse width modulation (SPWM) is a very popular scheme for both adjustable speed ac drives and UPS systems [3]. The manner of generating the switching points depends on the method of implementation of the modulation technique and may be classified as natural and uniform sampling techniques.

Figure 1.4a shows the general principle of the naturally sampled SPWM where a triangular carrier wave is compared with a reference modulating signal, and the natural points of intersection determine the switching points for the inverter switching devices. The distribution of the undesired harmonics depends on the frequency ratio of the carrier signal and the reference (modulating) signal. The higher the frequency ratio, the greater the 'gap' between the fundamental component and the dominant harmonics, i.e., the dominant harmonics occur at higher frequencies.

The uniform sampling method is based on the sample and hold principle. Figure 1.4b shows the principle of operation of the uniform sampling technique. The sine modulating signal is replaced by an equivalent stepped signal. This technique is popular in microcomputer implementation, since generating a real time reference modulating sine wave is a time consuming process for the microprocessor. The uniform sampling technique has the advantage of producing symmetrical pulses about the trough of the carrier wave. Thus no sub-harmonics exist in the frequency spectrum of the inverter output voltage [11].

The above modulation techniques have been successfully implemented in UPS applications [12,13]. Although, these techniques attenuate the low order harmonics and result in relatively small filter sizes, they suffer from complex control circuitry and moderate utilization of the dc supply voltage level.

In the harmonic elimination technique, the switching instants of the pulses which result in the elimination of selected order of harmonics are determined in



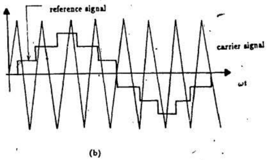


Figure 1.4: Sinusoidal Pulse Width Modulation (SPWM): (a) Natural sampling (b) Uniform sampling

advance. A generalized approach of eliminating a fixed number of harmonics was developed by Patel, et al [14].

To determine the switching instants of the inverter output pulses, elegant numerical techniques are used to solve the non-linear equations which describe these switching instants. Therefore the scheme has the disadvantage of being computation-intensive. As opposed to the natural sampling technique, it requires off-line calculations.

It is therefore proposed to investigate the use of delta modulation (DM) technique as a means of overcoming the disadvantages associated with the sine pulse width modulation scheme and the harmonic elimination technique.

DM technique has been extensively used in digital communication networks [15]. Recently, the DM technique has been used in power electronics applications and it has become an established alternative to sine PWM for producing a sinusoidal output [16,17,18]. Its attractive feature in UPS application is the provision of a modulation process, which combines the modulation technique and the harmonic elimination technique in a simple circuit implementation.

1.4 The Delta Modulation Technique

In many of the information signals, e.g., speech and TV signals, a significant correlation exists between successive samples at the Nyquist rate. Therefore, it is advantageous to encode the signal derivatives rather than the signal itself and reconstruct it again through a simple integrator circuit. Differential pulse code modulation (DPCM) is one of the methods which encodes the information signals into digital format [19].

Delta modulators are simple forms of differential pulse code modulation. It is one of the simplest known methods for converting analog signal into digital format and may be grouped into the following categories

- The linear delta modulator. (LDM)
- The sigma-delta modulator. ($\Sigma - \Delta M$)
- The adaptive delta modulator. (ADM)
- The asynchronous delta modulator. (ASDM)

1.4.1 The Linear Delta Modulator

Figure 1.5a shows the block diagram of the linear delta modulator (LDM). It consists of a comparator, quantizer, sampler in the feed-forward path and an integrator in the feedback path. The input analog signal $v_R(t)$ is compared with the feedback signal $v_c(t)$ to generate the error signal e(t). The output of the quantizer is regularly sampled at the clock frequency f_c, to produce an output waveform which is a binary encoding of the reference signal. This closed arrangement ensures that the integrator output tracks the input signal faithfully [20].

The performance of the basic LDM is strongly coupled with the input signal frequency. When the input signal frequency exceeds the clock frequency, the modulator loses its encoding ability and runs into what is known as slope overload conditions. When the modulator is overloaded, its binary output is no longer an accurate encoding of the reference analog signal. Under such condition, the frequency spectrum of the modulator output waveform will contain low order harmonics with high amplitudes. From UPS application viewpoint, the low order harmonics with high amplitude would require large load filter to suppress the undesired harmonics and produce a 'clean' load voltage.

1.4.2 The Sigma-Delta Modulator

In the Sigma-Delta modulator ($\Sigma - \Delta$ M), shown in Fig. 1.5b, the integrator in the feedback path of Fig. 1.5a, is placed in the feed-forward path after the error point. The modulator output is compared with the input signal to produce the error signal e(t) which is quantized and sampled at the clock frequency. A sample and hold circuit is used to synthesize the feedback signal $v_c(t)$. The modulator eliminates the strongly coupled relationship between the reference signal frequency and the limit at which slope overload condition takes place, and is therefore, able to encode input signals at high frequencies [21].

Since the reference signal frequency in UPS applications is fixed and it is normally equal to the supply frequency, such improved performance of the $\Sigma - \Delta M$ is of no significance in UPS applications.

1.4.3 The Adaptive Delta Modulator

The linear delta modulator has a serious limitation when encoding signals having a large dynamic range. To extend the dynamic range of linear delta modulators, adaptive delta modulator (ADM) is introduced [22]. Figure 1.6a shows the block diagram of continuous ADM. In this technique, the DM system is forced to adaptively respond to the rapid changes in the input signal by changing the step size of $v_c(t)$. The step size is controlled by the control signal obtained form the continuous derivative of the input signal. In UPS applications, such modulator feature is of no importance because the modulator reference signal is a sine wave

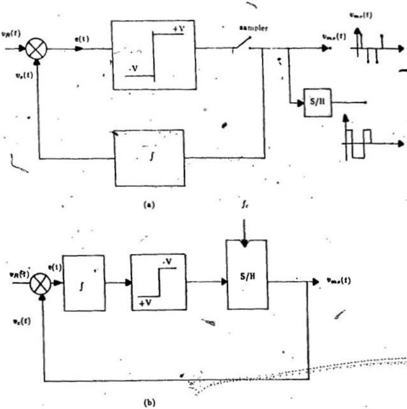


Figure 1.5: Delta Modulation technique: (a) Linear Delta Modulation (b) Sigma-Delta Modulation

at a frequency equal to the supply frequency. Although adaptive delta modulator overcomes the problem of encoding rapidly changing signals, its complex circuitry demolishes one of the main features of the DM family, which is simple circuit implementation. The modulator complex circuitry degrades the system reliability.

1.4.4 The Asynchronous Delta Modulator

Figure 1.6b shows one type of the asynchronous delta modulator (ASDM) called the rectangular wave delta modulator (RWDM). In this system, the information signal $v_R(t)$ is encoded into binary pulses with varying widths and quantized amplitudes. Thus, the output of the asynchronous delta modulation system is quantized only in amplitude but not in time, and no sampling is required [20], hence, the name asynchronous or free running delta modulator system. As a result the RWDM has a fast response and is best suited for analog implementation.

From the above discussion, it can be seen that rectangular wave delta modulation is very suitable for power electronics applications because of its simple circuit implementation and fast response to any changes in the reference signal. In addition, its output waveform is a binary output of the pulse width modulation type [23].

1.5 Objectives and Outline of the Thesis

Rectangular wave delta modulator has been successfully implemented in adjustable speed ac drives [24]. To the best of the author's knowledge, no thorough analysis of the application of rectangular wave delta modulator to uninterrupt-

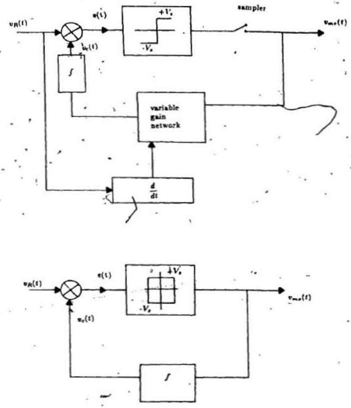


Figure 1.6: Delta Modulation technique: (a) Continuous Adaptive Delta Modulation (b) Rectangular Wave Delta Modulation

ible power supply applications, has been reported in the literature. The objective of this thesis is, therefore, to examine the application of rectangular wave delta modulator to the single phase version of the conventional UPS system.

Chapter 2 focuses on the basic characteristics of rectangular wave delta modulation technique for UPS applications. An analytical model of the modulator is derived and used to qualitatively describe the modulator performance. A quantitative analysis of the modulator performance from UPS application viewpoint, and curves describing the effect of various modulator parameters on the modulator performance are presented. Experimental verification of the predicted results is also provided.

Chapter 3 discusses the performance of the single phase UPS delta modulated inverter with resistive load for two frequently used switching schemes. The effect of various modulator parameters on the inverter output frequency spectrum is presented. Experimental verification and computer simulation of the inverter output frequency spectrum are also provided.

Chapter 4 is devoted to the analysis of a single phase delta modulated UPS inverter with L-C and tank circuit filters. Filter transfer characteristics are derived and used to examine the system performance with various types of loads. Curves describing the total harmonic distortion (THD) of the load voltage and the filter ratings are also provided. Computer simulation and experimental verification of the voltages and currents at various nodes of the filter with lagging power factor load are provided.

Chapter 5 outlines a general procedure for designing a single phase delta modulated UPS inverter. Various issues involved in the selection of the system parametres are presented along with a design example for R-L load to illustrate the general design procedure.

Finally, in chapter 6, a summary of the thesis highlighting the contribution of the research and suggestions for further work are outlined.

Chapter 2

CHARACTERISTICS OF THE RWDM FOR UPS APPLICATIONS

This chapter focuses on the analysis and performance of the rectangular wave delta modulation (RWDM) from UPS applications viewpoint. At the outset, the principle of operation of the modulator and its circuit implementation are briefly explained. An analytical equation governing the switching frequency of the modulator is developed and employed to provide an insight into the operation of the modulator. A methodology based on the use of the Discrete Fourier Transform (DFT) technique and the switching instants of the modulator digital output is used for evaluating the modulator frequency spectrum. The analytical model is used to evaluate the frequency spectrum of the RWDM and to obtain characteristic curves describing the modulator performance. Finally, predicted results along with their experimental verification are presented.

2.1 Principle of Operation of the Rectangular Wave Delta Modulation

The rectangular wave delta modulator is one of the simplest known methods of converting an analog signal into a digital format. Figure 2.1 shows the block diagram of the RWDM technique. It consists of a comparator, a hysteresis quantizer in the feed- forward path and an integrator or a low pass filter in the feedback path.

The principle of operation of the modulator can be described as follows : a reference signal $v_R(t)$ is compared with a feedback signal or the carrier wave $v_C(t)$, (obtained by integrating the modulator output signal), to produce the error signal e(t). According to the sign and predetermined magnitude of e(t), the output of the modulator has two possible levels $\pm V_s$, while, the time duration between two successive levels is determined by the slope of the reference signal. Referring to Fig. 2.1a, and assuming that the modulator outp[illegible] $+ V_s$, i.e., $V_{mo} = +V_s$, this output is integrated by the integrator in the feedback path to produce a signal which ramps up with a slope equal to the integrator gain. When the magnitude of the integrator output exceeds the magnitude of the reference signal by a preset value ΔV (defined by the hysteresis bandwidth), the modulator output switches to $-V_s$. Consequently, the integrator output ramps down with the same slope till the error signal e(t) reaches the preset value $+ \Delta V$ (the upper hysteresis limit) when the modulator output switches to $+ V_s$.

The modulator output can be expressed as

$$v_{mo}(t) \quad = \quad V_s sgn[e(t)] \tag{2.1}$$

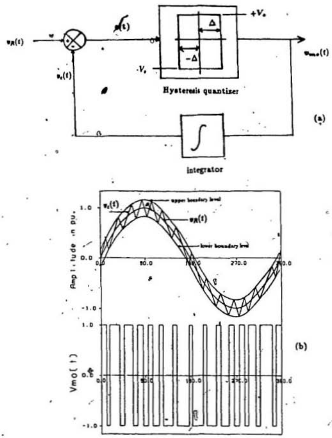


Figure 2.1: The Rectangular Wave Delta Modulation technique : (a) Block diagram (b) Ideal waveform

$$e(t) = v_R(t) - v_c(t) \tag{2.2}$$

where $v_{mo}(t)$ is the modulator output waveform.

V_s is the saturation level of the hysteresis comparator

$v_R(t)$ is the reference signal.

$v_c(t)$ is the carrier signal.

sgn is the sign function.

Figure 2.1b shows the waveforms at various nodes in the modulator block diagram. It can be seen that the feedback signal tracks the reference signal within the upper and lower boundary levels $\pm\Delta V$. From the modulator operating principles, it is observed that when the modulator digital output is decoded by the integrator in the feedback path, a replica $v_c(t)$ of the reference signal is produced (within allowable tolerance). The more faithful the feedback signal tracks the reference signal the more accurate is the encoding process of the analog reference signal into a digital one. Since recovering the reference signal (or a close replica) is done by a simple integration process, it can be concluded that the rectangular wave delta modulator encodes the derivative of the reference signal.

Two serious limitations inherent in DM systems, when encoding an analog signal into digital format, are known in the literature as [19]:

- The idle channel condition.
- The slope overload condition.

Idle channel condition occurs when the RWDM is required to encode dc signals. Idle channel condition does not usually exist in RWDM for UPS applications, since the input signal at the modulator is a sine wave at the utility frequency. Hence, idle channel condition is not discussed in this work.

Slope overload condition takes place when the rate of change of the reference signal is faster than that of the carrier wave. The latter fails to track the former faithfully and the encoding process is no longer an accurate one. For rapidly changing signals, slope overload condition can take place in some intervals of the signal where the rate of change of the signal is faster than the slope of the carrier wave. When the slope of the reference signal is greater than that of the carrier wave over the whole cycle, what is referred to as "square wave mode of operation" results. In this mode, the modulator output is a square wave with a frequency equal to the reference signal frequency. Under this condition, significant errors are introduced in the encoding process. To avoid slope overload condition, the maximum slope of the reference signal should be less than or equal to the slope of the carrier wave.

For a reference sine wave at the modulator input expressed as

$$v_R = V_R \sin \omega t \tag{2.3}$$

the maximum slope of the reference signal is obtained as

$$(S_R)_{max} = \omega V_R \tag{2.4}$$

The slope of the carrier wave, S_c is defined as

$$S_c = \frac{V_s}{\tau} \tag{2.5}$$

where τ is the integrator time constant.

To avoid slope overload condition,

$$(S_R)_{max} \leq S_c \tag{2.6}$$

or

$$\omega V_R \leq \frac{V_s}{\tau} \tag{2.7}$$

Equation 2.7 shows that slope overload can be avoided if small values of integrator time constant are used. Moreover, in UPS applications where the frequency of the reference signal is fixed but its amplitude is used for output voltage regulation, slope overload condition can be prevented by using higher hysteresis comparator switching levels V_s or small values of the reference signal amplitude. These voltage levels are circuit and devices dependent.

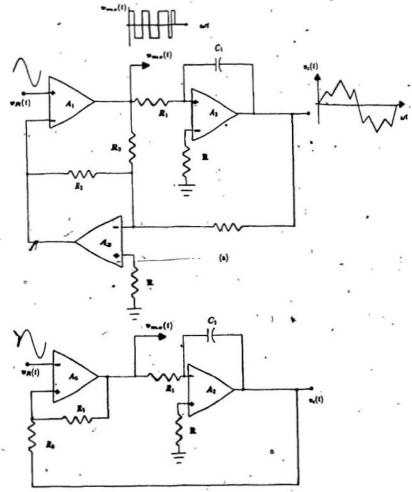
2.2 The Practical Rectangular Wave Delta Modulator

The rectangular wave delta modulator may be practically implemented using either an analog or digital scheme. A brief discussion of the principle of operation along with the main features of each scheme is presented in this section.

2.2.1 Analog Implementation of the RWDM

There are two types of analog RWDM, namely the single stage and the multistage RWDM.

Figure 2.2a shows one of the methods for realizing the single stage RWDM. In this circuit, three Operational amplifiers are used. A_1 functions as a hard limiter. A_2 is an integrator with time constant determined by the R-C combination. A_3



(b)

Figure 2.2: Circuit realization of RWDM : (a) Three Operational amplifiers circuit (hard limiter comparator) (b) Two Operational amplifiers circuit (hysteresis comparator)

functions as a summing point in which ΔV is added to the carrier wave. The magnitude of ΔV is determined by

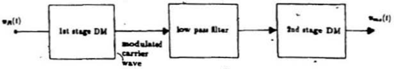
$$\Delta V = \frac{R_2}{R_3} V_s \tag{2.8}$$

where R_2, R_3 are resistance values.

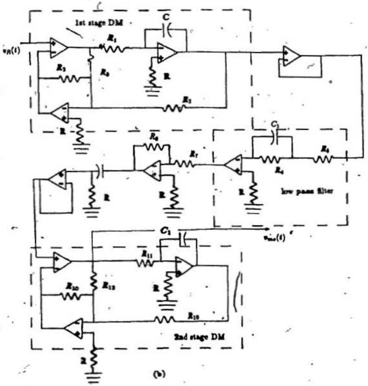
The circuit of figure 2.2a can be simplified by combining the functions performed by A_1 and A_3. Figure 2.2b shows the simplified circuit in which A_o functions as a hysteresis comparator.

A block diagram illustrating the multistage rectangular wave delta modulator (MSRWDM) for power electronics applications is shown in figure 2.3a [25]. A practical implementation of the scheme is shown in Fig. 2.3b. The scheme consists of two delta modulated stages , in which the modulator carrier wave of the first stage is filtered by a low pass filter and followed by a second DM stage which produces a filtered modulated wave with reduced harmonics. It has been shown by Rahman et al... [25] that multistage RWDM has improved harmonic spectrum and the ability to suppress certain undesired harmonics. Thus, with the proper choice of the filter components, the MSRWDM scheme allows harmonic elimination technique to be incorporated in the modulation scheme.

The Multistage delta modulator requires additional circuitry which complicates the simple circuit implementation of the DM technique. Besides, additional circuit components have the impact of degrading the system reliability which is one of the most essential specifications in UPS systems. Furthermore, in UPS applications where feedback control of the reference signal is employed to maintain a constant load voltage, the multistage system could result in a slow dynamic response.



(a)



(b)

Figure 2.3: The Multistage Rectangular Wave Delta Modulation : (a) Block diagram (b) Practical circuit [25]

2.2.2 Digital Implementation of the RWDM

Figure 2.4 shows the block diagram of the digital implementation of the rectangular wave delta modulation[26]. It consists of two main parts, the microprocessor part and the inverter part. The microprocessor part consists of the CPU with associated accessories, A/D and D/A converters. The output of the microprocessor part is processed by the logic circuit to provide appropriate signals to control the switching devices in the inverter circuit.

Three switching strategies, namely the natural sampling, the regular sampling, and the look-up tables have been proposed for the digital implementation of the RWDM. The natural and regular sampling schemes were found unsuitable for real time microcomputer implementation of rectangular wave delta modulation, because of the time constraints of the sampling and the A/D, D/A conversions [26].

In the look-up table method, the memory required to store the DM waveform switching instants is large. To overcome this disadvantage, the delta modulated switching instants are precalculated at particular values of modulator parameters and stored in the look-up table. This method has the advantage of eliminating the analog to digital converter stage. The main disadvantage of the look-up tables method is that it does not allow the generation of delta modulated switching signals for continuous values of the amplitude of the reference signal.

Although the digital RWDM has improved noise immunity, it is complex and costly. In addition, its dynamic response is slower than that of the single stage analog scheme.

In this thesis, the single stage analog RWDM is used to investigate the per-

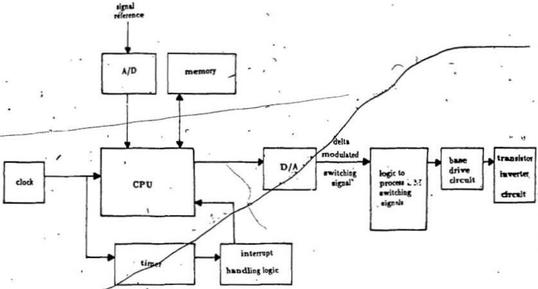


Figure 2.4: Block diagram of the digital implementation of the Rectangular Wave Delta Modulation [26]

formance of the delta modulation technique for UPS applications.

2.3 Analytical Model of the RWDM

The rectangular wave delta modulation, though conceptually simple, is difficult to analyze. The presence of the non-linear hysteresis comparator and the built-in carrier waveform make it difficult to obtain closed form equations for describing the modulator performance.

In this section, analytical procedures for obtaining qualitative and quantitative description of the modulator are presented. Initially, equations which describe the switching frequency of the modulator are derived. These equations are employed to qualitatively describe the performance of the modulator. A numerical approach based on the determination of the switching instants of the modulator output, and the use of the DFT technique is then employed to obtain characteristic curves, and the frequency spectrum of the modulator output. In particular, the numerical approach is used to investigate the effect of various modulator parameters on the performance of the modulator from UPS applications viewpoint.

2.3.1 Simplifying Assumptions

Upon examining the principle of operation of the analog RWDM, it can be seen that the modulator is not strictly periodic. Although, the carrier wave initially starts at the zero crossing point at the same time as the reference signal, there is no guarantee that the carrier wave will pass through the same point on the completion of a full cycle of the reference signal. Hence, it can be seen that the reference signal and the carrier waveform are not strictly synchronized. In some applications, for example, three phase inverters, it is essential to have a strictly periodic waveform at the modulator output, otherwise the output waveform will not be balanced. To synchronize the carrier wave with the reference signal, the carrier wave amplitude can be reset to zero at each zero crossing of the reference signal. This is practically achieved by discharging the capacitor (in the integrator circuit) through a small resistance at each zero crossing of the reference signal. However, if the carrier wave frequency is made very high compared to the reference signal frequency, the effect of the drift between the modulator output and the reference signal on the three phase output voltage is reduced. Alternately, synchronism can be achieved by using a phase locked loop as a frequency multiplier to produce synchronizing pulses from the reference signal [27].

The following assumptions are made to simplify the analytical model developed for the rectangular delta modulator:

1. The modulator switching frequency is assumed to be high so that a small portion of the reference signal can be approximated by a straight line during one switching cycle of the modulator.

2. The circuit components of the rectangular wave delta modulator are ideal.

2.3.2 Determination of the Modulator Switching Frequency

Figure 2.5 shows a small portion of the reference signal $v_R(t)$ and the carrier waveform $v_c(t)$ [20].

During the positive output pulse, the slope of the reference signal is given by

$$S_R|_{AB} = \frac{R}{T_+} \tag{2.9}$$

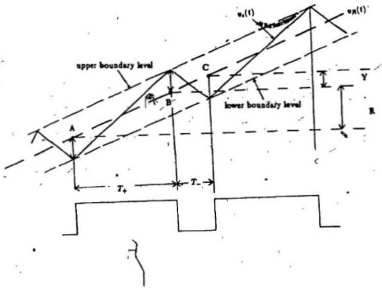


Figure 2.5: Graphical illustration of the RWDM for developing the analytical model

where $S_R|_{AB}$ is the slope of the reference signal between points A and B.

R is the vertical distance between points A and B.

T_+ is the time duration of the positive pulse of the modulator output.

The slope of the carrier wave S_c is obtained as

$$S_c = \frac{R + 2\Delta V}{T_+} \tag{2.10}$$

Substituting the value of R from equation 2.9 into 2.10 gives

$$S_c = S_R|_{AB} + \frac{2\Delta V}{T_+} \tag{2.11}$$

and

$$T_+ = \frac{2\Delta V}{S_c - S_R|_{AB}}. \tag{2.12}$$

Equation 2.12 shows that when the slope of the reference signal approaches that of the carrier wave, the output of the positive pulse reaches its maximum value and the modulator operates in the square mode of operation.

Similarly, during the negative output pulse, the slope of the reference signal is given as

$$S_R|_{BC} = \frac{Y}{T_-} \tag{2.13}$$

where $S_R|_{BC}$ is the slope of the reference signal between points B and C.

Y is the vertical distance between points B and C.

T_- is the time duration of the negative pulse of the modulator output

and

$$Y = -S_c T_- + 2\Delta V \tag{2.14}$$

substituting the value of Y from equation 2.14 into equation 2.13 gives

$$S_R|_{BC} = \frac{-S_c T_- + 2\Delta V}{T_-} \tag{2.15}$$

and

$$T_- = \frac{2\Delta V}{S_c + S_R|_{BC}} \tag{2.16}$$

The duration between two successive positive and negative pulses is given by

$$T = T_+ + T_- \tag{2.17}$$

and from equations 2.12 and 2.16

$$T = \frac{2\Delta V}{S_c - S_R|_{AB}} + \frac{2\Delta V}{S_c + S_R|_{BC}} \tag{2.18}$$

$$T = \frac{4\Delta V S_c}{S_c^2 - s_R(t)^2} \tag{2.19}$$

Equation 2.19 is obtained assuming that the slope of the reference signal does not change during the interval T, hence

$$S_R|_{AB} = S_R|_{BC} = s_R(t) \tag{2.20}$$

where $s_R(t)$ is the slope of the reference signal between points A and C.

The frequency of the carrier wave V_c is obtained from equation 2.19 as

$$f_c(t) = \frac{1}{T} = \frac{1}{4\Delta V S_c}(S_c^2 - s_R(t)^2) \tag{2.21}$$

or

$$f_c(t) = \frac{S_c}{4\Delta V}(1 - (\frac{s_R(t)}{S_c})^2) \tag{2.22}$$

For a reference sine wave signal, the instantaneous slope of the signal is given by

$$s_R(t) = V_R\omega \cos\omega t \tag{2.23}$$

Hence, the carrier frequency can be expressed as

$$f_c(t) = \frac{S_c}{4\Delta V}(1 - K\cos^2\omega t) \tag{2.24}$$

where

$$K = (\frac{\omega V_R}{S_c})^2 \tag{2.25}$$

Equation 2.25 shows the following:

1. The frequency of the carrier wave reaches its maximum value, and hence minimum output pulse width duration at

$$\begin{aligned} \omega t &= \frac{n\pi}{2} \\ where \quad n &= 1, 3, 5, ... \end{aligned}$$

The maximum frequency of the modulator is obtained from equation 2.24 as

$$F_{max} = \frac{S_c}{4\Delta V} \tag{2.26}$$

2. The frequency of the carrier wave has its minimum value, and hence maximum output pulse width duration at

$$\begin{aligned} \omega t &= \frac{n\pi}{2} \\ where \quad n &= 2, 4, 6, ... \end{aligned}$$

and its value is equal to

$$F_{min} = \frac{S_c}{4\Delta V}(1 - (\frac{\omega V_R}{S_c})^2) \tag{2.27}$$

3. The switching frequency of the modulator varies inversely with the hysteresis bandwidth ΔV. Thus, fairly small hysteresis bandwidth generally results in high switching frequencies, with associated high losses in the inverter of the power circuit. Conversely, a fairly large ΔV results in a lower switching frequency. However, allowing the carrier wave to track the reference signal with a fairly large hysteresis bandwidth results in errors in the encoding process and hence an output voltage with high harmonic distortion. Hence, it can be seen that there is a trade off between inverter losses and the harmonic distortion of the output voltage.

4. The modulator switching frequency increases with increasing values of the slope of the carrier wave.

5. The modulator switching frequency decreases with increasing either the amplitude or the frequency of the reference signal. However, increasing the amplitude or the frequency of the reference signal beyond certain critical values determined by the parameters of the modulator results in slope overload condition (equation 2.7).

6. The modulator provides an output waveform with an inherent minimum pulse width which corresponds to a maximum switching frequency. This gives the RWDM an advantage over Sine Pulse Width Modulation (SPWM) in which special efforts have to be made to provide minimum pulse width of the modulated waveform if simultaneous conduction of the power switches is to be avoided.

2.3.3 Determination of Modulator Average Switching Frequency

The average switching frequency of the RWDM is obtained by averaging the instantaneous switching frequency of the modulator over a full cycle of the reference signal. The average switching frequency is therefore given by:

$$F_{avg} = \frac{1}{2\pi}\int_0^{2\pi}\frac{S_c^2 - s_R^2(t)}{4\Delta V S_c}d(\omega t) \tag{2.28}$$

$$F_{avg} = \frac{1}{8\pi\Delta V S_c}\int_0^{2\pi}(S_c^2 - \omega^2 V_R^2\cos^2\omega t)d(\omega t) \tag{2.29}$$

where F_{avg} is the average switching frequency of the modulator

Hence,

$$F_{avg} = \frac{S_c}{4\Delta V}(1 - \frac{\omega^2 V_R^2}{2S_c^2}) \tag{2.30}$$

Since

$$F_{max} = \frac{S_c}{4\Delta V} \tag{2.31}$$

Equation 2.30 may be rewritten as

$$F_{avg} = F_{max}(1 - \frac{\omega^2 V_R^2}{2S_c^2}) \tag{2.32}$$

Equation 2.32 gives the average frequency of the carrier wave, and hence the modulator average switching frequency, with a sine wave at the modulator input. In general, the average switching frequency determines the dominant harmonic order of the modulator output frequency spectrum. The equation also shows that the order of the dominant harmonic of the modulator output waveform can be controlled by controlling the hysteresis bandwidth and the slope of the carrier wave. In addition, the switching power loss in the power circuit depends on the average switching frequency of the modulator. Thus equation 2.32 also shows that the system efficiency can be optimized by selecting appropriate values of the modulator parameters.

2.4 Evaluation of the Frequency Spectrum of the RWDM

For inverter applications, the knowledge of the frequency spectrum of the output waveform is an essential performance measure of the inverter performance. Moreover, controlling the position of the dominant harmonics of the modulator output waveform aids in optimizing the inverter output filter design.

In this section, a numerical procedure based on the use of numerical method to determine the switching instants of the modulator output and the use of Discrete Fourier Transform (DFT) technique to obtain the frequency spectrum of the modulator output is described.

2.4.1 Determination of the Switching Instants of the RWDM

To quantitatively examine the performance of the modulator output waveform, a numerical approach which enables the switching instants of the modulator output waveform to be determined, is developed.

As shown earlier, the modulator output waveform is non periodic, and hence the use of Fourier series technique to determine the frequency spectrum of the signal is not strictly accurate. This difficulty can be overcome by using an averaging technique [28].

In the averaging process approach Fourier analysis technique is used to obtain the frequency spectrum over integer multiples of the period of the modulated waveform. This approach assumes that for a time period equal to integer multiples of the reference signal period, the modulator output waveform becomes periodic. For a high carrier to fundamental frequency ratio, Fourier series analysis of the modulator output waveform gives accurate results when the analysis is carried out over a period several times that of the reference signal. This approach has the advantage of evaluating the sub-harmonic components of the output waveform. In this work, the averaging process is done over five cycles of the reference signal. Hence, the modulator output becomes periodic, with the period equal to five times that of the reference signal. Consequently, the separation between each harmonic component in the frequency domain of the modulator output waveform frequency spectrum is one-fifth that of the reference signal frequency.

Figure 2.6 shows the first few switching pulses in the modulation process. As shown in the figure, it is assumed that the carrier wave initially passes through the zero crossing point of the reference signal with a positive slope.

It can be seen that switching instants occur when the carrier wave reaches the upper or the lower boundary level of the reference signal. Thus, a switching instant occurs when ;

$$|e(t)| = |v_R(t) - v_c(t)| = |\Delta V| \tag{2.33}$$

The sign of the output voltage pulses is determined by the sign of the error signal. For a positive error value, the modulator output has a positive pulse till the error signal hits the upper boundary level when the modulator switches from a positive output pulse to a negative one and vice versa. A detailed derivation of the switching instants is given in Appendix A. The governing equations of the

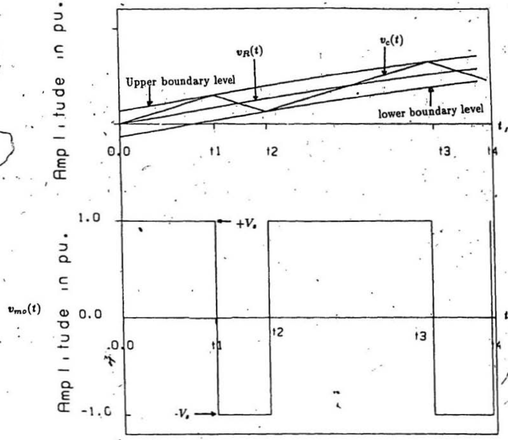


Figure 2.6: First few switching instants associated with the Rectangular Wave Delta Modulator

switching instants are as follows [24]:

The first switching instant t_1 is given by

$$t_1 = \frac{V_R \sin \omega t + \Delta V}{S_c} \tag{2.34}$$

and for subsequent switching instants t_i is given as,

$$t_i = \frac{2\Delta V + S_c t_{i-1}}{S_c} + V_R \frac{(\sin \omega t_{i-1} - \sin \omega t_i)}{S_c(-1)^i} \tag{2.35}$$

$$where \quad i = 2, 3, 4, ...n$$

where t_1 is the value of the first switching instant in seconds

t_i is the instantaneous values of subsequent switching instants in sec (i >1).

t_{i-1} is the value of the preceeding switching instant in sec.

n is the number of switching points

The transcendental nature of equation 2.35 suggests the need for a numerical solution method to obtain the switching instants. An International Mathematics and Statistics Library (IMSL) routine, ZREAL (Version 10.0) is used to solve equation 2.35. The list of the FORTRAN program for obtaining the switching points is given in Appendix B.

2.4.2 Determination of the Frequency Spectrum of the RWDM

Following the determination of the switching instants of the modulator output, a harmonic analysis technique based on the use of Discrete Fourier Transform (DFT) is employed to evaluate the frequency spectrum of the modulator output. The DFT approach involves the discretization of the modulator output waveform such that the time elapsed between two successive samples is smaller than the shortest pulse width that could be obtained at the modulator output. An IMSL routine (FFTSC : version 9.2) is employed to carry out the DFT operation. The program listing is given in Appendix B.

2.5 Performance Analysis of the RWDM

As indicated earlier, the parameters of the modulator which affect the frequency spectrum of the modulator output are:

- The hysteresis bandwidth, ΔV
- The integrator gain, S_c
- The amplitude and frequency of the reference signal, (V_R and ω)

In UPS applications, the frequency of the load voltage is determined by the frequency of the reference signal, and since the frequency of the load voltage is maintained constant, the reference signal frequency is kept constant. Hence, the effect of changing the frequency of the reference signal on the modulator output is not considered. However, the effect of changing the amplitude of the reference signal on the magnitude of the output voltage is of great importance for output voltage regulation.

In this section, a parametric study is carried out to investigate the relationship between the modulator switching frequency, modulator output frequency spectrum and various modulator parameters. The parametric study is carried out by using normalized modulator parameters to provide characteristics curves which describe the performance of the modulator. Finally, an empirical formula that governs the relationship between the amplitude of the fundamental component of the output voltage and the modulator parameters is developed.

2.5.1 Normalized RWDM Parameters

Normalized parameters of the RWDM are used to obtain general performance curves for the modulator, independent of the absolute values of the modulator parameters. Base values of the modulator parameters are chosen such that the analysis for the modulator output waveform can be adapted to the inverter output voltage waveforms.

The base value for voltages is chosen as the hysteresis comparator saturation level V_s.

Thus, the amplitude of the reference sine wave at the modulator input, has a normalized value given by

$$M = \frac{V_R}{V_s} \tag{2.36}$$

where M is the rectangular wave delta modulation index (the maximum value that M can take is unity.)

The normalized value of the hysteresis bandwidth is given by

$$\Delta V_n = \frac{\Delta V}{V_s} \tag{2.37}$$

The frequency of the reference signal (f=60 Hz), is chosen as the base frequency.

To avoid slope overload condition, the maximum value of the slope of the reference signal should be less than or equal to the slope of the carrier wave.

$$\omega V_R \leq S_c \tag{2.38}$$

Where S_c, the slope of the carrier wave (or the integrator gain) is given by

$$S_c = \frac{V_s}{R_1 C_1} \tag{2.39}$$

In equation 2.39,

R_1	is the integrator resistance.
C_1	is the integrator capacitance
V_s	is the saturation level of the hysteresis comparator.

Normalizing the modulator time constant to the angular frequency of the reference signal yields the normalized slope of the carrier wave, and is given by

$$S_{cn} = \frac{1}{R_1 C_1 \omega} \tag{2.40}$$

Substituting equation 2.39 into 2.38 gives

$$\frac{V_R}{V_s} \leq \frac{1}{R_1 C_1 \omega} \tag{2.41}$$

Using equation 2.36, equation 2.41 may be expressed in terms of the normalized modulator parameters as

$$M \leq S_{cn} \tag{2.42}$$

where S_{cn} is the normalized value of the carrier wave slope or the normalized value of the integrator gain.

2.5.2 Effect of Modulator Parameters on the Modulator Switching Frequency

Figure 2.7 shows the variation of the instantaneous switching frequency and average frequency of the modulator with various modulator parameters. It is observed that in general the relationship is periodic with a period equal to half the period of the reference sine wave. This is also indicated by the quarter wave symmetry that rectangular wave delta modulation possesses.

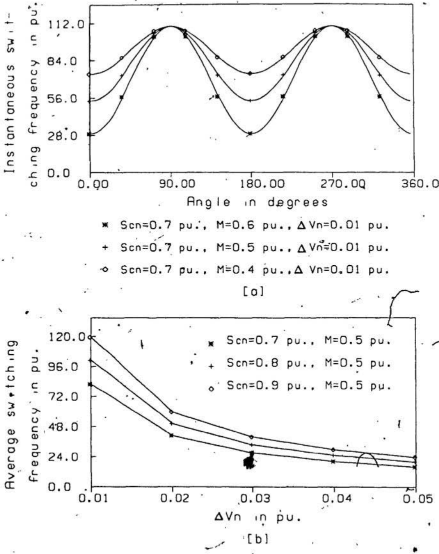


Figure 2.7: Effect of the modulator parameters on modulator switching frequency : (a) Instantaneous switching frequency (b) Average switching frequency

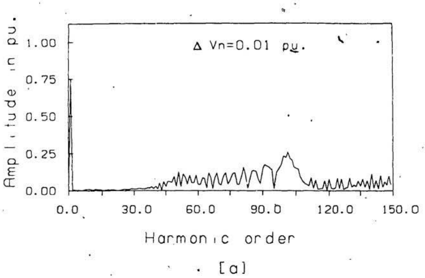
2.5.3 Effect of the Hysteresis Bandwidth on the Modulator Output Frequency Spectrum

Figure 2.8 shows the effect of the hysteresis bandwidth, ΔV_n on the frequency spectrum of the modulator output, while, Fig. 2.9 and Fig. 2.10 show the variation of the fundamental component and the order of the dominant harmonic in the modulator output with the hysteresis bandwidth respectively. The following are observed from the figures:

1. The dependence of the amplitude of the fundamental component of the output waveform on the hysteresis bandwidth is fairly weak. In general the value of ΔV_n does not affect the amplitude of the output fundamental component.

2. There is a significant correlation between the dominant harmonic order and the value of ΔV_n. The smaller the value of ΔV_n, the higher the order of the dominant harmonic and vice versa. For example, a 4 times increase in the value of the hysteresis bandwidth results in a five-fold decrease in the order of the dominant harmonic. This is explained by the fact that small ΔV_n provides a better replica of the reference signal at the expense of higher switching frequency of the modulator. Hence, the dominant harmonic components of the switching harmonics cluster around the order of the modulator average switching frequency.

   In inverters for UPS application, it is desirable to have the undesired harmonics at higher orders. This allows filtering out the undesired harmonics without affecting the amplitude of the fundamental component of the out-



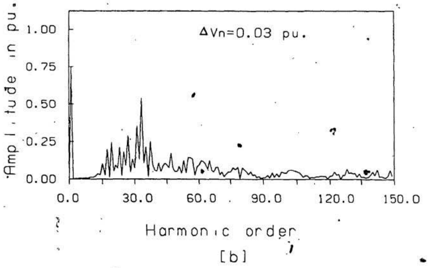


Figure 2.8: Effect of the hysteresis bandwidth on the frequency spectrum of the modulator output : (a) S_{cn}=0.68 pu., M=0.5 pu., ΔV_n=0.01 pu., (b) S_{cn}=0.68 pu., M=0.5 pu., ΔV_n=0.03 pu.

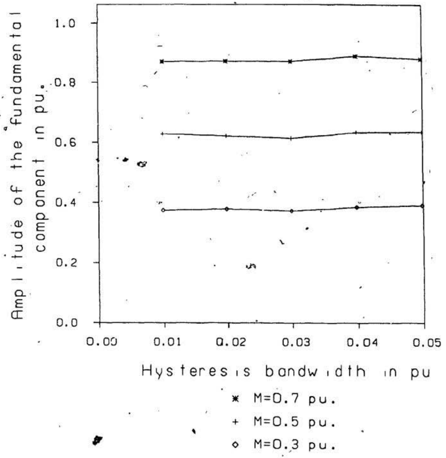


Figure 2.9: Effect of the hysteresis bandwidth on the amplitude of the fundamental component in the modulator output S_{cn}=0.8

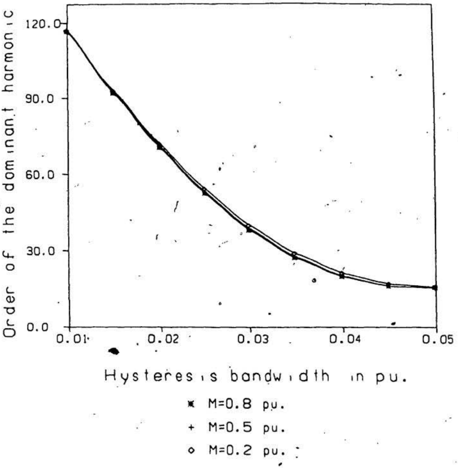


Figure 2.10: Effect of the hysteresis bandwidth on the order of the dominant harmonic in the modulator output S_{cn}=0.8

put voltage. Besides, the filter size required to filter out the higher order harmonics is small. Thus, from the harmonic viewpoint, small values of ΔV_n is desirable. However, small values of ΔV_n result in higher modulator switching frequency (Fig. 2.8) which in turn means higher inverter switching losses.

2.5.4 Effect of the Integrator Gain on the Modulator Output Frequency Spectrum

The effect of changing the integrator gain, S_{cn}, on the frequency spectrum of the modulator output is depicted in Fig. 2.11, Fig. 2.12 and Fig. 2.13. The figures show the variation of the fundamental component and the order of the dominant harmonic in the modulator output with the integrator gain. Figure 2.13 shows that higher values of integrator gain cause the dominant harmonic components to be shifted to higher orders. However, Fig. 2.12 shows that increasing the integrator gain has the adverse effect of reducing the fundamental component of the modulator output.

2.5.5 Effect of the Modulation Index on the Modulator Output Frequency Spectrum

The effect of changing the reference signal amplitude on the frequency spectrum of the modulator output is shown in Fig. 2.14. Fig. 2.15 and Fig. 2.16. Figure 2.15 shows the relationship between the amplitude of the fundamental component of the modulator output and the modulation index with S_{cn} as a parameter. The figure shows that the amplitude of the fundamental component of the output voltage increases with increasing M, until the modulation index is equal to the

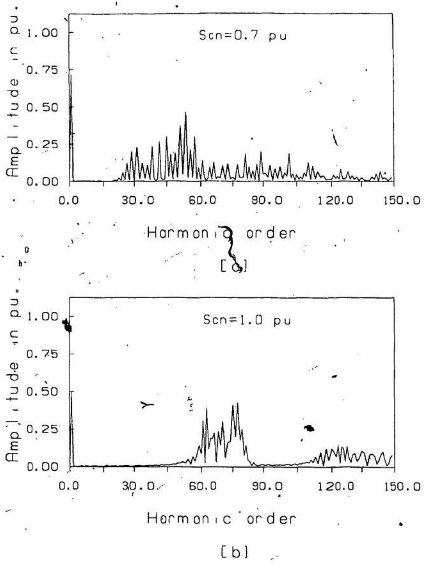


Figure 2.11: Effect of the integrator gain on the frequency spectrum of the modulator output: (a) S_{cn}=0.7 pu., M=0.5 pu., ΔV_n=0.02 pu., (b) S_{cn}=1.0 pu., M=0.5 pu., ΔV_n=0.02 pu.

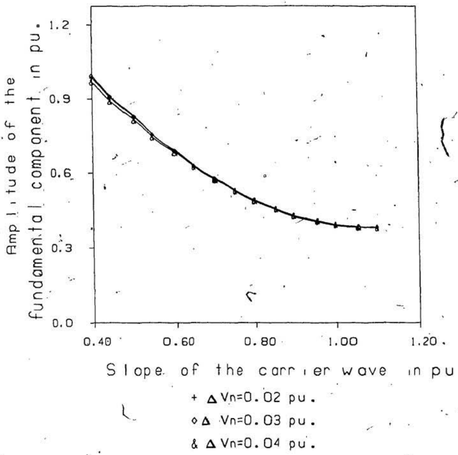


Figure 2.12: Effect of the integrator gain on the fundamental component of the modulator output (M=0.4 pu.)

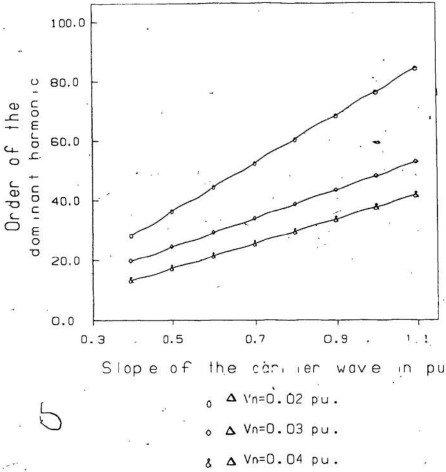


Figure 2.13: Effect of the integrator gain on the order of the dominant harmonic in the modulator output (M=0.4 pu.)

integrator gain, when the modulator enters the slope overload condition region, and the amplitude of the fundamental component remains fairly constant.

The relationship between the fundamental component of the modulator output and the modulation index in the linear region of the modulator characteristics is linear, and is described by the equation

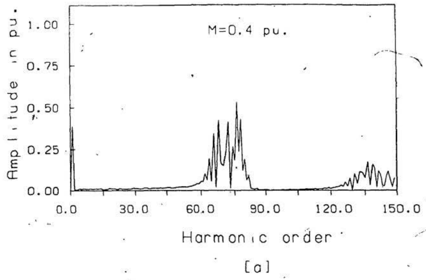
$$\hat{V}_{o1} = \frac{M}{S_{cn}} \quad pu. \tag{2.43}$$

where $\hat{V}_{o1}$ is the peak value of the fundamental component of the modulator output waveform

Figure 2.16 shows the relationship between the modulation index and the order of the dominant harmonic component in the modulator output. The figure shows that a fairly weak relationship exists between the two variables. In general, the value of the modulation index does not affect the order of the dominant harmonic. In UPS systems, where voltage regulation capability is one of the system specifications, the inherent linear relationship between the fundamental output voltage and the amplitude of the reference signal provides a means whereby the output voltage of the UPS system can be regulated independent of the dc supply voltage or load changes within specified limits. The linear relationship makes the RWDM attractive for UPS applications because it avoids the use of complex control circuitry which generally degrades system reliability.

The effect of the modulator parameters on the performance of the modulator may be summarized as follows (Table 2.1)

1. The modulator parameters which affect the order of the dominant harmonic component in the modulator output are the hysteresis bandwidth ΔV_n and the integrator gain S_c. The hysteresis bandwidth has a significant effect on



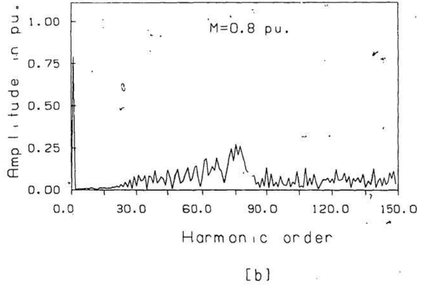


Figure 2.14: Effect of the reference signal amplitude on the frequency spectrum of the modulator output: (a) S_{cn}=1.0 pu., ΔV_n=0.02 pu., (b) S_{cn}=1.0 pu., ΔV_n=0.02 pu.

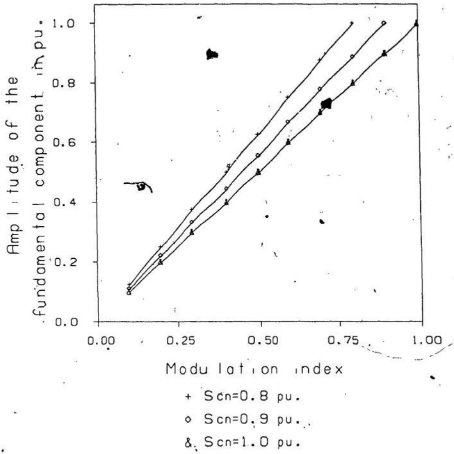


Figure 2.15: Effect of the modulation index on the amplitude of the fundamental component of the modulator output waveform (ΔV_n=0.02 pu.)

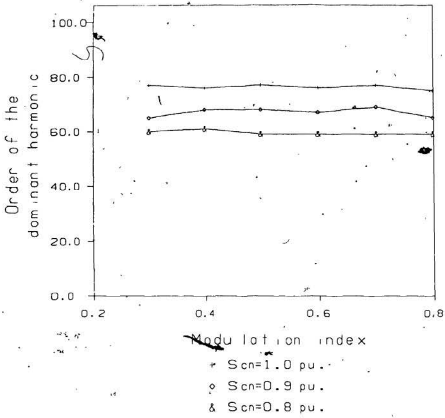


Figure 2.16: Effect of the modulation index on the order of the dominant harmonic in the modulator output (ΔV_n=0.02 pu.)

the order of the dominant harmonic component and a negligible effect on the fundamental component in the modulator output. However, the slope of the carrier wave S_c affects both the order of the dominant harmonic and the amplitude of the fundamental component significantly. Consequently, the selection of the value of S_c for the design of the modulator is dictated by the desired value of the amplitude of the fundamental component in the modulator output, while the selection of the value of ΔV_n is mainly determined by the order of the dominant harmonic component in the modulator output and the switching losses of the power circuit.

2. The modulation index, M has a negligible effect on the order of the dominant harmonic. However, for a given value of the integrator gain, the modulation index exhibits a linear relationship with the fundamental component of the modulator output.

3. In general, the choice of suitable modulator parameters involves some trade offs between the modulator switching frequency, the order of the dominant harmonic and the fundamental component of the modulator output.

Table 2.1: Summary of the effects of various modulator parameters on the modulator output frequency specrums

increasing	V_{o1}	H_n	f_s
M	increases	no effect	decreases
ΔV	no effect	decreases	decreases
S_c	decreases	increases	increases

where V_{o1} is the fundamental component of the inverter output voltage.

H_n is the order of the dominant harmonic of the inverter output voltage.

f_s is the inverter switching frequency.

2.6 Experimental Verification of the Performance of the RWDM

The circuit of Fig. C.1 (in Appendix C) was constructed and used to experimentally verify the behaviour of the RWDM. Due to the limitations of available standard resistance and capacitor values, both integrator gain and hysteresis bandwidth values were determined by the available resistance and capacitor standard values. These same standard values were used in the computer programs to obtain the corresponding predicted results.

Verification of the relationship between the modulation index and the fundamental component of the output waveform is carried out by fixing the values of both the integrator gain and the hysteresis bandwidth while changing the modulation index.

Table 2.2 shows the predicted and the experimental results. The results highlight the fact that the hysteresis bandwidth has a negligible effect on the fundamental component of the output waveform. The results also confirm the linear relationship between the fundamental component of the output waveform and the modulation index.

Table 2.3 shows the effect of the integrator gain on the fundamental component of the modulator output for a fixed value of the modulation index. The table shows a very good agreement between the predicted and the experimental results.

Figure 2.17 shows spectrum analyzer pictures indicating the effect of ΔV_n on the frequency spectrum of the modulator output. It can be seen that ΔV_n has a negligible effect on the fundamental component of the output waveform.

The verification of the effect of the integrator gain on the order of the

Table 2.2 Verification of the effect of the modulation index on the rms value of the fundemental component of the modulator output
V_s= 1 pu.(10V)

M	V_{o1} (rms) ($\frac{10M}{\sqrt{2}S_{cn}}$)							
	0.1 (pu.)		0.3 (pu.)		0.5 (pu.)		0.6 (pu.)	
	exp.	pred.	exp.	pred.	exp.	pred.	exp.	pred.
ΔV_n = 0.021 pu. S_{cn}=0.65 pu.	1.05	1.11	3.27	3.26	5.62	5.48	6.59	6.57
ΔV_n= 0.062 pu. S_{cn}= 0.65 pu.	1.09	0.94	3.22	3.20	5.5	5.61	6.36	6.73

Table 2.3 Verification of the effect of the integrator gain on the rms value of the fundemental component of the modulator output
V_s = 1 pu. (10V)

S_{cn}	V_{o1} (rms) ($\frac{M}{\sqrt{2}S_{cn}}$)							
	0.54 (pu.)		0.78 (pu.)		0.957 (pu.)		1.14 (pu.)	
	exp.	pred.	exp.	pred.	exp.	pred.	exp.	pred.
M = 0.5 pu. (5.0 V) ΔV_n = 0.02 pu. (0.2 V)	6.30	6.47	4.42	4.51	3.62	3.69	3.02	3.10
M = 0.8 pu (8.0 V) ΔV_n=0.02 pu. (0.2 v)	slope overload condition				5.87	5.90	4.92	4.96

dominant harmonic component is carried out for fixed values of modulation index and hysteresis bandwidth. Table 2.4 shows the measured and the predicted values of the dominant harmonic order for various values of S_{cn}. Experimental and predicted results show good agreement. The discrepancies obtained between the experimental and the predicted results vary in the range of ±10% and is due to the imperfections in the modulator practical circuit and spectral leakage of predicted frequency spectrum resulting from the use of the DFT technique.

Figures 2.18 shows spectrum analyzer pictures indicating the effect of the integrator gain on the frequency spectrum of the modulator output.

The effect of ΔV_n on the modulator output frequency spectrum is verified by changing ΔV_n for fixed values of both S_{cn} and M. Table 2.5 shows both experimental and predicted results of the dominant harmonic order of the modulator output waveform.

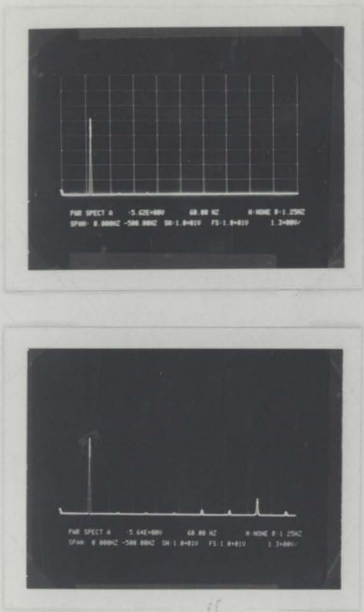
Figure 2.19 shows the slope overload condition. Figure 2.19a shows that slope overload condition can take place over certain intervals in the signal where the carrier signal can not track the reference signal. Figure 2.19b shows the square wave mode of operation, where the modulator is forced deeply into saturation. Under this condition, the carrier wave fails to track the reference signal over the whole cycle.

Table 2.4. Verfication of the effect of the integrator gain on the order of the dominant harmonic in the modulator output V_s= 1 pu. (10 V)

	Order of the dominant harmonic (pu.)							
S_{cn}	0.55 (pu.)		0.78 (pu.)		0.95 (pu.)		1.14 (pu.)	
	exp.	pred.	exp.	pred.	exp.	pred.	exp.	pred.
M = 0.2 pu. (2.0 V) ΔV_n= 0.05 pu. (0.5 V)	15.3	16.0	21.5	23.9	27.0	29.4	31.9	35.3
M = 0.5 pu. (5.0 V) ΔV_n= 0.05 pu. (0.5 V)	14.3	14.0	19.0	23.0	26.7	28.0	32.0	34.5

Table 2.5 Verification of the effect of the hysteresis bandwidth ΔV on the order of the dominant harmonic
V_s = 1 pu. (10V), S_{cn}= 0.78 pu. (2940 V/s)

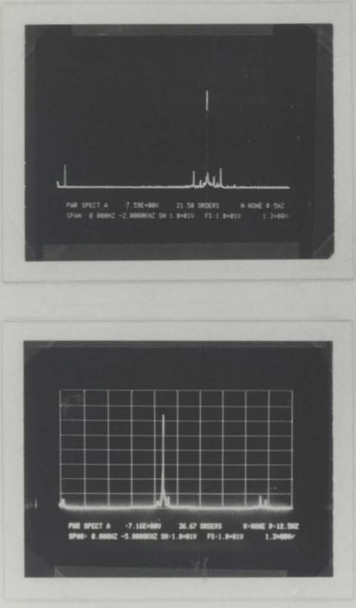
	Order of the dominant harmonic (pu.)							
ΔV_n	0.022 (pu.)		0.036 (pu.)		0.052 (pu.)		0.087 (pu.)	
	exp.	pred.	exp.	pred.	exp.	pred.	exp.	pred.
M= 0.5 pu. (5.0 V)	50.8	52.6	39.6	41.0	30.8	31.2	12.6	13.2



(a)

(b)

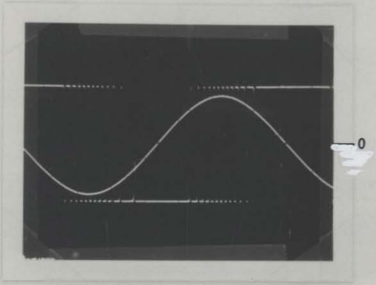
Figure 2.17: Spectrum analyzer pictures showing the effect of the hysteresis bandwidth on the frequency spectrum of the modulator output: (a) ΔV_n=0.022 pu., S_{cn}=0.65 pu., M=0.5 pu., (b) ΔV_n=0.065 pu., S_{cn}=0.65 pu., M=0.5 pu.



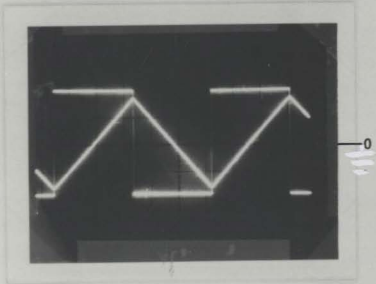
(a)

(b)

Figure 2.18: Spectrum analyzer pictures showing the effect of the integrator gain on the frequency spectrum of the modulator output: (a) ΔV_n=0.05 pu., S_{cn}=0.78 pu., M=0.2 pu., (b) ΔV_n=0.05 pu., S_{cn}=1.38 pu., M=0.2 pu.



(a)



(b)

Figure 2.19: Oscillograms showing slope overload conditions in the RWDM : (a) Some interval of the reference signal (b) Over the complete cycle (Square Mode of Operation)

Chapter 3

THE SINGLE PHASE DELTA MODULATED UPS INVERTER WITH A RESISTIVE LOAD

When the digital output of the delta modulator is used to control the power switching devices in a static inverter for UPS applications, this inverter is referred to as a delta modulated UPS inverter. In this chapter, the implementation of the delta modulation technique for a single phase UPS inverter with a resistive load is described. Two single phase bridge inverter topologies commonly used in static UPS inverters are presented and their main features are briefly outlined. The harmonic characteristics of two possible switching schemes for pulse width modulated inverters, namely the unipolar and the bipolar switching schemes, are examined with a view to selecting the appropriate scheme for the delta modulated UPS inverter. It is shown that the delta modulated UPS inverter using the bipolar switching scheme offers significant performance improvement. Finally, the results of the computer simulation and experimental verifications ~~of~~ the characteristics of the delta modulated UPS inverter with a resistive load are presented.

3.1 The Single Phase UPS Inverter

Two single phase bridge inverters commonly used in UPS applications are presented and their features are briefly outlined. Two commonly used switching schemes for PWM inverters, namely the unipolar and the bipolar switching schemes, are discussed with a view to selecting the appropriate scheme for delta modulated UPS inverter applications.

3.1.1 UPS Inverter Configurations

Figure 3.1 shows the single phase half-bridge and full-bridge inverters with resistive load. In the half-bridge inverter configuration, the dc supply V_{dc} is split up equally using two capacitors of equal value connected in series. Hence, the load voltage is equal to half the value of the dc supply voltage. The single phase full bridge inverter uses four switching devices to provide a load voltage with a voltage level equal to the dc supply voltage.

The single phase half-bridge inverter configuration has the advantage of using half the number of switching devices that are used in the full-bridge inverter. However, this configuration is not suitable for high power applications as well as for PWM techniques which require zero-voltage intervals at the inverter output (single pulse width modulation). Moreover, it requires a three-wire dc supply. On the other hand, the single phase full-bridge inverter configuration is suitable for high power applications. Besides, the configuration is suitable for PWM techniques which require zero-voltage intervals at the inverter output.

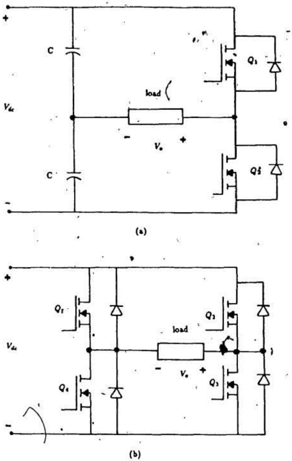


Figure 3.1: Single phase UPS inverter topologies: (a) half bridge inverter, (b) full bridge inverter

3.1.2 UPS Inverter Switching Schemes

Two switching schemes which are frequently employed in static pulse width modulated inverters are:

- The unipolar switching scheme.
- The bipolar switching scheme.

The basic features and the suitability of each switching scheme for delta modulated UPS inverter applications are discussed.

1. **The Unipolar Switching Scheme**

   In this switching scheme, shown in Fig. 3.2, the positive pulses of the modulator output during the positive half-cycle of the reference signal appear at the inverter output, while the negative pulses are replaced by zero-voltage intervals. During the negative half-cycle of the reference signal, the negative pulses appear at the inverter output while the positive pulses are replaced by zero-voltage intervals.

   The unipolar switching scheme can be implemented only in the full-bridge inverter configuration, since zero-voltage intervals at the inverter output are only achievable in this configuration. Zero-voltage intervals are practically implemented by turning on either Q1 and Q2 or Q3 and Q4 simultaneously. Figures 3.2b and 3.2c show the inverter output waveform and the sequence of the gating signals for the inverter switching devices respectively.

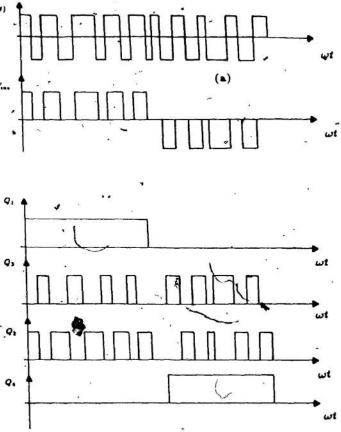


Figure 3.2: Ideal waveforms of the unipolar switching scheme: (a) Modulator output, (b) Sequence of the gating signals for the inverter switching devices

2. **The Bipolar Switching Scheme**

Figure 3.3 shows the inverter output waveform along with the sequence of the gating signals of the inverter switching devices for the bipolar switching scheme.

In this switching scheme, the inverter output waveform is a replica of the modulator binary output. The bipolar switching scheme can be implemented in both the half-bridge and full- bridge inverter configurations.

From the above discussion, it can be seen that the unipolar switching scheme requires more control circuitry to generate the gating signals for the control of the switching devices in the inverter compared to that needed in the case of the bipolar switching scheme. However, the bipolar switching scheme is susceptible to bus-shoot-through fault if a minimum dwell time is not provided between the positive and negative pulses.

3.2 Frequency Spectrum of the Output Voltage of the Delta Modulated Inverter

To determine the suitability of the aforementioned switching schemes for delta modulated UPS inverters, the frequency spectrum of the inverter output voltage with resistive load is examined for each switching scheme. The DFT technique described in section 2.4.2 is used to obtain the frequency spectrum of the inverter output voltage. The effect of various modulator parameters on the inverter output frequency spectrum is investigated for each switching scheme.

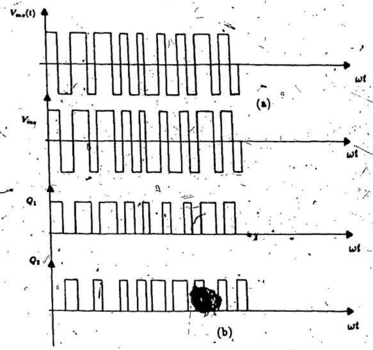


Figure 3.3: Ideal waveforms of the bipolar switching scheme: (a) Modulator output, (b) Sequence of the gating signals for the inverter switching devices

3.2.1 Frequency Spectrum of the Unipolar Switching Scheme

Figure 3.4 shows the frequency spectrum of the inverter output voltage for the unipolar switching scheme for various modulator parameters. The following are observed:

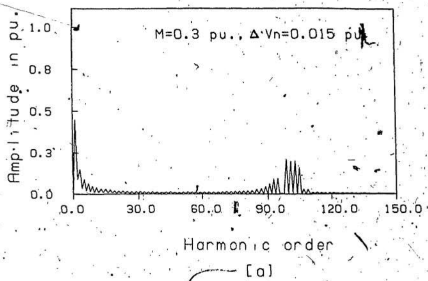
1. Significant amplitude of the low order harmonics (2nd, 3rd, 4th and 5th) are present in the inverter output voltage. The presence of the high amplitude, low order harmonics would require a fairly large filter size at the inverter output to produce a load voltage waveform with acceptable total harmonic distortion.

2. Increasing the value of ΔV decreases the order of the dominant harmonic and vice versa. However, variation in ΔV has a negligible effect on the amplitude of the fundamental component and the amplitudes of the low order harmonics (2nd, 3rd, 4th and 5th) of the inverter output voltage.

3. Although variations in the slope of the carrier wave affect both the order and the amplitude of the dominant harmonic, it has negligible effect on the amplitude and the order of the low order harmonics in the inverter output frequency spectrum.

3.2.2 Frequency Spectrum of the Bipolar Switching Scheme

Figure 3.5 shows the effect of changing the modulator parameters on the frequency spectrum of the inverter output voltage for the bipolar switching scheme. Neglecting the dwell time between the positive and the negative pulses of the inverter output results in an inverter output voltage which is a replica of the



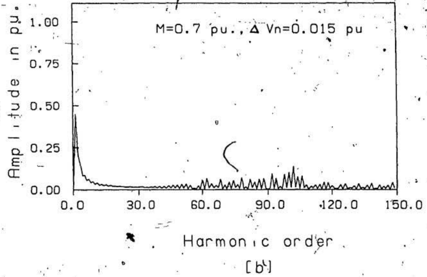
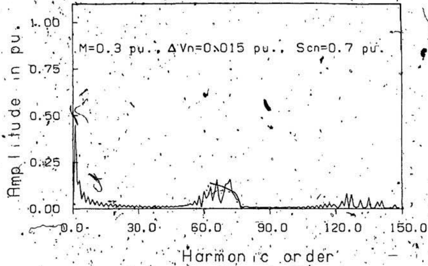


Figure 3.4: Effect of various modulator parameters on the frequency spectrum of the inverter output voltage for the unipolar switching scheme, S_{cn} =1.0 pu.



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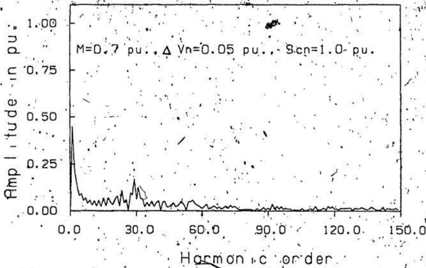


[d]

Fig. 3.4 (continued): Effect of various modulator parameters on the frequency spectrum of the inverter output voltage for the unipolar switching scheme modulator output voltage. Hence, the discussions of subsections 2.5.3, 2.5.4 and 2.5.5 would apply to the inverter output voltage.

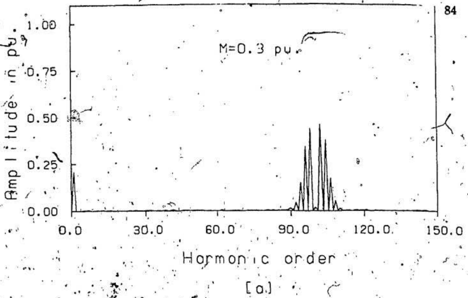
3.2.3 Selection of Inverter Switching Scheme and Inverter Configuration

Table 3.1 summarizes the main features of the unipolar and bipolar switching schemes. Referring to Table 3.1, it can be concluded that the delta modulated unipolar switching scheme is unsuitable for UPS applications for the following reasons:

1. The size of the load filter required to attenuate the undesired harmonics is large. This is due to the presence of the high amplitude of the low order harmonics in the inverter output voltage. As a result, system size becomes bulkier and its efficiency decreases.

2. A load filter with low series inductor is not recommended with this kind of switching scheme. In this case, the high amplitude of the low order harmonics will burden the supply and exert significant stresses on the switching devices.

Table 3.1 also shows that the bipolar switching scheme exhibits good characteristics which are desirable for UPS applications. The reduced amplitude of the low order harmonics implies that the filter size required to attenuate the high order harmonics is small. Besides, small filter series inductor size leads to improved voltage regulation. In UPS applications, where it is necessary to provide a means whereby the load voltage can be independently controlled, the bipolar scheme



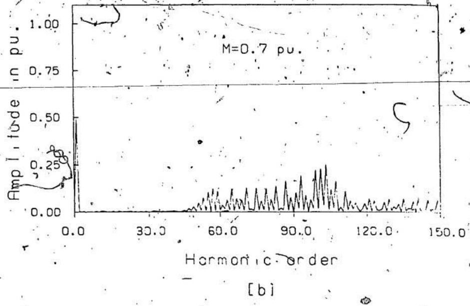
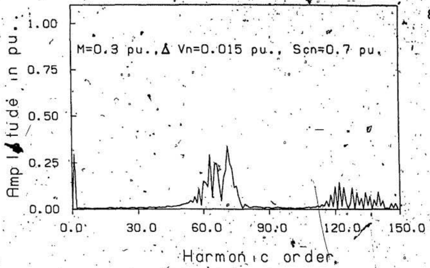


Figure 3.5: Effect of various modulator parameters on the frequency spectrum of the inverter output voltage for the bipolar switching scheme, S_c=1.0 pu., ΔV=0.015 pu



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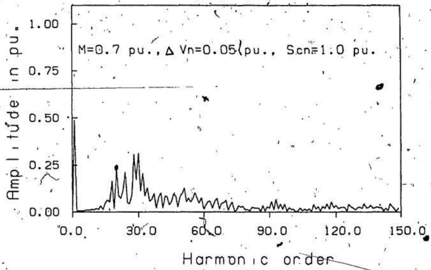


[d]

Fig. 3.5 (continued): Effect of various modulator parameters on the frequency spectrum of the bipolar switching scheme

Table 3.1 Summary of the main features of the unipolar and bipolar switching schemes

	Unipolar switching scheme	Bipolar switching scheme
Low order harmonics	Present High amplitude Not variable	Present Negligible amplitude Variable
Dominant harmonics	Can be controlled by ΔV or S_c	Can be controlled by ΔV, S_c.
Ease of implementation	Requires complex circuitry to generate the required gating signals for the switching devices	Simple control circuitry

allows output voltage control through the variation of the modulation index. In the present work, the bipolar switching scheme is used to investigate the basic characteristics of the single phase delta modulated UPS inverter. The single phase half-bridge inverter configuration is chosen for the practical implementation of the delta modulated single phase UPS inverter because of its relatively simple control circuit and high efficiency.

3.3 Performance Evaluation of the Single Phase Delta Modulated UPS Inverter With a Resistive Load

In addition to the harmonic attenuation characteristics of the delta modulation process, the two performance variables which determine the effectiveness of the delta modulation technique for UPS inverter applications are:

- The voltage utilization ratio VUR.
- The inverter switching frequency F_s.

In this section, the significance of the two variables in UPS inverters and the effect of various modulator parameters on the variables are discussed.

3.3.1 Effect of Various Modulator Parameters on the Voltage Utilization Ratio

Voltage utilization ratio is defined as the ratio of the rms value of the inverter fundamental output voltage, V_{o1} to the dc supply voltage, V_{dc}. Thus if the level of the dc supply voltage is chosen as the base value for the voltages in the power sub-circuit of the inverter, the voltage utilization ratio (VUR) may be expressed as

$$VUR = V_{o1} \qquad pu. \tag{3.1}$$

In general, high values of VUR imply that the inverter dc voltage is being used effectively, and the stresses on the power switching devices are reduced. Consequently, the inverter derating factor is reduced, system efficiency is improved and the cost of the inverter system is reduced. Equation 2.43 gives the relationship between the peak value of the fundamental component of the modulator output and the modulator parameters. Since the inverter output voltage waveform is a replica of the modulator output (for the bipolar switching scheme), equation 2.43 represents the relationship between the inverter output voltage and the modulator parameters. Hence the voltage utilization ratio is given by:

$$VUR = V_{o1} = \frac{M}{\sqrt{2}S_{cn}} \qquad pu. \tag{3.2}$$

Figure 3.6 shows the relationship between the VUR and the modulator parameters. The figure shows that the VUR is determined primarily by the modulation index M, and the slope of the carrier wave, S_{cn} in the modulator circuit. Figure 3.6 shows that the ideal maximum value of the voltage utilization ratio is 0.707 pu. Equation 3.2 shows that although small values of the slope of the carrier wave result in higher voltage utilization ratio, they lead to slope overload condition if higher values of the modulation index are used for the delta modulated inverter. Hence, in general, higher values of voltage utilization ratio are achieved at higher values of the ratio of M to S_{cn}.

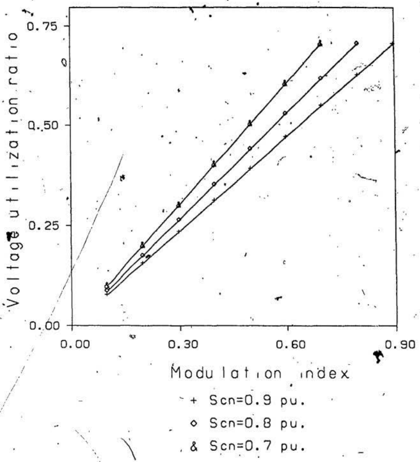


Figure 3.6: Ideal Voltage utilization ratio of the single phase delta modulated inverter

3.3.2 Effect of Modulator Parameters on the Inverter Switching Frequency

The inverter switching frequency plays a significant role in determining the inverter efficiency. High inverter switching frequency increases the switching losses in the inverter and hence causes a reduction in the inverter efficiency. On the other hand, high inverter switching frequency results in the dominant harmonic component in the inverter output voltage being shifted to higher frequencies. The use of power MOSFETs in the inverter circuit significantly reduces the inverter switching losses.

Figure 3.7 shows the effect of various modulator parameters on the inverter average switching frequency and hence the inverter losses. The figure shows that:

1. The inverter switching frequency increases with decreasing values of the modulation index. The maximum switching frequency occurs when the value of the modulation index reaches zero. In this condition, the maximum switching frequency is

$$F_{max} = \frac{S_c}{4\Delta V} \tag{3.3}$$

The minimum switching frequency that the inverter can have is equal to the reference signal frequency when the square wave mode of operation takes place in the modulator circuit.

2. The inverter switching frequency increases with increasing values of the slope of the carrier wave and decreasing values of the hysteresis bandwidth.

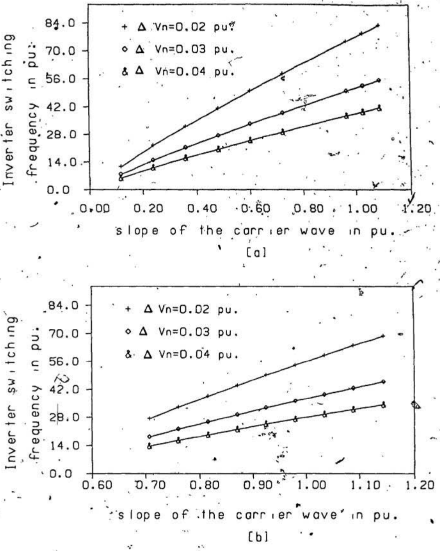


Figure 3.7: Effect of various modulator parameters on the average switching frequency of the single phase delta modulated inverter: (a) M=0.3, (b) M=0.7

3.4 Experimental Verification of the Delta Modulated UPS Inverter with a Resistive Load

To ascertain the validity of the predicted performance characteristics of the delta modulated UPS inverter, a 1 KVA prototype single phase, half-bridge delta modulated inverter was constructed and used to obtain the experimental results. In this section, various values involved in the practical inverter power circuit and the logic control circuit are discussed. Selected predicted results with a resistive load are experimentally verified and computer simulation of the inverter output frequency spectra along with experimentally obtained spectra are presented.

3.4.1 Practical Implementation of the Logic and Inverter Circuits

To successfully implement the bipolar switching scheme in the delta modulated UPS inverter, the inverter output voltage should be as close to the modulator output waveform as possible. However, to avoid bus-shoot through fault a minimum dwell time must be provided when switching from the upper to the lower switching device shown in Fig. 3.1a. To meet the above conditions, the inverter switching devices should be fast acting. Power MOSFETs possess all the characteristics required for the switching devices to be used in the delta modulated UPS inverter. In the present work IRF 450 devices are used as the inverter switching devices and a dwell time of $5\mu s$ is provided. The timing diagram and the block diagram of the logic circuit are given in figures C.2 and C.3 in Appendix C.

3.4.2 Computer Simulation and Experimental Verification

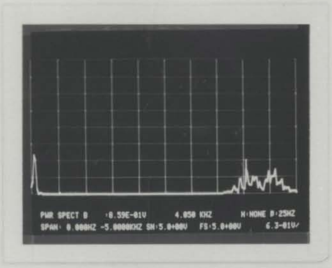
The computer simulation results were obtained by making the following assumptions.

1. The switching devices are ideal.
2. The dc source and the isolating transformer are ideal.
3. The dwell time provided between the positive and negative pulses is neglected.

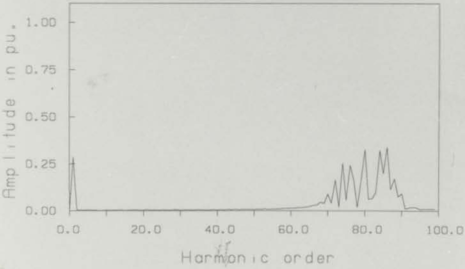
Experimental and computer simulated results of the inverter output voltage showing the effect of various modulator parameters on the frequency spectrum of the inverter output voltage are shown in figures 3.8 to 3.10. The figures confirm the dependance of the dominant harmonic components and the voltage utilization ratio of the inverter output voltage on the modulator parameters.

The discrepancies between the results of the computer simulation and of the experiment arise due to the following reasons:

1. Imperfections in the modulator practical circuit and inaccuracies in the measurements of the modulator practical circuit components and hence, modulator parameters.
2. Spectral leakage due to the use of DFT in obtaining the inverter output frequency spectrum. Spectral leakage can be minimized using windowing techniques [29].



(a)



(b)

Figure 3.8: Frequency spectrum of the inverter output voltage (M=0.4 pu., S_{cn}=1.0 pu., ΔV=0.015 pu.) : (a) Experimental (b) Simulated

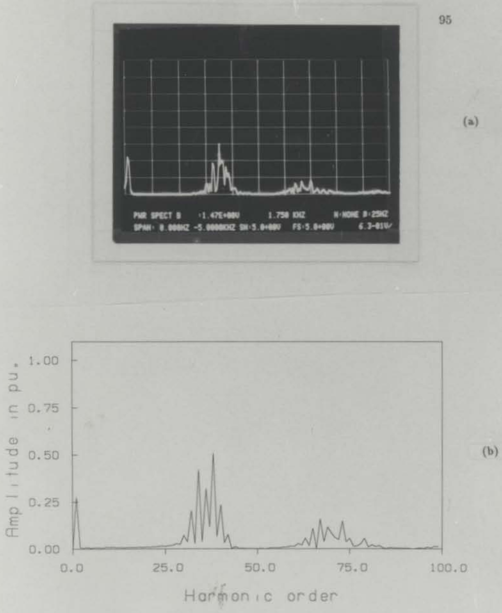
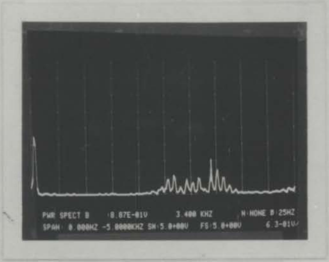
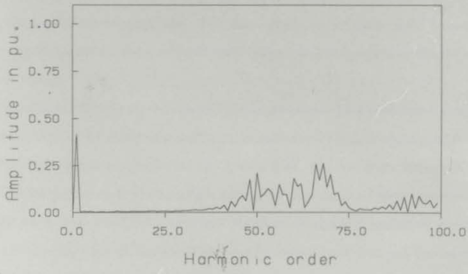


Figure 3.9: Frequency spectrum of the inverter output voltage (M=0.4 pu., S_{cn}=1.0 pu., ΔV=0.04 pu.) : (a) Experimental (b) Simulated





(b)

Figure 3.10: Frequency spectrum of the inverter output voltage (M=0.4 pu., S_c=0.78 pu., ΔV=0.015 pu.) : (a) Experimental (b) Simulated

Chapter 4

THE SINGLE PHASE DELTA MODULATED UPS INVERTER WITH LOAD FILTERS

Static UPS inverters employ load filters to further reduce the harmonic content of the inverter output voltage and produce load voltage with acceptable level of total harmonic distortion (THD). The filter should be efficient, light in weight and produce minimum attenuation of the fundamental component of the inverter output voltage.

This chapter focuses on the analysis of a single phase delta modulated inverter with load filters. A variety of load filter configurations which are commonly used in UPS applications are presented along with their main features. Based on the characteristics of various filter configurations, two types of load filters are selected for the delta modulated UPS inverter. Harmonic analysis of load filter currents and voltages for each of the load filter configuration is carried out for lagging, leading and unity power factor loads. Finally, simulation of the filter voltages and currents with a lagging power factor load is carried out and substantiated with experimental results.

4.1 The UPS Inverter Load Filter

Various types of load filters are examined to determine their suitability for delta modulated UPS inverters. The filter configurations and their basic features are qualitatively described. The main performance measures upon which the load filter of the uninterruptible power supply is selected is briefly outlined.

4.1.1 UPS Load Filter Configurations

Figure 4.1a shows the second order L-C filter. The load is connected across C_1 which provides a path for the harmonics in the inverter output voltage. The main features of this filter are its simplicity and high efficiency for linear loads.

Figure 4.1b shows the tank circuit filter. It consists of a series inductor L_1 and a parallel or tank circuit formed by C_1 and L_2. The tank circuit is tuned at the fundamental frequency of the inverter output voltage, so that irrespective of the the harmonic components in the inverter output and the type of load, the load voltage remains fairly sinusoidal. Thus the filter is capable of providing stable output voltage for both linear and nonlinear loads. In addition, the filter provides short transient suppression through the tank capacitor C_1. The capacitor C_1 is chosen large enough to provide a path for the high frequency components in the inverter output voltage.

The tank filter has the disadvantage of attenuating the fundamental component of the inverter output voltage. To keep this reduction at a low level, the series inductor of the filter, L_1, is chosen to be at a reasonably small value.

Figure 4.1c shows the fourth order tuned series-parallel filter. L_1-C_1 are tuned at the fundamental frequency. As a result, the filter ideally provides no attenu-

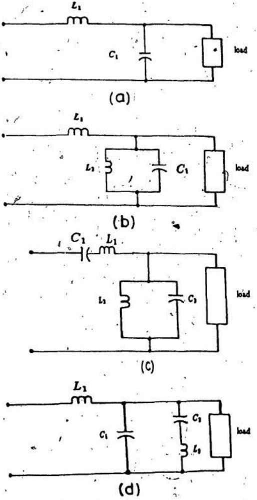


Figure 4.1: UPS load filter configurations: (a) Second order L-C filter, (b) Tank circuit filter, (c) Series-parallel tuned circuit, (d) Fifth order filter

ation of the fundamental component of the inverter output voltage. $L_2 - C_2$ are tuned at the frequency of the fundamental component to provide a low impedance path for higher-order harmonics contained in the inverter output voltage. However, unlike the tank circuit filter, shown in Fig. 4.1b, this filter creates instabilities in the load voltage in the case of non-linear dynamic loads. This is due to the interaction between the load and the series $L_1 - C_1$ circuit.

Figure 4.1d shows the fifth order filter. In this filter $L_2 - C_2$ are tuned at the frequency of the dominant harmonic in the inverter output voltage, so as to trap the higher order harmonics. The main disadvantage of this filter is that its filtering ability is a function of the load. Besides, its filtering performance is strongly related to the switching pattern of the inverter output voltage. Hence, the filter is not suitable for any modulation or switching scheme which produces variation in the order of the dominant harmonic, since this would require that the series $L_2 - C_2$ circuit be tuned at different frequencies.

Based on the basic features of the various filter configurations, it is found that the second order L-C and the tank filter circuits possess good characteristics which make them suitable for delta modulated UPS inverters. The second order L-C filter is simple and has high efficiency for linear loads. The two filter configurations are therefore employed to investigate the performance of the single phase delta modulated UPS inverter with various types of loads.

4.1.2 Performance evaluation of the UPS Inverter Load Filter

The main criteria upon which the load filter of the uninterruptible power supply inverter is selected are:

- The total harmonic distortion of the load voltage.
- The filter rating and efficiency.
- The attenuation level of the fundamental component of the inverter output voltage.

The total harmonic distortion (THD) of the load voltage is a measure of how close the load voltage waveform is to a sine wave. The lower the value of the total harmonic distortion of the load voltage the closer the load voltage waveform is to a sine wave and vice versa.

In the analysis which follows, the total harmonic distortion (THD) of the load voltage waveform is defined as

$$THD\% = \frac{100}{V_{L1}} \sqrt{\sum_{n=2}^{\infty} V_{Ln}^2} \tag{4.1}$$

where V_{Ln} is the rms value of the nth harmonic component of the load voltage.

V_{L1} is the rms value of the fundamental component of the load voltage.

n is the harmonic order.

In common practice, the load voltage is required to have a THD less than 5%.

In most UPS applications, systems of compact size are desirable. Since the load filter size contributes to the overall size of the system, a load filter with a small size and low rating is desirable. A load filter with low rating value indicates higher filter efficiency.

The load filter should provide the least possible attenuation of the fundamental component of the inverter output voltage and hence efficient utilization of the dc supply voltage level.

4.1.3 Assumptions

The analysis of the delta modulated inverter with loaded filters is carried out using the following assumptions:

1. The load is assumed to be equal to 1 pu impedance at the fundamental frequency.
2. The load voltage level of the dc supply is chosen as the base voltage and is assumed to be equal to 1 pu. voltage.
3. The load power factor is assumed to vary from 0.8 lagging to 0.8 leading.
4. The inverter output voltage waveform (filter input) is ideal.
5. The load transformer is assumed to be ideal and the effect of its leakage inductance on the inverter output frequency spectrum is included in the filter series inductor.

4.2 Analysis of The Single Phase Delta Modulated UPS Inverter with an L-C Load Filter

Harmonic analysis of the L-C load filter for delta modulated UPS inverters is carried out in this section. Expressions for the filter currents, and voltages are derived for lagging, unity and leading power factor loads.

4.2.1 Transfer Characteristic of the L-C Filter

Figure 4.1a shows the circuit diagram of the second order loaded L-C filter. The filter transfer characteristic with lagging power factor load is given by:

$$\frac{\overline{V}_{Ln}}{\overline{V}_{in}} = \frac{R_L + jnX_{LL1}}{R_L(1 - n^2\frac{X_{L1}}{X_{c1}}) + R_1(1 - n^2\frac{X_{L1}}{X_{c1}}) + jn[X_{L1} + \frac{R_1 R_{L1}}{X_{c1}} + X_{LL1}(1 - n^2\frac{X_{L1}}{X_{c1}})]} \tag{4.2}$$

where R_L is the resistive component of the load.

X_{LL1} is the inductive reactance of the load at the fundamental frequency of the inverter.

X_{c1} is the capacitive reactance of the filter shunt capacitor at the fundamental frequency of the inverter output.

X_{L1} is the inductive reactance of the filter series inductor at the fundamental frequency.

R_1 is the resistive component of the filter series inductor.

n is the harmonic order.

On the assumption that R_1 is negligibly small, equation 4.2 can be expressed as:

$$\frac{\overline{V}_{Ln}}{\overline{V}_{on}} = \frac{R_L + jnX_{LL1}}{R_L(1 - n^2)\frac{X_{L1}}{X_{c1}} + jn[X_{L1} + X_{LL1}(1 - n^2\frac{X_{L1}}{X_{c1}})]} \tag{4.3}$$

Equation 4.3 can be rewritten as:

$$\frac{\overline{V}_{Ln}}{\overline{V}_{on}} = \frac{R_L + jnX_{LL1}}{(1 - n^2 H_c)(R_L + jnX_{LL1}) + jnX_{L1}} \tag{4.4}$$

or

$$\frac{\overline{V}_{Ln}}{\overline{V}_{on}} = \frac{\cos\theta + jn\sin\theta}{(\cos\theta + jn\sin\theta)(1 - n^2 H_c) + jnX_{L1}} \tag{4.5}$$

where

$$H_c = \frac{X_{L1}}{X_{c1}} = \omega^2 LC \tag{4.6}$$

or

$$H_c = (\frac{\omega}{\omega_0})^2 \tag{4.7}$$

and

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{4.8}$$

where X_{L1} is expressed in pu of the load impedance.

θ is the load angle.

ω is the angular frequency of the fundamental component of the inverter output voltage.

ω_0 is the filter cutoff frequency in rad./sec.

The filter transfer characteristic for a leading power factor load can be derived from equation 4.5 by substituting the reactive component of the load impedance by $-j\frac{\sin\theta}{n}$. The resulting transfer characteristic for a leading power factor load is given by:

$$\frac{\overline{V}_{LCn}}{\overline{V}_{on}} = \frac{\cos\theta - j\frac{\sin\theta}{n}}{(1-n^2H_c)(\cos\theta - j\frac{\sin\theta}{n}) + jnX_{L1}} \tag{4.9}$$

The filter transfer characteristic for a resistive load is obtained by equating $\sin\theta$ and $\cos\theta$ in equation 4.5 to zero and unity respectively. The resulting transfer characteristic is given by:

$$\frac{\overline{V}_{LRn}}{\overline{V}_{on}} = \frac{1}{(1-n^2H_c) + jnX_{L1}} \tag{4.10}$$

Equations 4.5, 4.9 and 4.10 show that for a fixed switching pattern of the inverter output voltage, the filter transfer characteristic varies with the load power factor, filter series inductor and filter shunt capacitor. The expressions given in equations 4.5, 4.9 and 4.10 are employed to examine the effect of the filter parameters on the total harmonic distortion of the load voltage.

Figure 4.2 shows the effect of various filter parameters on the THD of the load voltage, for a fixed pattern of the inverter output voltage. The figure shows that for given values of the filter components, the THD of the load voltage is minimum in the case of capacitive loads, and is higher for inductive loads. The figure also indicates that the THD of the load voltage decreases by either increasing the filter shunt capacitance or the filter series inductance. For the range of shunt capacitance chosen, the figure further shows that in general THD values less than 5% can be achieved in delta modulated UPS inverter with L-C filters

4.2.2 Input Current of the L-C filter

In order to investigate the effect of the filter components on the inverter output current, and obtain the ratings of the filter components, expressions for the input impedance and the input current of the loaded filter are derived.

The filter input impedance with lagging power factor load is given by:

$$\overline{Z}_{iLn} = \frac{(\frac{-jX_{c1}}{n})(R_L + jnX_{LL1})}{R_L + j(nX_{LL1} - \frac{X_{c1}}{n})} + jnX_{L1} \tag{4.11}$$

or

$$\overline{Z}_{iLn} = \frac{X_{c1}[R_L(1 - n^2 H_c) + j(nX_{L1} + nX_{LL1} - n^3 H_c X_{LL1})]}{X_{c1} - n^2 X_{LL1} + jnR_L} \tag{4.12}$$

where H_c is defined in equation 4.6. Expressing the load in terms of the impedance Z_{L1} and load angle θ equation 4.12 may be expressed as:

$$\overline{Z}_{iLn} = \frac{|Z_{L1}|X_{c1}[\cos\theta(1 - n^2 H_c) + j(n\sin\theta + n\frac{X_{L1}}{|Z_{L1}|} - n^3 H_c \sin\theta)]}{|Z_{L1}|(\frac{X_{c1}}{|Z_{L1}|} - n^2 \sin\theta + jn\cos\theta)} \tag{4.13}$$

Normalizing all impedances and reactances to the load impedance, the normalized input impedance of the loaded filter at the nth harmonic is given by:

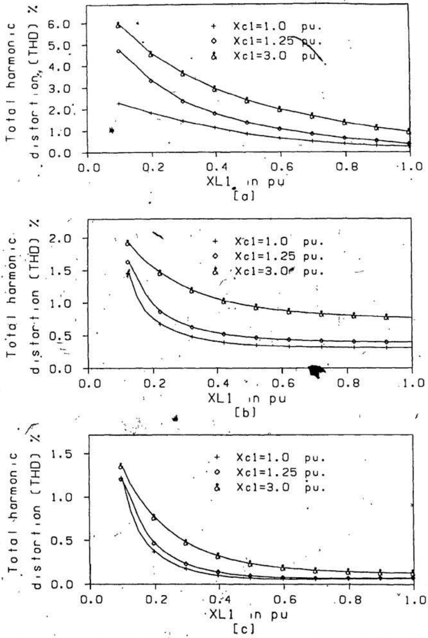


Figure 4.2: Effect of L-C filter parameters on the total harmonic distortion of the load voltage: (a) 0.8 pf lagging load, (b) Unity pf load , (c) 0.8 pf leading load

$$\overline{Z}_{iLn} = \frac{X_{c1}[\cos\theta(1-n^2H_c) + j(n\sin\theta + nX_{L1} - n^3H_c\sin\theta)]}{X_{c1} - n^2\sin\theta + jn\cos\theta} \tag{4.14}$$

where: X_{c1}, X_{L1} and Z_{iLn} are expressed in pu.

The input current of the loaded filter is given by

$$\overline{I}_{iLn} = \frac{\overline{V}_{on}}{\overline{Z}_{iLn}} \tag{4.15}$$

where $\overline{V}_{on}$ is the nth harmonic component of the inverter output voltage (in pu.)

$\overline{I}_{iLn}$ is the nth harmonic component of the input current of the filter with lagging power factor load (in pu.)

The nth harmonic component of the input impedance of the loaded filter with a leading power factor load can be derived from equation 4.12 by substituting the reactive component of the load impedance by $-j\frac{\sin\theta}{n}$. The resulting input impedance of the filter with a leading pf load is given by

$$\overline{Z}_{iCn} = \frac{X_{c1}[\cos\theta(1-n^2H_c) + j(nX_{L1} - n\sin\theta + n^3H_c\sin\theta)]}{X_{c1} + \sin\theta + jn\cos\theta} \tag{4.16}$$

and the filter input current is given by

$$\overline{I}_{iCn} = \frac{\overline{V}_{on}}{\overline{Z}_{icn}} \tag{4.17}$$

where $\overline{I}_{icn}$ is the nth harmonic component of the input filter with a leading power factor load (in pu.)

Finally, the input impedance of the load filter for the case of unity power factor load is obtained by setting the reactive component of the load in equation 4.12 to zero, and $\cos\theta$ to unity. The resulting input impedance is given by

$$\overline{Z}_{iRn} = \frac{X_{c1}(1-n^2H_c) + jnX_{L1}}{X_{c1} + jn} \tag{4.18}$$

and the filter input current is given by:

$$\overline{I}_{iRn} = \frac{\overline{V}_{on}}{\overline{Z}_{irn}} \tag{4.19}$$

where $\overline{I}_{iRn}$ is the nth harmonic component of the filter input current with unity pf load (in pu.)

In delta modulated inverters, the dominant harmonics are shifted to the high order frequencies and the resulting inverter output current with load filter is negligibly small. Hence the inverter output current may be assumed to comprise of mainly of the fundamental component. The fundamental component of the filter input current for the various loads can be obtained by substituting n=1 in equations 4.12 to 4.19.

Figure 4.3 shows the effect of various filter parameters on the fundamental component of the filter input current. The figure shows the following:

1. The fundamental component of the filter input current is highest for leading power factor loads.

2. For a given type of load, the variation of the fundamental component of the filter input current with the filter series inductor is dependent on the value of the filter shunt capacitor. In general, small values of shunt capacitive reactance result in high fundamental filter current.

3. Irrespective of the nature of the load, when the shunt capacitive reactance is 1 pu., the fundamental input current reaches its maximum value at a series inductive reactance of 0.5 pu. The value of the filter series inductive reactance which maximizes the fundamental component of the filter input

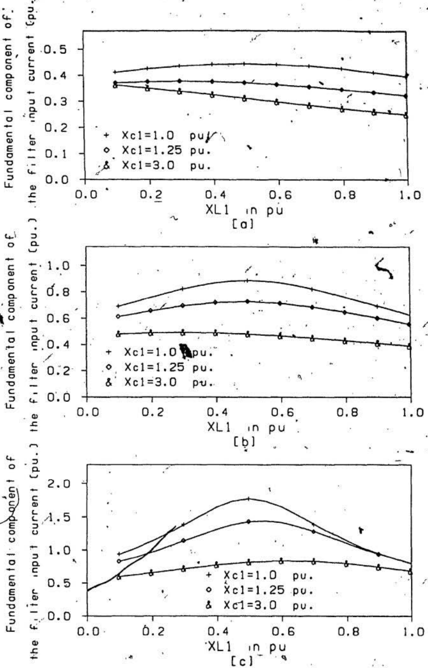


Figure 4.3: Effect of various filter parameters on the fundamental component of the input current of the L-C filter:(a) 0.8 pf lagging load , (b) Unity pf load, (c) 0.8 pf leading load

current can be determined by setting n=1 and obtaining an expression for the minimum value of the resulting expression.

A general expression which gives the value of the series inductive reactance X_{L1} in terms of the the filter shunt capacitive reactance, X_{c1} and the load angle is given by:

$$(\frac{X_{L1}}{\sin\theta} + 1 - \frac{X_{L1}}{X_{c1}})(\frac{X_{c1}}{\sin\theta} - 1) = cot^2\theta(1 - \frac{X_{L1}}{X_{c1}}) \tag{4.20}$$

Equation 4.20 represents a condition at which the maximum value of the fundamental component of the filter input current is produced. The resulting high filter current leads to a significant attenuation of the fundamental component of the inverter output voltage and over-rating of the filter components.

4. Generally, high values of shunt capacitive reactance ($X_{c1} > 1.25pu.$) and small values of series inductive reactance ($X_{L1} < 0.5pu.$) result in acceptable levels of fundamental input current. However, the choice of these components depends on the filter ratings, efficiency and the total harmonic distortion of the load voltage.

4.3 Analysis of the Tank Circuit Filter

The analysis and design of the tank circuit filter for the single phase delta modulated UPS inverter is carried out in this section. Expressions for the filter currents and voltages are derived for lagging, leading, unity power factor loads respectively.

4.3.1 Transfer Characteristic of the Tank Circuit Filter

Figure 4.4a shows the tank circuit filter with a load. The tank circuit components are tuned at the fundamental frequency of the inverter output voltage, so that the tank circuit ideally exhibits an infinite impedance to the fundamental component of the filter input current. Thus the fundamental component of the filter input current is independent of the tank circuit parameters.

Neglecting the small resistance associated with the filter shunt inductor and shunt capacitor, the relationship between the fundamental reactances of the tank circuit is given by

$$X_{21} = X_{c1} = X \tag{4.21}$$

where X_{c1} is the reactance of the filter shunt capacitor at the fundamental frequency of the inverter output voltage,

X_{21} is the reactance of the filter shunt inductor at the inverter fundamental frequency.

The equivalent impedance of the filter tank circuit at the nth harmonic component is given by

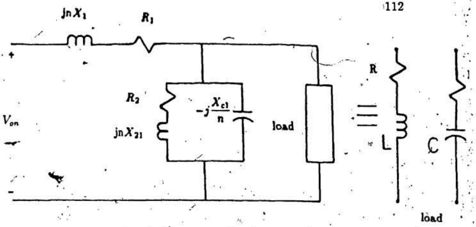
$$\overline{Z}_{tn} = \frac{jnX(\frac{-jX}{n})}{jnX - j\frac{X}{n}} \tag{4.22}$$

or

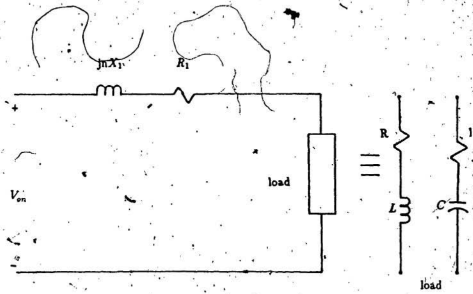
$$\overline{Z}_{tn} = \frac{nX}{j(n^2-1)} \tag{4.23}$$

The equivalent impedance of the parallel combination of the filter tank circuit and the lagging power factor load at the nth harmonic component is given by

$$\overline{Z}_{eqn} = \frac{(R_L + jnX_{LL1})(\frac{nX}{j(n^2-1)})}{R_L + jnX_{LL1} + \frac{nX}{j(n^2-1)}} \tag{4.24}$$



(a)



(b)

Figure 4.4: The tank circuit filter with load: (a) Circuit diagram at the nth harmonic component (b) Circuit diagram at the fundamental frequency of the inverter output voltage

or

$$\overline{Z}_{eqn} = \frac{nX(R_L + jnX_{LL1})}{n(1-n^2)X_{LL1} + nX + j(n^2-1)R_L} \tag{4.25}$$

The filter transfer characteristic is obtained as:

$$\frac{\overline{V}_{Ln}}{\overline{V}_{on}} = \frac{\overline{Z}_{eqn}}{\overline{Z}_{eqn} + jnX_{L1}} \tag{4.26}$$

or

$$\frac{\overline{V}_{Ln}}{\overline{V}_{on}} = \frac{nX(R_L + jnX_{LL1})}{nX(R_L + jnX_{LL1}) + jnX_{L1}[n(1-n^2)X_{LL1} + nX + j(n^2-1)R_L]} \tag{4.27}$$

Rearranging equation 4.27 and expressing the load in terms of its impedance and power factor, gives

$$\frac{\overline{V}_{Ln}}{\overline{V}_{on}} = \frac{X(\cos\theta + jn\sin\theta)}{(\cos\theta + jn\sin\theta)[X + (1-n^2)X_{L1}] + jnXX_{L1}} \tag{4.28}$$

where X is the tank circuit reactance at the fundamental frequency expressed in pu. of the load impedance.

X_{L1} is the series inductor reactance at the fundamental frequency expressed in pu. of the load impedance.

The filter transfer characteristic with a leading power factor load can be derived from equation 4.28 by replacing the reactive component of the load impedance by $-\frac{j\sin\theta}{n}$. The resulting transfer characteristic for a leading power factor is given by

$$\frac{\overline{V}_{oCn}}{\overline{V}_{on}} = \frac{X(\cos\theta - j\frac{\sin\theta}{n})}{(\cos\theta - j\frac{\sin\theta}{n})[X + (1-n^2)X_{L1}] + jnXX_{L1}} \tag{4.29}$$

Similarly, the filter transfer characteristic with a resistive load is obtained by setting the reactive component of the load impedance in equation 4.28 to zero and $\cos\theta$ to unity. The transfer characteristic for resistive load is given by

$$\frac{\overline{V}_{oRn}}{\overline{V}_{on}} = \frac{X}{X + (1-n^2)X_{L1} + jnXX_{L1}} \tag{4.30}$$

Equations 4.28 to 4.30 show that for a fixed switching pattern at the inverter output voltage, the filter transfer characteristic varies with the filter parameters (filter series inductor and tank circuit elements) and the load power factor.

The fundamental component of the load voltage V_{L1} is obtained from equation 4.28 by substituting n=1. The transfer characteristic of the load tank filter circuit with lagging power factor load at the fundamental frequency is given by

$$\frac{\overline{V}_{L1}}{\overline{V}_{o1}} = \frac{\cos\theta + j\sin\theta}{\cos\theta + j(\sin\theta + X_{L1})} \tag{4.31}$$

Equation 4.31 shows that the tank circuit component plays no role in the filter transfer characteristic at the fundamental frequency of the inverter output voltage. It also shows that the filter transfer characteristic is unity when the reactance of the filter series inductor is made very small compared to the load impedance.

The expressions given in equations 4.28 to 4.30 are employed to examine the effect of various filter parameters on the total harmonic distortion of the inverter output voltage. Figure 4.5 shows the effect of various parameters of the tank circuit filter on the THD of the load voltage. The load voltage THD decreases with either increasing the reactance of the filter series inductor or decreasing the reactance of the tank circuit elements. The figure shows that the load voltage THD is lowest for leading power factor loads and highest for lagging power factor loads.

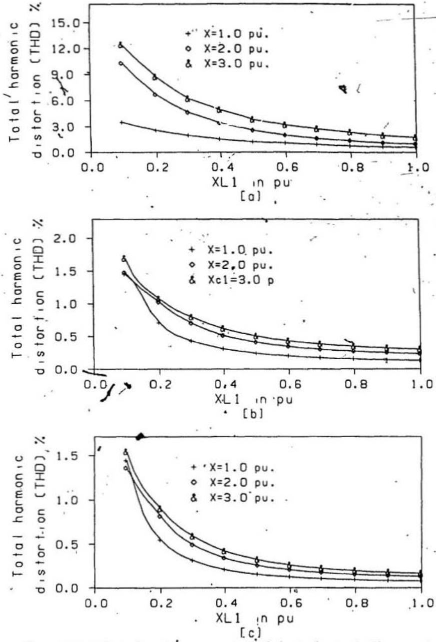


Figure 4.5: Effect of various parameters of the tank circuit filter on the total harmonic distortion of the load voltage: (a) 0.8 pf lagging load, (b) unity pf load, (c) 0.8 pf leading load

4.3.2 Input Current of the Tank Circuit Filter

In order to obtain the VA ratings of the filter components, expressions for the filter input impedance and input current of the loaded filter are derived.

The filter input impedance with a lagging power factor load at the nth harmonic component, $\overline{Z}_{iln}$, is given by

$$\overline{Z}_{iln} = \overline{Z}_{eqn} + jnX_{L1} \tag{4.32}$$

where $\overline{Z}_{eqn}$ is given by equation 4.25.

Substituting equation 4.25 into equation 4.32 and simplifying yields:

$$\overline{Z}_{iln} = \frac{n[X + (1-n^2)X_{L1}](R_L + jnX_{LL1}) + jn^2XX_{L1}}{(1-n^2)(nX_{LL1} - jR_L) + nX} \tag{4.33}$$

Rewriting equation 4.33 in terms of the load power factor results in the normalized input impedance expression given by

$$\overline{Z}_{iln} = \frac{n[X + (1-n^2)X_{L1}](\cos\theta + jn\sin\theta) + jn^2XX_{L1}}{(1-n^2)[n\sin\theta - j\cos\theta] + nX} \tag{4.34}$$

where $\overline{Z}_{iln}$, X, X_{L1} are expressed in pu. of the load impedance.

The nth harmonic component of the filter input current, $\overline{I}_{iln}$ is given by

$$\overline{I}_{iln} = \frac{\overline{V}_{on}}{\overline{Z}_{iln}} \tag{4.35}$$

The filter input impedance at the nth harmonic component with a leading power factor load can be derived from equations 4.24 and 4.34 by replacing the reactive component of the load impedance by $-\frac{j\sin\theta}{n}$ and is given by

$$\overline{Z}_{iCn} = \frac{n[X + (1-n^2)X_{L1}](\cos\theta - \frac{j\sin\theta}{n}) + jn^2XX_{L1}}{(n^2-1)(\frac{\sin\theta}{n} + j\cos\theta) + nX} \tag{4.36}$$

The corresponding filter input current is given by

$$\overline{I}_{iCn} = \frac{\overline{V}_{on}}{\overline{Z}_{iCn}} \tag{4.37}$$

Similarly, the filter input impedance at the nth harmonic component with a resistive load is derived from equation 4.34 by replacing the reactive component of the load with zero and $\cos\theta$ with unity . The resulting expression is given by

$$\overline{Z}_{iRn} = \frac{n[X + (1-n^2)X_{L1}] + jn^2XX_{L1}}{nX + j(n^2-1)} \tag{4.38}$$

and the corresponding filter input current is given by

$$\overline{I}_{iRn} = \frac{\overline{V}_{on}}{\overline{Z}_{iRn}} \tag{4.39}$$

Neglecting the effect of the higher order harmonics, The fundamental component of the filter input current for a lagging power factor load is given by:

$$\overline{I}_{iL1} = \frac{\overline{V}_{o1}}{\cos\theta + j(X_{L1} + \sin\theta)} \tag{4.40}$$

Similarly for a leading power factor load, the fundamental component of the filter input current is given by:

$$\overline{I}_{iC1} = \frac{\overline{V}_{o1}}{\cos\theta + j(X_{L1} - \sin\theta)} \tag{4.41}$$

and for a resistive load, the corresponding expression is given by:

$$\overline{I}_{iR1} = \frac{\overline{V}_{o1}}{1 + jX_{L1}} \tag{4.42}$$

As expected, equations 4.40 to 4.42 show that the fundamental component of the filter input current is independent of the tank circuit parameters . It is determined by the load power factor and the reactance of the filter series inductor. The equations also show that the filter input current is higher for the leading power factor load than that of lagging power load.

4.4 Component Ratings of the Load Filter

The peak and rms values of the current of the filter inductors are the quantities needed to determine the ratings of the inductors, while the peak voltage and rms current are the required quantities for determining the filter capacitor rating.

The nth harmonic component of the filter input current is defined by:

$$\overline{I}_{in} = \frac{\hat{V}_{in}}{|Z_{in}|}(\sin\omega t - \phi_n) \tag{4.43}$$

The peak value of the filter input current can be obtained by computing the sum of the individual harmonic components of the current at various values of ωt and determining the maximum value of the sum as defined by the equation:

$$\hat{I}_{in} = [\sum_{n=1}^{\infty} \frac{\hat{V}_{in}}{|Z_{in}|}(n \sin \omega t - \phi_n)]_{max} \qquad (4.44)$$

The rms value of the filter input current is given by:

$$I_{irms} = \sqrt{\sum_{n=1}^{\infty} I_{inrms}^2} \qquad (4.45)$$

where ϕ_n the phase angle of the filter input current.

I_{inrms} is the rms value of the nth harmonic component of the filter input current.

I_{irms} is the rms value of the total input current to the filter.

The peak voltage across the filter shunt capacitor is given by:

$$\hat{V}_{cp} = \hat{V}_{o1}|TF_1| = \frac{M}{S_{cn}} V_{dc}|TF_1| \qquad (4.46)$$

where $\hat{V}_{cp}$ is the peak voltage of the shunt capacitor

V_{dc} is the dc supply voltage level.

M is the modulation index.

$\hat{V}_{o1}$ is the peak value of the fundamental component of the inverter output voltage.

$|TF_1|$ is the magnitude of the filter transfer characteristics at the fundamental frequency of the inverter output voltage.

The rms value of the filter capacitor current is given by:

$$I_{crms} = \sqrt{\sum_{n=1}^{\infty}(\frac{V_{Lnrms}}{X_{cn}})^2} \tag{4.47}$$

$$X_{cn} = \frac{X_{c1}}{n} \tag{4.48}$$

where X_{cn} is the capacitive reactance of the filter shunt capacitor at the nth harmonic component.

The peak value of the filter shunt inductor current of the tank circuit filter is obtained by computing the sum of the individual harmonic components of the current at various values of ωt and determining the maximum value of the sum as defined by the equation:

$$\hat{I}_{21} = [\frac{\hat{V}_{Ln}}{nX_{21}}\sin(n\omega t - (\theta_n + \frac{\pi}{2}))]_{max} \tag{4.49}$$

where $\hat{I}_{21}$ is the peak value of the filter filter shunt inductor current of the tank circuit filter.

$\hat{V}_{Ln}$ is the peak value of the nth harmonic component of the load voltage.

The ratings of the filter components are given by:

$$X_{L1R} = \sum_{n=1}^{\infty} I^2_{inrms}X_{Ln} \tag{4.50}$$

$$X_{cR} = \sum_{n=1}^{\infty} \frac{V^2_{onrms}}{X_{cn}} \tag{4.51}$$

$$X_{21R} = \sum_{n=1}^{\infty} \frac{V^2_{onrms}}{X_{21n}} \tag{4.52}$$

$$\tag{4.53}$$

where

$$X_{Ln} = nX_{L1} \quad (4.54)$$

$$X_{21n} = nX_{21} \quad (4.55)$$

and X_{L1R} is the rating of the filter series inductor in pu.

X_{cR} is the rating of the filter shunt capacitor in pu.

X_{21R} is the rating of the tank circuit filter shunt inductor in pu.

In practice, the volt-ampere (VA) rating of the filter series inductor is assumed to be twice as expensive as the VA rating of the capacitive reactance. The normalized filter cost (NFC_{LC}) of the L-C filter is given by

$$NFC_{LC} = 2X_{L1R} + X_{cR} \quad (4.56)$$

The normalized filter cost of the tank circuit filter $(NFC_T)$is given:

$$NFC_T = 2(X_{L1r} + X_{21R}) + X_{cr} \quad (4.57)$$

Figure 4.6 shows the effect of various filter parameters on the normalized filter cost of the L-C filter. The figure shows that the normalized filter cost decreases with increasing values of the shunt capacitive reactance, and the filter cost is highest for leading power factor loads. Figure 4.6 shows that the normalized filter cost decreases for increasing values of the filter shunt capacitive reactance. Figure 4.6 also shows that, the normalized filter cost decreases with increasing values of the shunt capacitive reactance. Generally, low values of the normalized filter cost occures for low values of the filter series inductive reactance. The choice of filter parameters is a compromise between the filter ratings and the level of attenuation of the fundamental component of the inverter output voltage.

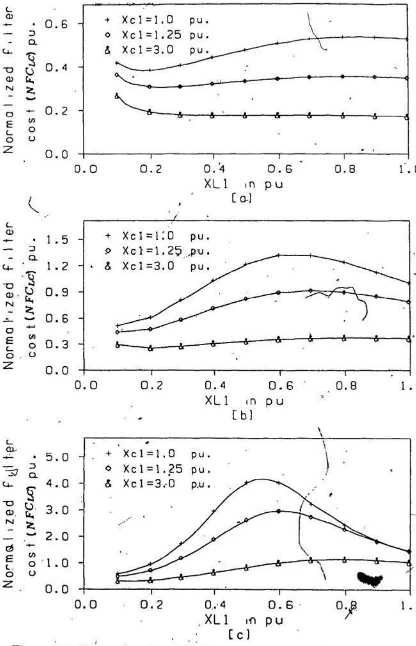


Figure 4.6: Effect of various L-C filter parameters on the normalized filter cost: (a) 0.8 pf lagging load, (b) unity pf load, (c) 0.8 pf leading load

Figure 4.7 shows the effect of various parameters of the tank circuit filter on the normalized filter cost. The figure shows that for both 0.8 pf lagging and unity power factor loads, the normalized filter cost decreases with increasing values of the filter shunt inductive reactance. For leading power factor loads, the NFC attains a minimum value at low values of the filter series inductor, and increases for increasing values of the filter series inductive reactance.

4.5 Computer Simulation and Experimental Verification of the Single Phase Delta Modulated inverter with Load Filters

To validate the analysis presented in the previous sections, computer simulation and experimental verification of the single phase half-bridge delta modulated inverter with load filters is presented. The experimental verification is carried out using the two types of filters previously discussed, namely the L-C filter and tank circuit filter. Since most practical loads are either lagging or resistive loads, the experimental verification is carried out for only these two types of load, to show the effect of various filter components on the UPS system performance. A computer program is developed using standard FORTRAN given in Appendix B to provide computer simulation of the various waveform in the filter circuit for R-L loads. The predicted results are substantiated by experimental results.

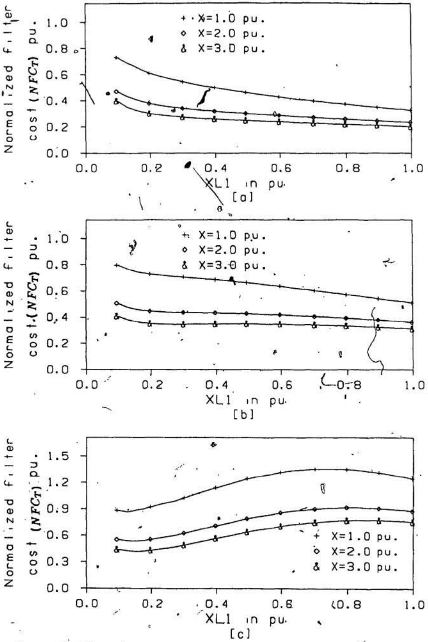


Figure 4.7: Effect of various parameters of the tank circuit filter on the normalized filter cost: (a) 0.8 pf lagging load, (b) Unity pf load, (c) 0.8 pf leading load

4.5.1 Computer Simulation and Experimental Results of the Single Phase Delta Modulated Inverter with L-C Filter.

A 1 kVA laboratory model of the single phase half-bridge delta modulated inverter with an L-C filter was set up. The set-up consisted of the following:

A single phase half-bridge inverter employing power MOSFETs as the inverter switching devices.

Inverter input dc voltage =100 volts.

An L-C load filter.

A load impedance of 9.1 ohm at a load power factor of 0.8 lagging and unity.

Table 4.1 shows the predicted and experimental results, for various filter components values for lagging and unity power factor loads. However, experimental waveforms were obtained at lagging power factor loads only. The modulator parameters at which the results were obtained are: ΔV = 0.18 V (0.018 pu.), V_R = 5.0 V (0.5 pu.) and S_c = 3000.0 V/s. (0.79 pu.).

Figures 4.8 and 4.9 show experimental waveforms of the single phase delta modulated inverter with 0.8 pf lagging load for filter components, L_1=3 mH and C_1=365 μF. Figures 4.10 to 4.12 show the corresponding computer simulation for the experimental results.

Figures 4.13 and 4.14 show the effect of changing the hysteresis bandwidth in the modulator circuit on the load voltage THD, filter input current and capacitor current for the same values of filter component as in figures 4.8 and 4.9. Figures 4.8, 4.9, 4.13 and 4.14 show that for the same VA rating of the load, as ΔV

increases the load voltage THD increases and both the filter input current and the shunt capacitor current increase as well. This result is expected since increasing ΔV shifts the dominant harmonics to lower frequencies, and the filter becomes ineffective in suppressing the undesired harmonics. Figures 4.15 through 4.17 show the computer simulation for the experimental waveforms shown in figure 4.13 and 4.14. The experimental and predicted results show close agreement.

The system efficiency at $L_1 = 3$ mH and $C_1 = 365\mu$F was measured to be 78 %. Since the inverter is operated at a low output power, it is expected that the system efficiency will be higher at higher output powers.

Table 4.1 Experimental and predicted results of the single phase half-bridge delta modulated inverters with L-C filters
ΔV=0.18 V (0.018 pu.), V_R = 5.0 (0.5 pu.), S_c=3000 V/s (0.79 pu.)
[a] for R-L loads, [b] for Resistive loads

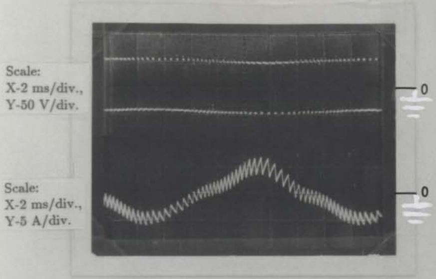
	Experimental results					Predicted results				
	I_{in1} Amps	V_l Volts	I_l Amps	THD %	V_{nl}	I_{in1} Amps	V_l Volts	I_l Amps	THD %	V_{nl}
$L_1 = 3mH$ $C_1 = 365\mu F$	2.7	22.6	2.5	3.2	28.2	2.8	24.0	2.6	2.9	26.0
$L_1 = 3mH$ $C_1 = 116\mu F$	1.9	20.4	2.3	11.5	26.0	1.9	21.4	2.35	13.8	23.0
$L_1 = 10.8mH$ $C_1 = 365\mu F$	3.0	25.3	2.9	0.75	53.0	3.3	28.6	3.1	0.5	49.5
$L_1 = 10.8mH$ $C_1 = 116\mu F$	1.7	18.6	2.1	3.5	31.9	1.7	19.2	2.1	3.1	26.9

[a]

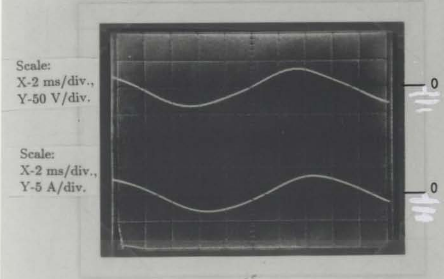
	Experimental results					Predicted results				
	I_{in1} Amps	V_l Volts	I_l Amps	THD %	V_{nl}	I_{in1} Amps	V_l Volts	I_l Amps	THD %	V_{nl}
$L_1 = 3mH$ $C_1 = 365\mu F$	4.4	23.3	2.7	2.7	28.2	4.8	26.1	2.9	1.4	26.0
$L_1 = 3mH$ $C_1 = 116\mu F$	2.60	21.3	2.41	4.8	26.1	2.8	23.0	2.6	2.6	23.0
$L_1 = 10.8mH$ $C_1 = 365\mu F$	5.1	26.3	3.2	1.2	53.0	5.5	32.5	3.7	0.3	49.5
$L_1 = 10.8mH$ $C_1 = 365\mu F$	2.6	21.1	2.4	1.2	31.9	2.9	23.5	2.7	0.8	26.9

[b]

I_{in1} : Fundamental component of the filter input current
V_l : Load voltage
I_l : Load Current
V_{nl} : No load voltage

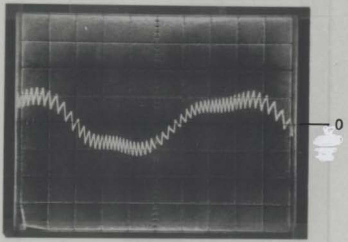


(a)



(b)

Figure 4.8: Experimental waveforms in the single phase delta modulated inverter with L-C filter and 0.8 pf lagging load: (a)Upper trace:filter input voltage, Lower trace:filter input current, (b) Upper trace:load voltage, Lower trace:load current, Modulator parameters: ΔV =0.18 Volt, V_R=5.0 Volt, S_c=3000 Volt/sec.



Scale:
X-2 ms/div.,
Y-5 A/div.

Figure 4.9: Experimental waveform of the capacitor current of the single phase delta modulated inverter with an L-C filter and 0.8 pf lagging load. Modulator parameters:ΔV=0.18 Volt, V_R=5.0 Volts, S_c=3000 Volt/sec

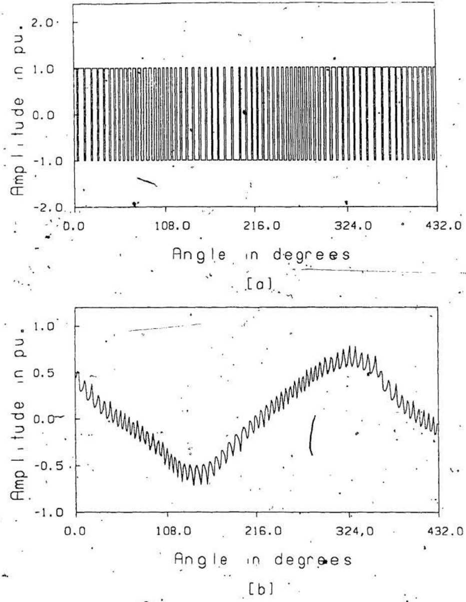
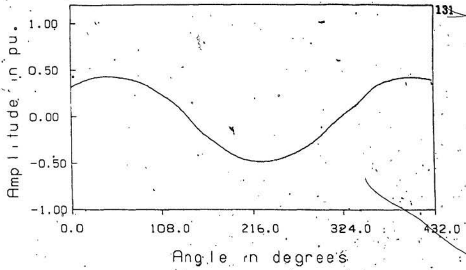
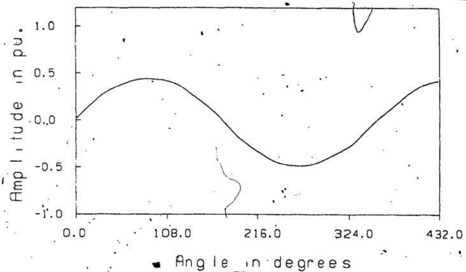


Figure 4.10: Simulated waveforms of the input voltage and input current in the single phase delta modulated inverter with an L-C filter and 0.8 pf lagging load: (a) Filter input voltage (b) Filter input current. Modulator parameters: ΔV=0.18 Volt, V_R=5.0 Volts, S_c=3000 Volt/sec



[a]



[b]

Figure 4.11: Simulated waveforms in the single phase delta modulated inverter with an L-C filter and 0.8 pf lagging load: (a) Load voltage (b) Load current. Modulator parameters: ΔV=0.18 Volt, V_R=5.0 Volts, S_c=3000 Volt/sec

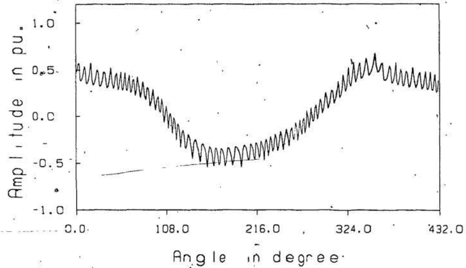


Figure 4.12: Simulated waveforms of the filter capacitor current in the single phase delta modulated inverter with an L-C filter and 0.8 pf lagging load. Modulator parameters: $\Delta V=0.18$ Volt, $V_R=5.0$ Volts, $S_c=3000$ Volt/sec

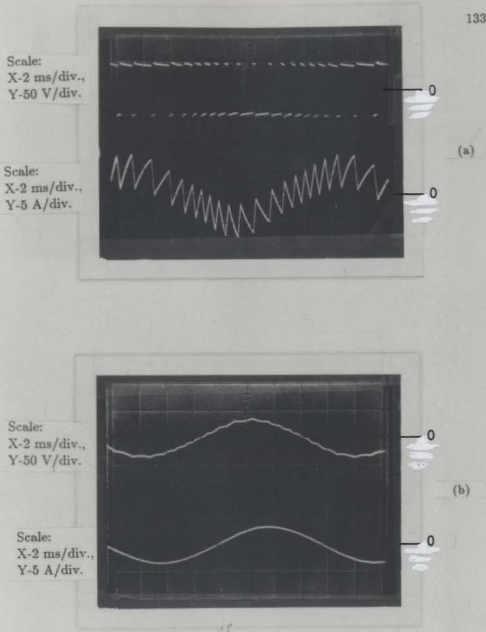
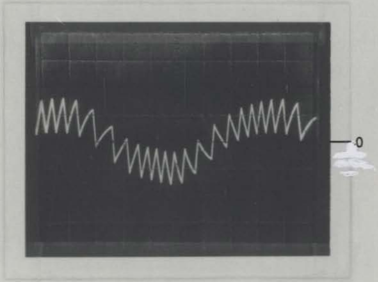


Figure 4.13: Experimental waveforms in the single phase delta modulated inverter with L-C filter and 0.8 pf lagging load: (a)Upper trace:filter input voltage, Lower trace:filter input current (b) Upper trace:load voltage, Lower trace:load current. Modulator parameters:ΔV=0.5 volt, V_R=5.0 volt, S_c=3000 V/sec.



Scale:
X-2 ms/div.,
Y-5 A/div.

Figure 4.14: Experimental waveform of capacitor current of the L-C filter and 0.8 pf lagging. Modulator parameters: ΔV=0.5 volt, V_R =5.0 volts, S_c=3000 volt/sec

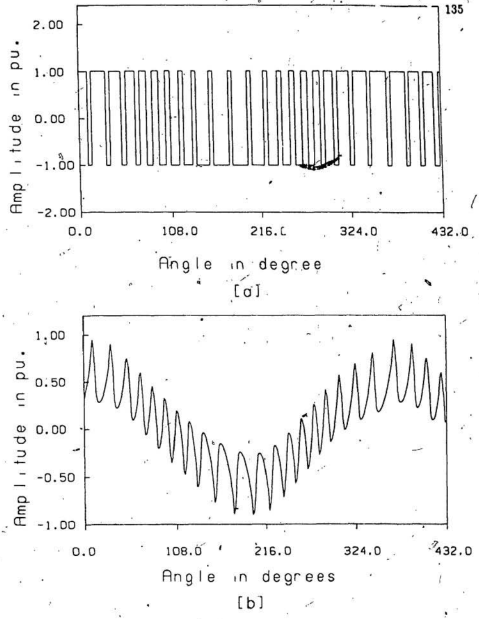
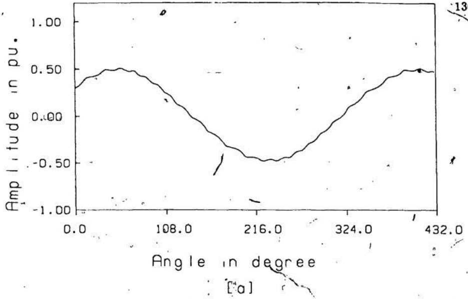


Figure 4.15: Simulated waveforms in the single phase delta modulated inverter with an L-C filter and 0.8 pf lagging load: (a) Filter input voltage (b) Filter input current. Modulator parameters: ΔV=0.5 volt, V_R=5.0 volts, S_c=3000 volt/sec



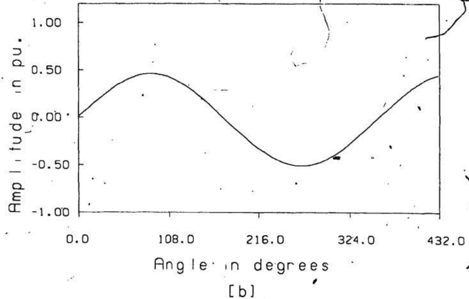


Figure 4.16: Simulated waveforms in the single phase delta modulated inverter with an L-C filter and 0.8 pf lagging load: (a) Load voltage (b) Load current. Modulator parameters: ΔV=0.5 volt, V_R=5.0 volts, S_c=3000 volt/sec

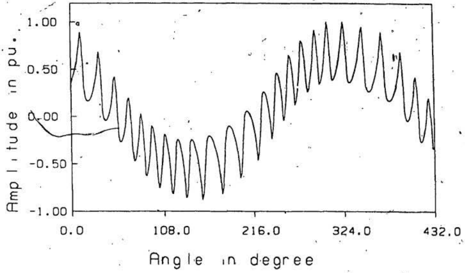


Figure 4.17: Simulated waveforms of the filter shunt capacitor current in the single phase delta modulated inverter with an L-C filter and 0.8 pf lagging load. Modulator parameters: ΔV=0.5 volt, V_R=5.0 volts, S_c=3000 volt/sec

4.5.2 Computer Simulation and Experimental Results of the Single Phase Delta Modulated Inverter with Tank Circuit Filter.

The L-C filter in the experimental setup described in subsection 4.4.1 is replaced with a tank circuit filter. Table 4.2 shows the experimental and predicted results of the tank circuit filter at various values of filter parameters. The results are obtained at the following modulator parameters: $\Delta V = 0.18$ Volts (0.018 pu.), $V_R = 5.0$ Volts (0.5 pu) and $S_c = 3000.0$ V/s. (0.79 pu). The discrepancies between the predicted and experimental results are due to the difficulty of obtaining exact tuning of the filter tank circuit component at the fundamental frequency.

Figures 4.18 and 4.19 show experimental waveforms of the single phase delta modulated inverter with a tank circuit filter and 0.8 pf lagging. Figures 4.20 through 4.22 show the corresponding computer simulation of the experimental waveforms shown in figures 4.18 and 4.19.

The effect of increasing the value of the hysteresis bandwidth $\Delta V = 0.5$ Volts (0 05 pu), in the modulator circuit on the filter performance is shown in figures 4.23 and 4.24. Figure 4.23b shows that for larger value of ΔV, the THD of load voltage increases for the same filter component values shown in figure 4.18 and 4.19. The amplitudes of the filter input current, filter shunt capacitor current and filter shunt inductor current also increase. Figures 4.25 through 4.27 are the simulated waveform of the experimental results shown in figure 4.23 and 4.24.

Table 4.2 Expermintal verification and predicted results of the half-bridge single phase delta modulated invertor with tank circuit filter
[a] For R-L loads, [b] Resistive loads
ΔV=0.18 V (0.018 pu.), V_R = 5.0 (0.5 pu.), S_c=3000 V/s (0.79 pu.)

	Experimental results					Predicted results				
	I_{in1} Amps	V_l Volts	I_l Amps	THD %	V_{nl}	I_{in1} Amps	V_l Volts	I_l Amps	THD %	V_{nl}
$L_1 = 1mH$ $X = 9.1\Omega$	2.1	21.3	2.4	9	24.7	2.4	21.5	2.4	9.5	22
$L_1 = 5mH$ $X = 9.1\Omega$	1.7	16.8	1.9	3.7	26.8	2.1	19	2.1	2.3	22

[a]

	Experimental results					Predicted results				
	I_{in1} Amps	V_l Volts	I_l Amps	THD %	V_{nl}	I_{in1} Amps	V_l Volts	I_l Amps	THD %	V_{nl}
$L_1 = 1mH$ $X = 9.1\Omega$	2.5	20.8	2.3	4.8	25.3	2.4	22	2.4	4.4	22.1
$L_1 = 1mH$ $X = 9.1\Omega$	2.3	19.6	2.1	2.4	26.2	2.4	21.5	2.4	1.3	22.9

[b]

I_{in1}: Fundamental component of the filter input current
V_l: Load voltage
I_l: Load Current
V_{nl}: No load voltage
X: Capacitive or inductive reactance of the tank circuit component

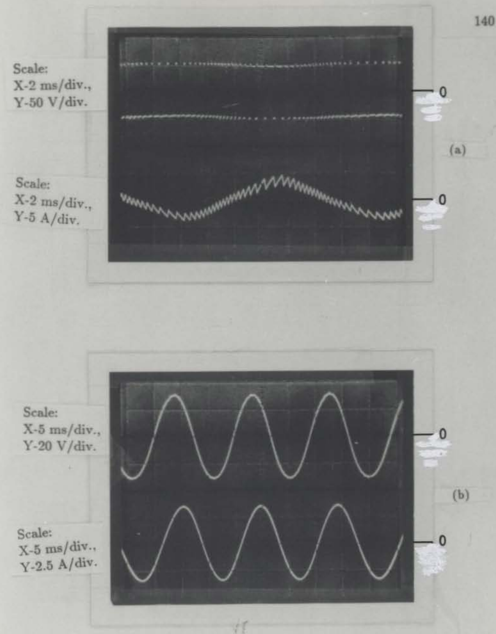
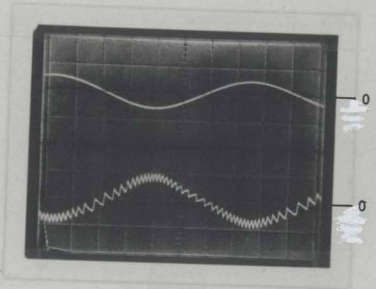
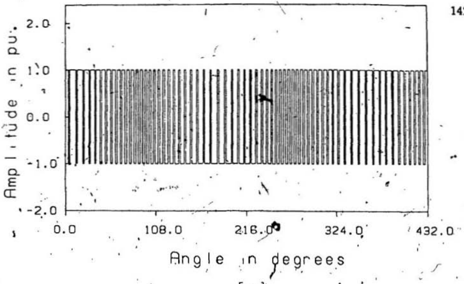


Figure 4.18: Experimental waveforms in the single phase delta modulated inverter with tank circuit filter and 0.8 pf lagging load: (a)Upper trace:filter input voltage, Lower trace:filter input current, (b) Upper trace:load voltage, Lower trace:load current. Modulator parameters:ΔV=0.18 V, V_R=5.0 V, S_c=3000 V/sec.



Scale:
X-2 ms/div.,
Y-5 A/div.

Figure 4.19: Experimental waveforms in the single phase delta modulated inverter with tank circuit filter and 0.8 pf lagging load: (b) Upper trace: filter shunt inductor current, Lower trace: filter shunt capacitor current. Modulator parameters:ΔV=0.18 V, V_R=5.0 V, S_c=3000 V/sec.



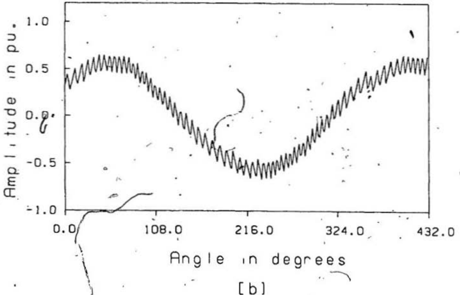


Figure 4.20: Simulated waveforms in the single phase delta modulated inverter with tank circuit filter and 0.8 pf lagging load: (a) Filter input voltage (b) Filter input current. Modulator parameters: ΔV =0.18 V, V_R=5.0 V, S_c=3000 V/sec.

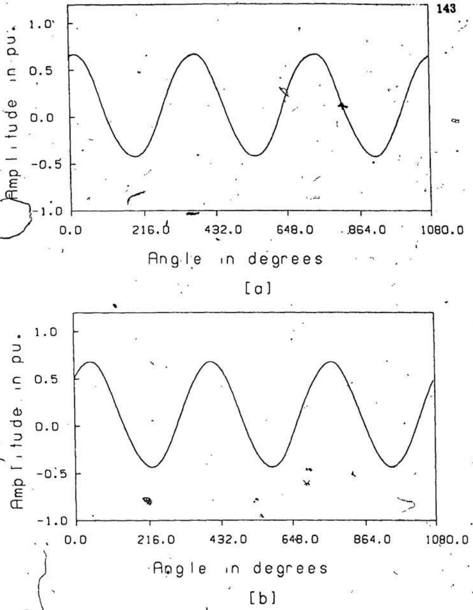


Figure 4.21: Simulated waveforms in the single phase delta modulated inverter with tank circuit filter and 0.8 pf lagging load: (a) Load voltage (b) Load current. Modulator parameters: ΔV=0.18 V, V_R=5.0 V, S_c=3000 V/sec.

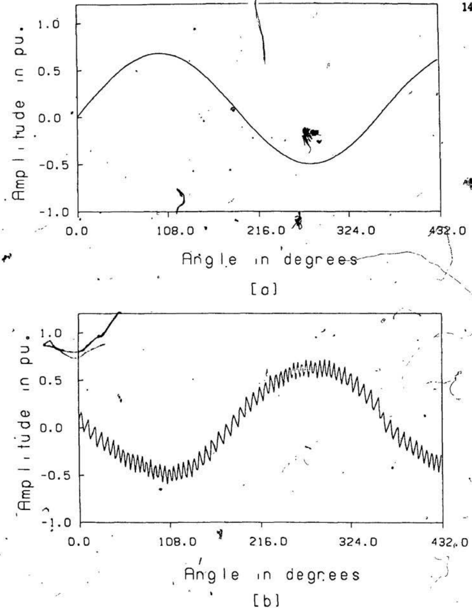


Figure 4.22: Simulated waveforms in the single phase delta modulated inverter with tank circuit filter and 0.8 pf lagging load: (a) Filter shunt inductor current (b) Filter shunt capacitor current. Modulator parameters: ΔV=0.18 V, V_R=5.0 V, S_c=3000 V/sec.

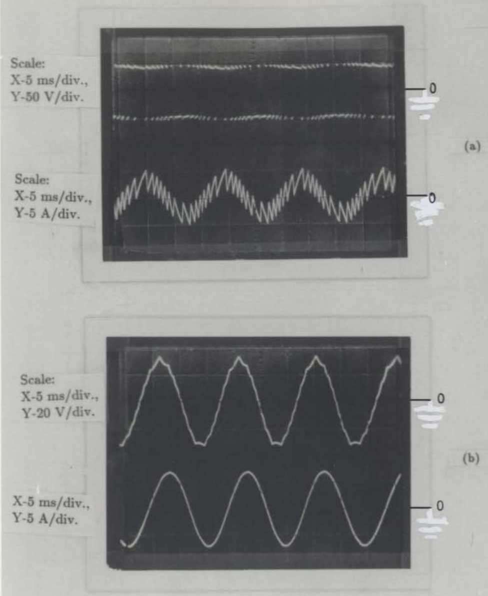
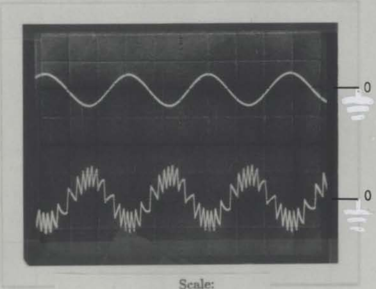


Figure 4.23: Experimental waveforms in the single phase delta modulated inverter with tank circuit filter and 0.8 pf lagging load: (a)Upper trace:filter input voltage, Lower trace:filter input current (b) Upper trace:load voltage, Lower trace:load current. Modulator parameters:ΔV=0.5 volt, V_R=5.0 volt, S_c=3000 v/sec.



Scale:
X-5 ms/div.,
Y-5 A/div.

Figure 4.24: Experimental waveforms in the single phase delta modulated inverter with tank circuit filter and 0.8 pf lagging load: (b) Upper trace:filter shunt inductor current, Lower trace : filter shunt capacitor current. Modulator parameters: ΔV =0.5 Volt, V_R=5.0 Volt, S_c=3000 V/sec.

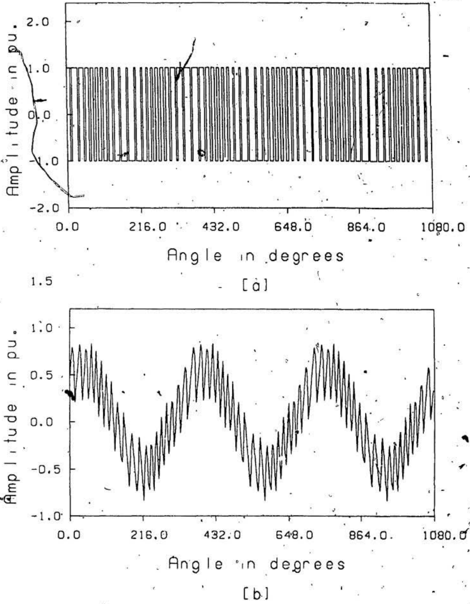
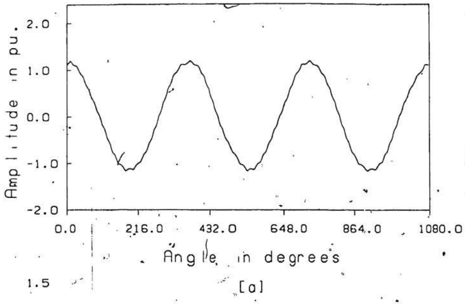


Figure 4.25: Simulated waveforms in the single phase delta modulated inverters with tank circuit filter and 0.8 pf lagging load: (a) Filter input voltage (b) Filter input current. Modulator parameters: ΔV=0.5 Volt, V_R=5.0 Volt, S_c=3000 V/sec.



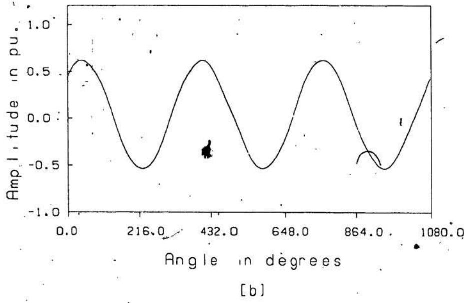


Figure 4.26: Simulated waveforms in the single phase delta modulated inverters with tank circuit filter and 0.8 pf lagging load : (a) Load voltage (b) Load current. Modulator parameters: ΔV=0.5 Volt, V_R=5.0 Volt, S_c=3000 V/sec.

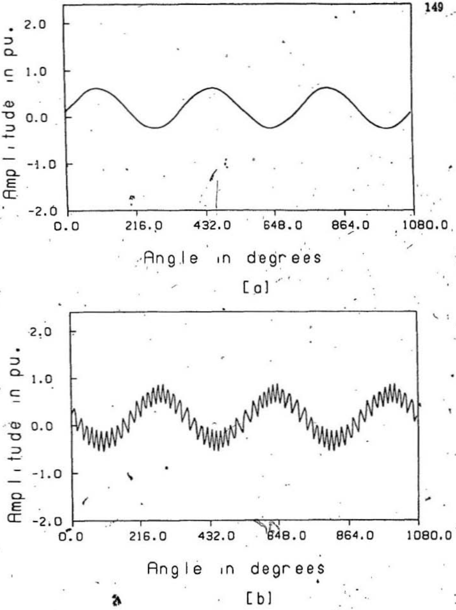


Figure 4.27: Simulated waveforms in the single phase delta modulated inverters with tank circuit filter and 0.8 pf lagging load: (a) Filter shunt inductor current (b) Filter shunt capacitor current. Modulator parameters: ΔV=0.5 Volt, V_R=5.0 Volt, S_c=3000 V/sec.

Chapter 5

DESIGN OF A SINGLE PHASE DELTA MODULATED UPS INVERTER WITH LOAD FILTER

The design of the single phase delta modulated inverter for UPS applications depends on both the delta modulator parameters and the power sub-circuit components. In the preceding chapters, the performance of the delta modulated inverter was described in terms of variations of the delta modulator parameters and the load filter parameters. In this chapter, the major considerations involved in choosing 'optimum' values for both the modulator parameters and the filter components are discussed with the aid of design curves. A brief methodology for determining the load transformer rating, system losses and efficiency is outlined. Finally, a numerical design example is given to illustrate the design procedures outlined in the chapter.

5.1 Selection of the Modulator Parameters

In this section, design considerations regarding the choice of suitable modulator parameters are discussed and a procedure for selecting optimum modulator parameters is outlined.

The effect of various modulator parameters on the the inverter output frequency spectrum was carried out in Chapter 2. It was shown that the inverter output frequency spectrum is controlled by the modulator parameters. Specifically, it was shown that the value of the slope of the carrier wave (S_c) affects both the amplitude of the fundamental component of the inverter output voltage (V_{o1}) and the order of the dominant harmonics in the frequency spectrum. However, the value of V_{o1} is determined by the ratio of the modulation index (M) to the slope of the carrier wave.

Figure 5.1 shows the relationship between the order of the dominant harmonic in the inverter output frequency spectrum and S_c for a fixed value of V_{o1} (56 %). The figure shows that increasing the slope of the carrier wave shifts the dominant harmonic in the inverter output frequency spectrum to higher frequencies. Shifting the dominant harmonic to higher frequencies means that small filter size can be used to obtain a load voltage of THD less than 5%. To marginally avoid slope overload condition and achieve high fundamental output voltage (i.e., high voltage utilization ratio) with dominant harmonics at higher frequencies, modulator parameters of $S_{cn} = 1.0$ pu. and M $= 0.8$ pu. are preferred and considered 'optimum'.

The value of ΔV has a significant effect on the harmonic spectra of the inverter output voltage and negligible effect on the amplitude of V_{o1}. Increasing the value

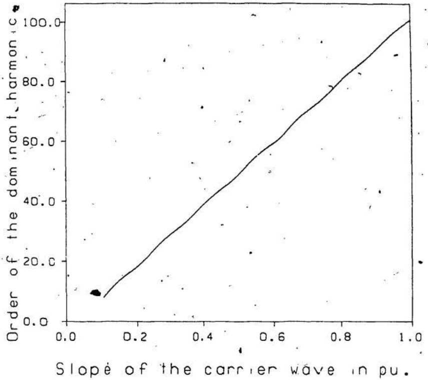


Figure 5.1: Effect of the slope of the carrier wave on the order of the dominant harmonic for constant value of voltage utilization ratio

of ΔV decreases the order of the dominant harmonic and vice versa. On the other hand, decreasing the value of ΔV results in higher inverter switching frequency.

The value of ΔV is chosen as small as practically possible. The limit on the small value of ΔV is mainly dictated by the speed of the voltage comparator in the modulator circuit (A_1 in Fig. 2.2) and the inverter switching losses. In general, values of ΔV ranging from 0.01 pu. to 0.02 pu. are preferred.

The value of ΔV also plays a part in determining the system step response. A full discussion on the choice of the value of ΔV has to take into account the effect of its variation on the overall system step and transient responses.

5.2 Design Considerations for the Power Sub-circuit

In the previous sections, the half-bridge inverter circuit was employed to carry out the experimental verification of the single phase delta modulated UPS inverter. However, for high power applications the full-bridge inverter circuit is used.

In this section, a design procedure for selecting component values and determining the ratings of the power sub-circuit is presented. Design curves showing the effect of the filter components on various UPS performance variables are employed to select values of filter components which meet certain performance criteria of the UPS system. Based on these values, the ratings of the components of the single phase delta modulated UPS inverter are determined.

5.2.1 Design Considerations of the Load filter Components

The choice of the filter components has to meet the following criteria:

1. The filter has to be small in size and provide the least possible attenuation to the fundamental component of the inverter output voltage. An indication of the filter size is the normalized filter cost (NFC). The smaller is the value of the NFC, the smaller the filter size.

   The attenuation of the fundamental component of the inverter output voltage due to the filter series inductor is defined by:

$$ATTN\% = 100\frac{V_{o1} - V_{L1}}{V_{o1}} \tag{5.1}$$

   Fundamental voltage attenuation should be kept to a minimum (usually 10 %), in order to optimally utilize the dc supply voltage.

2. The system voltage utilization should be kept at its highest possible value while the total harmonic distortion of the load voltage is kept below 5 %.

Design curves showing the effect of the filter components on the UPS performance variables are discussed below.

Figure 5.2 shows the effect of the filter components on the attenuation of the fundamental component of the inverter output voltage for both filters. Figure 5.2a shows that for the L-C filter, the attenuation of the fundamental component of the load voltage increases with increasing values of X_{L1}. Except for X_c values less than 2.0 pu., the shunt capacitor does not have significant effect on the attenuation level. The figures also show that there is a wide range of variations of attenuation level for values of X_{L1} greater than 0.2 pu. Figure 5.2b shows that for the tank circuit filter, attenuation levels less than 10 % can be achieved if X_{L1} is less than 0.2 pu. From the voltage utilization viewpoint, Fig. 5.2b suggests that the tank circuit components can have any value as long as they are tuned at the fundamental frequency.

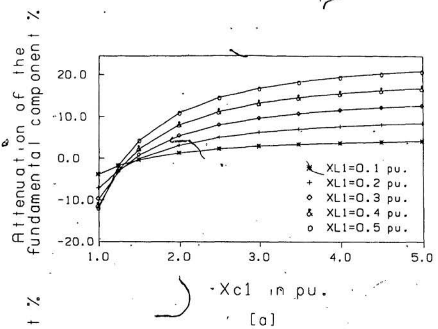
Figures 5.3 and 5.4 show the relationship between the voltage utilization ratio and the total harmonic distortion of the load voltage for the L-C filter and the tank circuit filter respectively. Figure 5.3 shows that for the L-C filter , a load voltage THD less than 5 % and voltage utilization ratio (VUR) of 0.65 pu. can be achieved with $X_{L1} = 0.2$ pu. and $X_{c1} = 3.0$ pu. However, with load voltage regulation, total harmonic distortion less than 5 % can be achieved at reduced VUR with the same filter components. Figure 5.4 shows that for the tank circuit filter, load voltage THD less than 5 % can be achieved with $X_{L1} < 0.2$ pu. and $X = 2.0$ pu. However, compared to the L-C filter, the voltage utilization ratio using a tank circuit filter is lower and it is further reduced with load voltage regulation.

Figure 5.5 shows the relationship between the normalized filter cost of both L-C and tank circuit filters and various filter parameters. The figure shows that the normalized filter cost of both filters generally decreases with increasing values of X_{L1} and X or X_{c1}.

The discussion above indicates that the choice of the 'optimum' filter components involves trade offs between the total harmonic distortion, filter cost, voltage attenuation and voltage utilization ratio. Based on the previous discussion, preferred filter components can be chosen as :

for L-C filter: $X_{L1} = 0.20$ pu. $X_{c1} = 3.0$ pu.

for tank circuit filter: $X_{L1} = 0.17$ pu. X=2.0 pu.



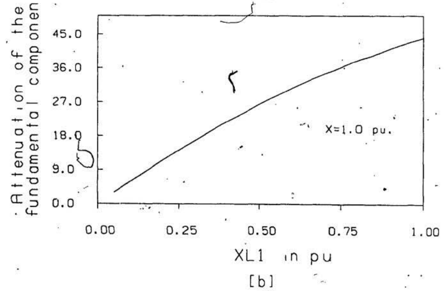


Figure 5.2: Effect of various filter parameters on the attenuation of the fundamental component of the inverter output voltage: (a) L-C filter , (b) Tank circuit filter

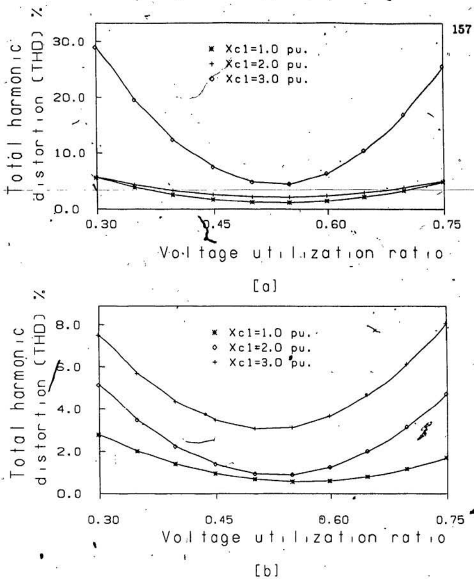


Figure 5.3: Effect of various L-C filter parameters on the total harmonic distortion of the load voltage: (a) $X_{L1} = 0.1$ pu., (b) $X_{L1} = 0.2$ pu.

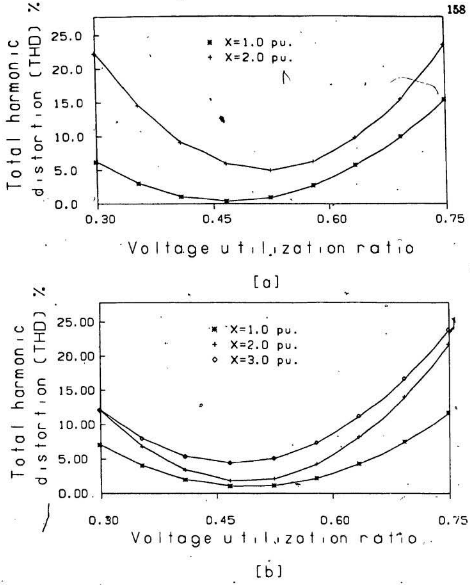
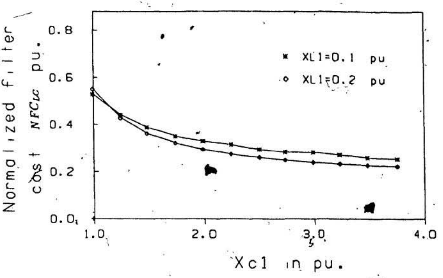
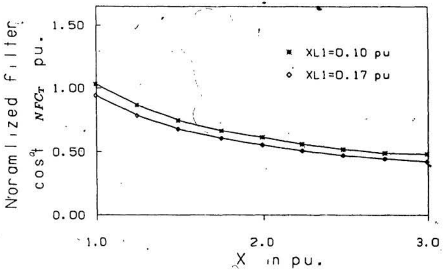


Figure 5.4: Effect of various parameters of the tank circuit filter on the load voltage THD: (a) $X_1 = 0.1$ pu., (b) $X_1 = 0.17$ pu.



[a]



[b]

Figure 5.5: Effect of various load filter parameters on the load filter normalized cost: (a) L-C filter, (b) Tank circuit filter

5.2.2 Determination of System Component ratings and efficiency

Figure 5.6 shows the schematic diagram of a single phase full-bridge inverter with an isolating transformer, L-C filter and load. The full-bridge inverter circuit is used, in this case, for high output ratigs of the inverter. A transformer is required at the load terminals to provide ohmic isolation between the load and the dc power supply and to match the specified load voltage with the dc voltage level at a particular value of modulation index.

1. Determination of the transformer rating

To specify the transformer, expressions for the turns ratio, current and voltage ratings are derived.

The fundamental component of the load voltage is given by:

$$\frac{V_{L1}}{V_{o1}} = |TF_1|\frac{N_s}{N_p} \tag{5.2}$$

where $|TF_1|$ is the magnitude of the filter transfer characteristic at the inverter fundamental frequency.

N_p is the number of turns of the transformer primary winding.

N_s is the number of turns in the transformer secondary winding.

Neglecting the harmonic content in the load voltage, the magnitude of the load voltage is given by:

$$V_{L1} = V_{o1}|TF_1|\frac{N_p}{N_s} \tag{5.3}$$

Since

$$V_{o1} = \frac{M}{\sqrt{2}S_{cn}}V_{dc} \tag{5.4}$$

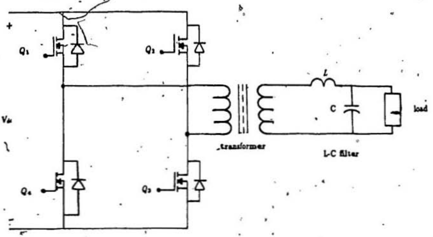


Figure 5.6: Schematic diagram of the single phase delta modulated UPS inverter

the transformer turns ratio is obtained from equations 5.3 and 5.4 as

$$\frac{N_p}{N_s} = \frac{\sqrt{2}V_{L1}S_{cn}}{|TF_1|MV_{dc}} \tag{5.5}$$

Equation 5.5 shows that increasing the level of the modulation index will reduce the value of the transformer turns ratio and hence its size. The magnitude of the filter transfer characteristic at the inverter fundamental frequency, TF_1 should be as close to unity as possible. For values of TF_1 much less than unity, the transformer turns ratio has to be high in order to compensate for the attenuation in V_{o1} and provide the specified level of the load voltage.

The fundamental component of the transformer secondary current, I_{s1} is given by:

$$I_{s1} = \frac{V_{L1}}{Z_{L1}} \tag{5.6}$$

where Z_{L1} is the load impedance at the fundamental frequency.

The fundamental component of the transformer primary current, I_{p1} is given by:

$$I_{p1} = I_{s1}\frac{N_p}{N_s} \tag{5.7}$$

The transformer VA rating is given by

$$VA_t = V_{o1}I_{p1} = V_L I_{s1} \tag{5.8}$$

The transformer rating is determined by neglecting the power losses due to higher order harmonics. To safely operate the transformer without overheating it, the transformer has to be derated.

2. Inverter Losses and Rating

Owing to the wide seperation between the switching frequency and the load frequency, the effective load at the inverter output appears highly inductive. Therefore, it is assumed that the inverter current is approximately constant during each switching cycle.

There are three different types of losses in the inverter, namely:

- Inverter switching loss.
- Conduction loss.
- Freewheeling diode conduction loss.

Using power MOSFETs as the inverter switching devices, the inverter average switching losses are given by [30]:

$$P_{s-avg} = \frac{2V_{dc}F_sI_o}{\pi}[2k + 2.47\sqrt{\frac{kI_o}{di/dt}} + 0.785\frac{I_o}{di/dt}] \quad (5.9)$$

where

$$k = \frac{Q_{rr}}{I_f} \quad (5.10)$$

where F_s is the inverter average switching frequency.

I_o is the rms value of the inverter output current.

Q_{rr} is the reverse recovery charge in the source drain diode (given in the device data sheet).

I_f is the diode forward current at which Q_{rr} is given.

The value of Q_{rr} depends on the transistor temperature and its drain current. Thus, the value of Q_{rr} has to be corrected when the transistor junction temperature deviates from that at which Q_{rr} is given.

The device conduction loss is given by [30]:

$$P_{c1-avg} = 0.462 I_o^2 R_{dc(on)} \tag{5.11}$$

and the diode conduction loss is given by [30]:

$$P_{c2-avg} = 0.068 I_o V_{sd} \tag{5.12}$$

where P_{c1-avg} is the average power loss due to the MOSFET channel resistance.

P_{c2-avg} is the average power loss in the MOSFET body diode.

V_{sd} is the forward voltage drop across the diode.

R_{ds} is the value of the on resistance of the transistor channel.

Inverter total losses (P_{l-inv}) are given by

$$P_{l-inv} = P_{s-avg} + P_{c1-avg} + P_{c2-avg} \tag{5.13}$$

The inverter switching device ratings are calculated at the highest possible permitted voltage and current.

The peak current flowing through the inverter switching devices is equal to the peak value of the filter input current referred to the transformer primary side and is given in equation 4.44. However, the rms value of the filter input current is given by equation 4.45.

The peak repetitive forward (V_{pf}) and reverse (V_{pr}) voltages across the inverter devices are given by

$$\hat{V}_{pf} = \hat{V}_{pr} = V_{dc} \tag{5.14}$$

3. UPS System Efficiency

The UPS system efficiency, η_{sys} is given by

$$\eta_{sys} = \eta_{inv} \times \eta_t \times \eta_F \tag{5.15}$$

where η_F is the load filter efficiency

η_t is the transformer efficiency

η_{inv} is the inverter efficiency

The filter efficiency is given by:

$$\eta_F = \frac{V_{L1} I_{L1} \cos\theta}{V_{L1} I_{L1} \cos\theta + F_l} \tag{5.16}$$

or

$$\eta_F = \frac{pf}{pf + F_{lp}} \tag{5.17}$$

where F_l is the load filter loss.

F_{lp} is the load filter loss per VA output.

pf is the load power factor

The load transformer efficiency is given by:

$$\eta_t = \frac{\frac{V_{L1} I_{L1} \cos\theta}{\eta_F}}{\frac{V_{L1} I_{L1} \cos\theta}{\eta_F} + T_l} \tag{5.18}$$

or

$$\eta_t = \frac{pf}{pf + \eta_F T_{lp}} \tag{5.19}$$

where T_{lp} is the transformer losses per VA output.

Similarly, the inverter efficiency is given by:

$$\eta_{inv} = \frac{pf}{pf + P_{lp-inv}\eta_t\eta_F} \tag{5.20}$$

where P_{lp-inv} is the inverter losses per VA output.

5.3 Design Example

A numerical example involving the L-C filter is given to illustrate the design procedures established in the previous sections.

The following are the requirements for the design of a single phase full-bridge delta modulated UPS system.

Rated apparent load power = 1000 VA

Rated load voltage = 110 V (rms)

Rated dc supply voltage = 155 ± 10 %

Operating frequency = 60.0 Hz

Transformer efficiency= 94 %

Load voltage THD ≤ 5 %

Load power factor is expected to vary form 0.8 lagging to unity.

5.3.1 Determination of the modulator parameters

In section 5.1, the following modulator parameters were chosen:

S_{cn}=1.0 pu., M=0.8 pu., and ΔV_n=0.015

If the hysteresis comparator saturation level is chosen as 10 V, the values of the modulator parameters are obtained from equations 2.36, 2.37 and 2.40 as:

$$V_R = M \times V_s = 0.8 \times 10 = 8.0 \quad (5.21)$$

$$\Delta V = \Delta V_n \times V_s = 0.015 \times 10 = 0.15 \quad (5.22)$$

and

$$S_c = \omega \times V_s \times S_{cn} = 377 \times 10 \times 1 = 3770 \tag{5.23}$$

If the integrator capacitor is chosen as 0.05 μF, then the value of the integrator resistance (R_1) in Fig. C.1 is given by:

$$R_1 = \frac{V_s}{C_1 S_c} \tag{5.24}$$

or

$$R_1 = 53k\Omega \tag{5.25}$$

5.3.2 Design of the Power Sub-circuit

The peak value of the fundamental component of the inverter output voltage is given by:

$$\hat{V}_{o1} = \frac{MV_{dc}}{S_{cn}} = 0.80 \times 155 = 124.0V(peak) \tag{5.26}$$

and

$$V_{o1} = 87.68V(rms) \tag{5.27}$$

The preferred L-C filter parameters are given in section 5.2 as

$$X_{L1} = 0.2pu. \tag{5.28}$$

$$X_{c1} = 3.0pu \tag{5.29}$$

These values produce load voltage THD less than 5 % for 0.8 pf lagging load. As shown in chapter 4, the load voltage THD is the worst in the case of lagging power factor loads. In other words, the same filter components that produce a load voltage with THD less than 5% for lagging power factor loads, will provide a load voltage with THD less than this value for unity power factor load.

The fundamental transfer characteristic of the load filter at the filter parameters given above is calculated from equation 4.3 by substituting n=1, and is obtained as:

$$TF_1 = 0.95 \tag{5.30}$$

Since the load voltage required is 110 V (rms), the turns ratio of the load transformer is calculated from equation 5.5 as

$$\frac{N_s}{N_p} = \frac{110}{0.95 \times 87.60} \tag{5.31}$$

or

$$\frac{N_p}{N_s} = 0.76 \tag{5.32}$$

The following base quantities are calculated:

The base voltage =155 V

The base impedance is given by :

$$\frac{V_{L1}^2}{VA} = \frac{(110)^2}{1000} = 12.1\Omega \tag{5.33}$$

The base impedance referred to the transformer primary side is calculated as:

$$Z_{base} = (\frac{N_p}{N_s})^2 \times 12.1 = (0.76)^2 \times 12.1 = 6.98\Omega \tag{5.34}$$

The base current is given by

$$I_{base} = \frac{155}{6.98} = 22.17A \tag{5.35}$$

1. **Filter component values**

   The actual values of the filter parameters (referred to the transformer secondary side) are given by:

$$X_{L1} = 0.2 \times 12.1 = 2.42\Omega \tag{5.36}$$

$$X_{c1} = 3.0 \times 12.1 = 36.3\Omega \tag{5.37}$$

The values of the filter series inductor and shunt capacitor are obtained as:

$$L_1 = \frac{2.42}{377.0} = 6.42mH \quad (5.38)$$
$$C_1 = \frac{1}{377 \times 36.3} = 73\mu F \quad (5.39)$$

Assuming that the quality factor of the filter series inductor is 8, the resistance associated with the filter series inductor is obtained as:

$$R_1 = \frac{2.42}{8} = 0.3\Omega \quad (5.40)$$

2. **Filter rating and efficiency**

   Since the filter input current is higher for unity power factor loads than that for lagging power factor loads, the currents flowing through various filter components are determined on the basis of unity power factor load (worst case design). Substituting the filter values in equation 4.19, 4.44 and 4.45 yield:

$$\hat{I}_i = 0.59 \quad pu. \quad (5.41)$$
$$I_{irms} = 0.53 \quad pu. \quad (5.42)$$
$$I_{crms} = 0.47 \quad pu. \quad (5.43)$$
$$I_{i1rms} = 0.52 \quad pu. \quad (5.44)$$

Converting the pu values into actual values yield:

$$\hat{I}_i = 0.59 \times 22.17 = 13.08 \quad A \ (peak) \quad (5.45)$$
$$I_{irms} = 0.53 \times 22.17.31 = 11.75 \quad A \ (rms) \quad (5.46)$$
$$I_{crms} = 0.47 \times 22.17 = 10.42 \quad A \ (rms) \quad (5.47)$$

$$V_{crms} = 110V \qquad (rms) \tag{5.48}$$

$$\hat{V}_c = \sqrt{2} \times 110 = 155.5 \qquad V \ (peak) \tag{5.49}$$

$$I_{i1rms} = 0.52 \times 30.31 = 15.76 \qquad A \ (rms) \tag{5.50}$$

The copper loss in the resistance associated with the filter series inductor is obtained by:

$$F_l = (11.75)^2 \times 0.3 = 41.40 \quad W \tag{5.51}$$

The filter efficiency is given by:

$$\eta_F\% = \frac{1 \times 100}{1 + \frac{41.40}{1000}} = 96.02\% \tag{5.52}$$

3. **Load Transformer rating**

The rms value fundamental component of the transformer primary current (inverter output) is given as:

$$I_{i1} = 11.53 \quad Amp \tag{5.53}$$

The transformer VA rating at the inverter fundamental frequency is given by

$$VA_t = 11.53 \times 87.68 = 1010.95 \quad VA \tag{5.54}$$

Allowing 10 % overating for the harmonic content in the inverter output voltage, the transformer VA rating is chosen as:

$$VA_t = 1010.95 \times 1.1 = 1112.0VA \tag{5.55}$$

4. **Inverter rating and efficiency**

Inverter switching devices should be rated to carry twice the rms value of the transformer primary current, hence the current flowing through switching device (I_Q) is given by:

$$I_Q = 2.0 \times 11.75 = 23.50\ A\ \ (rms) \tag{5.56}$$

The peak forward, ($\hat{V_{pf}}$) and reverse, ($\hat{V_{pr}}$) repetitive voltage are chosen to be equal to the maximum allowable level of the supply voltage (+ 10 %) and are given by:

$$V_{pf} = V_{pr} = 155 \times 1.1 = 170.50V \tag{5.57}$$

IRF 250 with current and voltage ratings of 30 Amp and 200 V respectively is chosen as the inverter switching device.

The reverse recovery charge Q_{rr} of the MOSFET body diode is given as Q_{rr}=8.1 μF at I_f of 30.0 Amp., hence

$$k = \frac{8.1}{30.0} = 0.27\mu C/Amp. \tag{5.58}$$

The inverter average switching frequency is obtained by substituting the modulator parameters in equation 2.32 to give:

$$F_{s-avg} = \frac{3770}{4 \times 0.15}[1 - (\frac{377 \times 8.0}{2 \times 3770})^2] \tag{5.59}$$

or

$$F_{s-avg} = 3770.0\ \ Hz \tag{5.60}$$

The inverter average switching loss is obtained from equation 5.9 as:

$$P_{s-avg} = K_1(2 \times 0.27 + 2.47\sqrt{\frac{0.27 \times 11.75}{100}} + \frac{0.78 \times 11.75}{100}) \tag{5.61}$$

where

$$K_1 = 10^{-6} \times \frac{2 \times 170.5 \times 11.75 \times 3770}{\pi} \tag{5.62}$$

Hence;

$$P_{s-avg} = 5.15 \;\; W \tag{5.63}$$

The average conduction loss in the MOSFET channel resistance is calculated from equation 5.10 as:

$$P_{c1-avg} = 0.462 \times (11.75)^2 \times 0.08 = 5.1 \;\; W \tag{5.64}$$

Since the forward voltage drop across the MOSFET body diode is 2.0 V, the average conduction loss in the device body diode is given by:

$$P_{c2-avg} = 0.068 \times 11.75 \times 2.0 = 1.59W \tag{5.65}$$

Total inverter losses are given by:

$$P_{l-inv} = P_{s-avg} + P_{c1-avg} + P_{c2-avg} \tag{5.66}$$

$$P_{l-inv} = 5.15 + 5.1 + 1.59 = 11.19 \;\; W \tag{5.67}$$

From equation 5.19, the inverter efficiency is calculated as:

$$\eta_{inv}\% = \frac{1 \times 100}{1 + 0.94 \times 0.92\frac{21.73}{1000}} = 98.98\% \tag{5.68}$$

5. **System efficiency**

The overall system efficiency is calculated from equation 5.14 as:

$$\eta_{sys} = 0.94 \times 0.96 \times 0.98 = 0.893 \tag{5.69}$$

or

$$\eta_{sys}\% = 89.3\% \tag{5.70}$$

The design of the single phase full-bridge delta modulated inverter with tank circuit filter follows along the same procedures as the L-C filter.

Chapter 6

CONCLUSIONS

In this thesis, the analysis and implementation of a rectangular wave delta modulation (RWDM) scheme for UPS applications have been carried out, and it has been shown that RWDM offers significant improved performance for UPS applications.

Three types of rectangular wave modulator, namely, single stage, multistage and digital RWDM were presented. It was shown that the single stage RWDM possesses all the desired requirement for UPS applications. The basic characteristics of the RWDM were evaluated and it was found that the modulator parameters which affect the performance of the modulator are the hysteresis bandwidth ΔV, the integrator gain S_c and the modulation index M. The effects of these parameters on the modulator performance were investigated further using Discrete Fourier Transform technique. It was shown that:

- The order of the dominant harmonic in the modulator output is strongly influenced by the hysteresis bandwidth ΔV and the integrator gain S_c. Consequently, control of the order of the dominant harmonic can be achieved by varying these parameters. However, it is recommended that ΔV should be used to control the order of the dominant harmonic, while S_c is selected to provide the desired value of the fundamental component of the modulator output and also to avoid slope overload condition.

- The amplitude of the fundamental component of the modulator output is determined by the modulation index and the integrator gain. Thus, the RWDM provides a means whereby harmonic minimization and voltage control technique can be combined in the modulation process.

The application of the delta modulation scheme to a single phase UPS inverter with resistive load was investigated. Two switching schemes, namely the unipolar and the bipolar, which are commonly used in pulse width modulated static inverters were examined for the delta modulation scheme. The bipolar switching scheme was found to be more suitable for the single phase delta modulated UPS inverter. The following basic features of the scheme made it attractive for UPS applications.

1. It provides significant attenuation of low order harmonic in the inverter output voltage.
2. It provides load voltage regulation through an independent control of the modulation index.
3. It provides significant improvements in the voltage utilization ratio.
4. It provides high order dominant harmonic with moderate modulator switching frequencies.

The application of the RWDM to a single phase delta modulated inverter with load filter was examined. Several types of load filters were presented, and based on their basic characteristics, two filters, namely the L-C filter and the tank circuit filter were selected for delta modulated UPS inverter.

The effect of the two filters in suppressing the undesired harmonics contained in the inverter output voltage was investigated for various loads by varying the values of various filter components. It was shown that for both filters, increasing the value of the filter series inductor or the shunt capacitor decreases the total harmonic distortion (THD) of the load voltage. It was also shown that for given filter component values and load VA rating, the THD of the load voltage was the highest for lagging power factor load. However, the characteristic curves presented in the thesis show that THD less than 5 % with small filter sizes is achievable.

An investigation of the effect of varying the filter components on the cost of the filter was carried out. It was shown that for both filters, the normalized filter cost decreases with decreasing values of the shunt capacitance. It was also shown that for given filter component values and load VA rating, the normalized filter cost was the highest for leading power factor load.

Experimental and predicted results showed that the delta modulation technique offers improved performance of the UPS inverter.

Finally, a numerical design example of a single phase delta modulated UPS inverter with L-C filter and lagging power factor load was presented. Various issues involved in selecting the modulator parameters and the load filter parameters were presented with the aid of design curves to determine 'optimum' components value of both the modulator and the load filter.

Suggestions for future work

The present work contains the analysis and analog implementation of the single phase delta modulated UPS inverter. Future work in the area of delta modulated UPS systems may be stated as follows:

- A detailed investigation of the suitability of three phase delta modulated UPS inverter, and evaluation of the system performance with the two commonly used switching schemes for static pulse width modulated inverter is recommended.
- The effect of various system parameters, modulator and load filter, on the system response to step changes in the load is recommended. In addition, a detailed procedure for determining the optimum parameters is required.
- A microprocessor implementation of the three phase delta modulated UPS inverter should be investigated, since a microprocessor-based system will enhance the noise immunity of the system.
- The characteristics and suitability of the second order rectangular wave delta modulator for UPS applications could be investigated.
- The application of the RWDM scheme to other UPS configurations (for example the current-fed UPS system) needs to be examined.

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Appendix A

Determination of The Delta Modulator Switching Instants

Figure A.1 shows various waveforms in the modulator circuit for the first few switching instants. The modulator output $v_{mo}(t)$ toggles between $\pm V_s$. The carrier wave oscillates around the reference signal with equal positive and negative slope, S_c. A modulator output switching instant takes place when the amplitude of the carrier wave exceeds the amplitude of the reference signal by the value of the hysteresis bandwidth ΔV. Assuming that both the carrier signal and the reference signal initially start at zero, the first switching instant takes place when:

$$S_c t_1 = V_R \sin\omega t_1 + \Delta V \qquad A.1$$

or the switching instant takes place at:

$$t_1 = \frac{V_R \sin\omega t + \Delta V}{S_c} \qquad A.2$$

The second switching instant takes place when:

$$S_c(t_2 - t_{t1}) = V_R \sin\omega t_1 - V_R \sin\omega t_2 + 2\Delta V \qquad A.3$$

or

$$t_2 = \frac{2\Delta V + S_c t_1}{S_c} + \frac{V_R \sin\omega t_1 - V_R \sin\omega t_2}{S_c} \qquad A.4$$

The third switching instant is determined by:

$$t_3 = \frac{2\Delta V + S_c t_2}{S_c} + \frac{V_R(\sin\omega t_3 - \sin\omega t_2)}{S_c} \qquad A.5$$

The ith switching instant can be determined as

$$t_i = \frac{2\Delta V + S_c t_{i-1}}{S_c} + V_R \frac{(\sin\omega t_{i-1} - \sin\omega t_i)}{S_c(-1)^i} \qquad A.6$$

i=2,3,4, ...

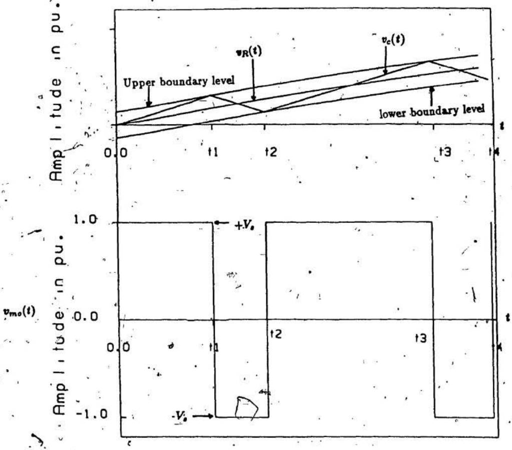

Figure A.1: First few switching instants for determining the modulator switching instants

where	ΔV	is the hysteresis bandwidth.
	S_c	is the slope of the carrier wave.
	ω	is the angular frequency of the reference signal $v_R(t)$.
	V_R	is the maximum value of the reference signal amplitude.
	i	is the pulse number.

The above equations (A.1-A.6), are numerically solved to determine the switching instants. The program listing is given in appendix B.

Appendix B

Computer Programs

To solve the governing equations of the modulator switching instants, an International Mathematics and Statistics Library (IMSL) ZREAL (version 10) is used. As the routine specifies, the equations have to be defined as external function and the routine is repeatedly called for computing each switching point. The routine employs Muller's algorithm to solve the governing equations of the modulator switching instants.

B.1 Numerical Solution of the Delta Modulation Switching Instants

```
C***********************************************************
C  PROGRAM SOLVES THE DELTA MODULATION GOVERNING EQUATIONS *
C  AND PROVIDES THE SWITCHING INSTANTS OF THE MODULATOR    *
C  WAVEFORM OUTPUT.                                        *
C  SW = OUTPUT DATA FILE: CONTAINS NUMBER OF SWITCHING     *
C  POINTS, THE MODULATOR OUTPUT SWITCHING INSTANTS.        *
C***********************************************************
      COMMON DELV,VR,S,OMGA,FLAG,EQN
      REAL EPS,ERRABS,ERRREL,ETA,OMGA
      REAL S1(800),M1(800),P1(800),E1(800)
      EXTERNAL F1,F,ZREAL,WVFRM
      OPEN(UNIT=7,FILE='MPLOT.DAT',TYPE='NEW')
      OPEN(UNIT=8,FILE='EPLOT.DAT',TYPE='NEW')
      OPEN(UNIT=9,FILE='SW.DAT',TYPE='NEW')
      OPEN(UNIT=10,FILE='REF.DAT',TYPE='NEW')
C
C  DV : IS THE HYSTERESIS BAND WIDTH IN VOLTS
C  VR : IS THE AMPLITUDE OF THE REFERENCE SIGNAL IN VOLTS
C  S  : IS THE SLOPE OF THE CARRIER WAVE IN VOLTS/s
C  E1 : IS THE INSTANTANEOUS VALUE OF tHE CARRIER WAVE
C  The PERIOD OF THE MODULATOR OUTPUT WAVEFOM IS CHOSEN
C  TO FIVE TIMES THE REFERENCE SIGNAL PERIOD.
C
      WRITE(6,*)'ENTER: DV, VR, S'
      READ(6,*)DV,VR,S
      FREQ=60.0
C
      PI=2.*ASIN(1.)
      OMGA=2.*PI*FREQ
```

```
      TMAX=5.0/(FREQ)
      CRIT=TMAX-(TMAX*20.E-6)
C
      S1(1)=0.0
      E1(1)=0.0
      WRITE(6,20)0,0.
 20   FORMAT(11X,I3,6X,E15.6)
C
      N=1
      EPS=1.E-8
      ERRABS=1.E-8
      ERRREL=1.E-8
      ETA=1.E-2
      ITMAX=100
      NROOT=1
      XGUESS=1.E-5
C
C     CALCULATE FIRST SWITCHING POINT
C
      CALL ZREAL(F1,ERRABS,ERRREL,EPS,ETA,NROOT,ITMAX,XGUESS,X,INFO)
      S1(N+1)=X
      E1(N+1)=VR*SIN(OMGA*X)+DV
C
C     CALCULATE SUBSEQUENT SWITCHING POINTS
C
 50        N=N+1
      IF(JMOD(N,2) .NE. 0) THEN
           FLAG=-1.0
      ELSE
           FLAG=1.0
      ENDIF
      EQN=2.*DV+S*X+FLAG*VR*SIN(OMGA*X)
      XGUESS=X*1.50
      CALL ZREAL(F,ERRABS,ERRREL,EPS,ETA,NROOT,ITMAX,XGUESS,X,INFO)
      IF(X .GE. TMAX)X=TMAX
      S1(N+1)=X
      E1(N+1)=VR*SIN(OMGA*X)-FLAG*DV
      IF (X .EQ. TMAX)GOTO 55
      IF (X .LE. CRIT)GOTO 50
C
 55   WRITE(6,*)'N =',N
      NPTS=N+1
      WRITE(9,*)NPTS
      DO 150 I=1,NPTS
      WRITE(9,*)S1(I)
 150  WRITE(8,*)S1(I),E1(I)
C
C     CALLING WVFRM ROUTINE WHICH CONSTRUCTS THE VARIOUS
```

```
C       WAVEFORMS IN THE MODULATOR CIRCUIT.
C
        CALL WVFRM(NPTS,S1,TMAX,OMGA,VR,M1,P1,L,T,AMP)
        DO 130 I=1,L
  130   WRITE(7,*)M1(I),P1(I)
        STOP
        END
C
C       FUNCTION DESCRIBING FIRST SWITCHING POINT EQUATION
C
        REAL FUNCTION F1(X)
        COMMON DV,VR,S,OMGA,FLAG,EQN
        REAL OMGA
        F1=(DV+VR*SIN(OMGA*X))/S-X
        RETURN
        END
C
C       GENERAL FUNCTION FOR ALL SEBSEQUENT SWITCHING POINTS
C
        REAL FUNCTION F(X)
        COMMON DV,VR,S,OMGA,FLAG,EQN
        REAL OMGA
        F=(EQN-FLAG*VR*SIN(OMGA*X))/S-X
        RETURN
        END
C*****************************************************
```

```
C************************************************************
C  ROUTINE TO CONSTRUCT VARIOUS WAVEFORM IN THE              *
C  MODULATOR CIRCUIT.                                        *
C  EPLOT = OUTPUT DATA FILE WHICH CONTAINS THE CARRIER       *
C  SIGNAL WAVEFORM.                                          *
C  MPLOT = OUTPUT DATA FILE WHICH CONTAINS THE MODULATOR     *
C  OUTPUT WAVEFORM.                                          *
C  REF = OUTPUT DATA FILE CONTAINS THE REFRENCE SINE WAVE.   *
C************************************************************
      SUBROUTINE WVFRM(NPTS,S1,TMAX,OMGA,VR,M1,P1,L)
      REAL S1(800),M1(800),P1(800),E1(800)
C
      AMPP=7.0
      AMPN=5.0
      E1(1)=0.0
C
C     GENERATE SWITCHING WAVEFORM FROM CALCULATED
C     SWITCHING INSTANTS
C
      M1(1)=S1(1)
      P1(1)=AMPP
      L=2
      FLAG=1.0
      DO 120 J=2,NPTS
      IF(J .NE. (NPTS)) THEN
      IF((S1(J) .EQ. TMAX) .AND. (P1(L-1) .EQ. AMPP)) FLAG=-1.0
         IF (FLAG .GT. 0.0) THEN
            IF(JMOD(J,2) .EQ. 0) THEN
                  M1(L)=S1(J)
                  P1(L)=AMPP
                  L=L+1
                  M1(L)=S1(J)
                  P1(L)=AMPN
                  L=L+1
            ELSE
                  M1(L)=S1(J)
                  P1(L)=AMPN
                  L=L+1
                  M1(L)=S1(J)
                  P1(L)=AMPP
                  L=L+1
            ENDIF
         ELSE
            IF((JMOD(J,2) .NE. 0) .AND. (S1(J) .NE. TMAX)) THEN
                  M1(L)=S1(J)
                  P1(L)=AMPP
                  L=L+1
                  M1(L)=S1(J)
```

```
                        P1(L)=AMPN
                        L=L+1
                ELSE
                        M1(L)=S1(J)
                        P1(L)=AMPN
                        L=L+1
                        M1(L)=S1(J)
                        P1(L)=AMPP
                        L=L+1
                ENDIF
              ENDIF
             ELSE
               IF(JMOD(J,2) .EQ. 0) THEN
                  M1(L)=S1(J)
                        P1(L)=AMPP
                        L=L+1
                        M1(L)=S1(J)
                        P1(L)=AMPN
                ELSE
                        M1(L)=S1(J)
                        P1(L)=AMPN
                        L=L+1
                        M1(L)=S1(J)
                        P1(L)=AMPN
               ENDIF
            ENDIF
  120    CONTINUE
C
C        CONSTRUCT THE RFERENCE SINE WAVE
C
         T=0.0
         DELT=TMAX/800.0
  77     AMP=VR*SIN(OMGA*T)
         WRITE(10,*)T,AMP
         T=T+DELT
         IF(T .LE. TMAX) GOTO 77
         RETURN
         END
C**************************************************
```

B.2 Determination of The Frequency Spectrum of The Modulator Output Waveform

```
C************************************************************
C  PROGRAM COMPUTES THE SINE AND COSINE TRANSFORMS OF         *
C  THE MODULATOR OUTPUT FREQUENCY WAVEFORM TO DETRMINE ITS    *
C  FREQUENCY SPECTRUM.                                        *
C  THE PROGRAM EMPLOYS AN IMSL ROUTINE FFTSC (VERSION 9.2)    *
C  SW.DAT  = INPUT DATA FILE CONTAINS THE MODULATOR           *
C  SWITCHING INSTANTS.                                        *
C  HCN.DAT = OUTPUT DATA FILE CONTAINS FOURIER COEFFICIENTS   *
C  RCW.DAT = OUTPUT DATA FILE CONTAINS VARIOUS WAVEFORMS IN   *
C  THE MODULATOR RECONSTRUCTED FROM FOURIER COEFFICIENTS      *
C************************************************************
C
C  THIS PART OF THE PROGRAM PROGRAM IS MEANT FOR DISRETIZING
C  THE SWITCHING WAVEFORM OF THE DELTA MODULATOR OUTPUT.
C
      DIMENSION A(4096),ST(2049),CT(2049),IWK(12),WK(12),
     * HN(2049),CN(2049),PHI(2049),S1(800)
      COMPLEX CWK(2049)
      REAL MAX
      OPEN(UNIT=7,FILE='SW.DAT',TYPE='OLD')
      OPEN(UNIT=9,FILE='HCN.DAT',TYPE='NEW')
C     OPEN(UNIT=11,FILE='RCW.DAT',TYPE='NEW')
C
      FREQ=60.0
      OMGA=2.0*PI*FREQ
      TMAX=5.0/FR
C
      READ(7,*)NPTS
      DO 10 I=1,NPTS
 10   READ(7,*)S1(I)
C
      P2=13
C
      TS=TMAX/(2.0**P2)
      DELTS=0.0
      NMAX=NPTS-1
      K=1
      DO 20 I=1,NMAX
      L=I+1
      IF(MOD(I,2) .NE. 0.)THEN
              FLAG=1.0
      ELSE
              FLAG=-1.0
      ENDIF
```

```
 100    A(K)=FLAG
        DELTS=DELTS+TS
        K=K+1
        IF(DELTS .LE. S1(L))GOTO 100
 20     CONTINUE
        KPTS=K-1
C*****************************************************
C  THIS PART OF THE PROGRAM COMPUTES THE COSINE AND SINE
C  TRANSFORM OF THE DELTA MODULATOR OUTPUT WAVEFORM.
C
        N=KPTS
        WRITE(6,*)'TS=',TS,'N=',N
 90     N1=N/2+1
        CALL FFTSC(A,N,ST,CT,IWK,WK,CWK)
C
C       TO DETERMINE THE FREQUENCY COMPONENTS...
C
        DO  J=1,N1
        HN(J)=(J-1)/(N*TS*60.0)
        END DO
        Y=FLOATJ(N)
        DO K=1,N1
        CT(K)=CT(K)/Y
        ST(K)=ST(K)/Y
        END DO
C
        CT(1)=CT(1)/2.0
        ST(1)=ST(1)/2.0
        CT(N1)=CT(N1)/2.0
        ST(N1)=ST(N1)/2.0
        CN(1)=CT(1)
        DO 21 I=2,1001
        CN(I)=SQRT(CT(I)**2.+ST(I)**2.)
        IF((CT(I) .EQ. 0.0) .AND. (ST(I) .EQ. 0.0))THEN
                       PHI(I)=0.0
                        GOTO 21
                ELSE
                      PHI(I)=ATAN2(ST(I),CT(I))
        ENDIF
 21     CONTINUE
        WRITE(9,*)1000
        DO 25 J=1,1001
 25     WRITE(9,*)HN(J),CN(J),PHI(J)
        WRITE(9,101)
 101    FORMAT()
C
C       SEARCHING FOR THE  ORDER OF THE DOMINANT HARMONIC
C
```

```
      MAX=ABS(CN(7))
      DO 103 I=7,1000
      IF( MAX .LT. ABS(CN(I+1)))THEN
              MAX=ABS(CN(I+1))
              XK=HN(I+1)
      ENDIF
103   CONTINUE
      WRITE(6,*)XK,MAX
C*****************************************************
```

B.3 Computer Simulation Programs

B.3.1 Computer Simulation Program For LC Load Filter

```
C*************************************************************
C  PROGRAM TO SIMULATE THE PERFORMANCE OF THE L-C FILTER FOR     *
C  DELTA MODULATED UPS INVERTER.                                 *
C  HCN.DAT:INPUT DATA FILE CONTAINS THE HARMONIC COMPONENTS      *
C  OF THE MODULATOR OUTPUT WAVEFORM                              *
C  VOTP.DAT: OUTPUT DATA FILE CONTAINS THE OUTPUT VOLTAGE        *
C  WAVEFORM                                                      *
C  CAPC.DAT: OUTPUT DATA FILE CONTAINS THE CAPACITOR CURRENT     *
C  WAVEFORM                                                      *
C  LCRNT.DAT: OUTPUT DATA FILE CONTAINS THE LOAD CURRENT         *
C  WAVEFORM                                                      *
C  ICRNT.DAT: OUTPUT DATA FILE CONTAINS THE INPUT CURRENT        *
C  WAVEFORM                                                      *
C*************************************************************
      DIMENSION HN(1010),CN(1010),VON(1010),PHIF(1010),VOTP(210),
     * THETA(1010),GAMA(1010),CRNT(1010),CPH(1010),CAPC(1010),
     * CAPH(1010),XLCRNT(1010),XLPHS(1010),CAPC1(210),XLCRNT1(210),
     * CRNT1(210)
      OPEN(UNIT=7,FILE='HCN.DAT',TYPE='OLD')
      OPEN(UNIT=8,FILE='VL.DAT',TYPE='NEW')
      OPEN(UNIT=9,FILE='CAPC.DAT',TYPE='NEW')
      OPEN(UNIT=10,FILE='LCRN.DAT',TYPE='NEW')
      OPEN(UNIT=11,FILE='ICRN.DAT',TYPE='NEW')
C
C  READ LOAD POWER FACTOR
C
      WRITE(6,*)'INPUT POWER FACTOR'
      READ(6,*)XK1
C
C  READ THE VALUE OF THE FILTER SERIES INDUCTIVE REACTANCE
C  AND THE FILTER SHUNT CAPACITIVE REACTANCE IN PU.
C
      WRITE(6,*)'INPUT X1,XC'
      READ(6,*)X1,XC
      XK2=SIN(ACOS(XK1))
      READ (7,*)N1
      DO 10 I=1,N1
 10   READ(7,*)HN(I),CN(I),THETA(I)
      HC=X1/XC
      TH=0.0
      FR1=0.0
      CAPC2=0.0
      CPH(1)=THETA(1)
```

```
      VON(1)=CN(1)
      XLCRNT(1)=CN(1)/XK1
      DO 11 I=2,N1
C
C  COMPUTE FILTER TRANSFER CHARACTERISTICS :
C  MAGNITUDE AND PHASE
C
      ZO=1-((HN(I)**2)*HC)
      Z1=XK1**2+(HN(I)*XK2)**2
      Y1=HN(I)*(X1+XK2*ZO)
      Y2=XK1*ZO
      Z2=Y1**2+Y2**2
      Z=SQRT(Z1/(Z2))
      PHIF(I)=(ATAN2(XK2*HN(I),XK1)-ATAN2(Y1,Y2))
C
C     COMPUTE OUTPUT VOLTAGE : MAGNITUDE AND PHASE
C
      VON(I)=CN(I)*Z/1.414
      GAMA(I)=-THETA(I)+PHIF(I)
C
C     COMPUTE FILTER INPUT IMPEDANCE,INPUT CURRENT (SERIES
C     INDUCTOR CURRENT)
C
      ZI1=XK1*ZO
      ZI2=(HN(I)*X1+XK2*HN(I)-XK2*HC*(HN(I)**3))
      ZI3=XC-(XK2*(HN(I)**2))
      ZI4=XK1*HN(I)
      ZT=XC*(SQRT((ZI1**2+ZI2**2)/(ZI3**2+ZI4**2)))
      CRNT(I)=CN(I)/(ZT)
      CPH(I)=ATAN2(ZI4,ZI3)-ATAN2(ZI2,ZI1)-THETA(I)
C
C     COMPUTE FILTER SHUNT CAPACITOR CURRENT
C
      CAPC(I)=VON(I)*HN(I)/XC
      CAPH(I)=GAMA(I)+ASIN(1.)
C
C     COMPUTE LOAD CURRENT
C
      XLCRNT(I)=VON(I)/(SQRT(XK1**2+(XK2*HN(I))**2))
      XLPHS(I)=GAMA(I)-ATAN2(XK2*HN(I),XK1)
      IF(HN(I) .EQ. 6)GOTO 12
      TH=VON(I)**2+TH
C
C     CALCULATE NORMALIZED FILTER COST
C
12    FR1=2.0*(CRNT(I)**2)*HN(I)*X1+VON(I)*CAPC(I)+FR1
11    CONTINUE
C
```

```
C       COMPUTE TOTAL HARMONIC DISTORTION OF THE LOAD VOLTAGE
C
        THD=100*SQRT(TH)/VON(2)

C*****************************************************************
C   CONSTRUCT VARIOUS WAVEFORMS OF THE LOAD LOAD FILTER
C
        FREQ=60.0
        TMAX=20.0E-3
        XOMGA=4.0*ASIN(1.)*FREQ
        INDX=1
        PI =2.0*ASIN(1.)
        T=0.0
        DELT=TMAX/200.0
  650   VOTP(INDX)=0.0
        CAPC1(INDX)=0.0
        XLCRNT1(INDX)=0.0
        CRNT1(INDX)=0.0
        SUMT1=0.0
        SUMT2=0.0
        SUMT3=0.0
        SUMT4=0.0
        DO 700 I=2,1000
        XII=HN(I)*(XOMGA*T)
        SWX1=VON(I)*COS(XII+GAMA(I))
        SWX2=CAPC(I)*COS(XII+CAPH(I))
        SWX3=XLCRNT(I)*COS(XII+XLPHS(I))
        SWX4=CRNT(I)*COS(XII+CPH(I))
        SUMT1=SUMT1+SWX1
        SUMT2=SUMT2+SWX2
        SUMT3=SUMT3+SWX3
        SUMT4=SUMT4+SWX4
  700   CONTINUE
        VOTP(INDX)=CN(1)+SUMT1
        CAPC1(INDX)=SUMT2
        XLCRNT1(INDX)=CN(1)/XK1+SUMT3
        CRNT1(INDX)=CN(1)/XK1+SUMT4
        WRITE(8,*)T,VOTP(INDX)
        WRITE(9,*)T,CAPC1(INDX)
        WRITE(10,*)T,XLCRNT1(INDX)
        WRITE(11,*)T,CRNT1(INDX)
        T=T+DELT
        INDX=INDX+1
        IF(T.LE. TMAX)GOTO 650
C
        STOP
        END
C*****************************************************************
```

B.3.2 Computer Simulation Program For Tank Circuit Load Filter

```
C*****************************************************************
C  PROGRAM TO SIMULATE THE PERFORMANCE OF THE TANK CIRCUIT       *
C  FILTER FOR DELTA MODULATED UPS INVERTER                       *
C  HCN.DAT   : INPUT DATA FILE CONTAINS FOURIER COEFFICIENT      *
C  OF THE DELTA MODULATED UPS INVERTER OUTPUT VOLTAGE            *
C  VOTP.DAT  : OUTPUT DATA FILE CONTAINS LOAD VOLTAGE WAVEFORM   *
C  CAPC.DAT  : OUTPUT DATA FILE CONTAINS CAPACITOR CURRENT       *
C  WAVEFORM                                                      *
C  LCRNT.DAT: OUTPUT DATA FILE CONTAINS LOAD CURRENT WAVEFORM    *
C  ICRNT.DAT: OUTPUT DATA FILE CONTAINS INPUT CURRENT WAVEFORM   *
C  SCIOL.DAT: OUTPUT DATA FILE CONTAINS FILTER SHUNT INDUCTOR    *
C  CURRENT                                                       *
C*****************************************************************
       DIMENSION HN(1010),CN(1010),VON(1010),PHIF(1010),
     * VOTP(210),THETA(1010),GAMA(1010),CRNT(1010),CPH(1010),
     * CAPC(1010),CAPH(1010),XLCRNT(1010),XLPHS(1010),CAPC1(210),
     * XLCRNT1(210),CRNT1(210),SCOIL(1010),SCPH(1100),XIND(210)
       OPEN(UNIT=7,FILE='HCN.DAT',TYPE='OLD')
       OPEN(UNIT=8,FILE='VLT.DAT',TYPE='NEW')
       OPEN(UNIT=9,FILE='CAPCT.DAT',TYPE='NEW')
       OPEN(UNIT=10,FILE='LCRNT.DAT',TYPE='NEW')
       OPEN(UNIT=11,FILE='ICRNT.DAT',TYPE='NEW')
       OPEN(UNIT=13,FILE='SCOIL.DAT',TYPE='NEW')
C
C READ FOURIER COEFFICIENTS OF THE DELTA MODULATED OUTPUT
C WAVEFORM
C
       READ (7,*)N1
       DO 10 I=1,N1
 10    READ(7,*)HN(I),CN(I),THETA(I)
C
C READ THE VALUE OF FILTER SERIES INDUCTIVE REACTANCE
C AND THE AND THE LOAD POWER FACTOR
C
       WRITE(6,*)'I/P FLTR SERIES INDUCTOR X1 & THE LOAD PF'
       READ(6,*)X1,XK1
C
C  INPUT SHUNT INDUCTIVE AND CAPACITIVE REACTANCE :
C  FOR TUNING THE TANK CIRCUIT AT THE FUNDAMENTAL FREQUENCY: X2=X3
C
       WRITE(6,*)'I/P FILTR SHUNT INDUCTIVE & CAPACTIVE
     * REACTANCE X2,X3'
       READ(6,*)X2,X3
C
       TH     =0.0
       FR1    = 0.0
```

```
      CRNT(1)=CN(1)/XK1
      CPH(1) =-THETA(1)
      PHIF(1)=0.0
      CAPCR  =0.0
      XK2    =SIN(ACOS(XK1))
      DO 11 I=2,N1
C
C COMPUTE FILTER TRANSFER CHARACTERISTICS :
C MAGNITUDE AND PHASE
C
C
      Z10 =X2*X3+X1*(X3-(X2*(HN(I)**2)))
      Z1  =X2*X3*XK1
      Z2  =X2*X3*XK2*HN(I)
      Y1  =XK1*Z10
      Y2  =HN(I)*(XK2*Z10+X1*X2*X3)
      TF  =SQRT((Z1**2+Z2**2)/(Y1**2+Y2**2))
      PHIF(I)=ATAN2(Z2,Z1)-ATAN2(Y2,Y1)
C
C     COMPUTE OUTPUT VOLTAGE MAGNITUDE AND PHASE
C
      VON(I) =CN(I)*TF
      GAMA(I)=-THETA(I)+PHIF(I)
C
C     COMPUTE FILTER INPUT IMPEDANCE,INPUT CURRENT
C
      ZI1     =HN(I)*XK1*Z10
      ZI2     =(HN(I)**2)*(XK2*Z10+X1*X2*X3)
      ZI3     =HN(I)*(X2*X3+XK2*(X3-(HN(I)**2)*X2))
      ZI4     =XK1*((HN(I)**2)*X2-X3)
      ZT      =SQRT((ZI1**2+ZI2**2)/(ZI3**2+ZI4**2))
      CRNT(I)=CN(I)/ZT
      CPH(I) =ATAN2(ZI4,ZI3)-ATAN2(ZI2,ZI1)-THETA(I)
C
C     COMPUTE FILTER SHUNT CAPACITOR CURRENT...
C
      CAPC(I)=VON(I)*HN(I)/X3
      CAPCR  =CAPC(I)**2+CAPCR
      CAPH(I)=GAMA(I)+ASIN(1.)
C
C     COMPUTE FILER SHUNT INDUCTOR CURRENT
C
      SCOIL(I)=VON(I)/(HN(I)*X2)
      SCPH(I) =GAMA(I)-ASIN(1.)
C
C     COMPUTE LOAD CURRENT...
C
```

```
      XLCRNT(I)=VON(I)/(SQRT(XK1**2+(HN(I)*XK2)**2))
      XLPHS(I) =GAMA(I)-ATAN2(XK2*HN(I),XK1)
      IF(HN(I) .EQ. 6.0)GOTO 12
      TH=VON(I)**2+TH
C
C     COMPUTE NORMALIZED FILTER COST...
C
 12   FR1=(CRNT(I)**2)*HN(I)*X1*2.0+VON(I)*CAPC(I)+2.0*VON(I)*SCOIL(I)
 11   CONTINUE
C
C     CALCULATE TOTAL HARMONIC DISTORTION OF THE LOAD VOLTAGE
C
      THD=100*(SQRT(TH)/VON(2))

C****************************************************************
C  RECONSTRUCT WAVEFORMS OF VARIOUS NODES IN THE LOAD FILTER
C
      FREQ=60.0
      TMAX=20E-3
      XOMGA=4.0*ASIN(1.)*FREQ
      INDX=1
      T=0.0
      DELT=TMAX/200.0
 650  VOTP(INDX)=0.0
      CAPC1(INDX)=0.0
      XLCRNT1(INDX)=0.0
      CRNT1(INDX)=0.0
      XIND(INDX)=0.0
      SUMT1=0.0
      SUMT2=0.0
      SUMT3=0.0
      SUMT4=0.0
      SUMT5=0.0
      DO 700 I=2,1000
      XII=HN(I)*XOMGA*T
      SWX1=VON(I)*COS(XII+GAMA(I))
      SWX2=CAPC(I)*COS(XII+CAPH(I))
      SWX3=XLCRNT(I)*COS(XII+XLPHS(I))
      SWX4=CRNT(I)*COS(XII+CPH(I))
      SWX5=SCOIL(I)*COS(XII+SCPH(I))
      SUMT1=SUMT1+SWX1
      SUMT2=SUMT2+SWX2
      SUMT3=SUMT3+SWX3
      SUMT4=SUMT4+SWX4
      SUMT5=SUMT5+SWX5
 700  CONTINUE
      VOTP(INDX)=CN(1)+SUMT1
      CAPC1(INDX)=SUMT2
```

```
      XLCRNT1(INDX)=CN(1)/XK1+SUMT3
      CRNT1(INDX)=CN(1)/XK2+SUMT4
      XIND(INDX)=CN(1)+SUMT5
      WRITE(8,*)T,VOTP(INDX)
      WRITE(9,*)T,CAPC1(INDX)
      WRITE(10,*)T,XLCRNT1(INDX)
      WRITE(11,*)T,CRNT1(INDX)
      WRITE(13,*)T,XIND(INDX)
      T=T+DELT
      INDX=INDX+1
      IF(T .LE. TMAX)GOTO 650
C
      STOP
      END
C*************************************************
```

Appendix C

To practically verify the predicted results, a single phase half bridge delta modulated UPS inverter is constructed employing power MOSFETs as the switching devices. The inverter is supplied from dc supply of 100 volts which is split up equally using two capacitor of equal value (6000 μF) connected in series.

Figure C.1 shows the practical circuit used to realize the delta modulator circuit. The Op-Amp used to realize the integrator should have very low dc offset. This will ensure better encoding and decoding of the reference signal. The hysteresis comparator should be a fast acting device.

The timing and the logic circuit block diagrams used in processing the delta modulator output waveform are shown in Fig. C.2 and C.3 respectively. The switching signals at the output of the logic circuit are used to control the inverter switching devices through the MOSFET's driving circuit.

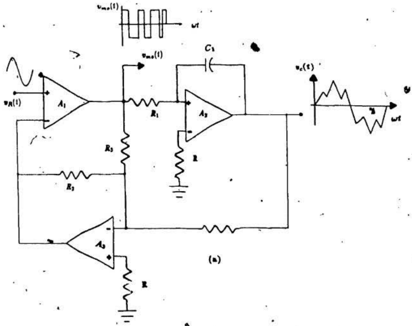

Figure C.1: Circuit diagram of the rectangular wave delta modulator.

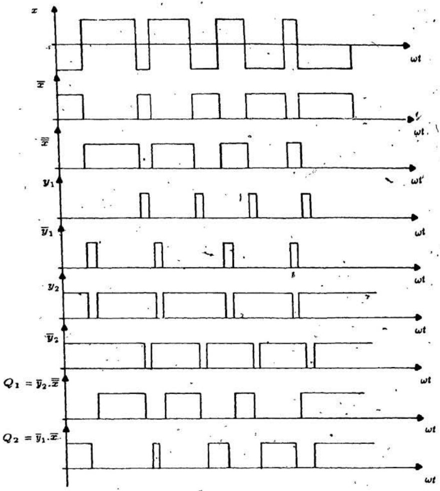

Figure C.2: Timing diagram for processing the rectangular wave delta modulator output waveform.

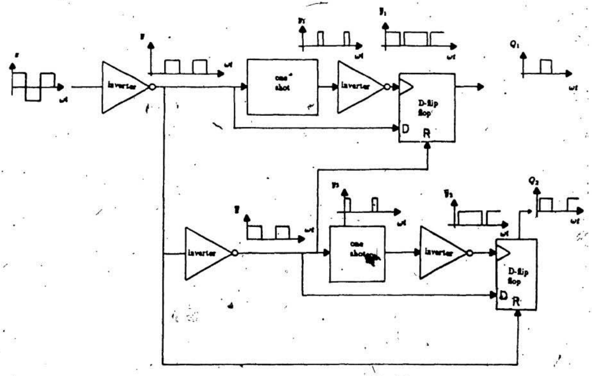

Figure C.3: Block diagram of the logic circuit for processing the rectangular wave delta modulator output waveform