SOFTWARE CONTROLLED DELTA PWM INVERTERS

RAJIV KUMAR SRIVASTAVA

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BY

©RAJIV KUMAR SRIVASTAVA, B.Sc., B.Tech.

A thesis submitted to the School of Graduate
Studies in partial fulfillment of the
requirements for the degree of
Master of Engineering

Faculty of Engineering and Applied Science
Memorial University of Newfoundland
January 1988

St. John's Newfoundland Canada

ISBN 0-315-45072-X

ABSTRACT

The family of delta modulators can be characterized as uniformly sampled, zero hysteresis, bang-bang type of controllers. Such systems are widely used in communication and instrumentation applications for encoding band-limited analog signals into binary waveforms i.e. A/D conversion. The inherent V/f ratio control and low order harmonic attenuation of modulated output are some of the attractive features of delta modulation which can be employed in voltage control of inverters and rectifiers.

Delta modulated voltage source inverters, implemented by analog means, have shown improved performance over conventional PWM inverters. However, software controlled delta modulated inverters require less complex control circhitry and offer easier control of system parameters. This thesis is the study of the performance of voltage source inverters using different types of delta modulation strategies. Continuous time variables of delta modulators transformed into discrete time domain are able to generate switching waveforms to control a single phase voltage source inverter. Three types of delta modulation strategies are investigated. The results obtained from their implementation are compared and a suitable choice of a modulation strategy for on-line inverter operation is investigated.

The effect of filter coefficients, input signal amplitude, sampling rate, and tracking step (Δ) on the modulator performance is presented. In order to study the harmonic behaviour of the inverter output, a Fourier analysis is carried out.

The predicted performance results confirm the advantageous features of the delta modulation techniques.

For experimental verification, a single phase bridge inverter and associated base drive circuits are built. Microprocessor-generated switching signals are applied to control the operation of the inverter. The inverter is tested with passive as well as dynamic loads and a comparison between various modulation techniques is presented. Implications for further research are discussed.

ACKNOWLEDGEMENTS

The author would like to express his deep and sincere gratitude to his supervisors, Dr. M. A. Rahman, and Dr. J. E. Quaicoe of the Faculty of Engineering and Applied Science, for their continual support, encouragement, and many useful suggestions which improved the quality of this thesis and also made the work enjoyable.

The support shown by Dr. T. R. Chari, Associate Dean of Engineering, and other professors of the Faculty of Engineering and Applied Science were highly appreciated.

Special thanks are due to the author's colleagues. The hours of help, ideas, and moral support offered by fellow graduate students particularly M. A. Choudhury and K. S. R. Prasad were appreciated beyond words and have made this experience a memorable one.

I am indebted to my wife, Rani who gave many hours of her time and unceasing efforts in editing and bringing this thesis to its final form.

Lastly, I would like to dedicate this work to my mother, Kamla and my late father, Bishun Kant whose wisdom and guiding influence inspired me to initiate and achieve my goals.

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CHAPTER 1

INTRODUCTION

The advent of computer controlled techniques employed in voltage source inverters has revolutionized the field of dc/ac power conversions. Computer control of dc/ac converters and variable speed drives offers a viable alternative over hardware control. High performance dc/ac converters, whether software or hardware controlled, are characterized by the following features:

1. wide control range of output voltage and frequency
2. high converter efficiency
3. fast system response
4. good output spectral characteristics
5. small filter components, and
6. low acoustic noise levels.

Voltage source inverters employing various modulation techniques have been shown to realize many of the above features. Output harmonic contents and spectral characteristics of such inverters depend on the modulation technique employed. The output voltage harmonic content is the factor which determines the choice of modulation technique.

The most common modulation techniques presently in use are the multiple pulse modulation, sinusoidal pulse width modulation, optimized pulse width modulation, and the delta modulation. Pulse width modulation (PWM) voltage

source inverters are the outcome of developments in modulation strategies. Various real-time and off-line PWM strategies have been proposed and implemented through both digital and analog means. In the past few years researchers have focused on sine PWM and subsequently delta PWM schemes for inverter applications. Extensive research on these modulation schemes showed improved performance of voltage source inverters over other conventional voltage source inverters.

Sine PWM technique has been an area of research for the past several years. This technique was first proposed and implemented using analog components. Microprocessor-based sine PWM and optimised PWM inverters were later proposed. Microprocessor-based as well as analog sine PWM inverters have shown good performances. However, inverters employing this modulation scheme require relatively complex control circuitry and hence involve associated cost.

In the past few years, delta modulation scheme has received attention in PWM inverter applications. The interest is due to various inherent properties it offers when applied in inverter operation. Constant V/f ratio control and wider output frequency range are the most attractive features of delta modulation.

Analog implementation of delta modulation scheme and its basic features in voltage source inverters have been reported [1,2]. However, its digital implementation was not done prior to this research. Implementation of delta modulated PWM inverters through analog means has resulted in good performance of such systems [1,3]. These results motivated researchers to investigate the possibility of

implementing delta modulated PWM inverter with microprocessor control. Software control of delta modulation offers ease of variation in controlling parameters and optimization of system performance.

The main objectives of this thesis are to identify various switching strategies for delta modulated PWM inverters and develop a suitable methodology to generate delta modulated switching signals under software control. Another objective is to examine the spectral characteristics of existing modulation systems in the context of PWM voltage source inverters. Such a system can be characterized as zero hysteresis, bang-bang type controllers.

The next few sections of this chapter deal with a brief description of literature review followed by objectives of the present work and thesis organization.

1.1. Literature Review

The need for voltage and frequency control and minimum tolerable harmonic content at the inverter output voltage have resulted in the pulse width modulated (PWM) techniques of inverter switching. Earlier modulation techniques employed in inverter applications were single pulse and multiple pulse modulation [1-6]. These modulation techniques were capable of controlling the inverter output voltage and frequency, but could eliminate only selected harmonics at the inverter output.

At a later stage the sinusoidal pulse width modulation (SPWM) although needing more complex control circuitry, was proved to have improved

performance in inverter applications [7,8]. The SPWM is a variation of multiple pulse modulation where the pulse duration and number of pulses per half cycle are determined by comparing a modulating sine wave and a triangular carrier wave.

At first sine pulse width modulation was incorporated in asynchronous PWM mode and later, the synchronous mode of this PWM technique was introduced [9]. In asynchronous mode the sine wave is compared with a constant frequency carrier wave. The disadvantage of such operation is that with constant frequency carrier, the ratio of sine and triangular wave frequencies cannot be maintained at an integer value. This gives rise to sub-harmonics at the inverter output when the frequency ratio is not the desired integer value. This problem is overcome in synchronized sine PWM mode where the carrier wave frequency is varied with the modulation wave frequency to keep the frequency ratio to the desired integer value. However, this additional requirement for synchronized PWM operation, complicates the implementation of such a technique. The principal disadvantage of synchronous SPWM technique is that the carrier frequency must vary over a wide range as the output frequency changes. Wide variation in carrier frequency is not very practical especially in inverters for ac motor drive applications. Furthermore, as the carrier frequency is increased, the number of commutations per cycle increases, which in turn gives rise to increased commutation losses in the power circuit of the inverter. A very low carrier frequency is also not desired, since the motor constants become insufficient for adequate smoothing of current drawn by the motor. To overcome this problem with fixed ratio method, pulse

width modulation with ratio changing at various operating frequencies was suggested [9-11]. In the variable ratio scheme the carrier signal steps through a sequence of ratios as the operating frequency is increased and hence maintains a high carrier frequency throughout the operating range, thereby producing only high frequency harmonics at the output of the inverter. These high frequency harmonics are easily filtered out in ac motor drives.

The analog sine PWM technique is based on natural sampling of the reference signal. However, microprocessor-based sine PWM techniques [12-15] require regular sampling, so as to ensure the synchronized operation. In a microprocessor-based sine PWM system, the sine modulating wave is sampled at a regular interval and the switching points are determined from crossover points of the carrier triangular wave. A sample and hold circuit, operating at the carrier frequency maintains a constant level during the inter sample period. As a result of this operation, the output sine PWM switching waveforms have pulse widths proportional to the amplitude of the modulating wave.

Another approach, based on the minimization of certain performance variables, used optimal PWM switching strategies [16-18]. Elimination or minimization of particular harmonics, minimization of harmonic current distortion, peak current, torque ripple etc., are such examples. In contrast to the natural and regular sampling, it has been a usual practice to generate optimised PWM switching waveforms by defining a general PWM waveform in terms of a set of switching angles rather than determining these switching angles using numerical methods.

The most recent technique to generate pulse width modulated switching signals is delta modulation. Essentially, delta modulation techniques have been used in digital communication to convert analog signals into digital codes before transmission [3]. The delta modulation technique requires a very simple circuit implementation, and provides a smooth transition between PWM and single pulse modes of operation [1,2]. It also offers constant volts per hertz operation without the need of additional circuit complexity. The inherent characteristics of delta modulation process are the linear variation of fundamental voltage with frequency up to base frequency and constant voltage beyond the base frequency. These in turn provide constant torque characteristic up to base frequency and constant power characteristic beyond the base frequency. The harmonic content in delta modulation is low and the dominant harmonics are at or near high carrier frequency.

Analytical and experimental results have proved that the delta modulation technique has a superior performance over other commonly used PWM techniques [1,2]. Subsequent researchers have made an attempt to implement delta modulation technique using discrete digital and analog circuit components [19,20]. Recently, delta modulation techniques for resonant link inverters have been reported [20-23]. Since the frequency of switching pattern is generally limited by switching losses of the device used in the inverter. Therefore, by using zero switching loss inverter topologies [22-23], much higher switching frequencies are achievable. Although the digital delta modulator, in its various forms, has been reported by various researchers in the past [24-35], no attempt has been made to

develop a software implementation of delta modulation (DM) techniques for inverter applications. The models and implementation of delta modulation techniques described by various researchers [29-35] are mainly for communication applications and hence are not easily applied to inverters.

1.2 Present Work

The performance of delta modulation technique in inverter applications has been established. Although analog implementation, analysis and digital implementation of delta modulation technique have been reported [18-20], so far no significant work on software controlled delta modulation strategies has been carried out. The present work explores the implementation of delta modulation techniques under software control. A detailed and comprehensive analysis of various forms of delta modulation techniques under software control is presented. A systematic approach for generating the delta modulated switching waveforms is outlined.

Three types of delta modulation techniques are studied: linear delta modulation, exponential delta modulation and sigma delta modulation. First, a linear delta modulator (LDM) is implemented and its performance characteristics are obtained. The effects of variation in various modulator parameters on the harmonic content and power spectra of the inverter output voltage are studied.

The work is then extended to exponential delta modulation, and sigma delta modulation. The results obtained from the implementation of exponential delta

modulator and the sigma delta modulator are compared with those of linear delta modulator. For experimental verification of theoretical results, a single phase (1–ϕ) transistor inverter and associated base drive circuitry were built. The switching signals generated by various types of delta modulators were then applied to the inverter. Experimental results thus obtained show a close correspondence with the theoretical results.

1.3 Thesis Organization

In the following chapter, various schemes of Delta Modulation are described. The principle of operation and theoretical analysis of different type of delta modulation techniques are discussed.

Chapter 3 contains the description of software implementation of the three main types of delta modulators. The implementation criteria and step by step procedure for software generation of delta modulated switching signals are discussed.

Chapter 4 contains the results obtained from simulation of different modulation strategies. DC, sinusoidal input response and various output characteristics, due to different parameter variations, are obtained. Harmonic analysis of various delta modulator output voltages is performed, and the output voltage harmonic spectra are obtained.

Chapter 5 presents the experimental results of software controlled delta modulators. Switching signals generated by different modulators are used to

control a 1-ϕ bridge inverter. Inverter output voltage harmonic contents are obtained by using spectrum analyzer. The results of the software controlled delta modulated inverter for resistive and dynamic load conditions are obtained. The performance of various delta modulators, based on theoretical and experimental results, is compared and results tabulated.

Chapter 6 presents the summary, conclusion, and recommendations for further research.

CHAPTER 2

THE DELTA MODULATION

In this chapter the principle of operation and detailed analysis of four types of delta modulation systems are described. Analytical expressions are developed to describe the characteristics of each system. A brief comparison between various forms of Delta Modulation is made, and the characteristic features of each are compared.

For induction motors, the general requirement is to operate the motors at desired slip and keep the voltage to frequency (V/f) ratio constant to maintain the flux density at a particular value. For permanent magnet synchronous motors, the starting characteristics require the same V/f characteristics up to the base speed. Also a substantial increase in inverter switching frequency is required in order to minimize the lower order harmonics at the output of the inverter. These requirements are inherent features of delta modulation technique. By employing the delta modulation technique, a smooth transition between the PWM and square wave modes of operation and constant V/f operation is possible.

2.1 Linear Delta Modulator

The schematic block diagram of a linear delta modulator is shown in Fig. 2.1. The modulator encodes a band-limited analog signal x(t), into a two-level

output y(t). The output binary waveform is fed back through an integrator and compared with the reference signal. The error signal is quantized into one of two possible levels depending upon its polarity. The quantizer (comparator) output is regularly sampled by a sampler operating at a clock frequency (f_s) to produce the output binary pulses. The closed loop arrangement of the modulator ensures that the integrated output faithfully tracks the input reference signal.

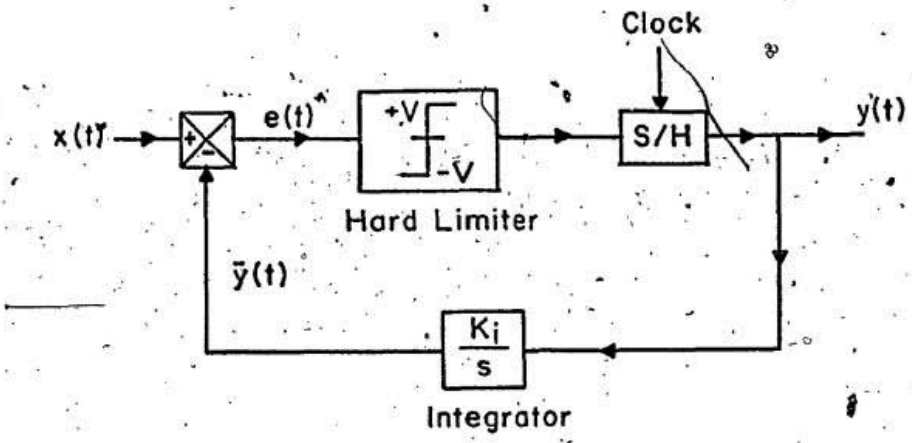


Fig. 2.1 Linear Delta Modulator

2.1.1 Principle of Operation

The delta modulator converts an analog band limited signal into a binary output signal y(t). The relationship between x(t) and y(t) is such that y(t) is a binary representation of x(t), where the rate of occurrence of each binary pulse is

directly proportional to the instantaneous slope of reference signal x(t) [3]. If the slope of the input signal x(t) is positive, then while this condition exists, the output waveform y(t) has more positive pulses than negative ones. This situation is reversed when x(t) has a negative slope.

When these output pulses are integrated by an integrator in the feedback path, the resulting waveform $\bar{y}(t)$ consists of steps having magnitude $\pm \Delta$ volts and duration T seconds, which oscillate about the analog input signal x(t). The difference between x(t) and $\bar{y}(t)$ is the error signal e(t). This error signal is quantized to limits $\pm V$ volts. Here, the sign of the error signal is quantized and not the magnitude. The output of the quantizer is sampled at every T seconds to produce y(t) pulses.

If at an instant, the error signal $e(t) \geq 0$, a positive pulse will be produced at the output of the modulator. When this pulse is integrated, $\bar{y}(t)$ is increased by a positive step $+\Delta$. This increase in $\bar{y}(t)$ is subtracted from x(t) and a change in the magnitude of the error signal occurs. If the error has not become negative by the next clock instant, the output of the modulator will again be a positive pulse. As long as $e(t) \geq 0$ at successive clock instants, a sequence of positive pulses is produced. Eventually, $\bar{y}(t)$ will become greater than x(t). At that clock instant $e(t) < 0$, thereby producing a negative pulse at the output of the modulator, resulting in a diminution in the $\bar{y}(t)$ waveform by an amount $-\Delta$. Thus when an input is present, the modulator attempts to minimize the error waveform, by varying the polarity of the pulses at the output of the modulator at successive clock instants.

It should be noted that when the slope of the sinusoid is large and negative, more negative pulses are generated than positive pulses. The situation is reversed when the slope is large and positive. At maxima and minima of the reference signal, where the slope is close to zero, there are approximately equal numbers of positive and negative output pulses. Thus the modulator attempts to generate a y(t) pattern whose mean value approximates the mean value of the slope of the sinusoid over a short period of time.

A practical delta modulator encoder has a zero order hold (ZOH) circuit following the sampler. This circuit causes its input value to be held at a constant amplitude for one clock period. As a result, the output waveform y(t) now consists of binary levels which may or may not change at clock instants. The output of a linear delta modulator can thus be described by:

$$y(t) = \sum_{k=0} V \, \mathrm{Sgn}[\, x(kT) - \bar{y}(kT) \,] \, \delta(t-kT) \qquad (2.1)$$

where,

V is the level of quantization

Sgn(t) is the sign function : +ve for $t \geq 0$ and -ve for $t < 0$

x(kT) is the reference signal amplitude at k^{th} clock instant

$\bar{y}(kT)$ is the predicted signal at k^{th} clock instant

and T is the sampling interval

2.1.2 Idling Characteristic

Idling characteristic of linear delta modulator (LDM) is shown in Fig. 2.2. When LDM is turned on and no input is applied, after sufficient settling time, the output of the LDM has a sequence of ...010101... . This sequence represents a square wave output. However, since no input is applied, this state of the modulator is called the idling state.

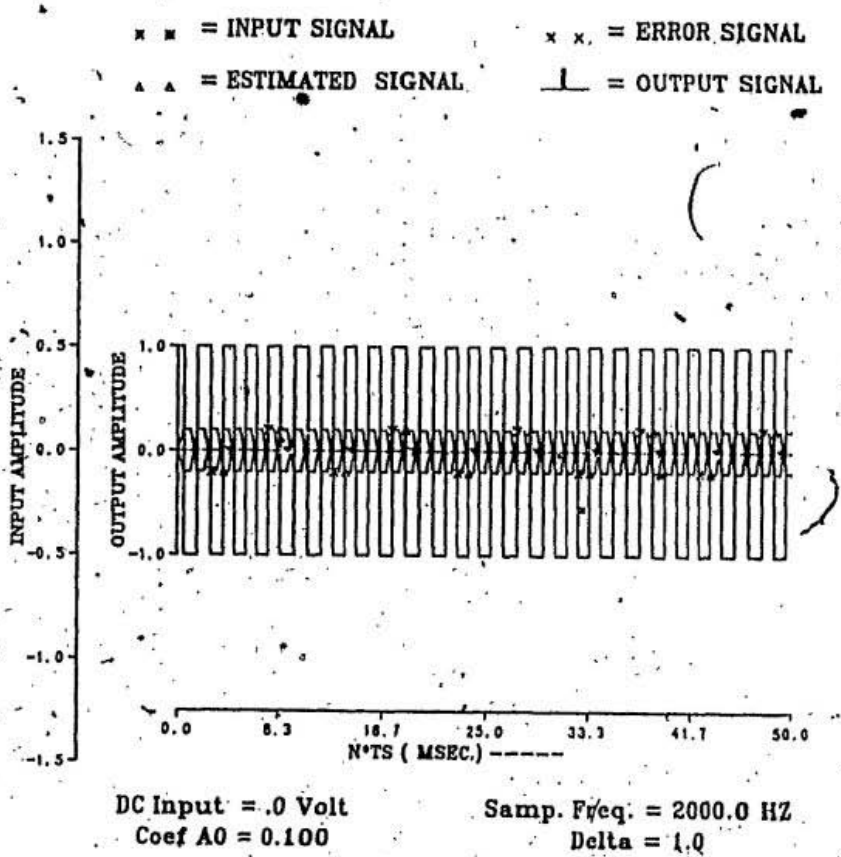


Fig. 2.2 Idling Characteristic of LDM

2.1.3 Overload Characteristic

In order to ensure that the feedback signal $\bar{y}(t)$ tracks the reference, a slope overload condition must be satisfied. This requires that $\frac{d}{dt}x(t)$ should never exceed the maximum rate of change of $\bar{y}(t)$. Let

$$x(t) = A \sin(2\pi ft) \tag{2.2}$$

then,

$$x'(t) = 2\pi fA\cos(2\pi ft) \tag{2.3}$$

with maximum slope of

$$x'(t) = 2\pi fA \tag{2.4}$$

and maximum slope of

$$\bar{y}(t) = \frac{V}{T} = Vf_s \tag{2.5}$$

where,

f_s is sampling frequency in Hz

f is the frequency of the reference signal in Hz

V is the comparator output switching level

A is the amplitude of the input sinusoidal signal

From equations (2.4) and (2.5), the slope overload condition can be written as :

$$2\pi fA \leq Vf_s \tag{2.6}$$

Fig. 2.3 represents the slope overload characteristics of various delta modulators. For linear delta modulator, the slope overload occurs at a frequency $f = f_b$ which is called base frequency. For operating frequencies higher than the base

frequency, the LDM is overloaded and can not track the input signal.

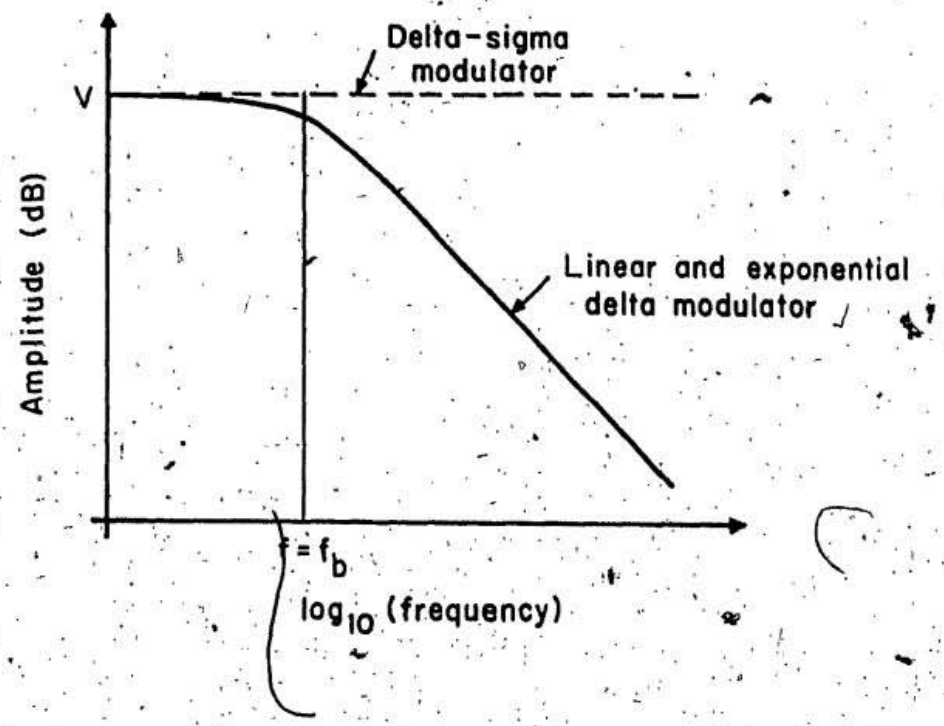


Fig. 2.3 Overload Characteristics of various delta modulators

2.1.4 Amplitude Range

The maximum amplitude A_{max} of the input sinusoid which does not overload the encoder is given by the equality of equation (2.6), i.e.,

$$A_{max} = \frac{V f_s}{(2\pi f)} \qquad (2.7)$$

The ratio of A_{max} and the minimum value of A which gives an acceptable decoded signal to noise ratio, is referred to as the dynamic range (DR) of the input. However, the amplitude range (AR) is defined as the ratio of A_{max} and that value of the input voltage amplitude which overloads the encoder. Therefore,

$$AR = \frac{\text{Signal amplitude which overloads the encoder}}{\text{Signal amplitude which just disturbs the idling pattern}}$$

The value of the input signal which just disturbs the idling pattern is, $\frac{V}{2}$ [3], therefore,

$$AR = \frac{A_{max}}{\frac{V}{2}}$$

$$= \frac{Vf_s}{[(2\pi f)\frac{V}{2}]}$$

$$= \frac{f_s}{\pi f} \qquad (2.8)$$

AR is maximized by ensuring that the highest frequency to be encoded is in excess of the Nyquist rate [3].

2.2 Exponential Delta Modulator

The exponential delta modulation system (EDM) was first described by Johnson [29]. The perfect integrator shown in Fig. 2.1, can be replaced by an RC combination so that integration of a constant input results in an output which follows an exponential curve instead of a straight line. Hence, this configuration is called an exponential delta modulator.

If a perfect integrator rather than an RC circuit is used in the encoder, the predicted waveform $\bar{y}(t)$ is composed of straight lines which have either positive or negative slopes of equal magnitude. The polarity of these slopes only change when the binary levels of y(t) change. On the other hand, if RC circuit is used, the shape of $\bar{y}(t)$ becomes exponential. The schematic block diagram of EDM is

shown in Fig. 2.4.

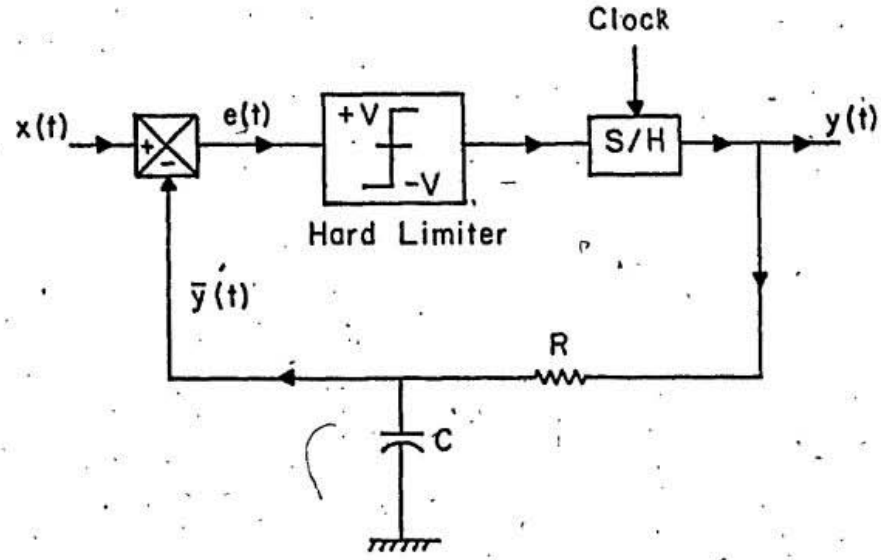


Fig. 2.4 Exponential Delta Modulator

2.2.1 Principle of Operation

A continuous sequence of 1,1,1... applied to the RC circuit causes $\bar{y}(t)$ to rise exponentially to the voltage representing a logic one. Thus when encoding, the increase or decrease in $\bar{y}(t)$ following a change in the binary level of y(t) depends on the actual value of $\bar{y}(t)$.

Consider the value of $\bar{y}(t)$ to be positive at a value close to +V just prior to a sampling instant. If y(t) becomes a logic 1, $\bar{y}(t)$ will increase and if y(t) becomes a logic 0, it will decrease. If the changes in the values of $\bar{y}(t)$ are compared one clock period later, the negative change is larger than the positive

change. This is because the capacitor C has a voltage difference which is small when $y(t)$ is a logic 1 but large when $y(t)$ is a logic 0. The change in $\bar{y}(t)$ is a function of the difference between the voltage to which the capacitor is being charged and the actual voltage on the capacitor.

It is, therefore, apparent that by replacing a perfect integrator with an RC circuit in the feedback loop, the values of $\bar{y}(t)$ are more difficult to estimate. Further, the amplitude range and overload characteristics are also modified [16].

The transfer function of the RC integrator in the feedback path of Fig. 2.4 is given by:

$$H(j\omega) = \frac{1}{(1+j\omega CR)} \tag{2.9}$$

assuming,

$$f_b = \frac{1}{2\pi RC} = \frac{1}{2\pi T_1} \tag{2.10}$$

$$H(j\omega) = \frac{1}{(1+j\frac{f}{f_b})}$$

$$= \frac{f_b}{(f_b+jf)} \tag{2.11}$$

For input frequencies f, when $f >> f_b$, equation (2.11) becomes,

$$H(j\omega) = \frac{f_b}{jf} \tag{2.12}$$

But the transfer function of a perfect integrator is given by,

$$H_I(j\omega) = \frac{1}{j2\pi f}$$

Thus from equation (2.12) it follows that, except for a scaling factor, equation (2.12) is the equation of a perfect integrator. Thus if f_b is chosen to be much

smaller than the lowest input frequency to be encoded, then the RC circuit performs as an integrator and predicted signal $\bar{y}(t)$ is composed of straight line segments.

2.2.2 Idling Characteristic

In order to understand the idling behavior of EDM, consider the situation when power to EDM is switched on and there is no input signal. The output voltage of the encoder will be ± V volts. Suppose, the initial output voltage of EDM is - V, the capacitor will charge from 0 to - V and the error signal $|x(t) - \bar{y}(t)|$ will be positive since input signal x(t) is zero. Positive error signal will cause y(t) to switch to + V and $\bar{y}(t)$ to start to charge to this positive voltage.

If $\bar{y}(t)$ becomes positive by the next sampling time, the error will be negative and y(t) will switch to - V. However, if $\bar{y}(t)$ is still negative at the next sampling instant y(t) will maintain a voltage of +V. Eventually, $\bar{y}(t)$ will go positive at a sampling instant and y(t) will have a negative level -V. Thus after a certain settling time, y(t) will show a ...1010... i.e. square wave idling pattern. This occurs irrespective of the initial polarity of the output signal y(t).

The idling pattern of EDM is the same as LDM. The RC time constant of EDM is much greater than the sampling period thereby ensuring that RC circuit behaves like a perfect integrator and hence maintains $\bar{y}(t)$ close to zero during idling period. Idling characteristic of EDM is shown in Fig. 2.5.

It is observed that during the idling period, due to presence of a sample and hold circuit, the output waveform y(t) is a square wave and $\bar{y}(t)$ is a small triangular wave. These waveforms are shown in Fig. 2.6.

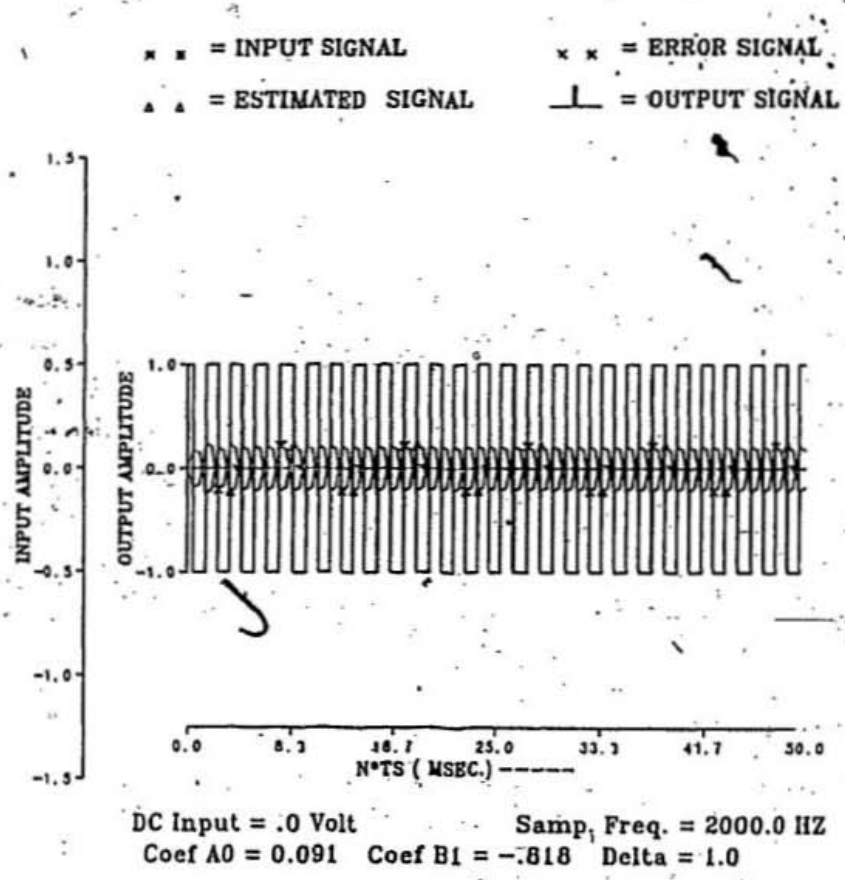


Fig. 2.5 Idling Characteristic of EDM

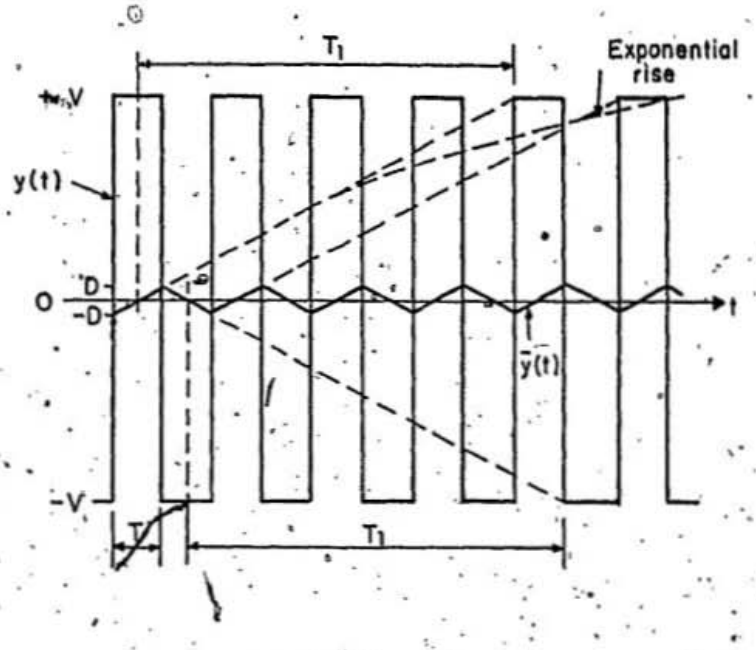


Fig. 2.6 Idling Waveform in EDM

Time constant T_1 is found by drawing a tangent at the origin of $\bar{y}(t)$ curve to intersect the $y(t)$ waveform at V. Thus T_1 is the time between the origin and the point of intersection. By applying the properties of similar triangle:

$$\frac{D}{\frac{T}{2}} = \frac{V}{T_1} \tag{2.13}$$

From equation (2.10), $T_1 = \frac{1}{2\pi f_b}$. Therefore,

$$D = \frac{VT}{2T_1} = \frac{\pi V f_b}{f_s} \tag{2.14}$$

where,

f_b is the characteristic frequency of the RC combination

$f_s = \frac{1}{T}$ is the sampling frequency

D is the amplitude of the predicted signal during idling condition of EDM

2.2.3 Overload Characteristic

In exponential delta modulator (EDM), the maximum rate of increase in predicted signal $\bar{y}(t)$ is exponential. Suppose, the input signal $x(t)$ is a sine wave of amplitude A. Overload condition is defined as the situation where the slope of the signal is equal to the slope of the exponential at some particular amplitude, but at all other amplitudes the slope of the signal is less than that of the exponential. Let

$$\begin{aligned} x(t) &= A \sin(\omega t) \\ x'(t) &= A\omega \cos(\omega t) \\ &= \omega[A \cos(\omega t)] \\ &= \omega\sqrt{A^2 - x^2(t)} \end{aligned} \tag{2.15}$$

Assuming that the EDM is tracking correctly, then the instantaneous value of $\bar{y}(t)$ i.e. the voltage across the capacitor C closely approximates to $x(t)$. When $x(t)$ is increasing monotonically with time, $\bar{y}(t)$ changes exponentially and its slope is the voltage difference between the aiming potential V and the voltage $x(t)$ on the capacitor divided by the RC time constant T_1.

Therefore, the slope of the exponential $= \frac{V - x(t)}{T_1}$ The slope of the sine wave at any amplitude $= \omega\sqrt{A^2 - x^2(t)}$

The difference in slopes between the signal $\bar{y}(t)$ and $x(t)$ is:

$$D = \frac{V - x(t)}{T_1} - \omega\sqrt{A^2 - x^2(t)} \tag{2.16}$$

when x(t) is decreasing monotonically, the slope of y(t) is:

$$= -\frac{V - x(t)}{T_1}$$

and the slope of x(t) will be negative. Equation (2.16) is therefore valid for all x(t).

The slope difference D is a function of x(t). As long as the slope of y(t) remains greater than the slope of x(t), the overload condition is avoided. In order to find the value of x(t) which just causes slope overload, we calculate the value of x(t) for which D is a minimum (i.e. the value of the instantaneous input for which the two slopes are nearly equal). It is determined from equation 2.16.

Differentiating equation (2.16) with respect to x(t) :

$$\frac{dD}{dx(t)} = -\frac{1}{T_1} + \frac{\omega x(t)}{\sqrt{A^2 - x^2(t)}} \tag{2.17}$$

equating equation (2.17) to zero and solving for x(t) gives:

$$\frac{x(t)}{\sqrt{A^2 - x^2(t)}} = \frac{1}{\omega T_1}$$

$$x(t) = \frac{A}{\sqrt{1 + \omega^2 T_1^2}} \tag{2.18}$$

D will be minimum if $\frac{d^2D}{dx^2(t)} > 0$. Differentiating (2.17) once again yields:

$$\frac{d^2D}{dx^2(t)} = \omega[A^2 - x^2(t)]^{-1/2} + \omega x^2(t)\,[A^2 - x^2(t)]^{-3/2}$$

$$= \omega[A^2 - x^2(t)]^{-1/2}\left[1 + \frac{x^2(t)}{A^2 - x^2(t)}\right] \tag{2.19}$$

Substituting the value of x(t) from equation (2.18) into equation (2.19) gives:

$$\frac{d^2D}{dx^2(t)} = \omega\left[A^2 - \frac{A^2}{1+\omega^2T_1^2}\right]^{-1/2}\left[1 + \frac{A^2}{1+\omega^2T_1^2}\left(A^2 - \frac{A^2}{1+\omega^2T_1^2}\right)^{-1}\right]$$

$$= \omega \left[\frac{A^2 + \omega^2 T_1^2 A^2 - A^2}{1 + \omega^2 T_1^2} \right]^{-1/2} \left[1 + \frac{A^2}{1 + \omega^2 T_1^2} \left\{ \frac{A^2 + \omega^2 T_1^2 A^2 - A^2}{1 + \omega^2 T_1^2} \right\}^{-1} \right]$$

$$= \frac{1}{A\omega^2 T_1^3} \left[1 + \omega^2 T_1^2 \right]^{3/2} \qquad (2.20)$$

Since all constants in equation (2.20) are positive, therefore,

$$\frac{d^2D}{dx^2(t)} > 0$$

Equation (2.18) thus gives the value of x(t) for which D is a minimum. Hence substituting x(t) from equation (2.18) in equation (2.16) gives

$$D_{min} = \frac{V}{T_1} - \frac{1}{T_1} \frac{A}{\sqrt{1+\omega^2 T_1^2}} - \omega \left[A^2 - \frac{A^2}{1+\omega^2 T_1^2} \right]^{1/2}$$

$$= \frac{V - A\sqrt{1+\omega^2 T_1^2}}{T_1} \qquad (2.21)$$

The overload condition is characterized by $D_{min} = 0$, therefore equation (2.21) for overload condition yields:

$$A_{max} = \frac{V}{\sqrt{1+\omega^2 T_1^2}} \qquad (2.22)$$

This gives the desired relationship between A and ω and hence the overload characteristic. From equation (2.22) one obtains:

$$A_{max} = V|H(j\omega)| \qquad (2.23)$$

where

$$H(j\omega) = \frac{1}{\sqrt{1+\omega^2 T_1^2}}$$

The overload characteristic of EDM, described by equation (2.22) is shown in Fig. 2.3.

From fig. 2.3 it is observed that the overload characteristic of EDM has the same slope as the transfer characteristic (output voltage vs. frequency) of RC network. The curve falls off at 6db per octave with increasing frequency, which corresponds to the slope limiting condition (i.e. the EDM will be overloaded whenever the slope of the input signal becomes too high).

The overload characteristic gives the values of amplitude A_{max} for each frequency to avoid overload condition. For operating frequencies, $f < [redacted]$ amplitude A can be as large as V before overload occurs. At higher frequencies, $f >> f_b$, the RC circuit behaves like perfect integrator and the maximum value of A (A_{max}) decreases with frequency.

2.2.4 Amplitude Range (AR)

The amplitude range (AR) for EDM is defined as:

$$AR = \frac{A_{max}}{D} \tag{2.24}$$

Where, A_{max} and D are given by equations (2.22) and (2.14) respectively.

$$AR = \frac{V}{\sqrt{[1+\omega^2 T_1^2]}} \Big/ \left[\frac{\pi V f_b}{f_s}\right]$$

substituting $T_1 = \frac{1}{2\pi f_b}$ yields:

$$AR = \frac{V}{\sqrt{1+\omega^2 \frac{1}{4\pi^2 f_b^2}}} \Big/ \left[\frac{\pi V f_b}{f_s}\right]$$

$$= \frac{f_s}{\pi \sqrt{f_b^2 + f^2}} \tag{2.25}$$

Where,

f_s is the clock frequency

f_b is the characteristic frequency of the RC network

f is the signal frequency

In the slope limiting mode when $f >> f_b$, the AR of EDM as given by equation (2.24) is the same as AR of LDM given by equation (2.8). In EDM the value A_{max} is independent of sampling rate whereas for linear delta modulator, the value of A_{max} can be increased by increasing sampling rate f_s (since A_{max} is proportional to f_s for LDM).

2.3 Sigma Delta Modulator

Linear delta modulator, preceded by a single integrator is called Delta Sigma Modulator or more precisely Sigma Delta Modulator (SDM) [3]. The schematic block diagram of LDM with an integrator at the input is shown in Fig. 2.7.

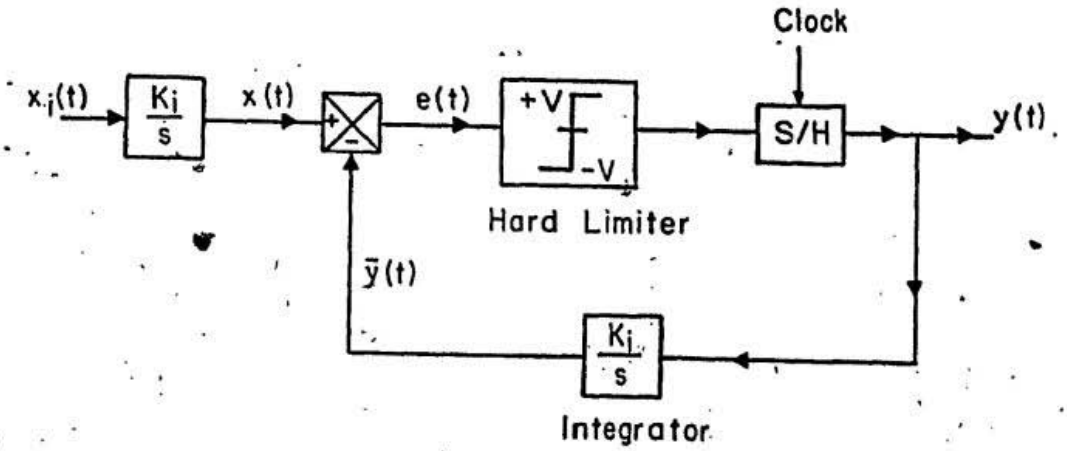


Fig. 2.7 Linear Delta Modulator with Integrator at the input

The two integrators in Fig. 2.7 can be replaced by one integrator after the error detector. Since,

$$\int x(t)dt - \int y(t)dt = \int e(t)dt$$

The equivalent form of figure 2.7 can therefore be represented by Fig. 2.8.

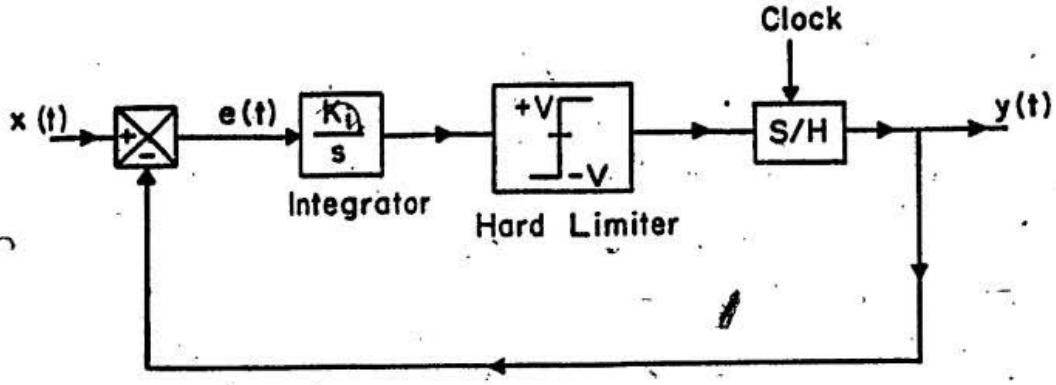


Fig. 2.8 Sigma Delta Modulator

2.3.1 Principle of Operation

The principle of operation of sigma delta modulator is similar to that of linear delta modulator. The integration process in SDM takes place in the feed-forward path. Thus, in SDM the sign of integrated error is quantized rather than quantizing the sign of error signal, as in case of LDM and EDM.

The arrangement shown in fig. 2.8 is advantageous when the energy distribution in the spectrum of input signal is substantially flat. The integrator at the input can be regarded as shaping the flat spectrum to have attenuation at higher frequencies [29]. The advantage of prefiltering is related to the processes of over-sampling and subsequent rejection of out-of-band noise [36]. Due to these

properties, harmonic content of the output voltage of SDM are lower than that of LDM and EDM. Therefore, harmonic contents of the output voltage of an inverter employing SDM scheme are also low.

2.3.2 Idling Characteristic

Idling characteristic of SDM is similar to those of LDM and EDM. When SDM is initially turned on, after sufficient settling time, the modulator produces a ...1010... pattern at its output. Fig 2.9 shows the idling characteristic of SDM.

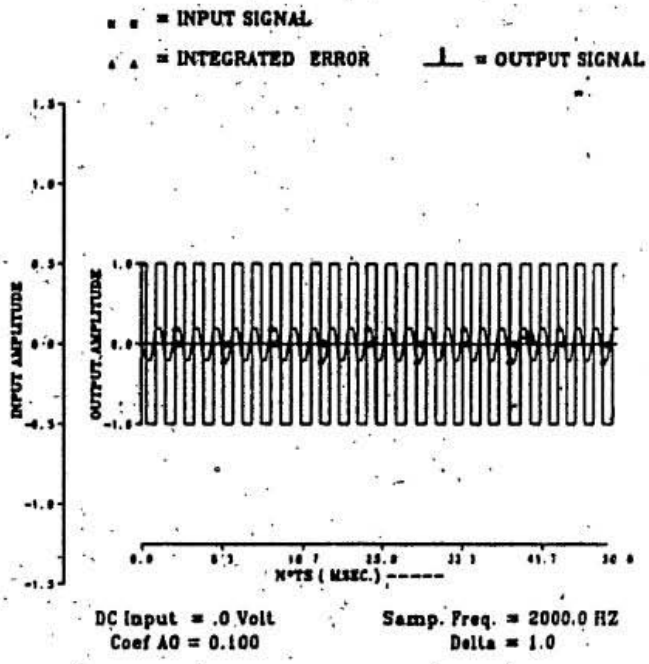


Fig. 2.9 Idling Characteristic of SDM

2.3.3 Overload Characteristic

The repositioning of the integrator in the SDM compared to LDM results in some performance changes [3]. Let us assume that the input signal applied to SDM be sinusoidal as given by

$$x(t) = A\sin\omega t \tag{2.26}$$

then,

$$\int x(t)dt = \frac{-A}{\omega}\cos\omega t + C \tag{2.27}$$

setting initial conditions to 0, the above equation yields:

$$\int x(t)dt = \frac{-A}{\omega}\cos\omega t \tag{2.28}$$

The maximum slope of the input signal after integration is given as:

$$\frac{d}{dt}\left[-\frac{A}{\omega}\cos\omega t\right]_{max} = A \tag{2.29}$$

In LDM, the maximum slope of the feedback signal $\bar{y}(t) = V f_s$

Therefore, from slope overload condition,

$$A \leq Vf_s \tag{2.30}$$

hence,

$$A_{max} = Vf_s \tag{2.31}$$

From equation (2.30), it is evident that the overload characteristic of SDM is independent of the frequency of the input signal and consequently SDM operates in PWM mode for a wide range of frequencies. This property of SDM makes it an ideal device for A/D conversion [29]. The overload characteristic of SDM is shown in Fig. 2.3.

2.3.4 Amplitude Range

Amplitude range (AR) is defined as:

$$AR = \frac{\text{Signal amplitude which overloads the encoder}}{\text{Signal amplitude which just disturbs the idling pattern}}$$

Now, if V/2 is the amplitude of a sine wave which just disturbs the idling pattern of a LDM, then the corresponding input for a SDM is:

$$\frac{V}{2}\sin\omega t = \int A\sin(\omega t dt)$$

$$= \frac{A}{\omega}\sin(\omega t - \frac{\pi}{2}) \qquad (2.32)$$

where initial conditions are set to 0.

Thus a sinusoidal voltage of an amplitude $\frac{A}{\omega}$ when applied to the input of SDM will just disturb the idling conditions. Consequently,

$$A = V\frac{\omega}{2}$$

From equation (2.31), the maximum signal amplitude which will just overload the system can be given by,

$$A_{max} = Vf_s \qquad (2.33)$$

The amplitude range is therefore:

$$AR = \frac{Vf_s}{\pi Vf}$$

$$= \frac{f_s}{\pi f} \qquad (2.34)$$

AR of SDM is the same as LDM. Thus, although A_{max} and A are different for a linear delta modulator and a sigma delta modulator, their ratios are identical.

2.4 Rectangular Wave Modulator

The rectangular wave modulator (RWM) consists of basically the same building blocks as LDM except for the quantizer. In RWM the memory-less quantizer of LDM is replaced by another non-linear element called quantizer with in-built hysteresis. The RWM is shown in Fig. 2.10.

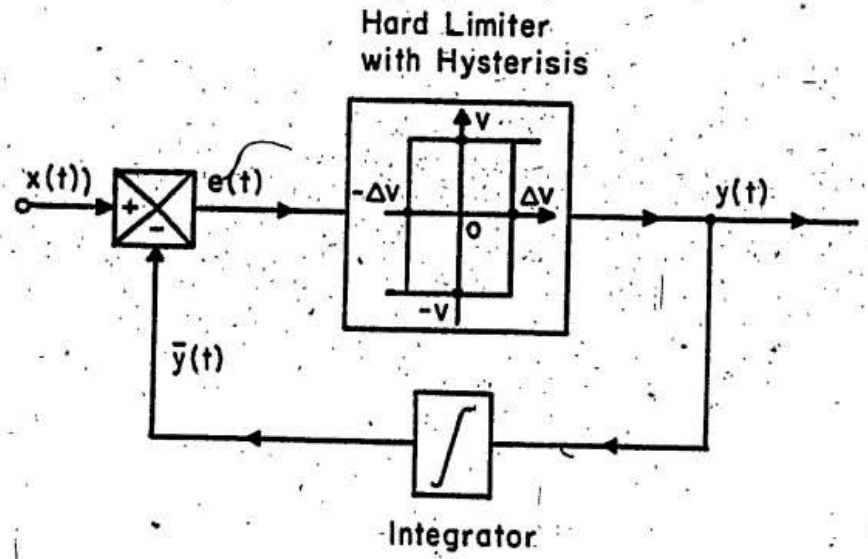


Fig. 2.10 Rectangular Wave Modulator

2.4.1 Principle of Operation

The operation of RWM can be explained as follows: a delta shape carrier waveform is allowed to oscillate within a defined window extending equally above and below the reference signal. The minimum window width and the maximum carrier slope determines the maximum switching frequency.

The binary waveform y(t) at the output of the RWM has levels of ± V volts. Suppose at any instant $y(t) = +V$, then the predicted waveform after integrator $\bar{y}(t)$ has a slope gradient of +V. When the error signal e(t) is reduced to $-\frac{\Delta}{2}$, the output voltage y(t) changes to -V. The estimated signal $\bar{y}(t)$ continues to decrease until $e(t) > \frac{\Delta}{2}$, then output y(t) reverse to +V. Thus the output waveform y(t) consists of a binary level of ± V volts. The time duration between these levels depends on the slope of the input signal x(t). The output signal y(t), when passed through a sample and hold circuit, gives the switching waveform having a voltage level of ± V volts. The switching waveform can be expressed as:

$$y(t) = \sum_{n=1}^{k} V \, \mathrm{sgn}[\, x(nT) - \bar{y}(nT)]$$

where,

V is the voltage level of switching pulses

$x(nT) = \sin(n\omega T)$ is the reference signal at instant nT

$\bar{y}(nT)$ is the predicted signal at instant nT

$T = \frac{1}{f_s}$ is the sampling interval

The switching frequency of RWM can be altered by:

1. Changing the amplitude of the reference input
2. Changing the slope of triangular carrier wave, and
3. Changing the window width.

2.4.2 Idling Characteristic

In the idling condition, when no signal is applied to RWM, the rate of zero crossing of error e(t) signal is greatest. During this condition y(t) is a square wave and $\bar{y}(t)$ is a triangular wave whose peak values are $\pm V/2$.

2.4.3 Overload Characteristic

If the slope of carrier wave and sampling rate are constant, and the frequency of input signal is increased, the overload of RWM takes place at a particular frequency. Beyond this frequency RWM remains in the overload condition. During this condition, the output waveform y(t) is a square wave and the predicted signal $\bar{y}(t)$ is a triangular wave.

Since RWM has not been implemented in the thesis, detailed analysis of RWM is not presented. Analog implementation of RWM is discussed elsewhere [37].

2.5 Application of DM techniques in Inverters

In inverter applications, the aim of the modulation technique is to approximate a sinusoidal waveform by a pulse width modulated waveform such that the error of approximation is minimized and the low order harmonics are eliminated.

The signal generated by a delta modulator at each sampling instant is held at the same value and polarity until the next sample arrives. If the next incoming sample has the same polarity as the previous one, the voltage level and polarity remain the same. However, if the next sample has opposite polarity, then at that instant the polarity of the switching signal changes and the voltage level is held until the next sample arrives. This sample and hold process produces a pulse width modulated switching signal which has a voltage level of $\pm$ V volts and approximates the input sinusoidal signal.

The output from the sample and hold circuit is then processed to produce actual switching waveforms which correspond to the positive and negative half cycle of the sinusoidal reference signal. These signals are then applied to the base drive circuits to generate the collector and base signals to be applied to each of the inverter switches. A single phase bridge inverter is shown in Fig. 2.11.

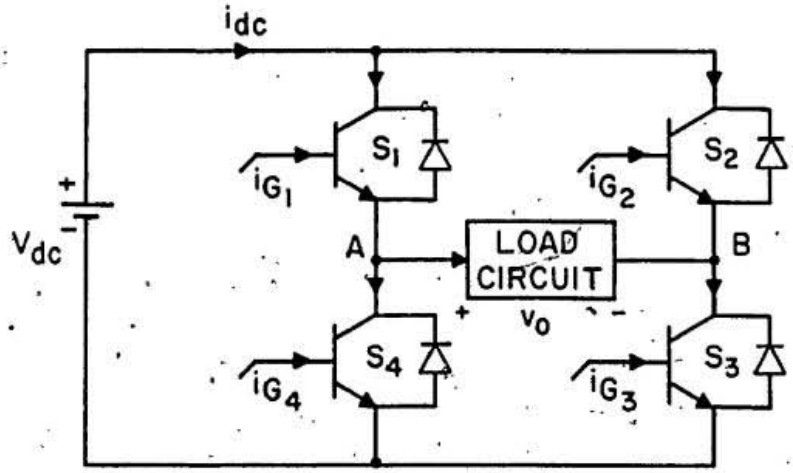


Fig. 2.11 Single Phase Bridge Inverter

The inverter responds to the variation in the frequency of the reference signal applied at the delta modulator input. Since the characteristics of various delta modulation strategies are different, therefore, the performance of the delta modulated inverter depends on the type of modulation technique applied.

CHAPTER 3

SOFTWARE IMPLEMENTATION OF DELTA MODULATION

Generation of delta modulated signal using software techniques offers many advantages over the hardware version. Parameters such as sampling rate, tracking step, filter coefficients and output voltage level are very easily controlled by merely changing the parameter values. The most important feature of the software based delta modulation technique is that ideal characteristics and describing equations of various blocks can be simulated to produce switching waveforms. Since a software based DM system does not have device level limitations, as in actual hardware based DM system, it is expected that software based delta modulation units will produce more accurate switching signals. The output characteristics of software controlled delta modulators are similar to analogue schemes. Thus the modulator has the following properties:

1. Inherent fixed voltage to frequency ratio (LDM).
2. Controlled operation within the overmodulation region with well defined minimum off times.
3. Voltage boosting at low frequencies to overcome motor winding resistance (Sigma delta modulation).
4. The V/f slope can be a user controlled variable.
5. Generation of sub-harmonics can be eliminated by ensuring quarter wave symmetry.

6. Noise immunity can be increased and DC offsets can be eliminated.

In the following section various blocks of delta modulators are described. For each device, the z-domain transfer function is obtained from corresponding s-domain transfer function.

3.1 DM System components

The operational characteristic of various building blocks of a DM system can be simulated to generate a DM signal [38]. A delta modulation system consists of the following building blocks:

1. Hard limiter
2. D/A converter
3. Integrator
4. Error detector

3.1.1 Hard limiter

The hard limiter is a non-linear device, which produces a bipolar output depending upon the sign of the input signal. The transfer characteristic of a hard limiter is shown in Fig. 3.1.

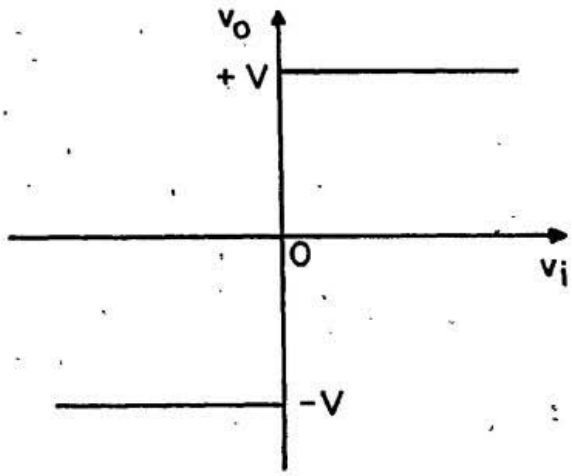


Fig. 3.1 Transfer Characteristic of a Hard Limiter

For a hard limiter, the transfer function with normalized output is given by:

$$g(x) = 1 \qquad \text{for } x \geq 0$$
$$= -1 \qquad \text{for } x < 0 \tag{3.1}$$

The bilateral laplace transform of the characteristic function is :

$$F(\omega) = \int_{-\infty}^{\infty} g(x)\, e^{-\omega x}\, dx$$

$$= \int_{-\infty}^{0} g(x)\, e^{-\omega x}\, dx + \int_{0}^{\infty} g(x) \cdot e^{-\omega x}\, dx \tag{3.2}$$

The integrals converge when $R(\omega) > 0$, yielding

$$F(\omega) = \frac{2}{\omega} \tag{3.3}$$

or,

$$F(s) = \frac{2}{s} \tag{3.4}$$

S-domain transfer function of the hard limiter can be transformed into z-domain transfer function by using bilinear z transformation [39]. Bilinear transformation is given by:

$$s = \frac{2(z-1)}{T(z+1)} \tag{3.5}$$

The z-domain transfer function of a hard limiter can be written as:

$$F(z) = T\frac{(z+1)}{(z-1)} \tag{3.6}$$

Where T, s, and z are sampling rate, s-domain, and z-domain variables respectively.

3.1.2 Digital to Analog Converter

The digital to analog converter is modelled as a zero order hold (ZOH) because the device output has no slope information. A ZOH converts the numerical content of some register of the digital processor to an analog voltage and holds the voltage constant until the content of the register is updated, and then the output of D/A is updated and held again [38, 39]. In short, ZOH is a device which produces a staircase output u(t) from a uniformly spaced sequence of numbers, $u_0, u_1, u_2, \ldots$ such that

$$u(t) = u_k \qquad kT \leq t < (k+1)\,T$$

The input and output waveforms of a ZOH are shown in Fig. 3.2.

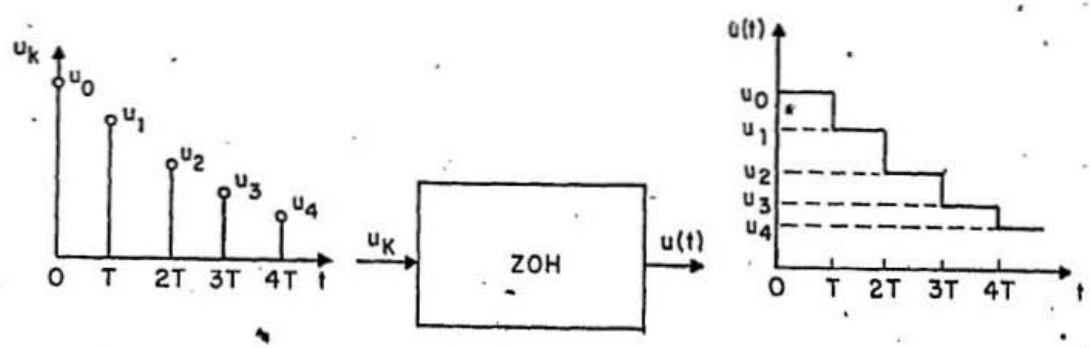


Fig. 3.2 Input and Output Waveforms of a ZOH

The output waveforms of the zero order hold is a step approximation to the continuous signal, and increasing the sampling rate tends to improve the approximation of the continuous signal. The impulse response of the zero order hold is shown in Fig. 3.3.

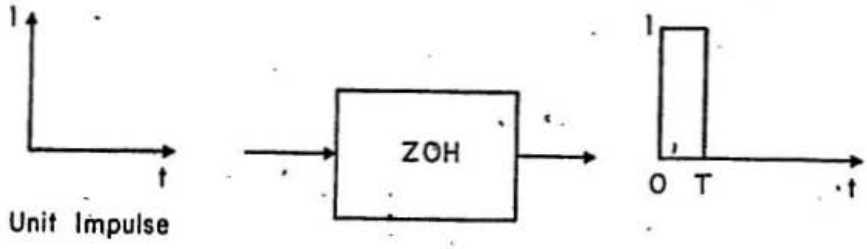


Fig.3.3 Unit Impulse Response of Zero order hold-

The impulse response of the ZOH can be expressed as:

$$g_{h0}(t) = u_s(t) - u_s(t-T) \tag{3.7}$$

where, $u_s(t)$ is the unit step function. The transfer function of ZOH, in the s-domain therefore, can be written as:

$$G_{h0}(j\omega) = \frac{1-e^{-Ts}}{s} \tag{3.8}$$

replacing s by $j\omega$, we have:

$$G_{h0}(j\omega) = \frac{1-e^{-j\omega T}}{j\omega} \tag{3.9}$$

The above equation can be written as:

$$G_{h0}(j\omega) = \frac{2e^{-j\omega\frac{T}{2}}\left[e^{j\omega\frac{T}{2}} - e^{-j\omega\frac{T}{2}}\right]}{j2\omega}$$

$$= \frac{2}{\omega}\sin\left(\frac{\omega T}{2}\right) e^{-j\omega\frac{T}{2}}$$

$$= \frac{\left[T \sin\frac{\omega T}{2} e^{-j\omega\frac{T}{2}}\right]}{\frac{\omega T}{2}} \qquad (3.10)$$

Since T is the sampling period in seconds and $T = 2\frac{\pi}{\omega_s}$, where ω_s is the sampling frequency in rad/sec., the above equation becomes:

$$G_{ho}(j\omega) = 2\frac{\pi}{\omega_s} \frac{\sin\pi(\frac{\omega}{\omega_s})}{\frac{\pi\omega}{\omega_s}} e^{-j\frac{\omega}{\omega_s}} \qquad (3.11)$$

The gain and phase characteristics of ZOH as functions of ω are shown in Fig. 3.4.

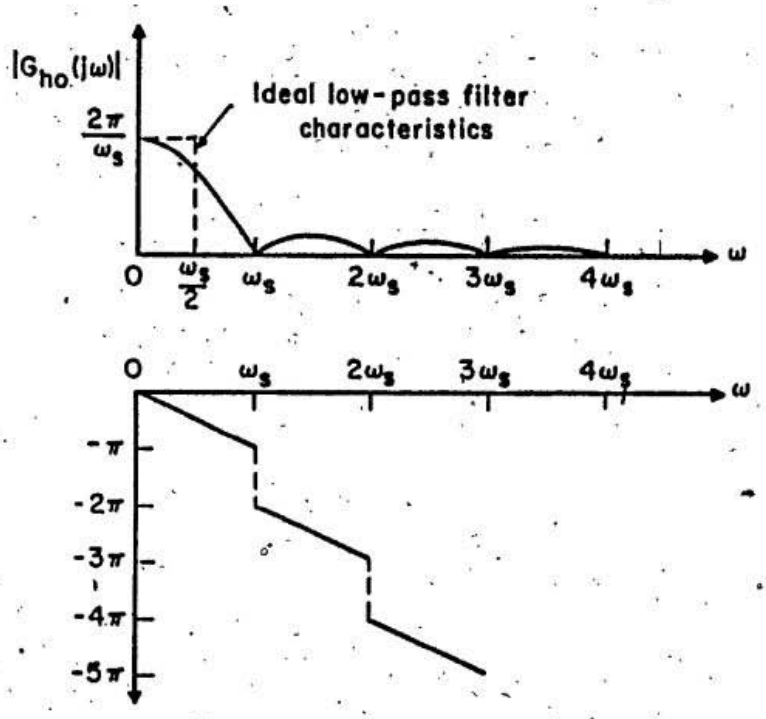


Fig. 3.4(a) Gain and (b) Phase Characteristics of ZOH

The accuracy of ZOH depends greatly on the sampling frequency ω_s.

The z-domain transfer function of ZOH is obtained by using bilinear z transformation on the s-domain transfer function of ZOH. The s-domain transfer function is given by:

$$G(s) = \frac{1 - e^{-Ts}}{s} \tag{3.12}$$

so that,

$$G(z) = G(s) \Big/_{s = \frac{2}{T}\frac{(z-1)}{(z+1)}}$$

$$= \frac{1 - z^{-1}}{\left[\frac{2}{T}\frac{(z-1)}{(z+1)}\right]}$$

$$= \frac{T}{2}(1 + z^{-1}) \tag{3.13}$$

3.1.3 Integrator

The s-domain transfer function of an ideal integrator is given by:

$$H(s) = \frac{K_i}{s} \tag{3.14}$$

Where, K_i is called the dc gain constant.

The frequency response (FR) characteristic of an ideal integrator is shown in Fig. 3.5.

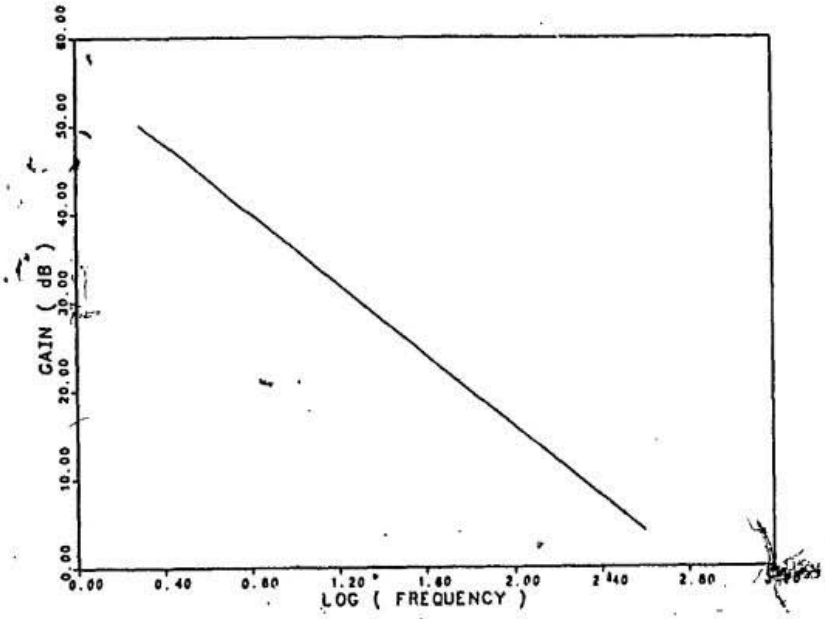


Fig. 3.5 Frequency Response of an Ideal Integrator

From the frequency response characteristic of the integrator, it is clear that an integrator acts as a low pass filter also. Thus higher frequency components are attenuated by the integrator. In normalized units, integrator transfer function can be written as:

$$H(s) = \frac{1}{s}$$

and the impulse response of an integrator :

$$h(t) \leq 1$$

Impulse response $h(t) < 1$ represents a leaky integrator which is usually the case of practical integrators.

An RC op-amp integrator is shown in Fig. 3.6

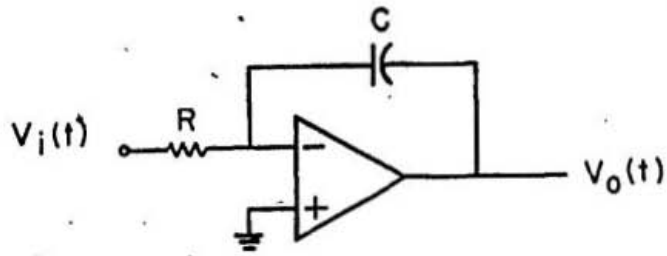


Fig. 3.6 RC Op-amp Integrator

The integrator transfer function is given by:

$$H(s) = \frac{1}{RCs} \tag{3.15}$$

The z-domain transfer function of the above integrator can be obtained by using bilinear z transformation as follows:

$$H(z) = \frac{Y(z)}{X(z)} = H(s) \Big/_{s=\frac{2}{T}\frac{(z-1)}{(z+1)}}$$

$$= \frac{T}{2RC}\frac{(1+z^{-1})}{(1-z^{-1})} \tag{3.16}$$

Simplification of equation (3.16) yields,

$$Y(z) = \frac{T}{2RC}X(z) + \frac{T}{2RC}z^{-1}X(z) + z^{-1}Y(z)$$

$$= \frac{T}{2RC}X(z) + \frac{T}{2RC}X(z-1) + Y(z-1) \tag{3.17}$$

In discrete time domain, the above expression can be written as:

$$Y_k = a_0 X_k + a_1 X_{k-1} + b_1 Y_{k-1} \tag{3.18}$$

where,

$a_0 = a_1 = \frac{T}{2RC}$

$b_1 = 1$ and,

$T = \frac{1}{f_s}$ is the sampling rate

R and C are the resistance and capacitance values of the integrator. X_{k-1} and Y_{k-1} represent the previous input and output values respectively.

The z-domain block diagram of an active RC integrator is shown in Fig. 3.7. In the simulation of LDM and SDM, the integrator shown in fig. 3.7 is used. However, EDM uses a passive RC circuit in the feedback path which is shown in Fig. 3.8.

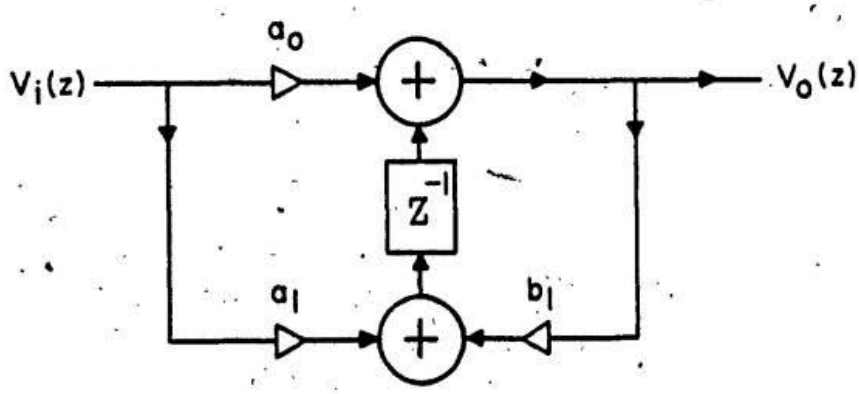


Fig. 3.7 z-domain representation of OP-AMP Integrator

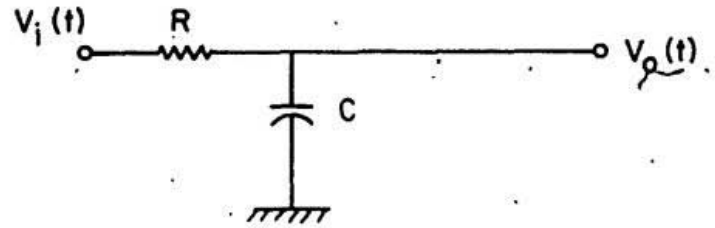


Fig. 3.8 A passive RC Integrator

The transfer function of an RC integrator can be written as:

$$H(s) = \frac{K_i}{1+RCs} \tag{3.19}$$

$$|H(j\omega)| = \frac{K_i}{\sqrt{1+R^2C^2\omega^2}} \tag{3.20}$$

Where, K_i is known as the dc gain constant

The frequency response characteristic of an RC integrator given by equation 3.20 is shown in Fig. 3.9.

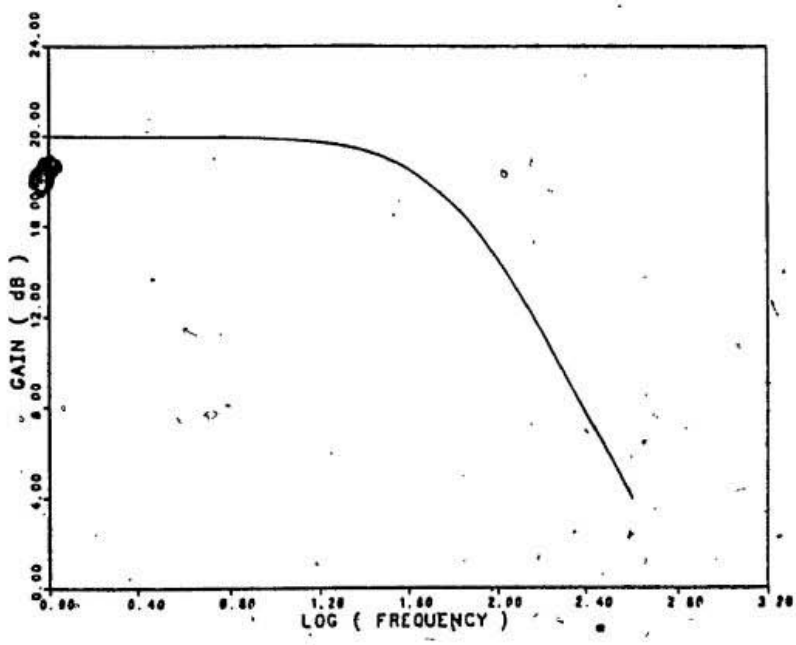


Fig. 3.9 Frequency Response of a Passive RC Integrator

From fig. 3.9, it is observed that frequency response of a passive RC integrator is similar to the frequency response of a low pass filter. Due to this characteristic high frequency components of the EDM output are attenuated.

Using bilinear z-transformation, the z-domain transfer function of RC circuit can be obtained as:

$$H(z) = \frac{Y(z)}{X(z)} = H(s) \Big/_{s=\frac{2}{T}\frac{(z-1)}{(z+1)}}$$

$$= \frac{1}{1+RCs} \Big/_{s=\frac{2}{T}\frac{(z-1)}{(z+1)}}$$

$$= \frac{T(z+1)}{T(z+1) + 2RC(z-1)} \qquad (3.21)$$

Transposition and simplification of equation 3.21 yields:

$$Y(z) = \frac{T}{T+2RC}X(z) + T\frac{z^{-1}}{T+2RC}X(z) - \frac{(T-2RC)}{(T+2RC)}z^{-1}Y(z) \qquad (3.22)$$

Since z^{-1} represents a delay by one sample unit, the above equation may be written as,

$$Y(z) = \frac{T}{T+2RC}X(z) + \frac{T}{T+2RC}X(z-1) - \frac{(T-2RC)}{(T+2RC)}Y(z-1) \qquad (3.23)$$

In discrete time domain, the above equation can be expressed as:

$$Y_k = a_0X_k + a_1X_{k-1} - b_1Y_{k-1} \qquad (3.24)$$

where, X_{k-1} and Y_{k-1} represent the input and output values of the integrator at previous sampling instant,

$$a_0 = a_1 = \frac{T}{T+2RC} \qquad (3.25)$$

$$b = \frac{T-2RC}{T+2RC} \qquad (3.26)$$

T is the sampling rate, and R and C are resistance and capacitance values of the passive RC integrator.

The z-domain representation of the passive RC integrator is shown in Fig. 3.10.

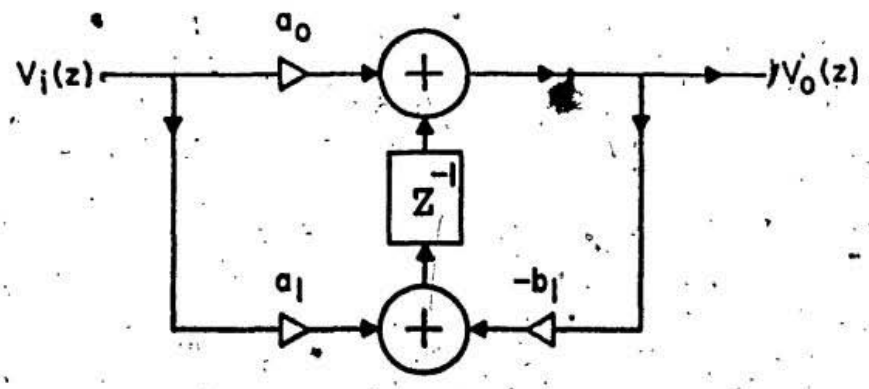


Fig. 3.10 z-domain representation of a Passive RC Integrator

3.1.4 Error Detector

The error detector in a DM system performs the operation of signed addition of all the quantities appearing at its input. The sign of the output error signal is then quantized by the quantizer. In z-domain, the output of an error detector can be expressed as:

$$e(z) = x(z) - \bar{y}(z) \tag{3.27}$$

where, $x(z)$ and $\bar{y}(z)$ are the input and feedback signals respectively.

3.2 DM System Design

A DM system design consists of two steps;

(a) system level design and

(b) circuit level design.

System level design requires suitable choice of DM system parameters so that the modulator ensures sufficiently high signal to noise ratio (SNR) while satisfying overload conditions. However, circuit level design demands fulfillment of additional requirements such as sufficient turn-on and turn-off times of inverter switching devices, minimum switching losses and synchronized operation of the system so that sub-harmonics can be avoided.

3.2.1 DM System Requirements

The behaviour of a DM system depends markedly on the level of the input signal. The signal range can be divided into three distinct regions:

(a) high input or overload

(b) medium input or normal

(c) low input or idle channel

Obviously, for normal operation of the DM system, signal amplitude should not be too high, and yet the signal-to-noise ratio should be sufficiently high so that overloading is avoided at low frequencies.

The next step is a suitable choice of sampling frequency. A high sampling frequency improves signal-to-noise ratio and hence provides better approximation of the input signal. However, increase in sampling frequency will increase the number of pulses per cycle of the DM output. This increase in the number of pulses will in turn increase the inverter system switching losses. This requirement forces one to choose a high enough sampling frequency so that higher signal-to-noise ratio is ensured and yet inverter switching losses are minimized. The sampling frequency however must satisfy the Nyquist criterion given by:

$$f_s \geq 2f_{max} \tag{3.28}$$

Normally, the sampling frequency is chosen 10 or 20 times of the Nyquist rate so that aliasing can be avoided and sufficiently high signal-to-noise ratio is ensured.

The next parameter to be considered is the tracking step (Δ). This is the level by which the predicted signal is increased or decreased in order to successfully track the input signal. Since delta is directly related to the input signal, the selection of delta is made in the range $.5A_{max} < \Delta < 1.5A_{max}$ for the normal operation of the DM system. This range of values is based on simulation and experimental results. Δ, however, is independent of sampling frequency and filter parameters.

Digital filter coefficients vary with the variation in sampling frequency, and the values of the resistance and capacitance of the integrator. From equations (3.18), (3.25), and (3.26) it is apparent that filter coefficients are always less than unity. For proper operation of a DM system, filter coefficients, a_0 and a_1, should lie in the range $0 < \text{coef.} < 0.5$.

3.2.2 PWM Control Requirements

The most important factor of a pulse width modulated (PWM) control scheme is undoubtedly the switching strategy used to generate the edges of the PWM pulses.

Since present work involves the microprocessor controlled delta PWM, it is necessary to explore the options associated with switching strategy. Switching strategy can be categorized as follows:

(a) Natural sampled switching. This can be hardware or software based. When certain conditions are satisfied or amplitude level goes above the reference level,

switching takes place.

(b) Regular sampled switching. In this method the reference signal is sampled at regular time intervals. Based on computation results, upon which certain conditions are satisfied, switching takes place. In this method the time required for the A/D and D/A conversions and the computation time must be less than one sampling interval. Also the Nyquist criterion of sampling rate must be satisfied.

(c) Memory based, look-up table, or pattern retrieval method [40, 41]. If the memory of the microcomputer contains the value of the switching angles, (i.e., the switching pattern), only the retrieval of this pattern from memory is needed to generate proper gating signals. The choice of switching angles is purely optional. One can obtain output voltage waveform with minimum total harmonic contents or minimum harmonic power loss in the specific load conditions. In any case, it is necessary to derive the mathematical expressions from which the gating angles are evaluated. Generally, these expressions result in a set of non-linear equations and numerical methods with optimization techniques are employed to solve them.

In this research, to generate delta modulated switching signals, the pattern retrieval method is used. A microprocessor based delta modulated inverter is shown in the Fig. 3.11.

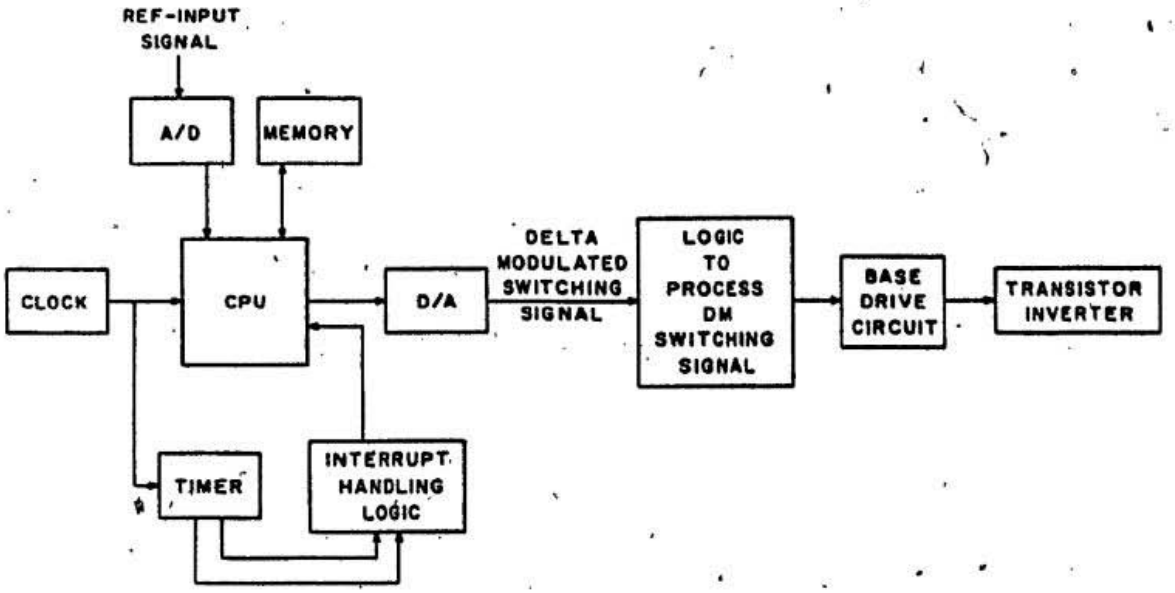


Fig. 3.11 Microprocessor based delta modulated inverter

3.3 Software Implementation of DM strategies

In this section software implementation of various Delta Modulation techniques are developed. The algorithm for the implementation of linear delta modulator, sigma delta modulator, and exponential delta modulator are described in this section. These DM techniques can easily be simulated by coding the algorithm in a suitable programming language. However, for microprocessor based generation of DM switching signal, it may be necessary to use assembly language programming so that timing constraint of the DM system can be met.

3.3.1 Linear Delta Modulator

The block diagram of the linear delta modulator (LDM) is shown in Fig. 2.1. If the integrator in the feedback path is replaced by the digital integrator shown in Fig. 3.10, the LDM of Fig. 2.1 can be represented by Fig. 3.12 in the digital domain.

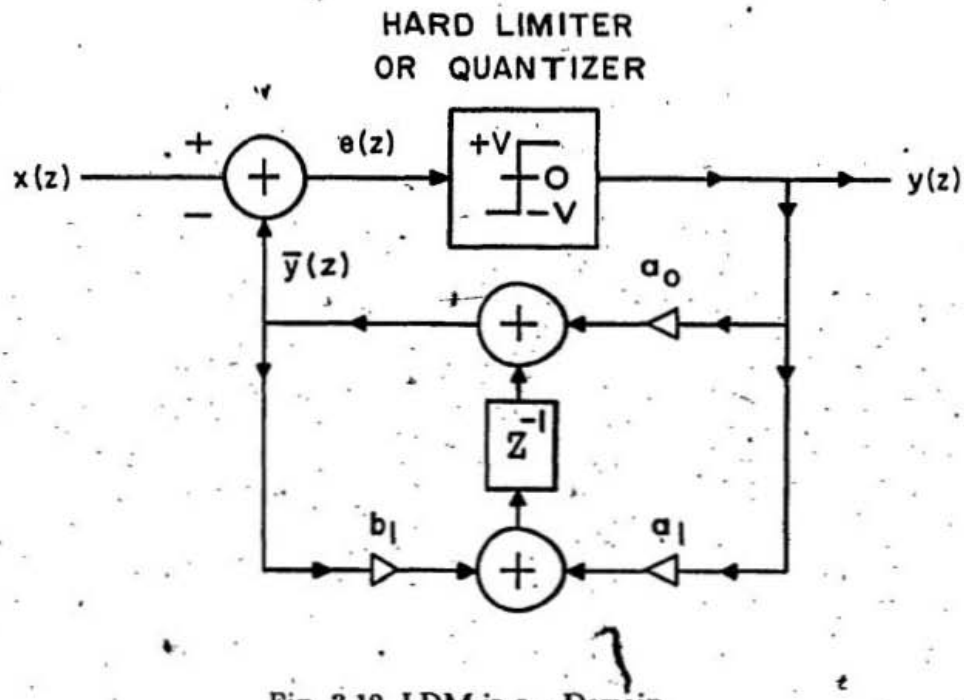


Fig. 3.12 LDM in z - Domain

In the above figure, the ZOH is eliminated for simplicity. Fig. 3.12 can be described by the following equations:

$$e(z) = x(z) - \bar{y}(z) \tag{3.29}$$

$$y(z) = V\mathrm{Sgn}[e(z)] \tag{3.30}$$

$$\bar{y}(z) = a_0 y(z) + a_1 y(z-1) + b_1 \bar{y}(z-1) \tag{3.31}$$

where,

$$a_0 = \frac{T}{2RC} \tag{3.32}$$

$$a_1 = a_0 \tag{3.33}$$

$$b_1 = 1 \tag{3.34}$$

Equations 3.29 to 3.34 are used to simulate the operation of linear delta modulator and generate real-time switching signals.

3.3.1a Algorithm Design

The algorithm to generate the Delta PWM switching waveform follows from the z-domain block diagram of linear delta modulator and its describing equations. The main steps involved in the implementation are outlined below:

1. Choose LDM system parameters , i.e. sampling frequency, filter parameters, signal amplitude and tracking step.
2. Calculate filter coefficients
3. Initialize variables
4. Sample the input reference signal
5. Calculate the error $e(k) = x(k) - \bar{y}(k)$
6. Update filter variables.
7. Based on the sign of the error signal, calculate the LDM output i.e. if $e(k) \geq 0$ then $y(k) = +V$ else $y(k) = -V$
8. Calculate integrator output :

$$\bar{y}(k) = a_0 y(k) + a_1 y(k-1) + b_1 \bar{y}(k-1)$$

9. Go to step 4.

3.3.1b Program Flow Chart

A simplified program flow chart is shown in Fig. 3.13. The program generates and stores switching instants and bilevel amplitudes of LDM output switching signals. The switching waveform is then processed and applied to the bases of inverter switches through respective base drive circuits, which in turn control the operation of inverter. The listing of the program is given in the appendix.

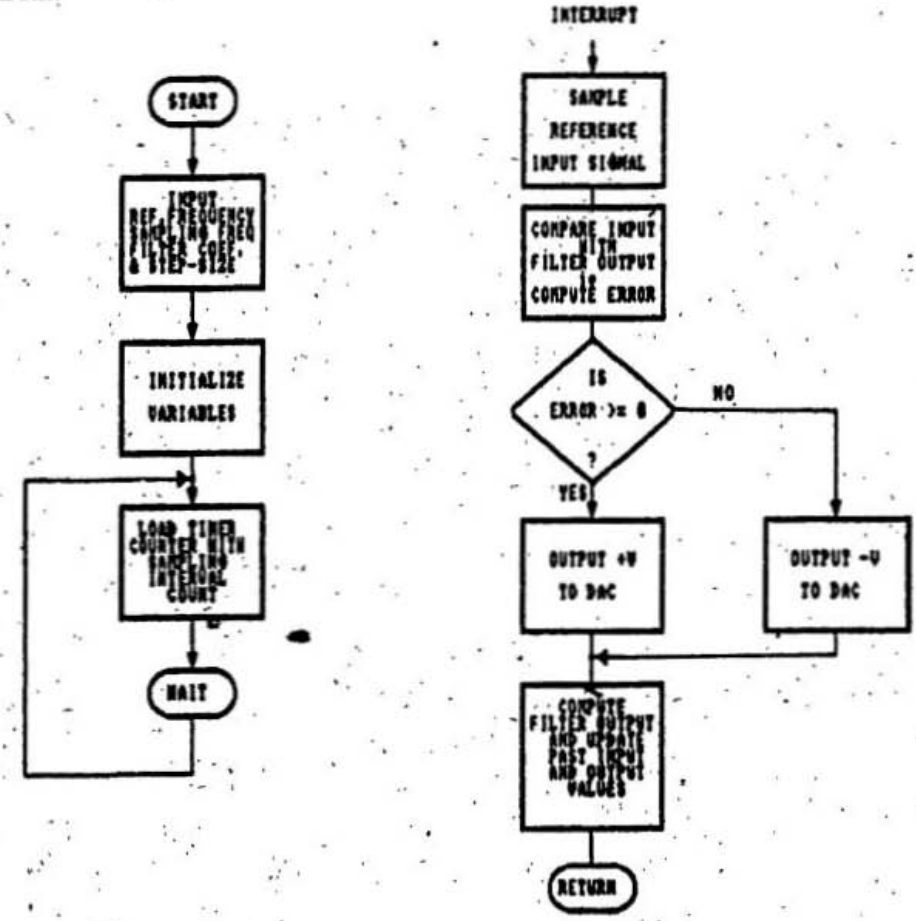


Fig. 3.13 Flow Diagram of LDM

3.3.2 Exponential Delta Modulator

The feedback path of an EDM employs a passive RC circuit having a transfer function given by $H(s) = \frac{1}{1+RCs}$. Replacing RC circuit by the z-domain block diagram shown in Fig. 3.10, the z-domain block diagram of exponential delta modulator can be obtained as shown in Fig. 3.14. It should be noted that the z-domain block diagram of exponential delta modulator is same as that of linear delta modulator except for the difference in digital filter coefficients. However, the R and C values are taken to be the same, as in the case of linear delta modulator and sigma delta modulator, so that necessary comparisons among the performance characteristics of the three systems could be made.

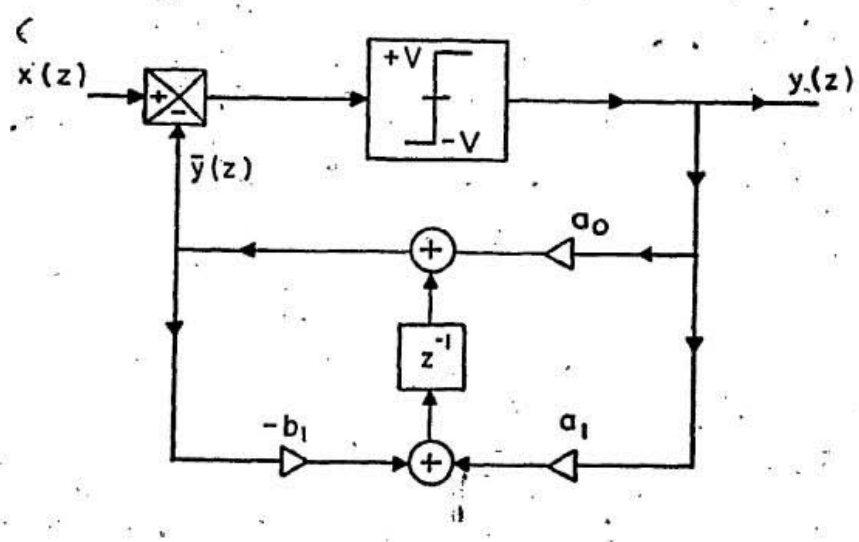


Fig. 3.14 EDM in z - Domain

The describing equations of EDM are given as follows:

$$e(z) = x(z) - \bar{y}(z) \tag{3.35}$$

$$y(z) = VSgn[e(z)] \tag{3.36}$$

$$\bar{y}(z) = a_0 y(z) + a_1 y(z-1) - b_1 \bar{y}(z-1) \tag{3.37}$$

$$a_0 = \frac{T}{T + 2RC} \tag{3.38}$$

$$a_1 = a_0 \tag{3.39}$$

$$b_1 = \frac{T - 2RC}{T + 2RC} \tag{3.40}$$

where,

$T = \frac{1}{f_s}$ is the sampling rate

Equations 3.35 to 3.40 describe the function of an exponential delta modulator which are programmed to simulate its operation and generate real-time switching signal.

3.3.2a Algorithm Design

1. Choose EDM system parameters , i.e. sampling frequency, filter parameters, signal amplitude and tracking step.
2. Calculate filter coefficients
3. Initialize variables
4. Sample the input reference signal
5. Calculate the error $e(k) = x(k) - \bar{y}(k)$
6. Update filter parameters.
7. Based on the sign of the error signal, calculate the EDM output i.e. if $e(k) \geq 0$ then $y(k) = +V$ else $y(k) = -V$

8. Calculate integrator output :

$$\bar{y}(k) = a_0 y(k) + a_1 y(k-1) - b_1 \bar{y}(k-1)$$

9. Go to step 4.

3.3.2b Program Flow Chart

The flow chart to simulate the operation of EDM is shown in Fig. 3.15. The program flow is essentially the same as that of LDM except that in EDM, filter coefficients and integrator equations are different.

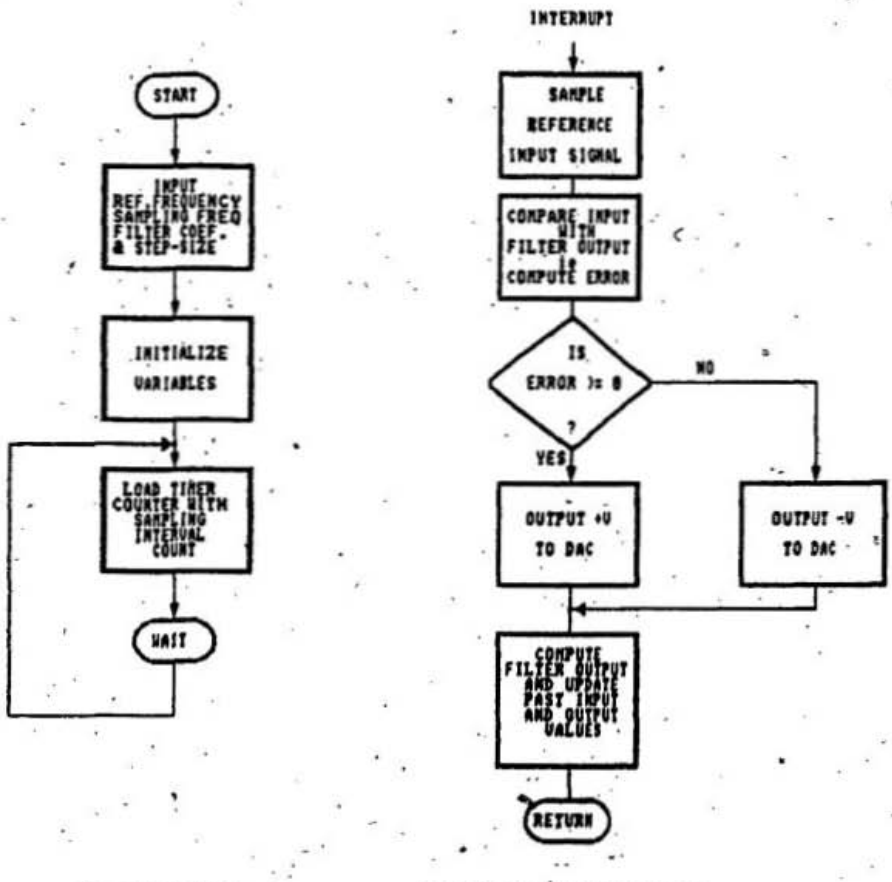


Fig. 3.15 Flow Diagram of EDM.

3.3.3 Sigma Delta Modulator

The z-domain block diagram of sigma delta modulator is obtained by replacing the integrator in the feed-forward path of Fig. 2.8 by a digital integrator of Fig. 3.7. The z-domain block diagram of SDM is shown in Fig. 3.16.

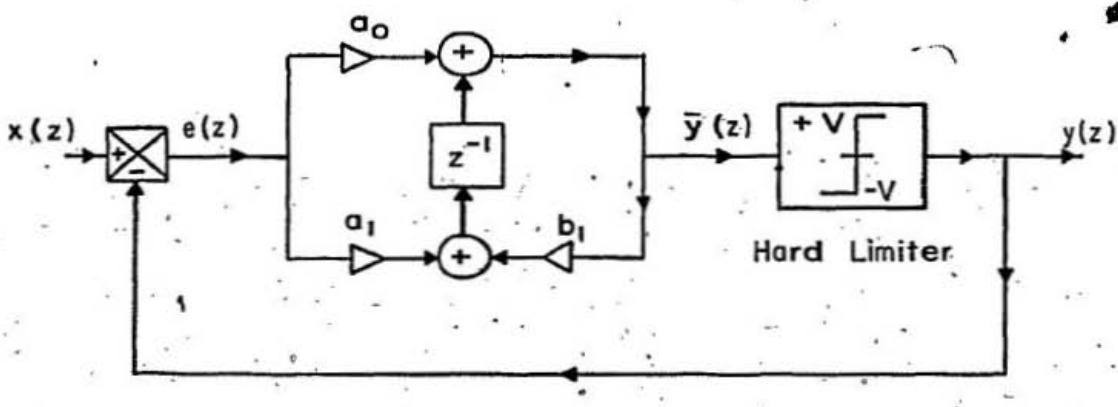


Fig. 3.16 SDM in Z-Domain

The describing equations of SDM are:

$$c(z) = x(z) - y(z) \tag{3.41}$$

$$\bar{y}(z) = a_0 c(z) + a_1 c(z-1) + b_1 \bar{y}(z-1) \tag{3.42}$$

$$y(z) = V\mathrm{Sgn}[\bar{y}(z)] \tag{3.43}$$

$$a_0 = \frac{T}{2RC} \tag{3.44}$$

$$a_1 = a_0 \tag{3.45}$$

$$b_1 = 1 \tag{3.46}$$

where, T is the sampling rate.

Equations 3.41 to 3.46 describe the function of a sigma delta modulator which are programmed to simulate its operation and generate real-time switching signals. Note that filter coefficients of sigma delta modulator are same as those of linear delta modulator but differ from exponential delta modulator.

3.3.3a Algorithm Design

The main steps involved in the algorithm which simulates the operation of SDM shown in Fig. 3.16 are outlined below:

1. Choose SDM system parameters.
2. Calculate filter coefficients.
3. Initialize local variables.
4. Sample the input reference signal.
5. Calculate the error.
6. Update filter variables.
7. Calculate integrator output $\bar{y}(z)$
8. Calculate the SDM output, $y(z) = +V$ if $\bar{y}(z) \geq 0$ else $y(z) = -V$
9. Go to step 4.

3.3.3b Program Flow Chart

Fig. 3.17 represents the flowchart to simulate the operation of sigma delta modulator. This flow chart differs from that of linear delta modulator since in this case the integration process takes place in the feed forward path. Program

listing of SDM is given in the appendix.

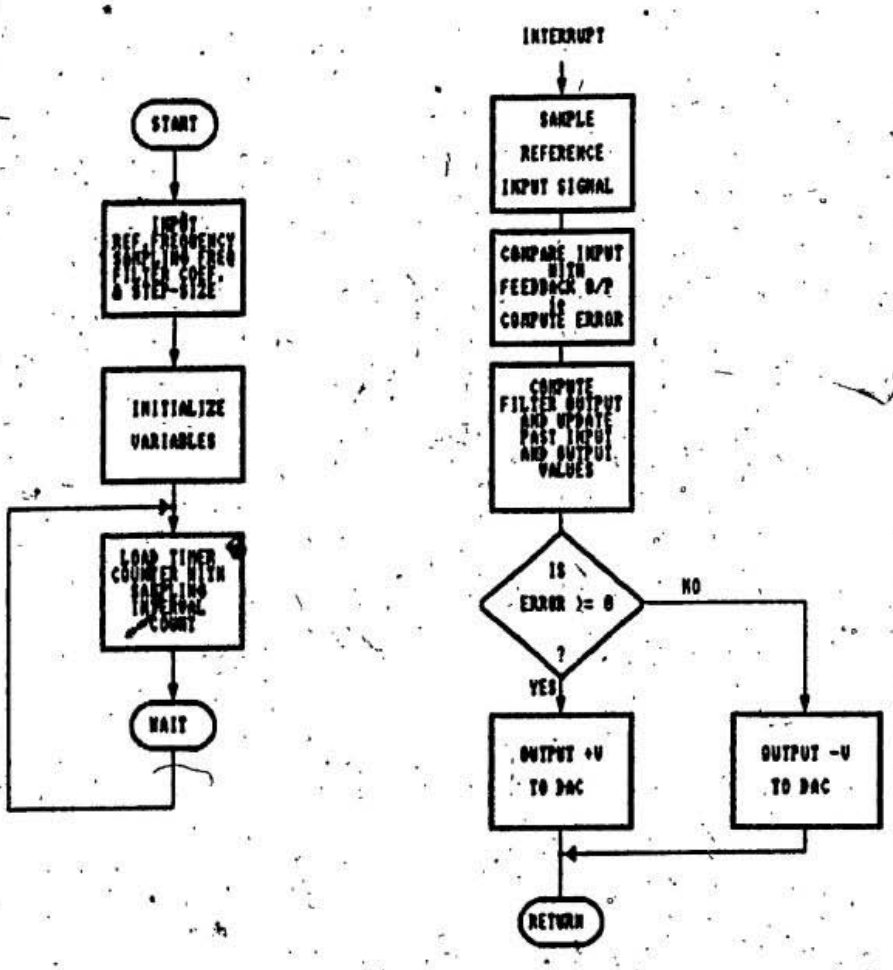


Fig. 3.17 Flow Diagram of SDM

LDM, EDM and SDM are simulated using algorithms developed in preceding sections. Results obtained from these simulations are presented in the next chapter. It is evident that in contrast to the hardware control, software control

of delta modulated inverters offers easier control of the modulator parameters, as well as easier control of number of commutations, output voltage and frequency of the inverter. The performance of the modulator and inverter can be optimised by varying the system parameters.

CHAPTER 4

RESULTS OF SIMULATED DELTA MODULATED SYSTEMS

Delta modulated (DM) systems implemented under software control generate a binary waveform at the output. This chapter describes the results obtained from simulated DM systems. Each system responds to variation in parameters such as input signal frequency, sampling frequency and tracking step. Effect of parameter variation is reflected in the harmonic content and spectral characteristics of the DM output signal.

4.1 DC Input Response

All the three DM systems were successfully simulated to encode a dc signal. Initially, when the system is turned on, there is a large error. However, the error decreases until estimated signal approaches the input dc level. From this instant onwards, the error signal changes its sign at half the clock rate and the output waveforms are identical to those of idling condition. Thus linear delta modulator (LDM), exponential delta modulator (EDM), and sigma delta modulator (SDM) generate binary waveforms consisting of alternate positive and negative pulses.

Figs. 4.1 - 4.3 show various waveforms, when a dc signal is applied at the input of the modulators under consideration. The time taken to reach the input level is minimum in sigma delta modulator. However, the exponential delta modulator has the highest average value at its output.

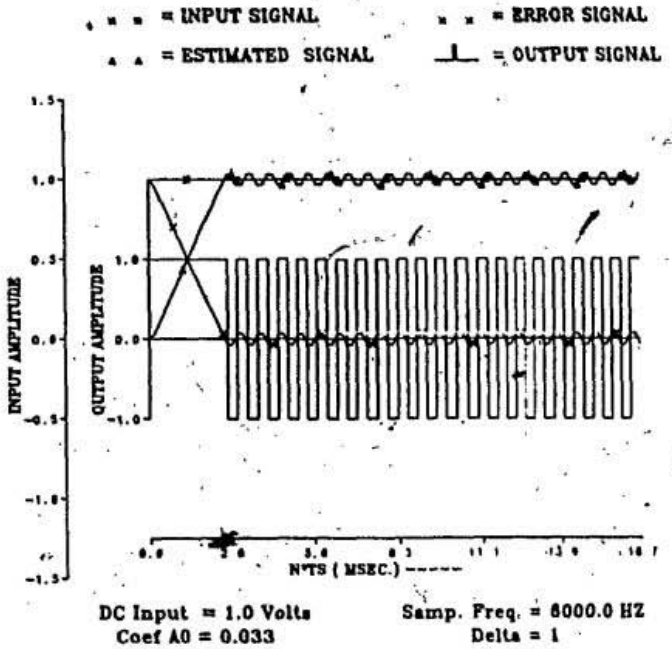


Fig. 4.1 LDM Waveforms for DC Input

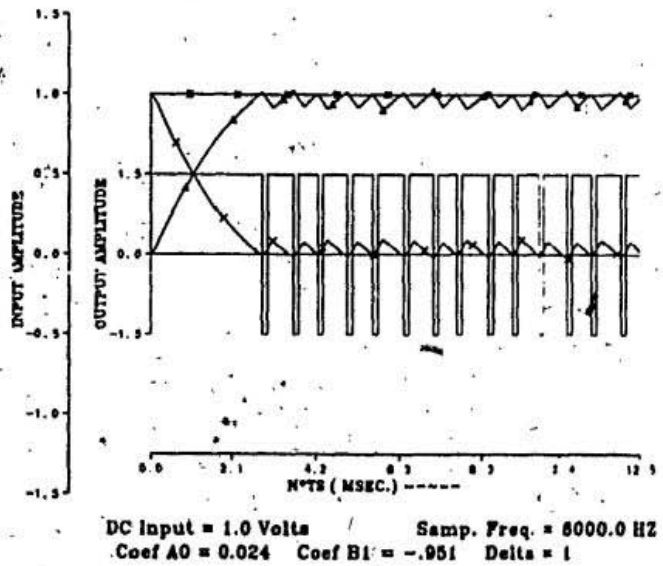


Fig. 4.2 EDM Waveforms for DC Input

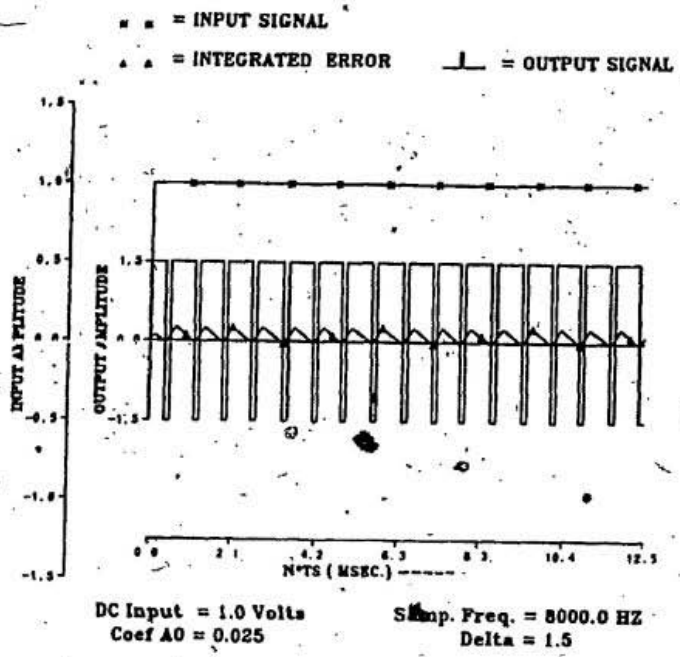


Fig. 4.3 SDM Waveforms for DC Input

4.2 System Response on Parameter Variations

This section deals with the response of the simulated DM system when time varying signal is applied at the input. In time varying signals, the slope at sampling instants also varies with time. The ability of the modulator to successfully track the input signal depends on the input frequency, amplitude of the input signal, sampling rate, and the tracking step. These parameters can be varied and their effects on the performance of various delta modulation techniques can be described.

4.2.1 Variation in Input Frequency

Figs. 4.4 - 4.12 represent the response of linear delta modulator (LDM), exponential delta modulator (EDM), and sigma delta modulator (SDM) respectively for various operating frequencies. Sampling frequency and step size are kept constant. From these figures it is observed that:

1. As the operating frequency is increased, the number of output pulses decreases. However, at higher operating frequencies, modulator output switches from PWM to square wave mode.
2. For the same input frequency, the number of output pulses per half cycle is highest in the linear delta modulator.
3. The tracking of signal is poor at higher frequencies for LDM and EDM. This situation corresponds to the overload condition of the modulator. SDM, however, shows good tracking at higher frequencies.
4. As the input frequency is increased , the output waveform changes from a PWM signal to a square wave signal. In linear and exponential dalta modulators the mode change occurs at lower base frequencies . However, the mode change in sigma delta modulator occurs at relatively higher base frequencies. This is the case because the frequency response of SDM is independent of the input frequency. Thus sigma delta modulator is suitable for a wide range of input frequencies.

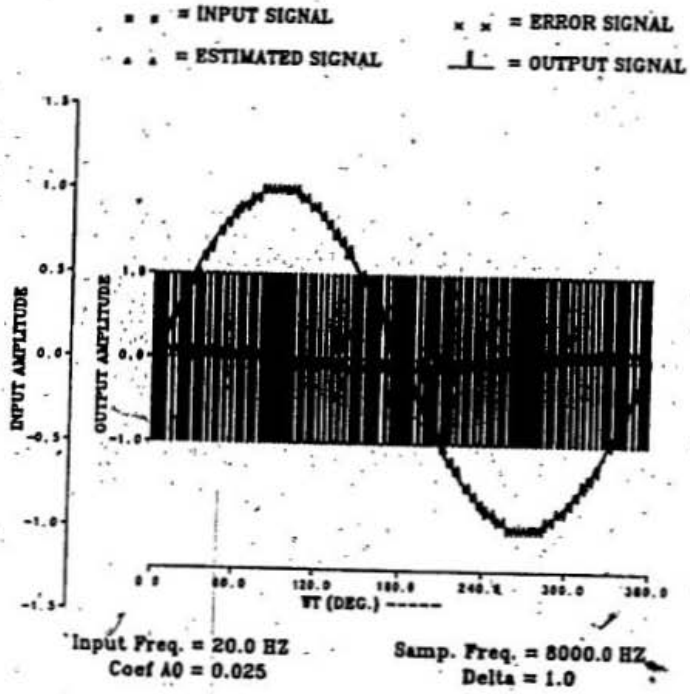


Fig. 4.4 LDM Waveforms for f = 20 Hz.

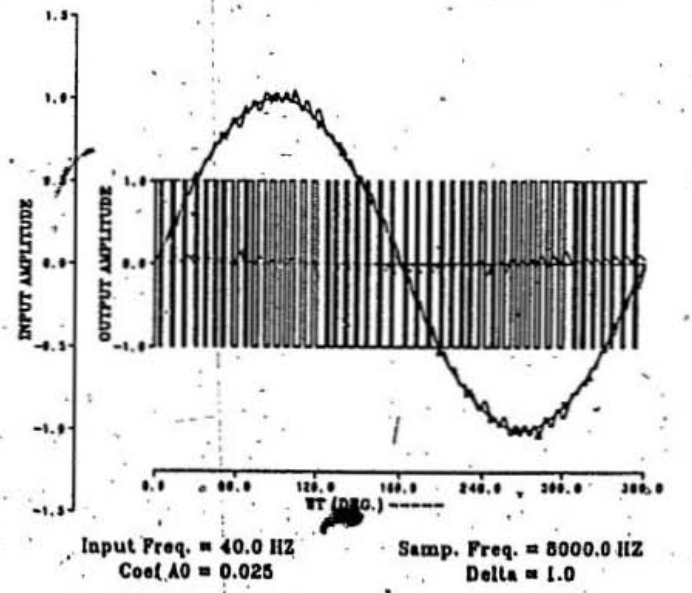


Fig. 4.5 LDM Waveforms for f = 40 Hz

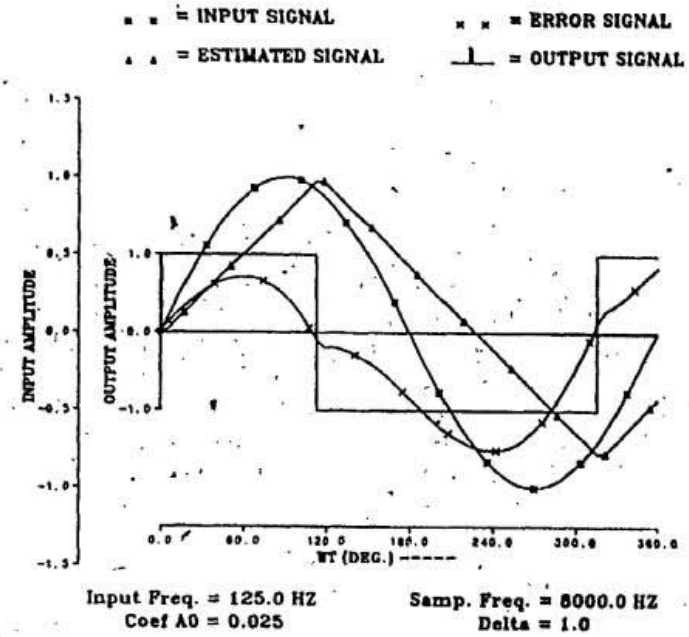


Fig. 4.6 LDM Waveforms or f = 125 Hz

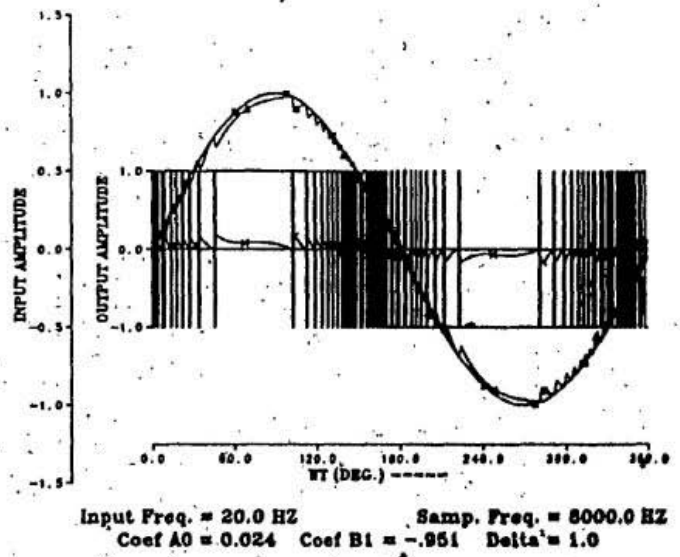


Fig. 4.7 EDM Waveforms for f = 20 Hz

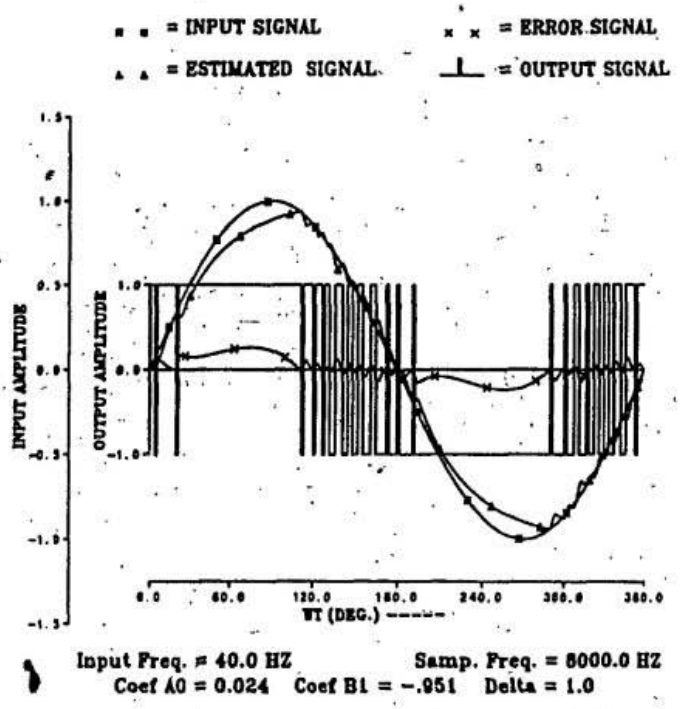


Fig. 4.8 EDM Waveforms for f = 40 Hz

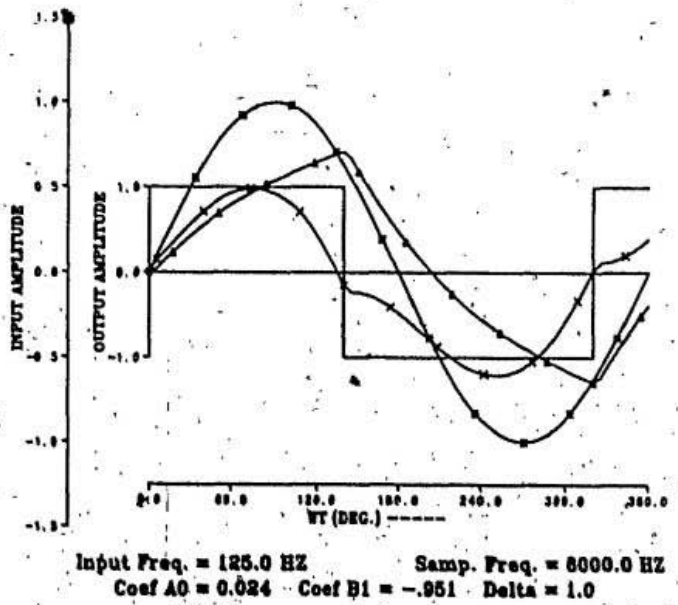


Fig. 4.9 EDM Waveforms for f = 125 Hz

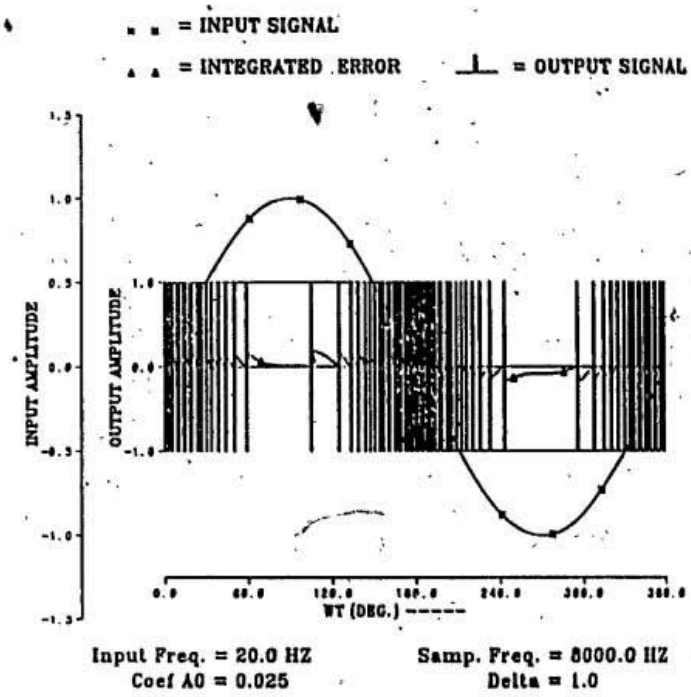


Fig. 4.10 SDM Waveforms for f = 20 Hz

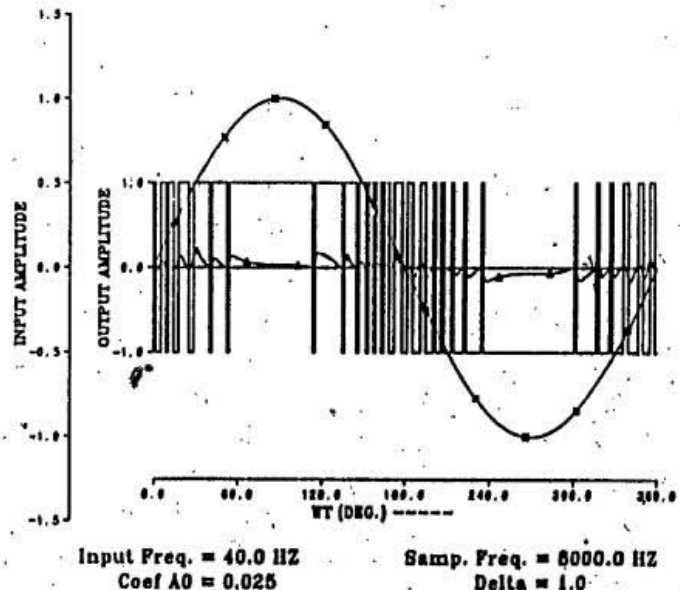


Fig. 4.11 SDM Waveforms for f = 40 Hz

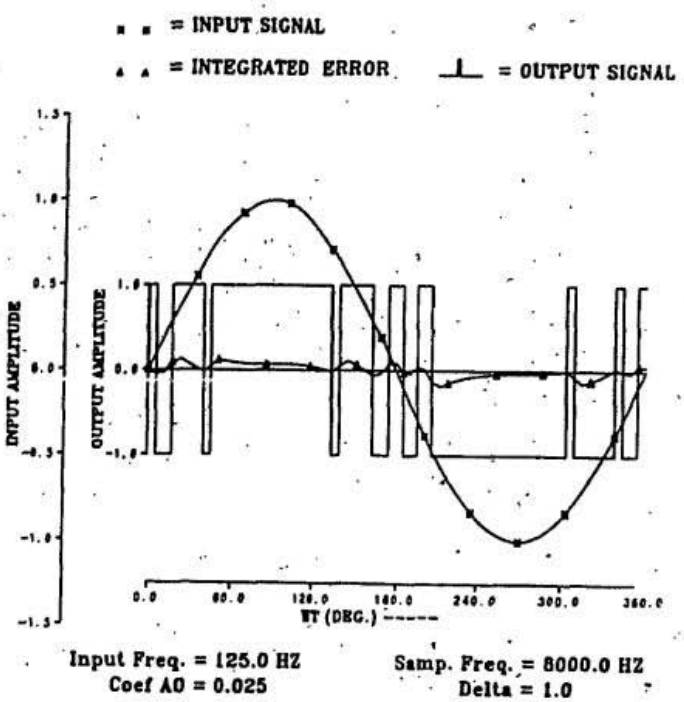


Fig. 4.12 SDM Waveforms for f = 125 Hz

4.2.2. Variation in Sampling Frequency

Sampling frequency is an important parameter of sampled data systems. At lower sampling rates estimation of the input signal is inaccurate and gives rise to aliasing phenomenon in the power spectrum of the DM output signal. As the sampling rate is increased the error of quantization decreases and estimated signal closely follows the input. However, with an increase in sampling frequency, the number of output pulses per cycle also increases. In order to minimize quantization error in the encoding process, maximum possible sampling frequency is desired.

Figs. 4.13 - 4.21 represent the effect of sampling frequency on the output of delta modulators. From these figs. it is observed that for a given set of parameters, LDM generates larger number of output pulses than EDM and SDM. Although minimum sampling frequency is restricted by the Nyquist criterion, in actual practice, input signal is sampled in excess of 20 or 30 times the Nyquist rate so that quantization error is minimized and the output power can be maximized [3, 29].

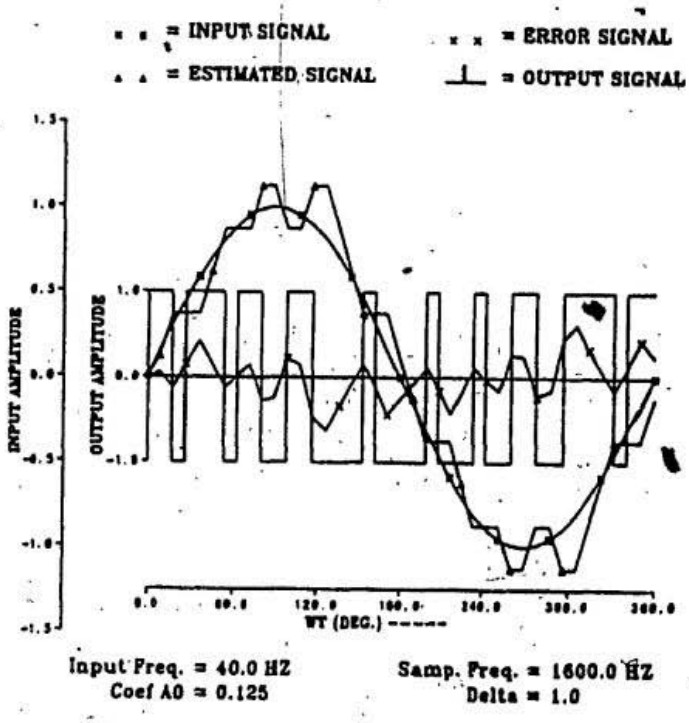


Fig. 4.13 LDM Waveforms for $f_s = 1600$ Hz

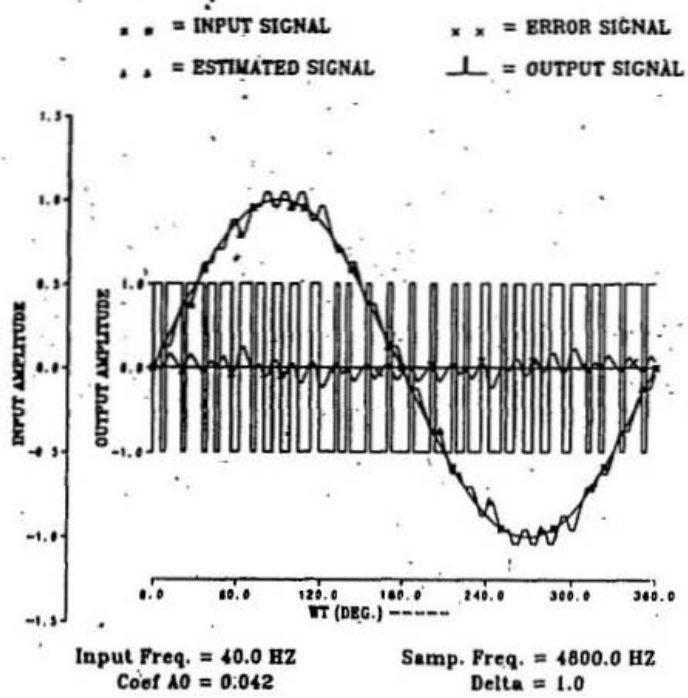


Fig. 4.14 LDM Waveform for $f_s = 4800$ Hz

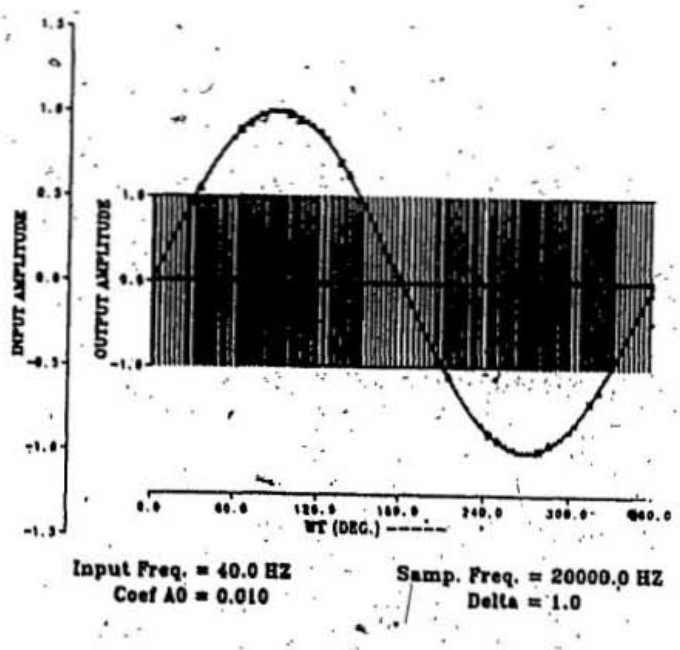


Fig. 4.15 LDM Waveforms for $f_s = 20$ kHz

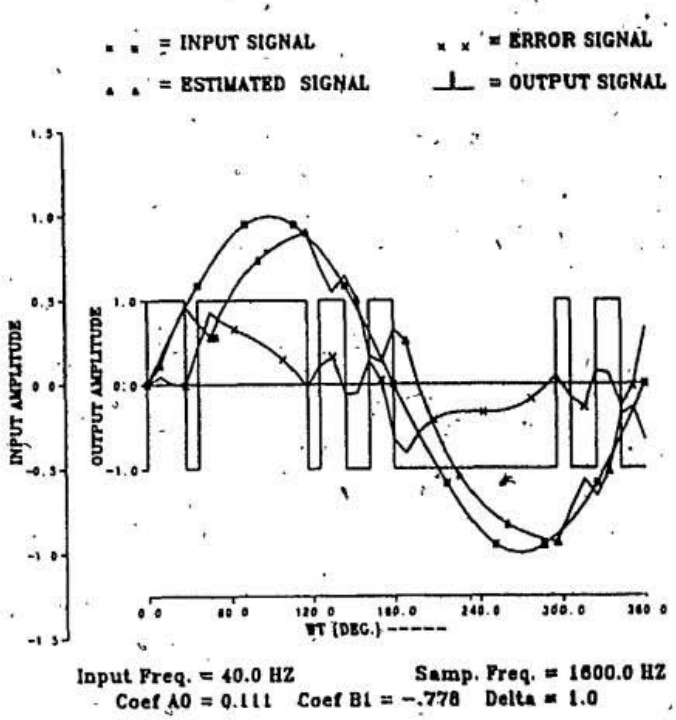


Fig. 4.16 EDM Waveforms for $f_s = 1600$ Hz

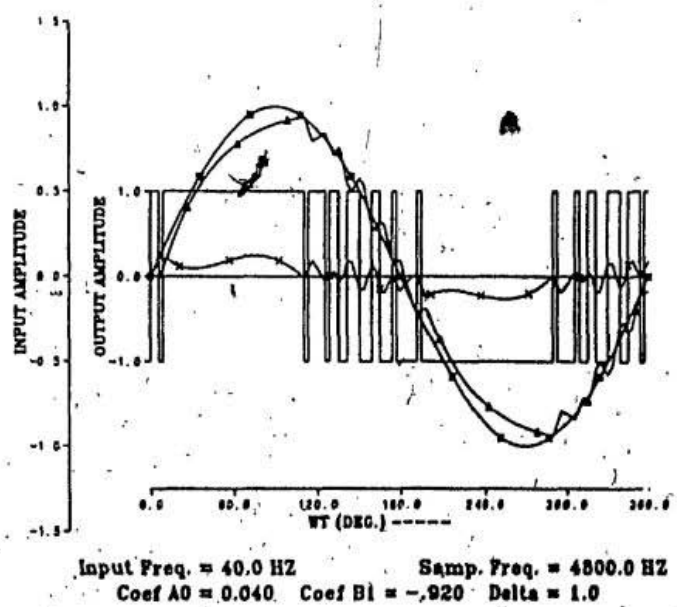


Fig. 4. 17 EDM Waveforms for $f_s = 4800$ Hz

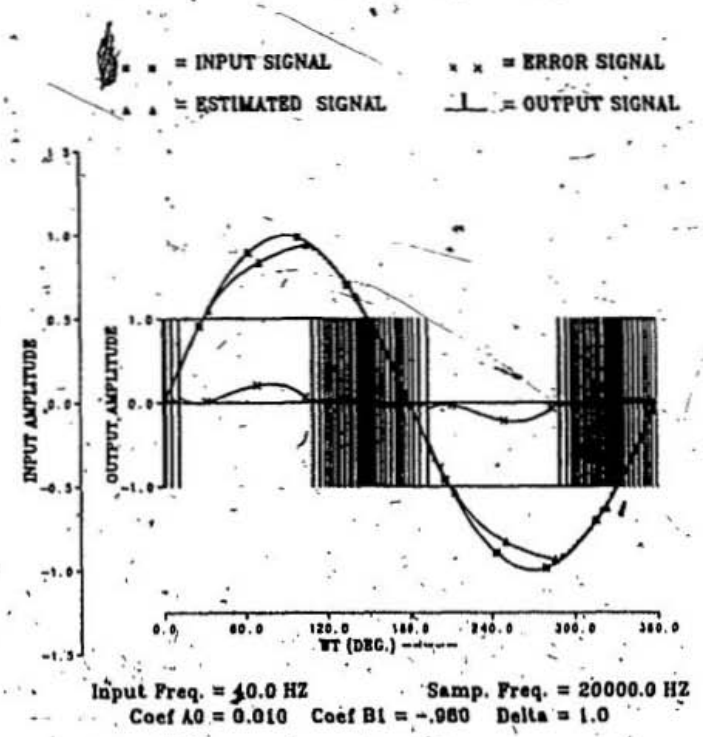


Fig. 4. 18 EDM Waveforms for $f_s = 20$ kHz

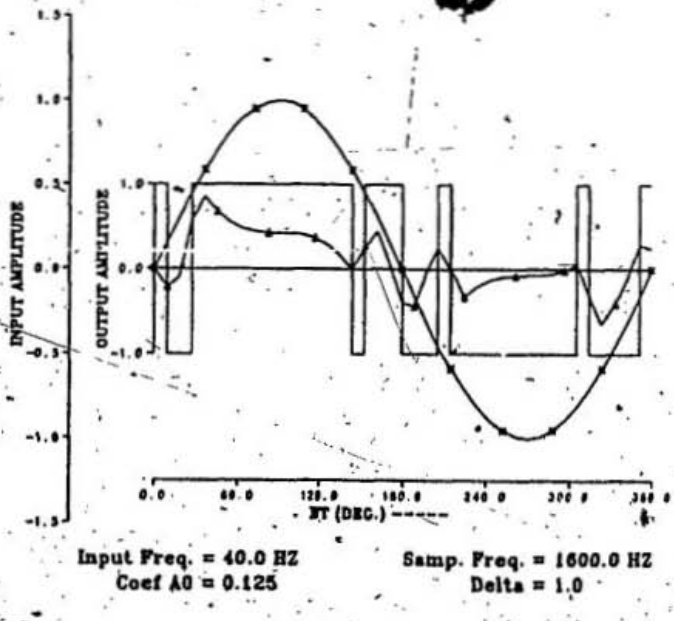


Fig. 4.19 SDM Waveforms for $f_s = 1600$ Hz

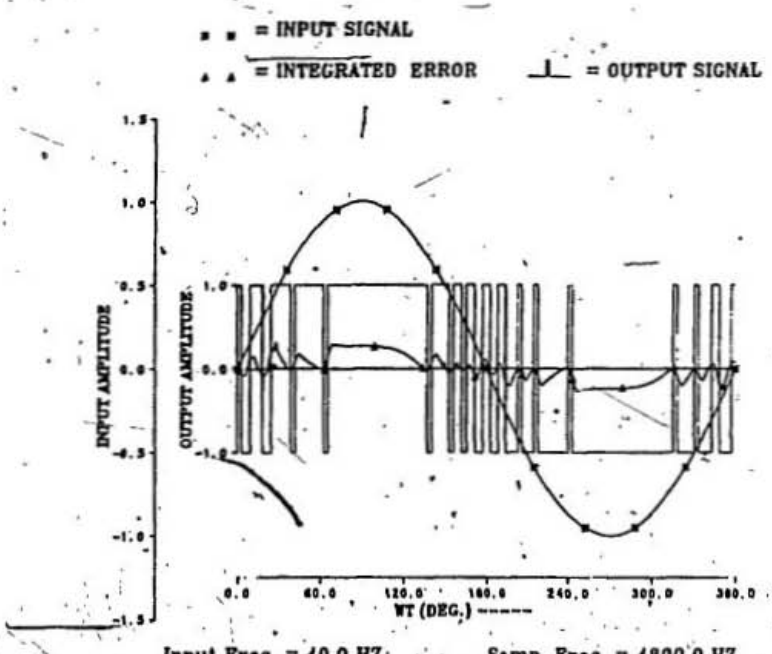


Fig. 4.20 SDM Waveforms for $f_s = 4800$ Hz

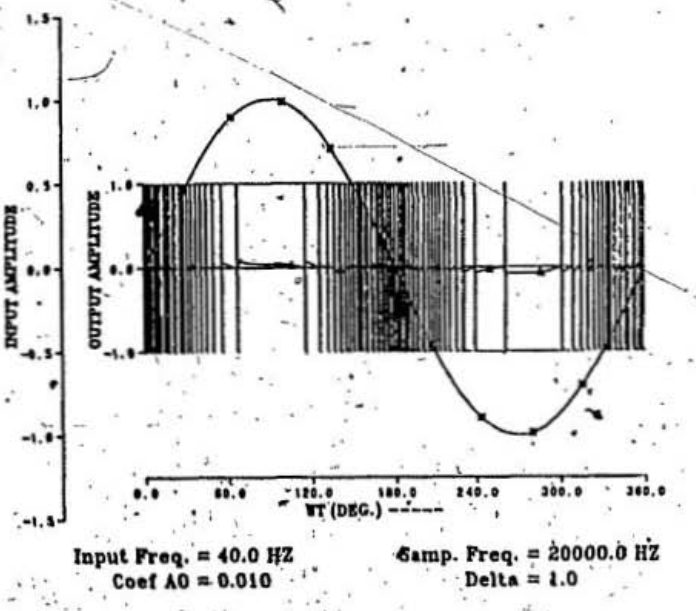


Fig. 4.21 SDM Waveforms for $f_s = 20$ kHz

4.2.3 Variation in Step Size (Δ)

Step size (Δ) is another important parameter in delta modulated systems. If step size of the tracking signal is too small, modulator takes longer time to track the input signal and if the slope of the input signal is too high, slope overload occurs. Figs. 4.22-4.30 represent the effect of variation in step size on the output of linear delta modulator (LDM), exponential delta modulator (EDM) and sigma delta modulator (SDM). For $\Delta = 0.2$, all the three systems show the overload condition. Similarly, for larger values such as $\Delta = 3.0$, although modulators are able to track the input signal, the quantization error is high. Therefore, from simulation and experimental results, for normal operation of DM systems, the value of Δ it is chosen such that:

$$0.5\,A < \Delta < 1.5\,A$$

Where, A is the amplitude of the input signal.

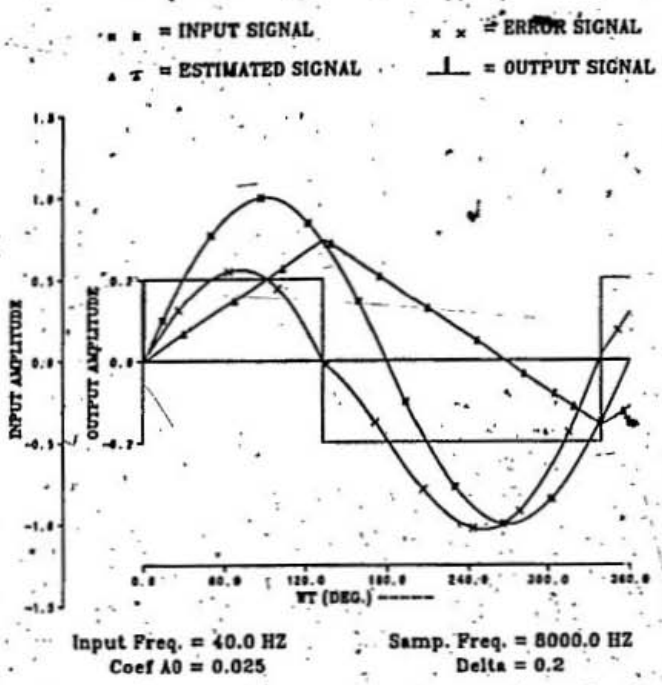


Fig. 4.22 LDM Waveforms for $\Delta = 0.2$

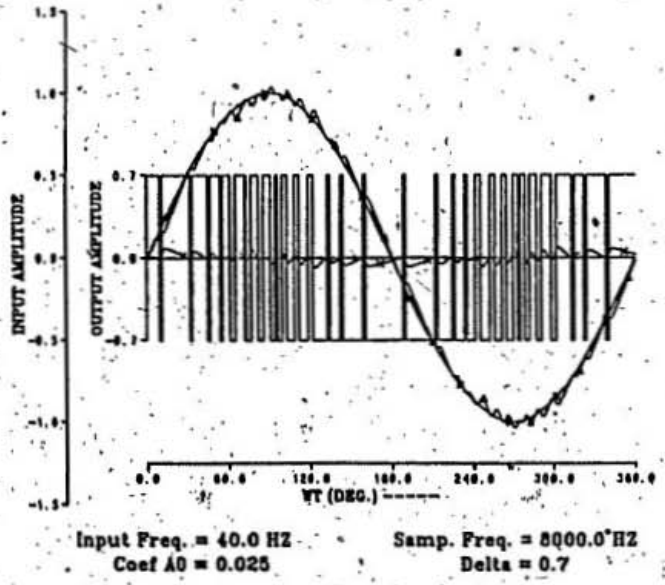


Fig. 4.23 LDM Waveforms for $\Delta = 0.7$

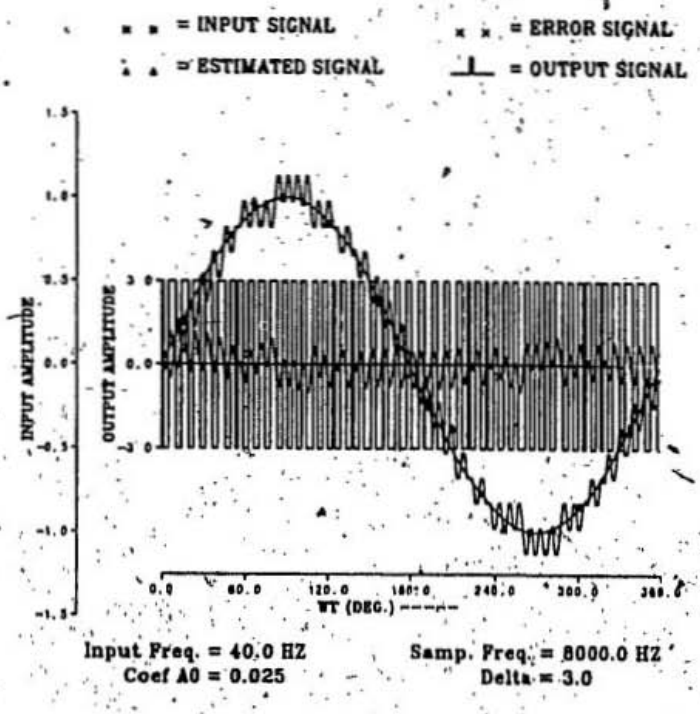


Fig. 4.24 LDM Waveforms for $\Delta = 3.0$

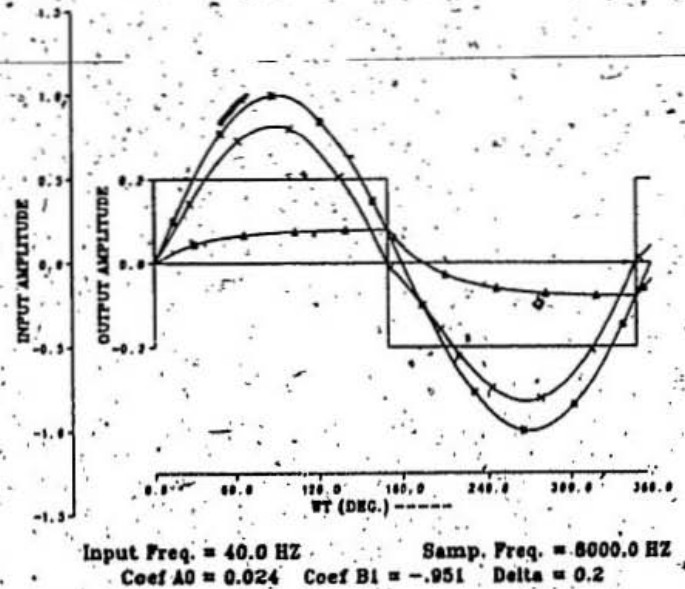


Fig. 4.25 EDM Waveforms for $\Delta = 0.2$

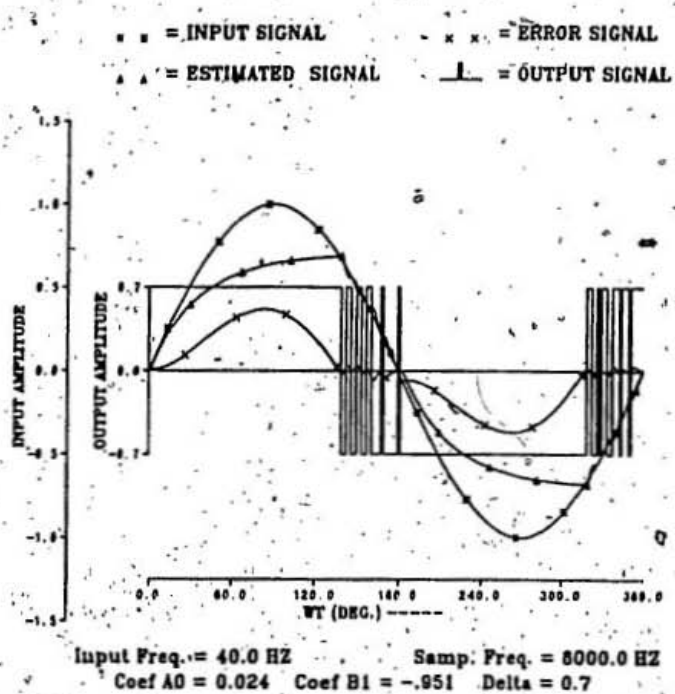


Fig. 4.26 EDM Waveforms for $\Delta = 0.7$

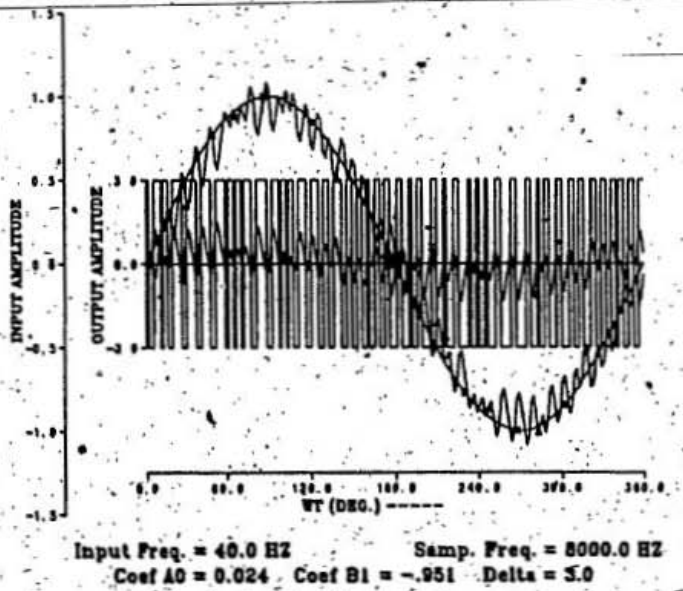


Fig. 4.27 EDM Waveforms for $\Delta = 3.0$

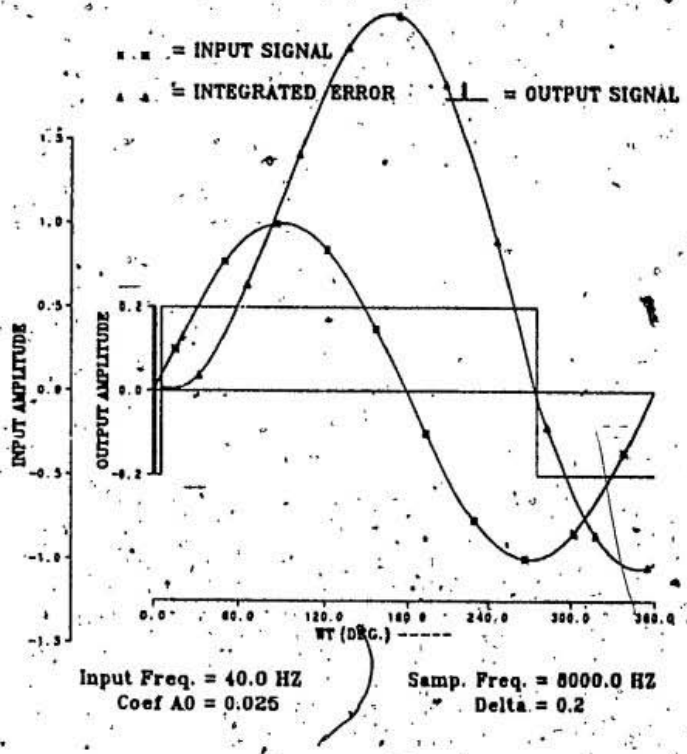


Fig. 4.28 SDM-Waveforms for $\Delta = 0.2$

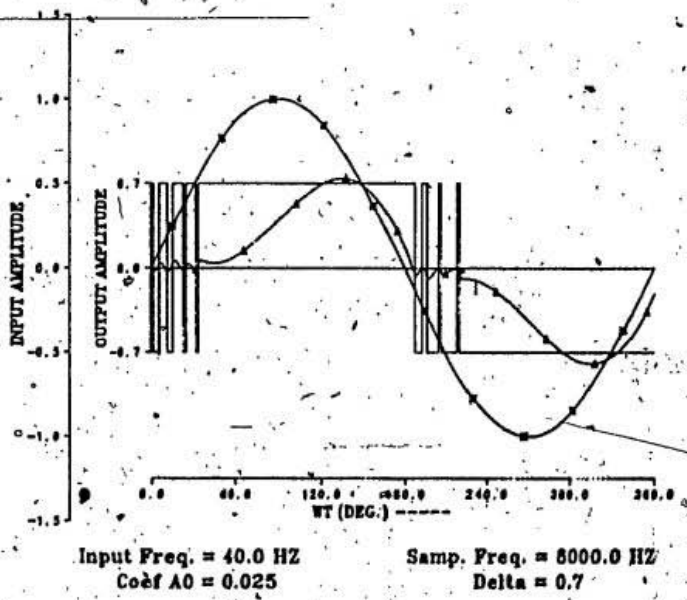


Fig. 4.29 SDM Waveforms for $\Delta = 0.7$

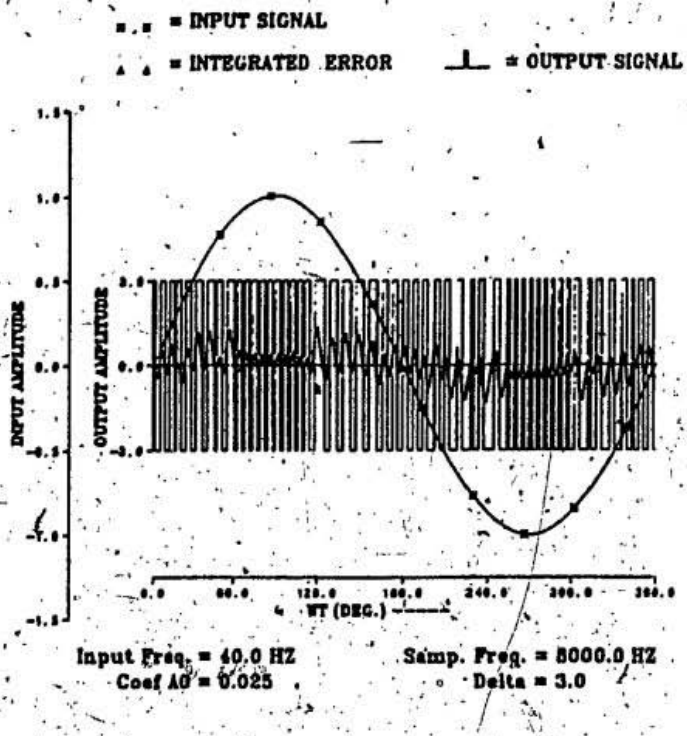


Fig. 4.30 SDM Waveforms for $\Delta = 3.0$

4.3 Harmonic behaviour of DM Systems

Harmonic content of the output of DM system can be calculated by using Fourier series method. If the number of pulses per half cycle and pulse positions are known, the Fourier coefficients can be given as follows [37]:

$$A_1 = \frac{2V}{\pi} \sum_{i=1}^{N} \left[-1^{i+1} \int_{\delta_i}^{\delta_{i+1}} \cos(\omega t)\, d(wt) \right] \tag{4.1}$$

$$= \frac{2V}{\pi} \sum_{i=1}^{N} \left[-1^{i+1} \left(\sin\delta_{i+1} - \sin\delta_i \right) \right] \tag{4.2}$$

Similarly,

$$A_3 = \frac{2V}{3\pi} \sum_{i=1}^{N} \left[-1^{i+1} \left(\sin 3\delta_{i+1} - \sin 3\delta_i \right) \right] \tag{4.3}$$

In general,

$$A_n = \frac{2V}{n\pi} \sum_{i=1}^{N} \left[-1^{i+1} \left(\sin n\delta_{i+1} - \sin n\delta_i \right) \right] \qquad (4.4)$$

and,

$$B_n = \frac{2V}{n\pi} \sum_{i=1}^{N} \left[-1^{i+1} \left(\cos n\delta_i - \cos n\delta_{i+1} \right) \right] \qquad (4.5)$$

Finally,

$$V_n = \sqrt{A_n^2 + B_n^2} \qquad (4.6)$$

where,

δ_i is the position of i^{th} pulse

N is the number of pulses per $\frac{1}{2}$ cycle

n is the order of harmonic

A_n & B_n are the n^{th} order Fourier coefficients respectively

V_n is the Amplitude of the n^{th} order harnonic

V is the Amplitude level of the DM output signal

Using the above expressions, the amplitudes of various harmonics in the DM output voltage can be calculated. Figs. 4.31 to 4.39 show the harmonic content of the output waveform of LDM, EDM and SDM for input frequencies of 20, 40, and 125 Hz respectively.

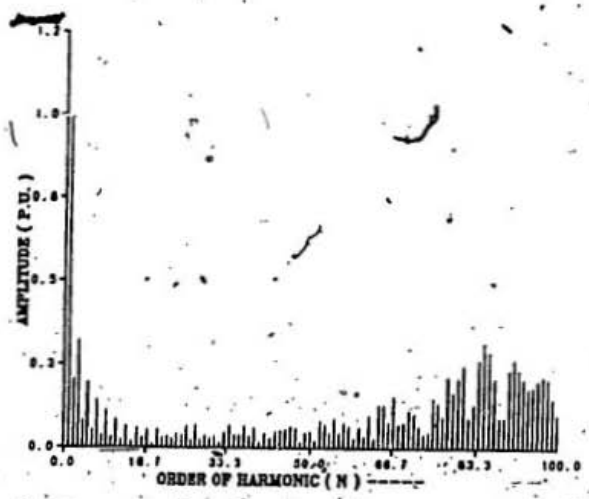


Fig. 4.31 Harmonic Content of LDM Output f = 20 Hz

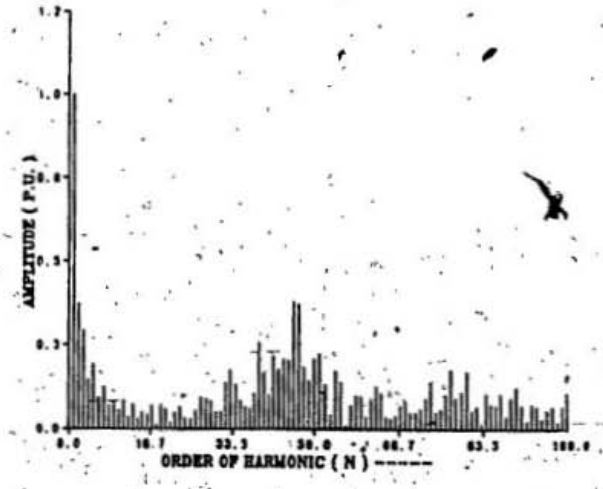
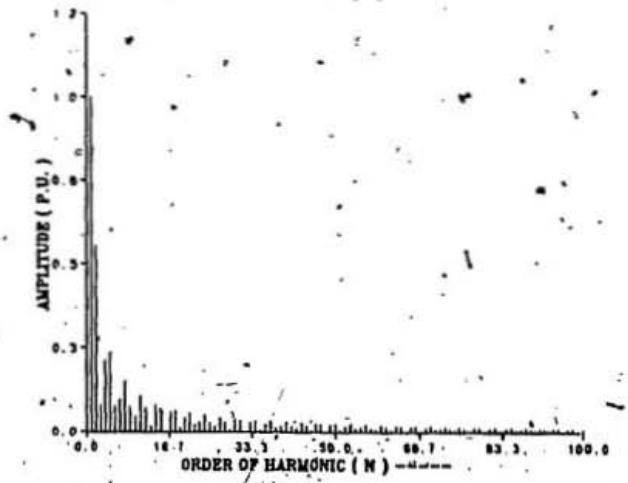
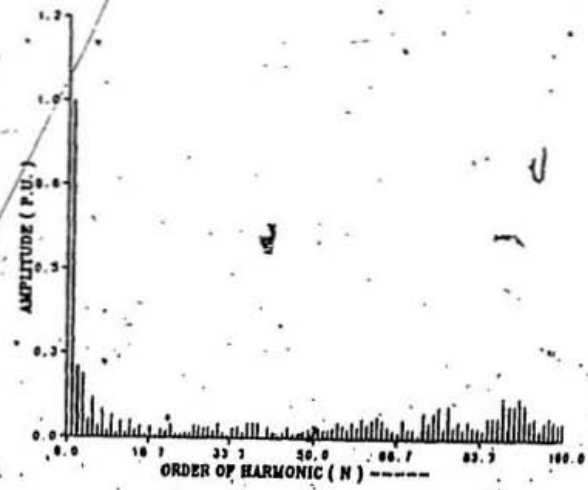


Fig. 4.32 Harmonic Content of LDM Output f = 40 Hz



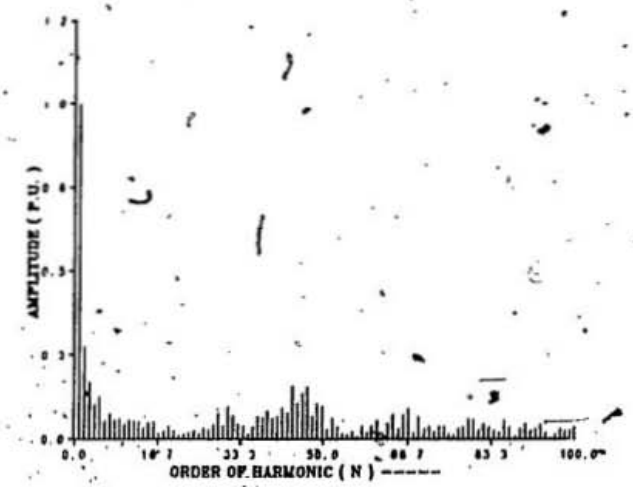
Input Freq. = 125.0 HZ Samp. Freq. = 8000.0 HZ
Coef A0 = 0.025 Delta = 1.0

Fig. 4.33 Harmonic Content of LDM Output f = 125 Hz



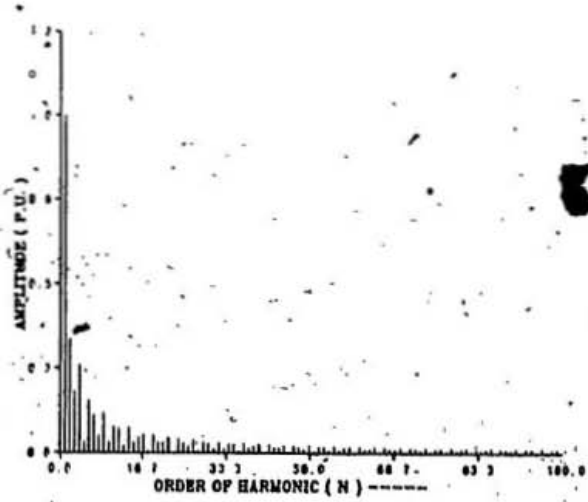
Input Freq. = 20.0 HZ Samp. Freq. = 8000.0 HZ
Coef A0 = 0.024 Coef B1 = -.951 Delta = 1.0

Fig. 4.34 Harmonic content of EDM Output f = 20 Hz



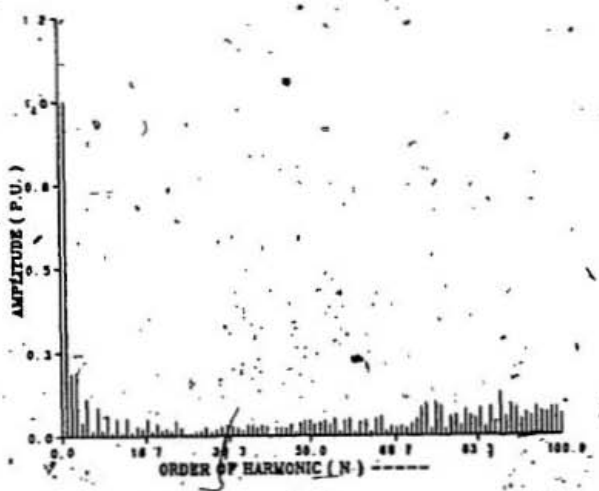
Input Freq. = 40.0 HZ Samp. Freq. = 8000.0 HZ
Coef A0 = 0.024 Coef B1 = -.951 Delta = 1.0

Fig. 4.35 Harmonic Content of EDM Output f = 40 Hz



Input Freq. = 125.0 HZ Samp. Freq. = 8000.0 HZ
Coef A0 = 0.024 Coef B1 = -.951 Delta = 1.0

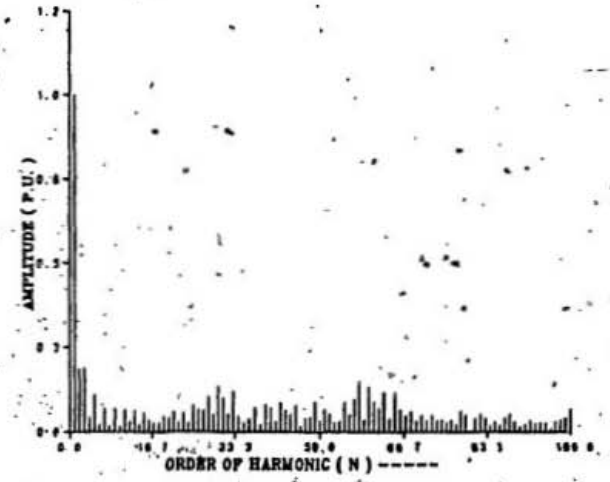
Fig. 4.36 Harmonic Content of EDM Output f = 125 Hz



Input Freq. = 20.0 HZ
Coef A0 = 0.025

Samp. Freq. = 8000.0 HZ
Delta = 1.0

Fig. 4.37 Harmonic Content of SDM Output f = 20 Hz



Input Freq. = 40.0 HZ
Coef A0 = 0.025

Samp. Freq. = 8000.0 HZ
Delta = 1.0

Fig. 4.38 Harmonic Content of SDM Output f = 40 Hz

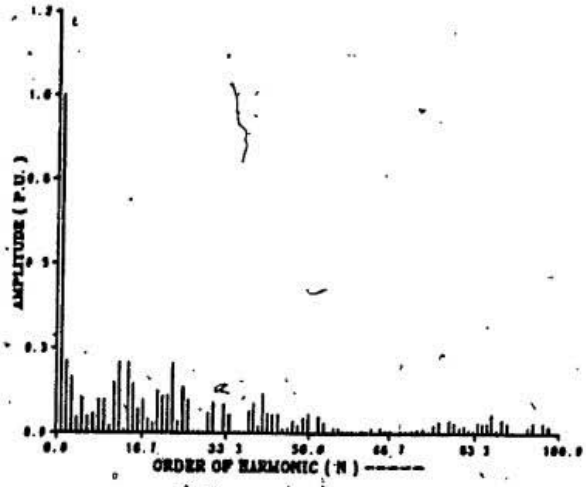


Fig. 4.39 Harmonic Content of SDM Output f = 125 Hz

Figures 4.31 - 4.39 clearly demonstrate that at lower input frequencies, the magnitude of the lower order harmonics are low, whereas the magnitude of the higher harmonics are greater. At high frequency operation, the higher harmonics gradually decrease and the prominence of fundamental component increases. It is observed that spectral characteristics of LDM are poor and those of SDM are best. The output voltage harmonic contents in the LDM are highest whereas in SDM, the harmonic contents are lowest. Thus, spectral characteristics of sigma delta modulator are superior to those of linear and exponential delta modulators.

CHAPTER 5

EXPERIMENTAL RESULTS OF SOFTWARE CONTROLLED DELTA MODULATED INVERTERS

This chapter describes the results obtained by software controlled DM inverters. Different delta modulators simulated by software, successfully generate modulated output signal. The modulated output signal is subsequently processed to produce base drive signals which are applied to the inverter transistors through base drive circuits. Base drive circuits generate actual gating signals which control the switching operation of inverter transistors. DM output signal corresponding to one full cycle of input frequency and a given set of parameters, are stored in the RAM of the microcomputer in the form of look-up tables. The microcomputer then generates actual switching signals by using pattern retrieval method to control the operation of the inverter.

5.1 Operational Characteristics of Different DM Techniques

In this section, output waveforms generated by various microprocessor based delta modulators are described. The output signal generated by the microprocessor, closely resembles the signals obtained by the simulation of DM system. The power spectrum of the outputs of various delta modulators are obtained by using the WAVETEK spectrum Analyser, Model 5820A.

5.1.1 DM Output and Harmonic Content

The input and output waveforms generated by the microprocessor based delta modulators are shown in Figs. 5.1 to 5.3 for linear delta modulator, exponential delta modulator, and sigma delta modulator respectively. Input amplitude, sampling frequency, R and C values and step size are chosen to be 1, 4 kHz, 50 kohm, and 0.05 microfarads and 1 respectively. The frequency is varied from 20 Hz to 200 Hz. From these figs. 5.1 - 5.3, it is clear that higher operating frequencies overload the modulator. Due to this overloading effect, modulator produces a square wave at the output.

The power spectrum of the output of various microprocessor based delta modulators obtained from Spectrum Analyser are shown in Figs. 5.4 to 5.6. These figs. 5.4 - 5.6, clearly demonstrate that at low frequency operations, dominant harmonic components lie far away from the fundamental component. The harmonic content decreases with an increase in the operating frequency. At high frequency operation the fundamental component becomes prominent and the amplitude of subsequent harmonic components decreases.

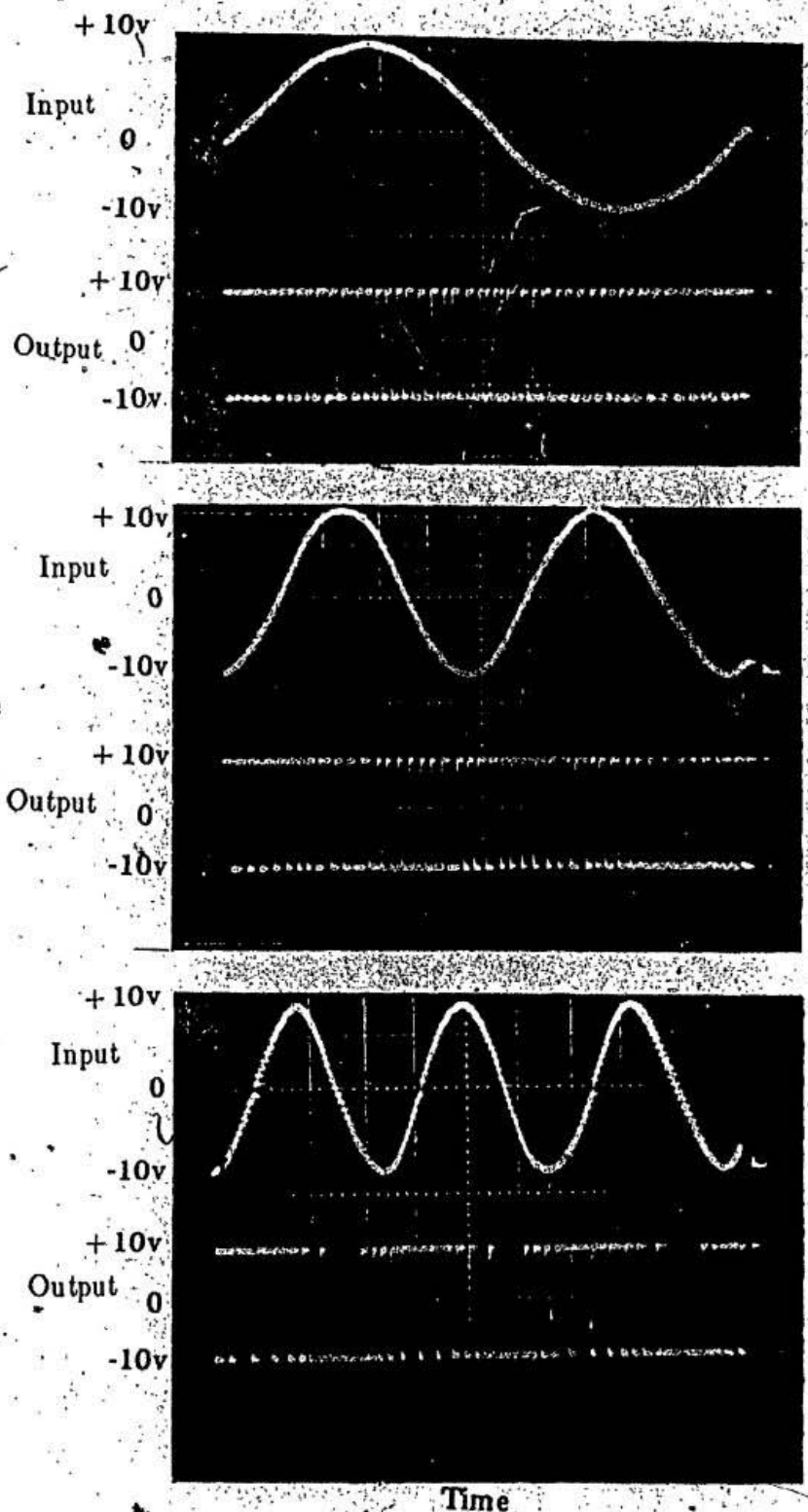


Fig.5.1a LDM Input and Output Waveforms for f = 20, 40, and 60 Hz

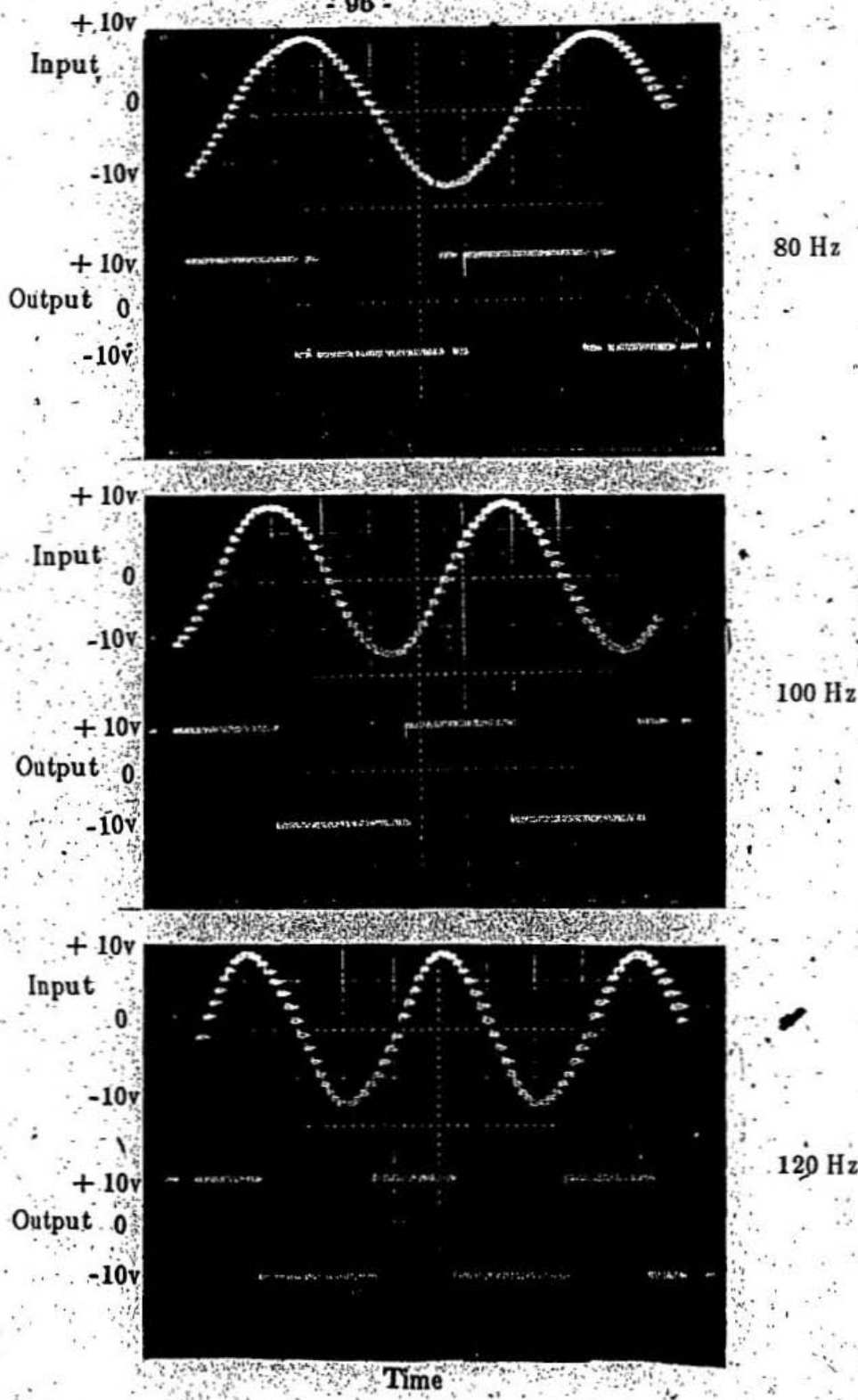


Fig. 5.1b LDM Input and Output Waveforms for f = 80, 100, and 120 Hz

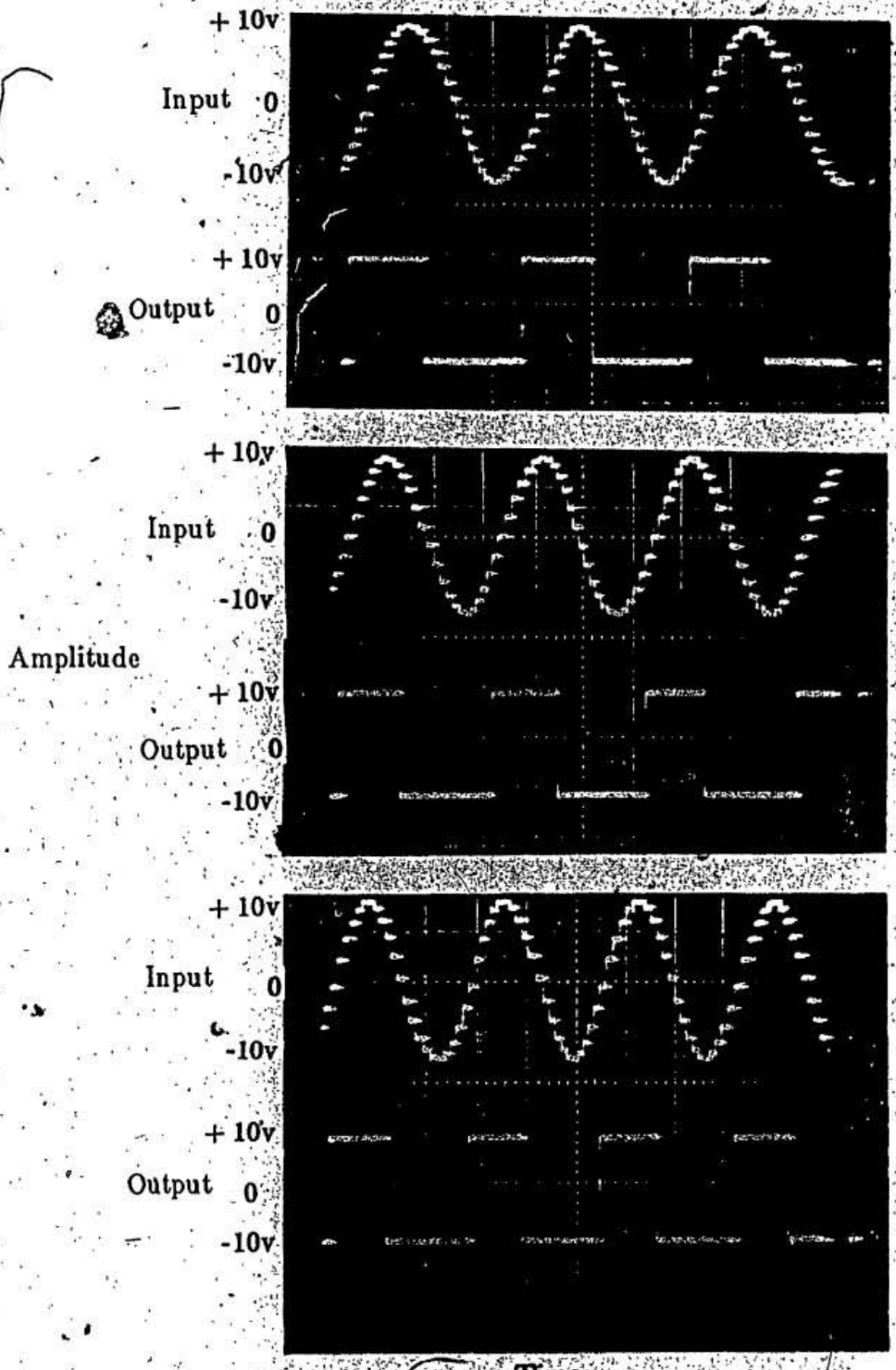


Fig. 5.1c LDM Input and Output Waveforms for f = 140, 160, and 180 Hz

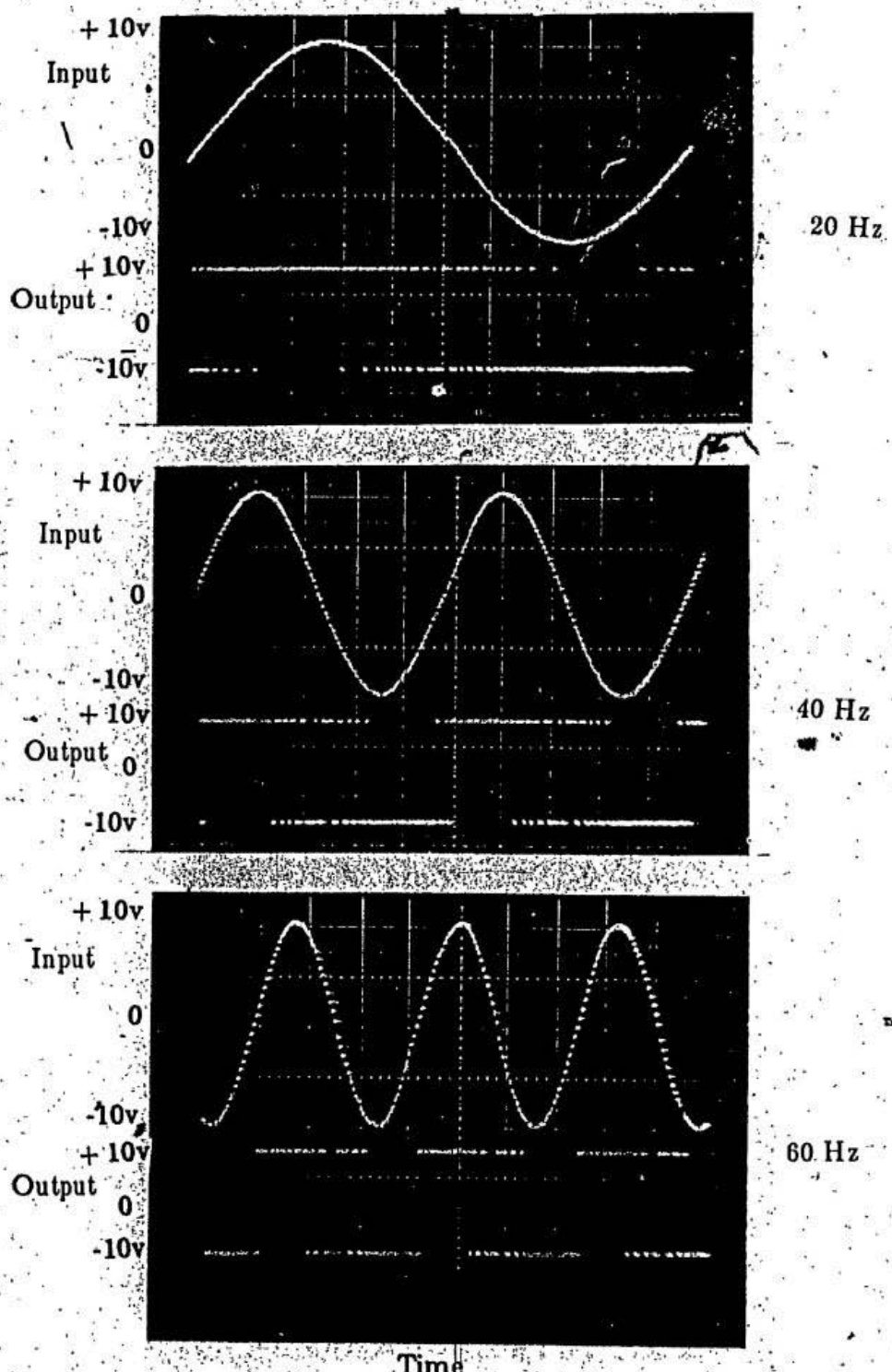


Fig. 5.2a EDM Input and Output Waveforms for f = 20, 40, and 60 Hz

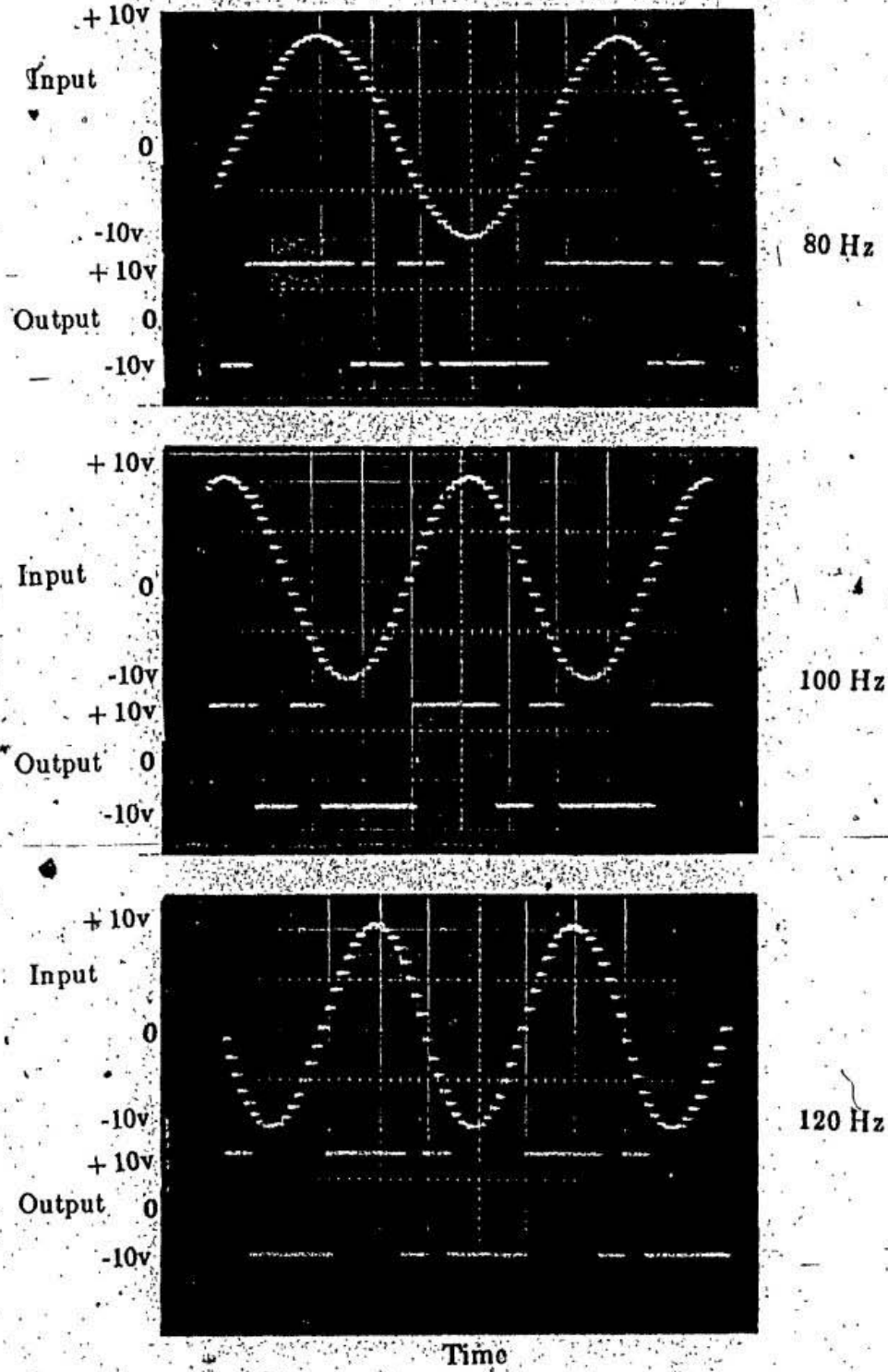


Fig. 5.2b EDM Input and Output Waveforms for f = 80, 100, and 120 Hz

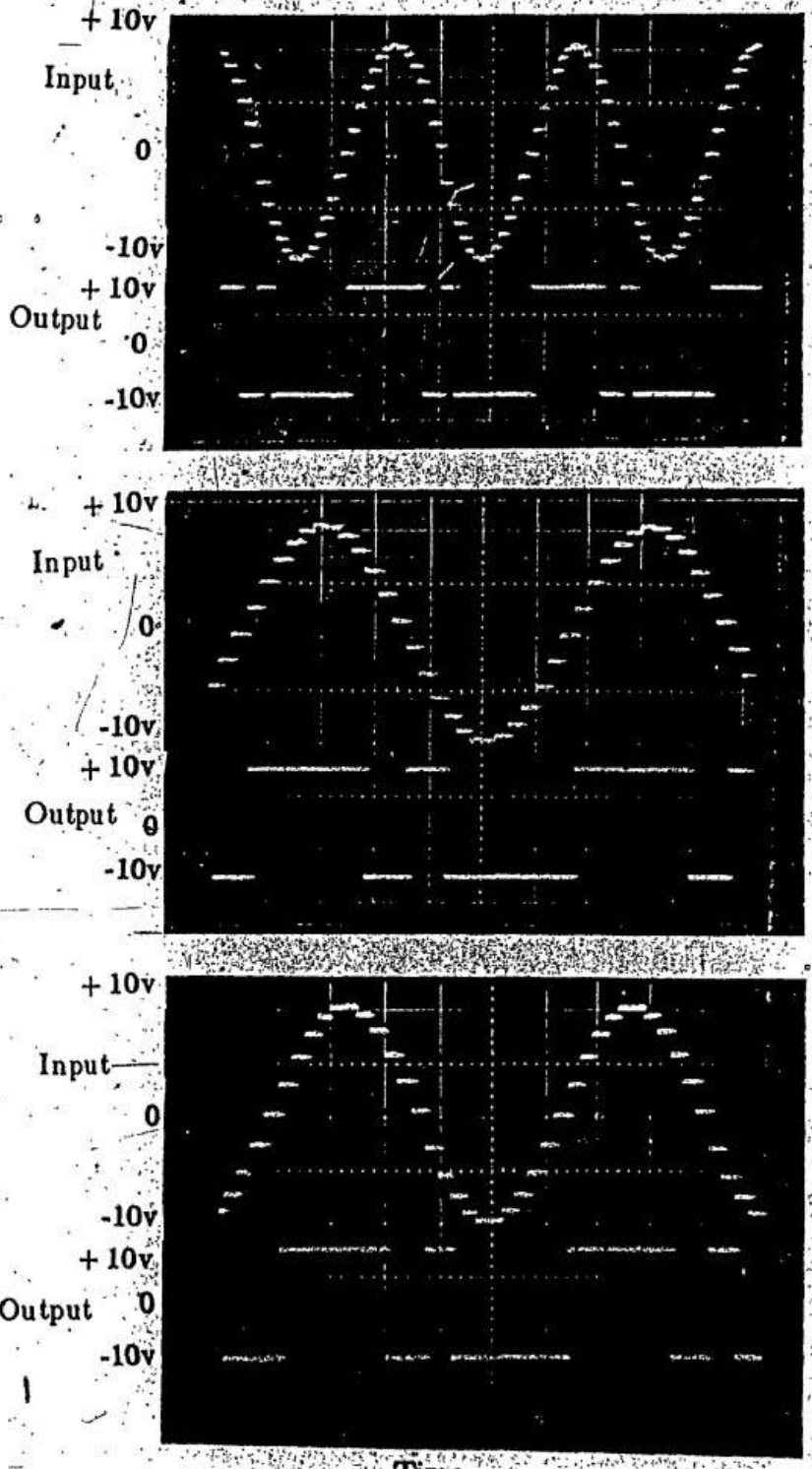


Fig. 5.2c EDM Input and Output Waveforms for f = 140, 160, 180 Hz

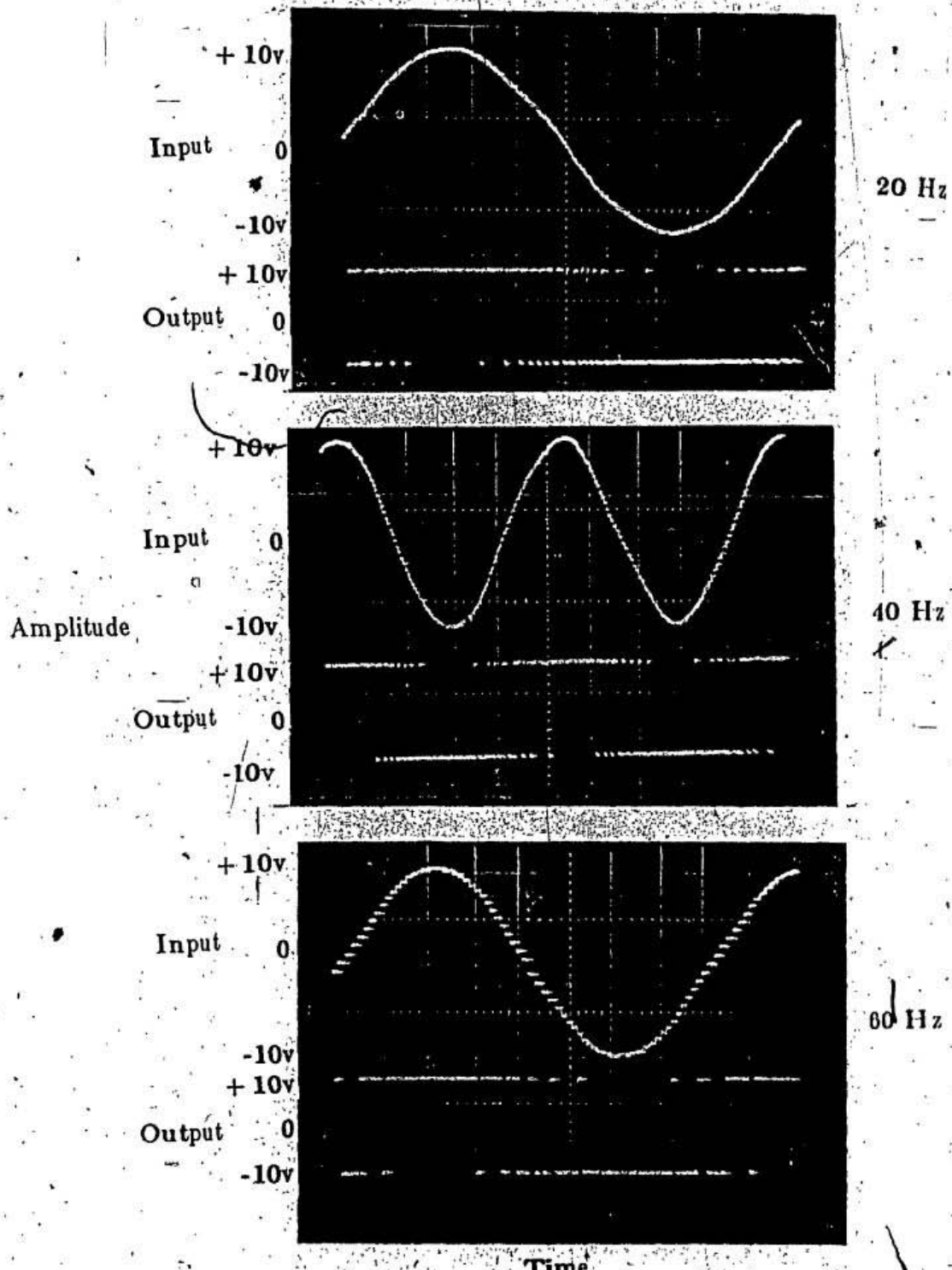
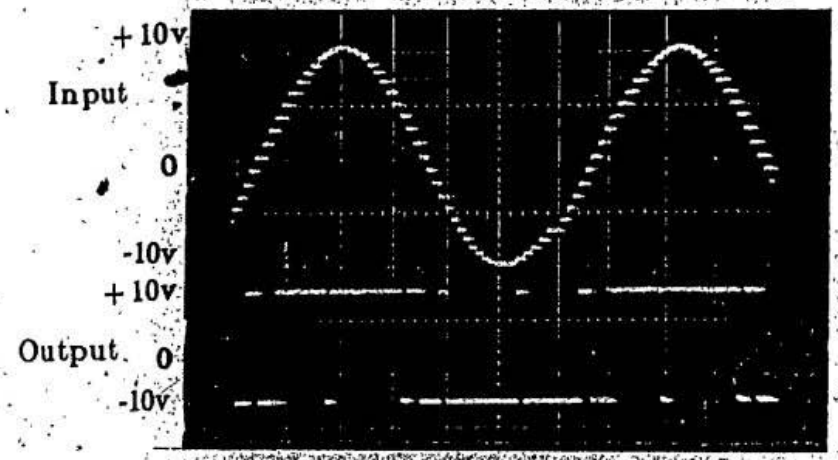
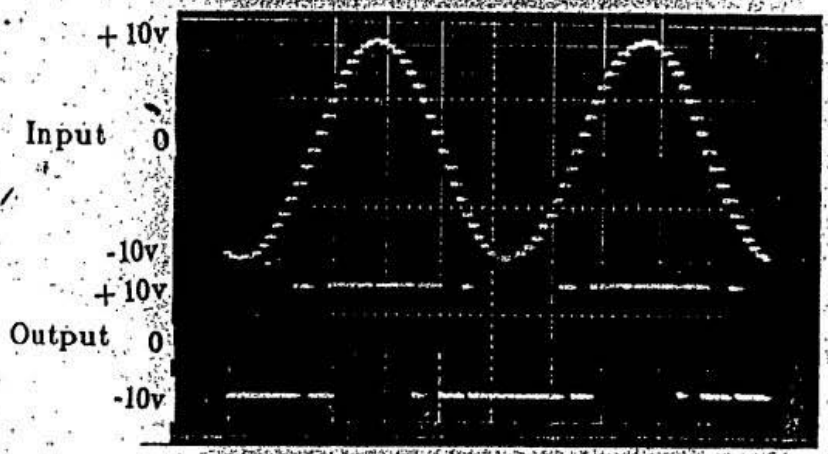
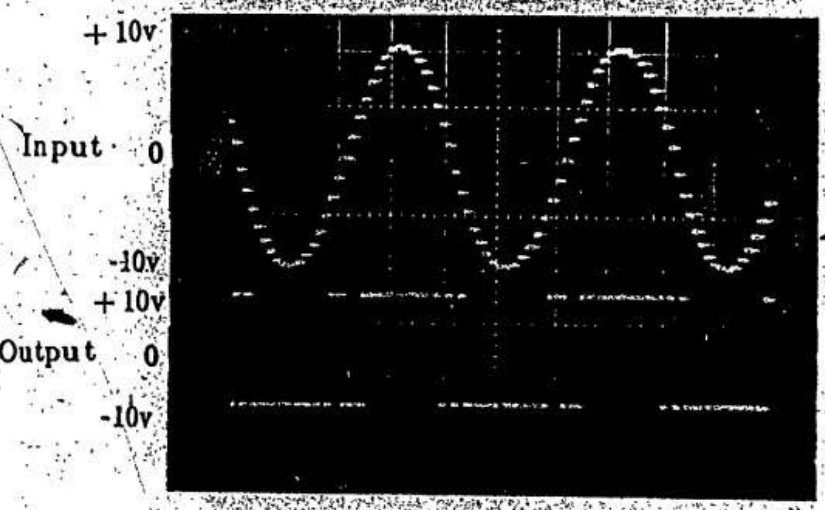


Fig. 5.3a SDM Input and Output Waveforms for f = 20, 40, and 60 Hz







Time

Fig. 5.3b SDM Input and Output Waveforms for f = 80, 100, and 120 Hz

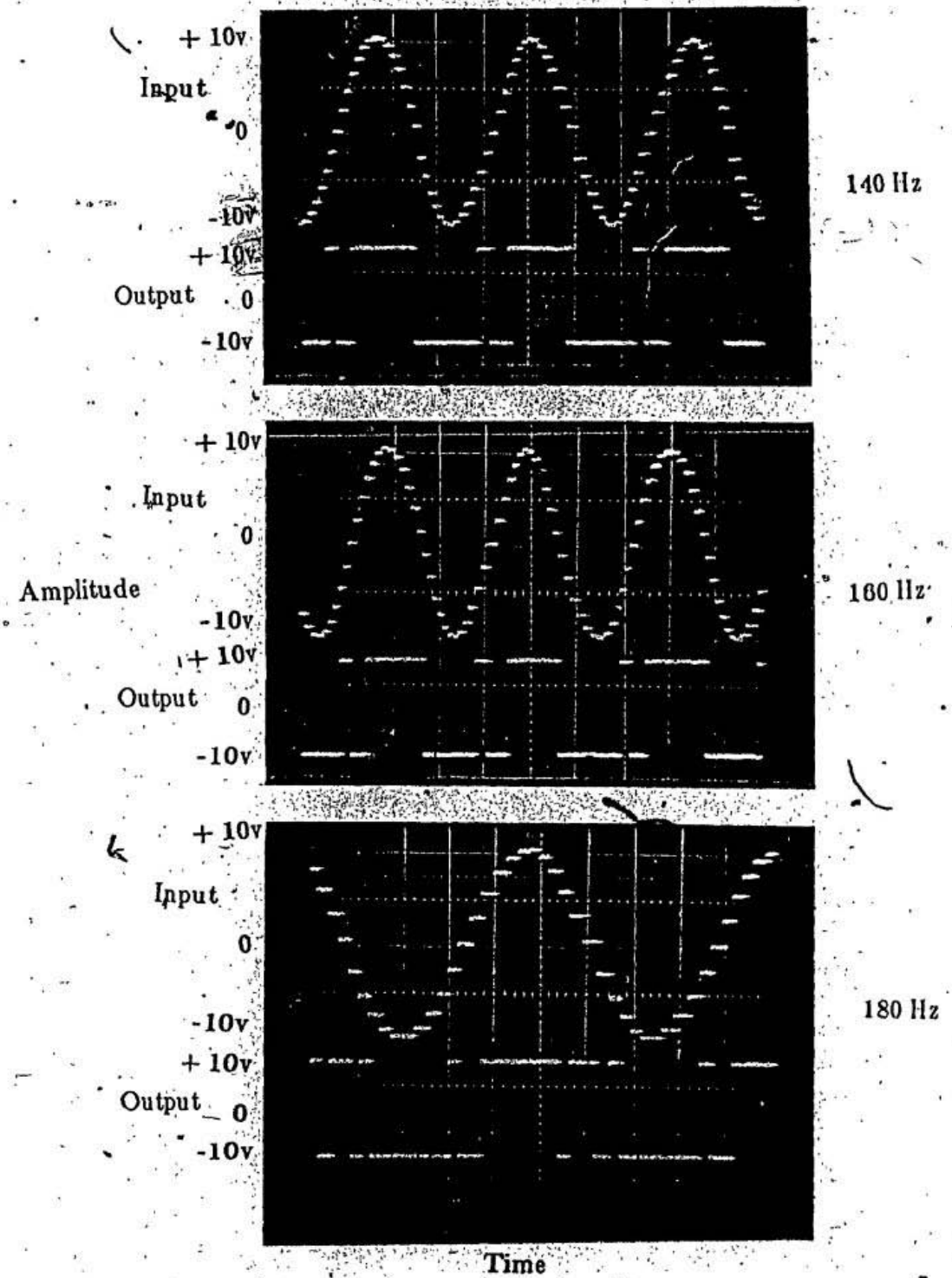


Fig. 5.3c SDM Input and Output Waveforms for f = 140, 160, and 180 Hz

Figs. 5.4 to 5.6 show that in case of linear delta modulator (LDM), the fundamental voltage increases with frequency up to base frequency and remains at a constant level after base frequency. At lower frequencies of operation, the magnitude of the lower order harmonics (3rd, 5th, 7th, etc.) is very low, whereas the magnitude of the higher order harmonics is greater. At higher operating frequencies, the amplitude of higher order harmonics gradually decreases and the prominence of fundamental component increases.

When operating frequency is gradually increased, the fundamental voltage of exponential delta modulator (EDM) output decreases. In the case of sigma delta modulator (SDM) however, fundamental voltage remains constant at all frequencies above and below the base frequency.

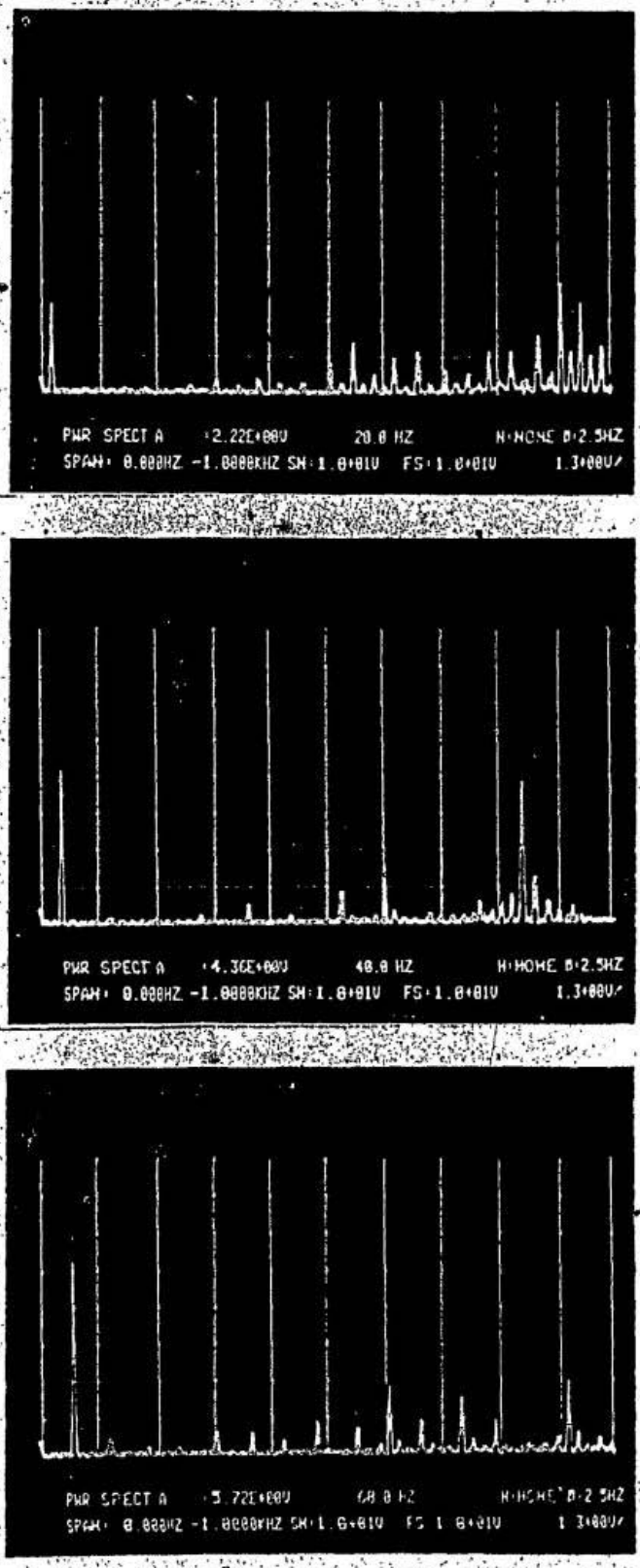
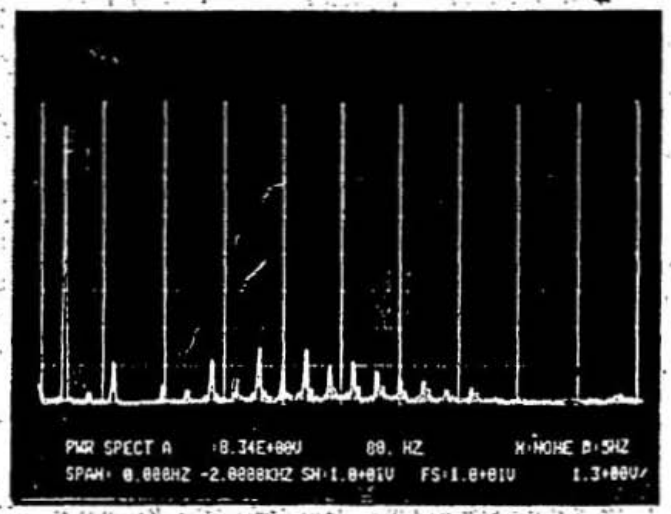
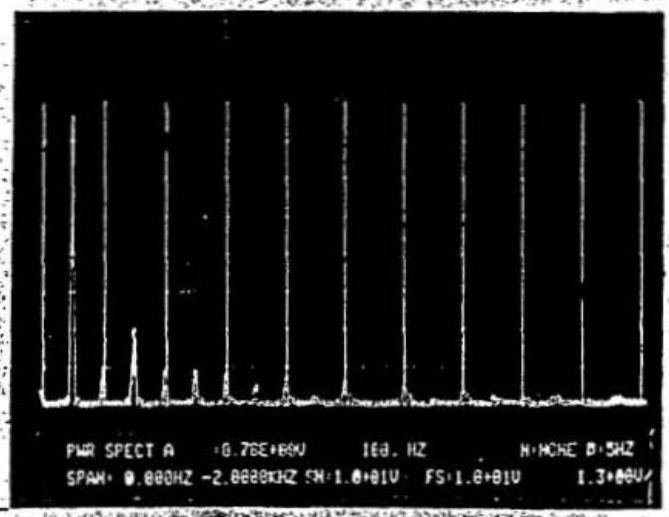


Fig. 5.4a Power Spectrum of LDM Output at f = 20, 40, and 60 Hz





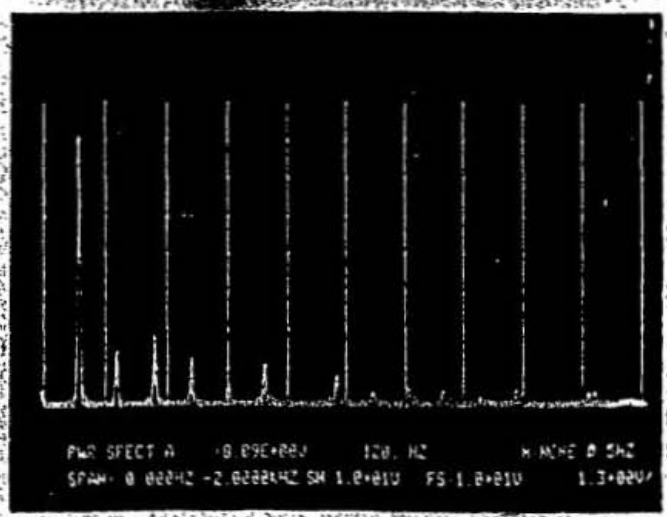
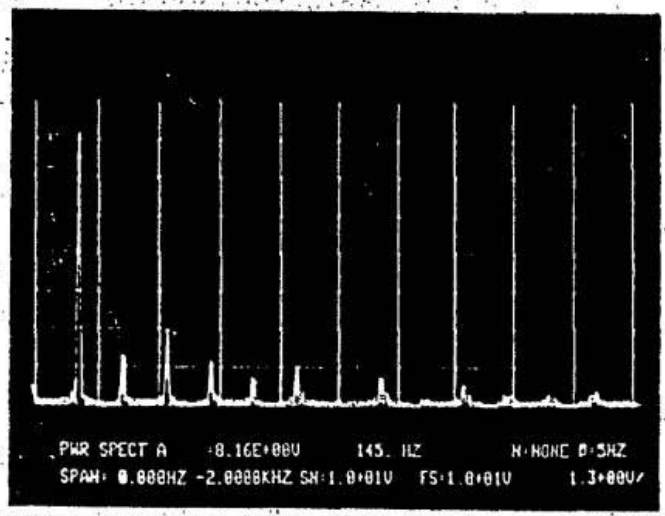
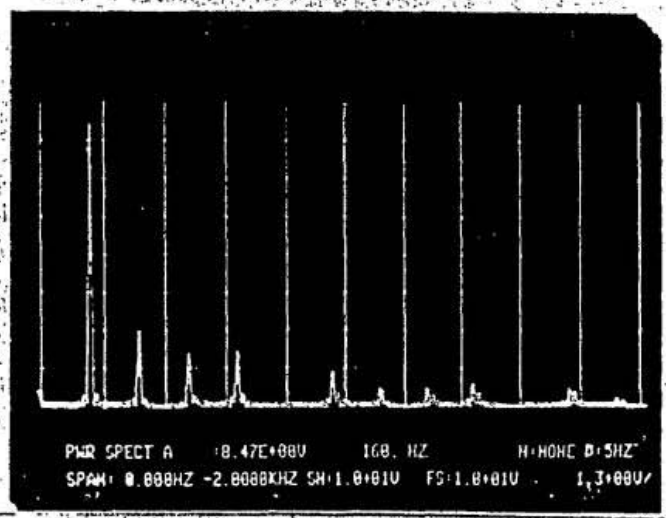


Fig. 5.4b Power Spectrum of LDM Output at f = 80, 100, and 120 Hz





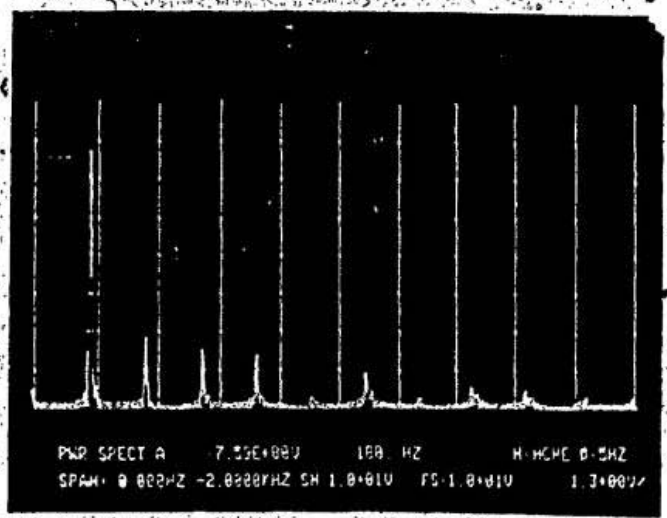


Fig. 5.4c Power Spectrum of LDM Output at f = 145, 160, and 180 Hz.

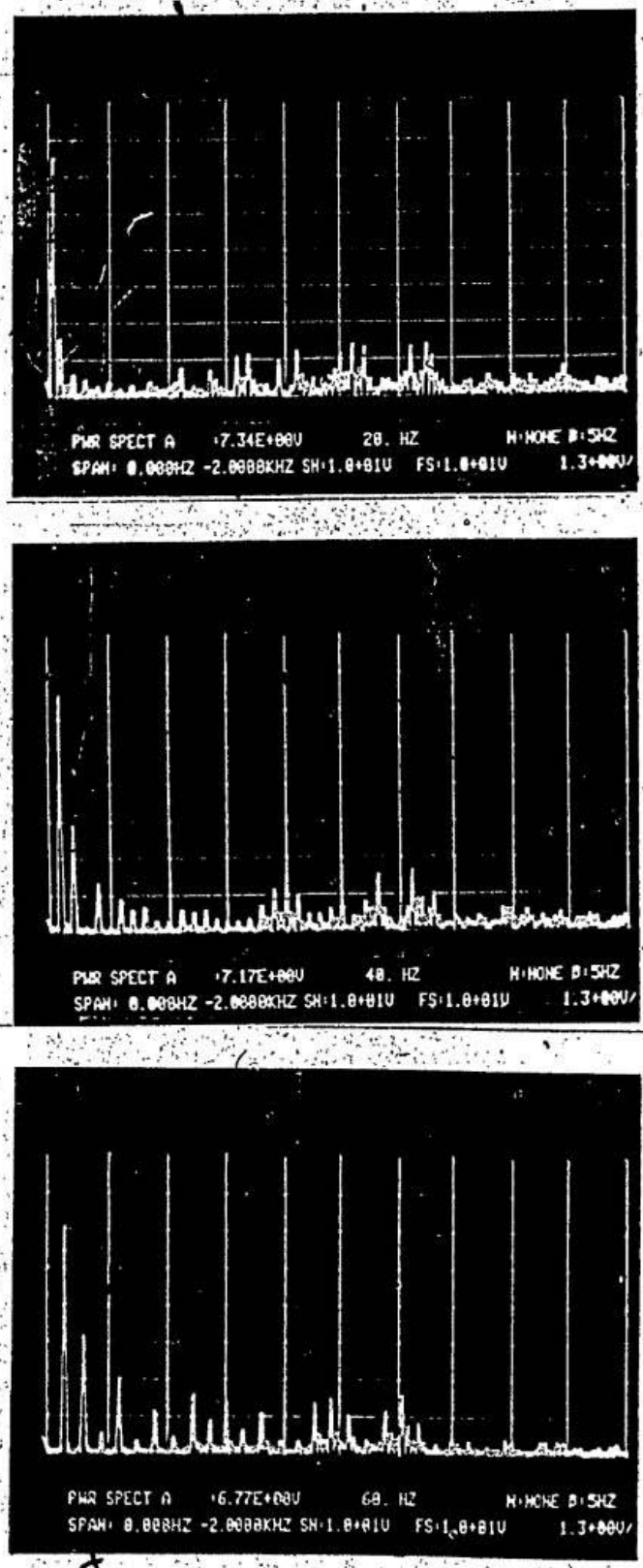


Fig. 5.5a Power Spectrum of EDM Output at f = 20, 40, and 60 Hz

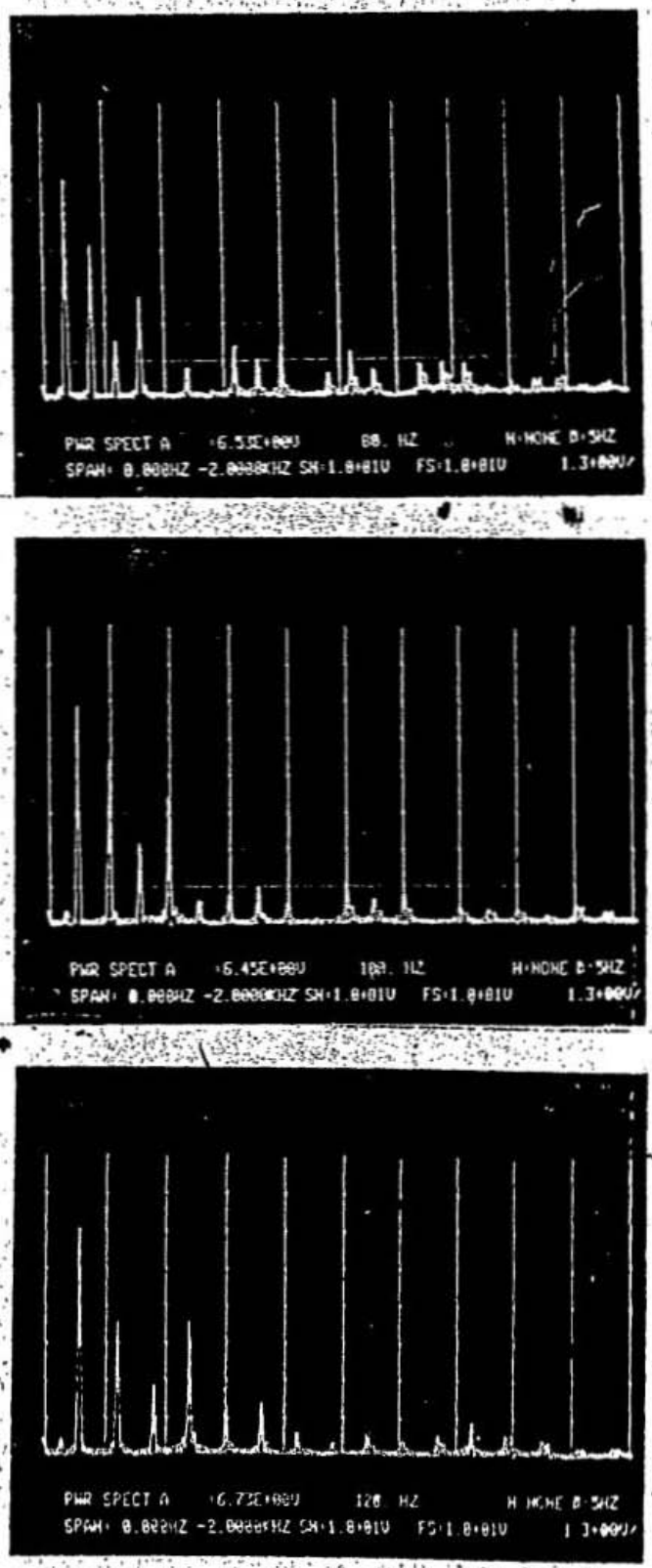


Fig. 5.5b Power Spectrum of EDM Output at f = 80, 100, and 120 Hz

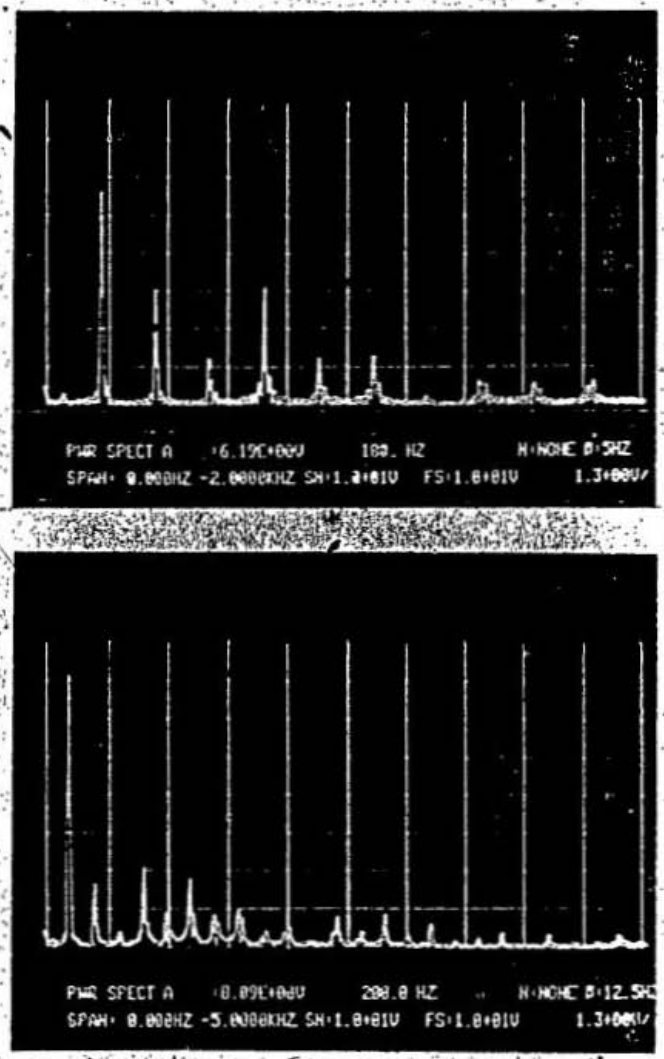
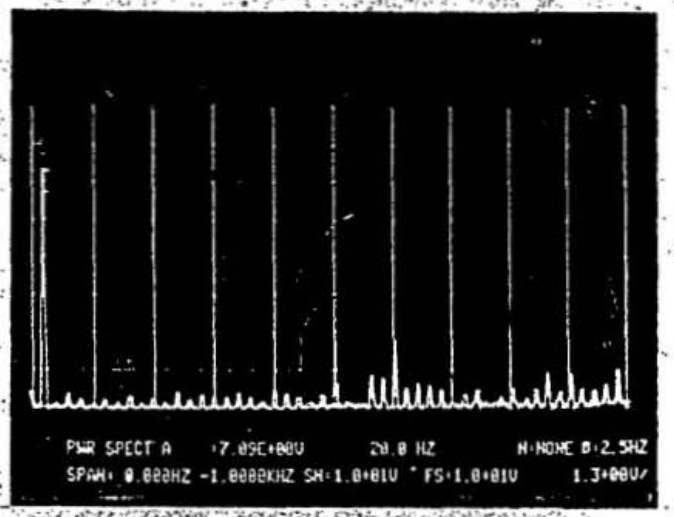
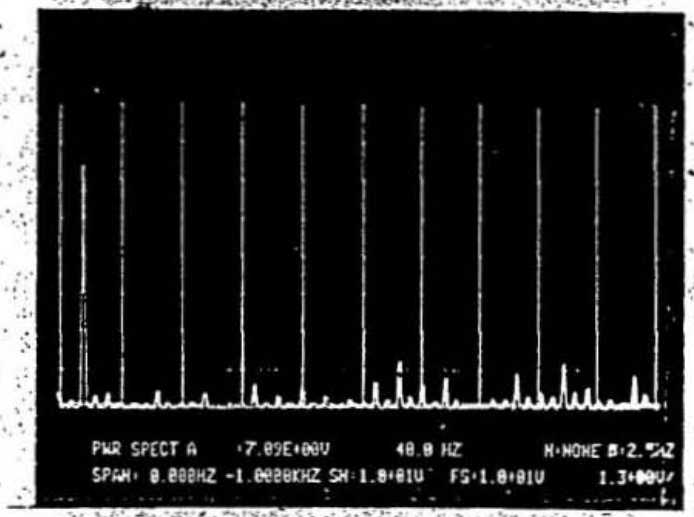


Fig. 5.5c Power Spectrum of EDM Output at f = 180 and 200 Hz





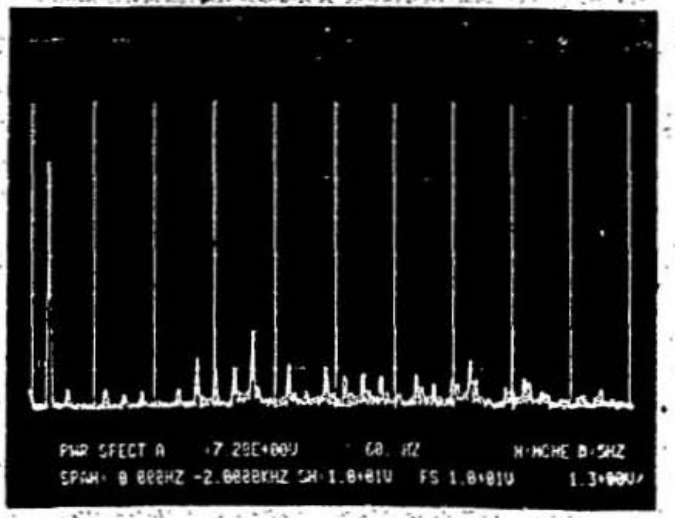


Fig. 5.6a Power Spectrum of SDM Output at f = 20, 40, and 60 Hz

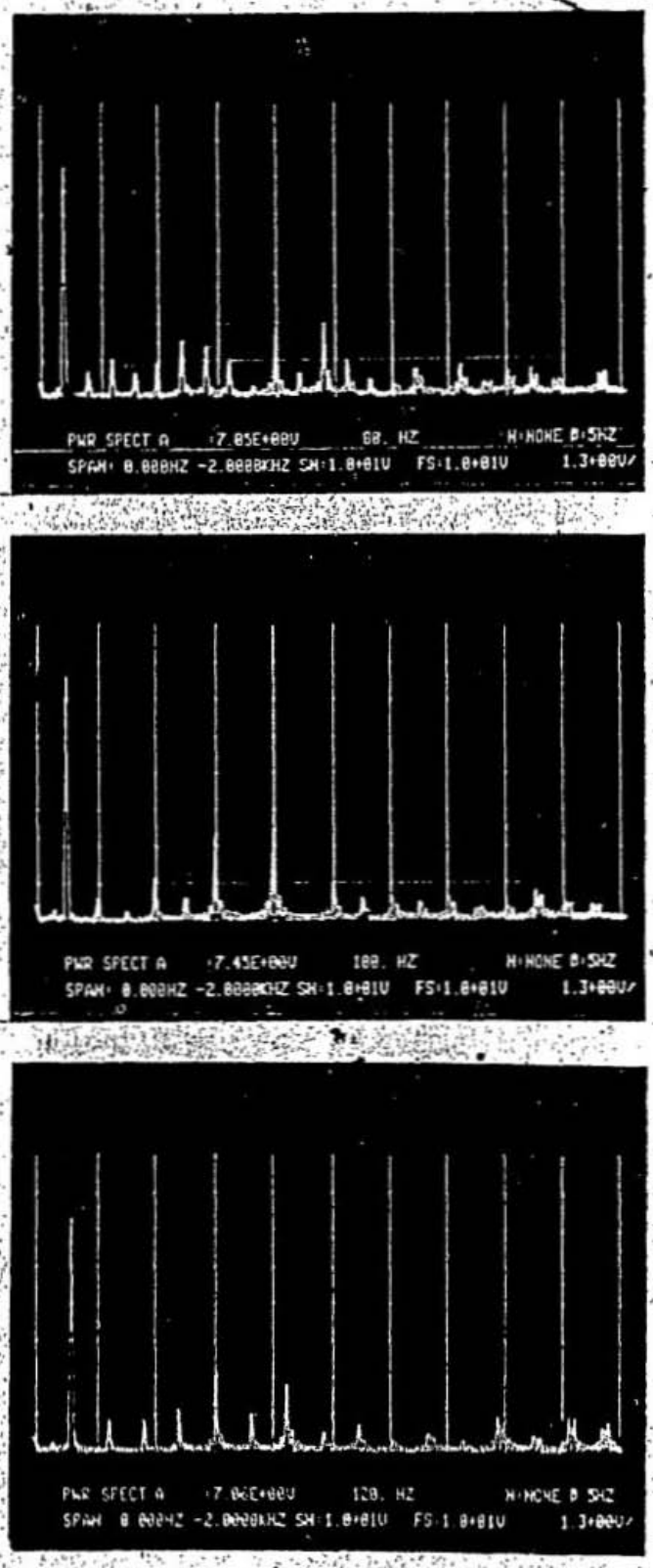


Fig. 5.6b Power Spectrum of SDM Output at f = 80, 100, and 120 Hz

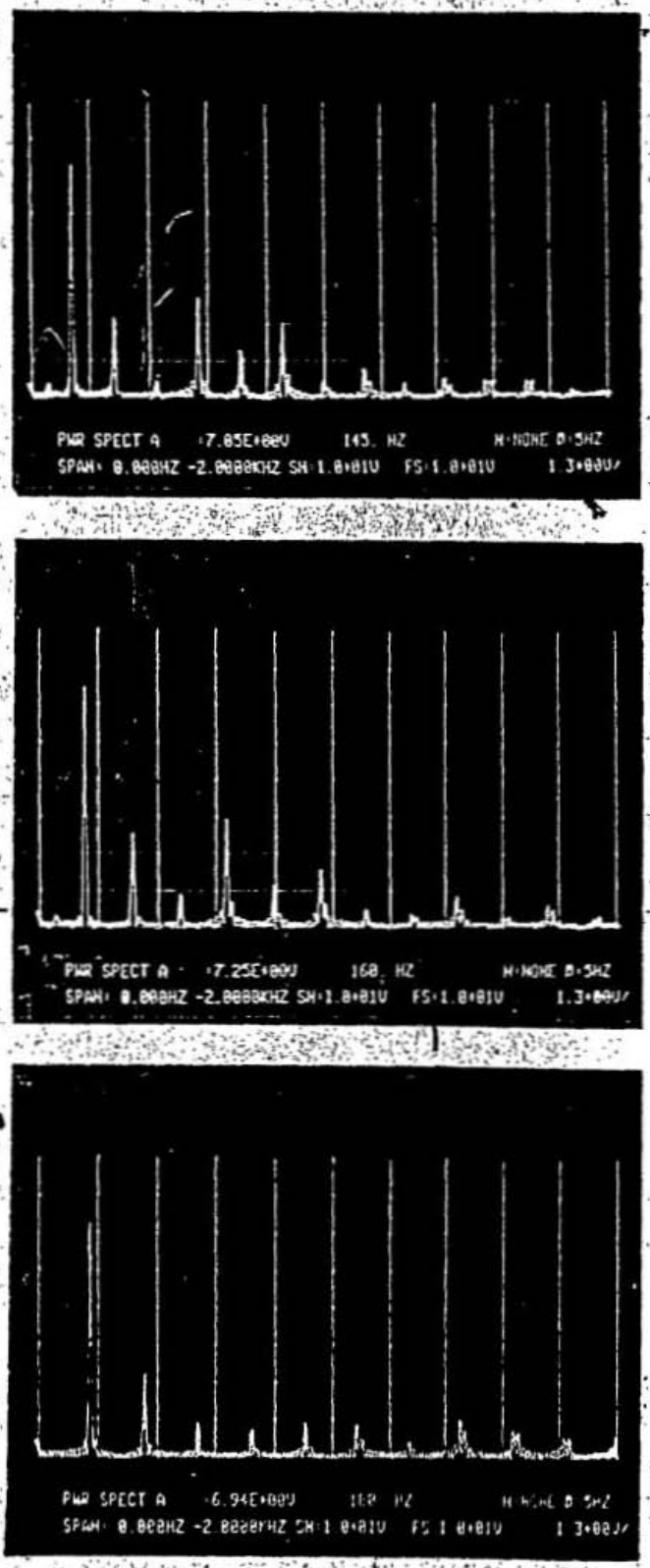


Fig 5.6c Power Spectrum of SDM Output at
f = 145, 160, and 180 Hz

5.1.2 Number of Commutations

From preceding discussion of various results, it is clear that the number of output pulses produced by various DM systems depends on the selection of parameter values. As sampling frequency is increased, number of pulses generated by the three DM systems also increases. For a fixed sampling rate, the number of output pulses decreases as the operating frequency increases. The number of output pulses is directly proportional to the number of commutations in the inverter, since commutation takes place at every switching point of the modulated wave pulse. The number of commutations is associated with commutation losses in the inverter. Therefore, as the number of commutations increases, commutation loss in the inverter also increases. The latter situation is not desired.

Figs. 5.7 to 5.9 show the variation of number of commutations with frequency in the three DM systems under consideration for three sampling frequencies (f_s = 2 kHz, 4 kHz, and 6 kHz respectively)

These figures demonstrate that at lower operating frequencies, the number of commutations is more in linear delta modulator than in exponential delta modulator and sigma delta modulator. However, at higher operating frequencies, the number of commutations becomes the same for all three DM systems.

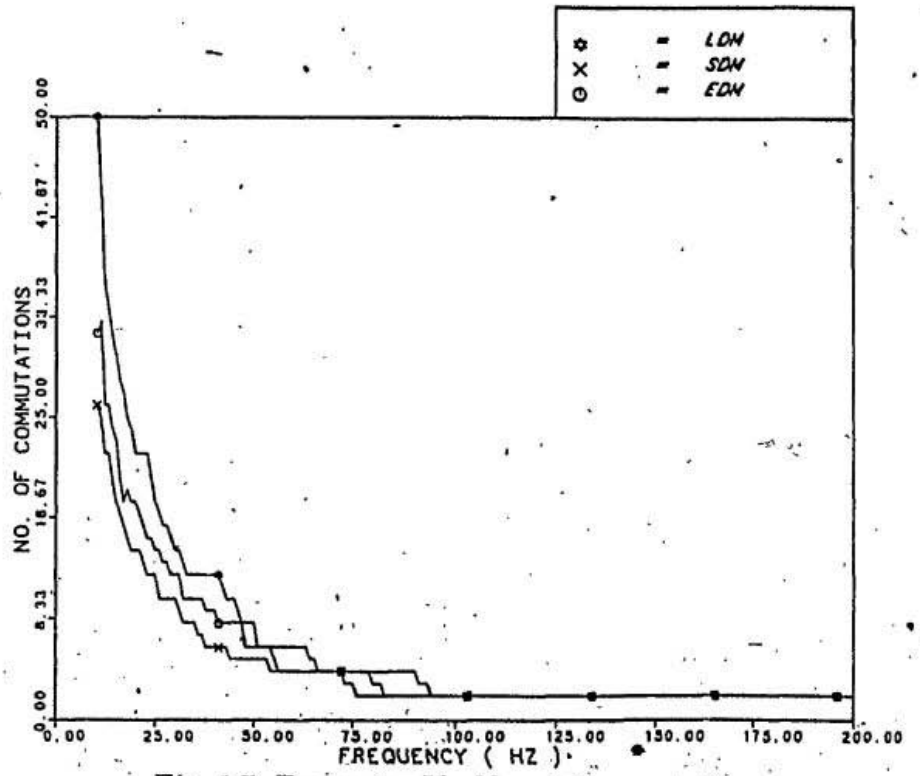


Fig. 5.7 Frequency Vs. No. of Commutations
R = 50 K-Ohms, C = 0.05 Microfarads, f_s = 2000 Hz, Delta = 1.0

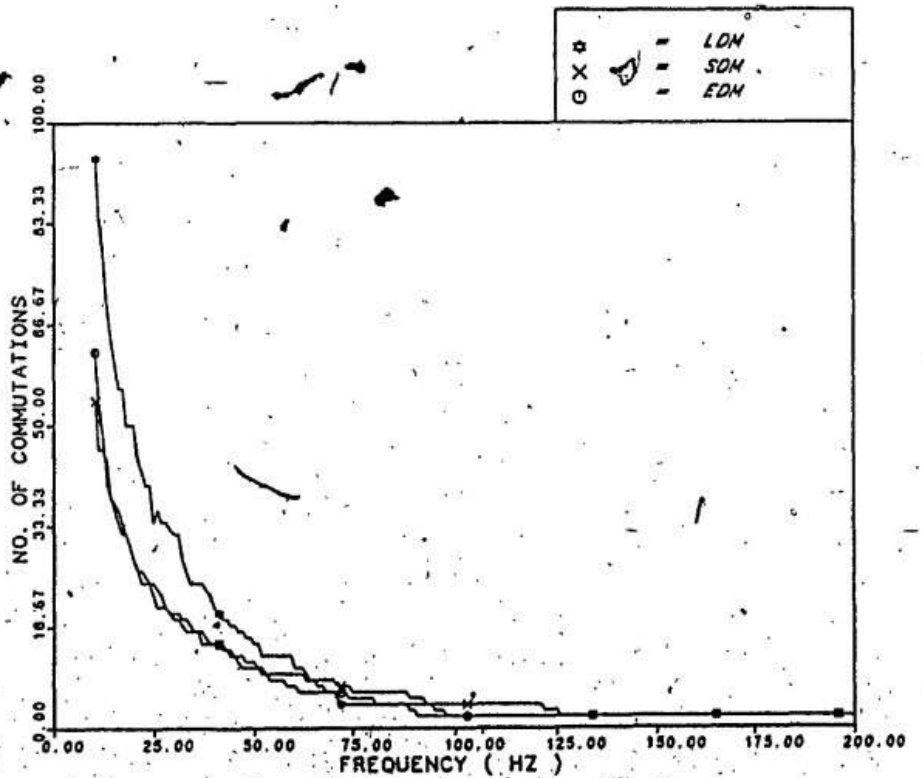


Fig. 5.8 Frequency Vs No. of Commutations
R = 50 K-Ohms, C = 0.05 Microfarads, f_s = 4000 Hz, Delta = 1.0

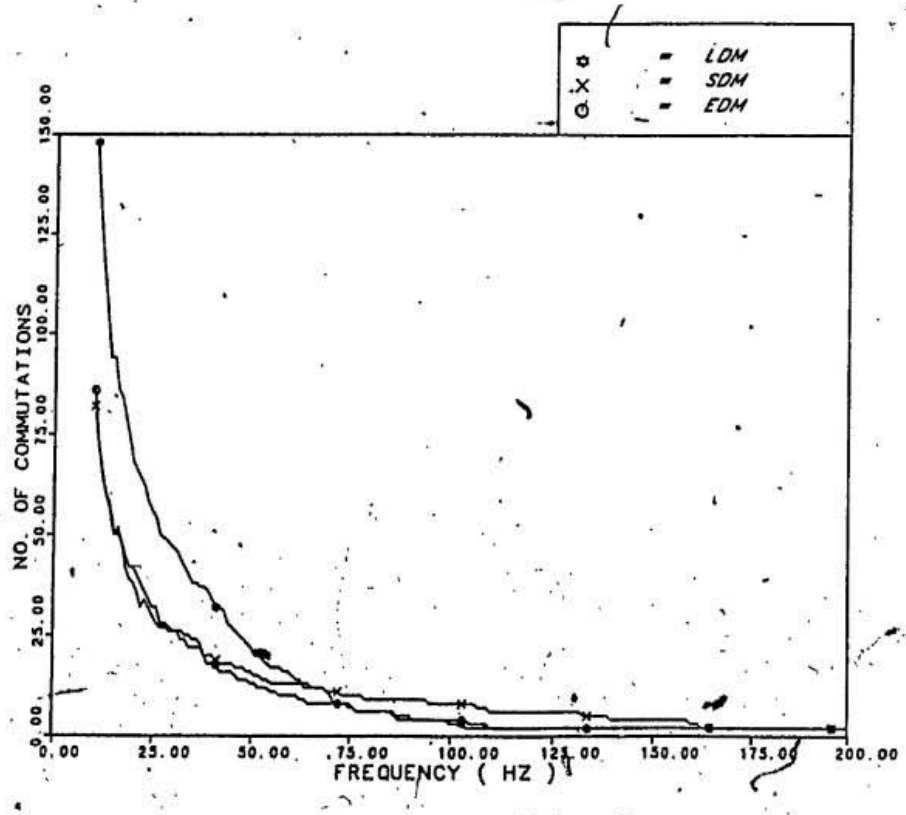


Fig. 5.9 Frequency Vs No. of Commutations
R = 50 K-Ohms, C = 0.05 Microfarads, f_s = 6000 Hz, Delta = 1.0

5.1.3 Available Voltage

Voltage available at the output of the inverter for various operating frequencies is shown in Fig. 5.10. Sampling frequency and delta are kept constant at 4 kHz and 1 respectively. The operating frequency is varied from 20 to 200 Hz.

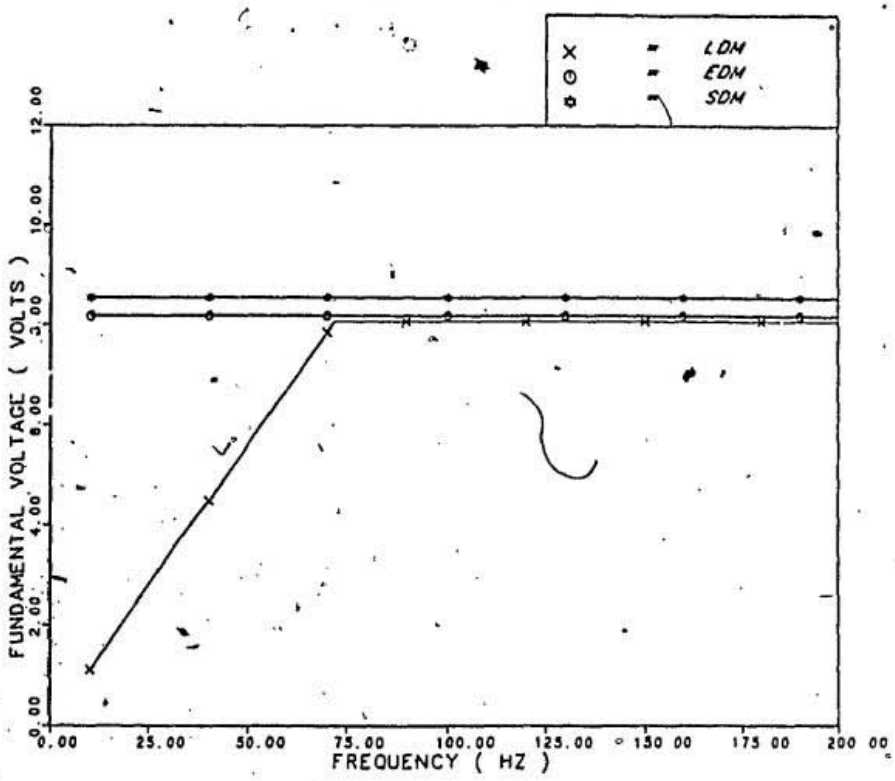


Fig. 5.10 Output Voltage vs. Frequency Characteristics of LDM, EDM and SDM

From Fig. 5.10, it is observed that for LDM the output voltage of the inverter increases with frequency up to base frequency and remains constant beyond base frequency. However, the output voltage in EDM and in SDM is constant at all frequencies. This agrees with the theoretical results.

5.2 Single-Phase Inverter with Resistive and Motor Load

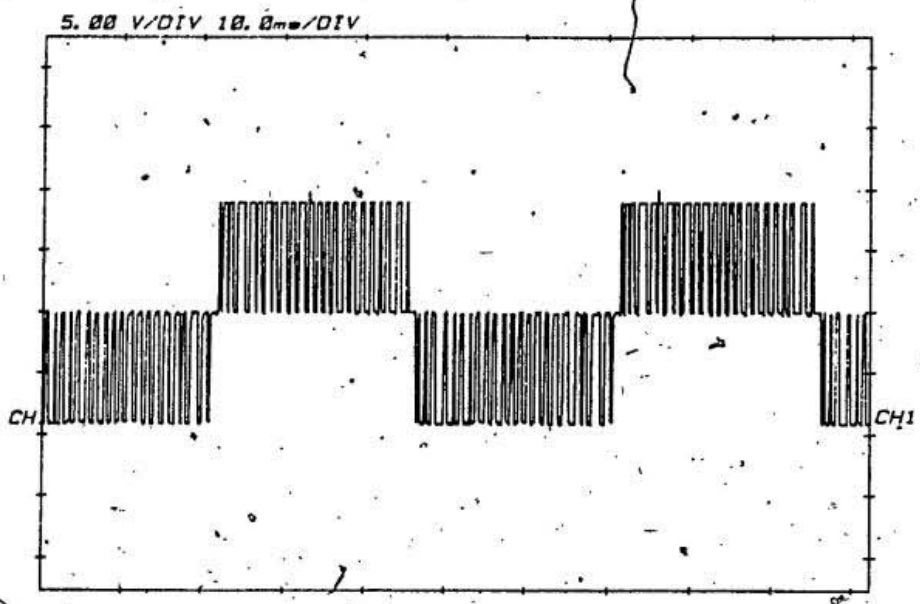
This section deals with the results obtained from a single phase (1- ϕ) full bridge inverter controlled by delta modulated switching signals which are generated by microprocessor. The loads applied at the inverter output are resistive and motor loads.

Like other inverters, the output of a delta modulated inverter contains harmonics. The harmonic content, together with the fundamental component, determine the performance of the load under study. As shown in previous sections, in delta modulated inverters, the harmonic contents are such that, at lower frequency of operation, lower order harmonics are insignificant and higher order harmonics are dominant. For high frequency operation, lower order harmonics are dominant but at reduced magnitude. The dominant harmonics at the output of the delta modulated inverter operation determine the current and power into a given passive or dynamic load. For passive loads, the harmonics affect the current, voltage, and power delivered to the load and hence determine the wave shape of the load current as well.

Figs. 5.11 to 5.40 show the inverter output voltage and power spectrum for various operating frequencies for linear delta modulator (LDM), exponential deta modulator (EDM), and sigma delta modulator (SDM) respectively. For resistive loads, the output of the inverter closely resembles the output of the corresponding simulated modulator. However, from the power spectrum of the output voltage of the inverter, it is seen that due to commutation and switching

effects, lower order harmonics also appear in the power spectrum. However, dominant harmonics, at low operating frequencies, are still far away from the fundamental component. Also, the magnitude of lower order harmonics is still insignificant as compared to the fundamental component.

In addition, the magnitude of the fundamental component of linear delta modulator inverter output varies with frequency, up to base frequency and remains at a constant level after base frequency; whereas, in case of exponential delta modulator and sigma delta modulator, the fundamental component remains constant at all frequencies of interest. This result agrees with the theoretical results obtained from power spectrum of DM output as discussed in the previous chapter.



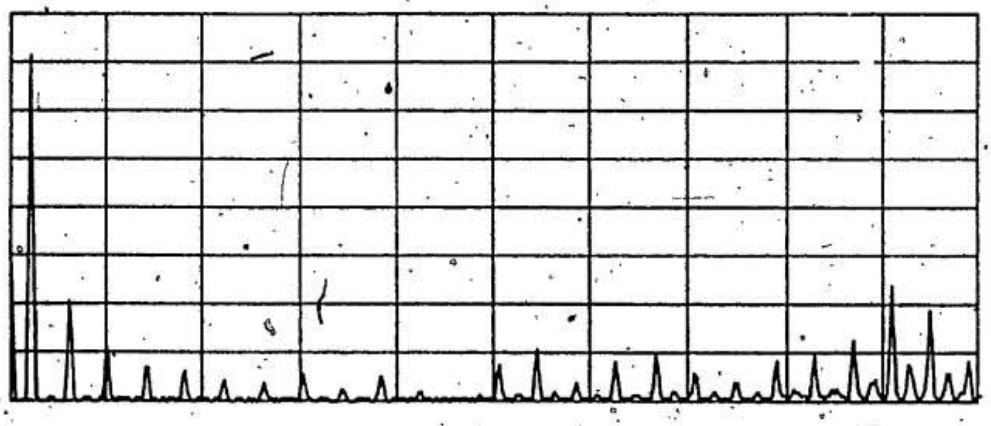
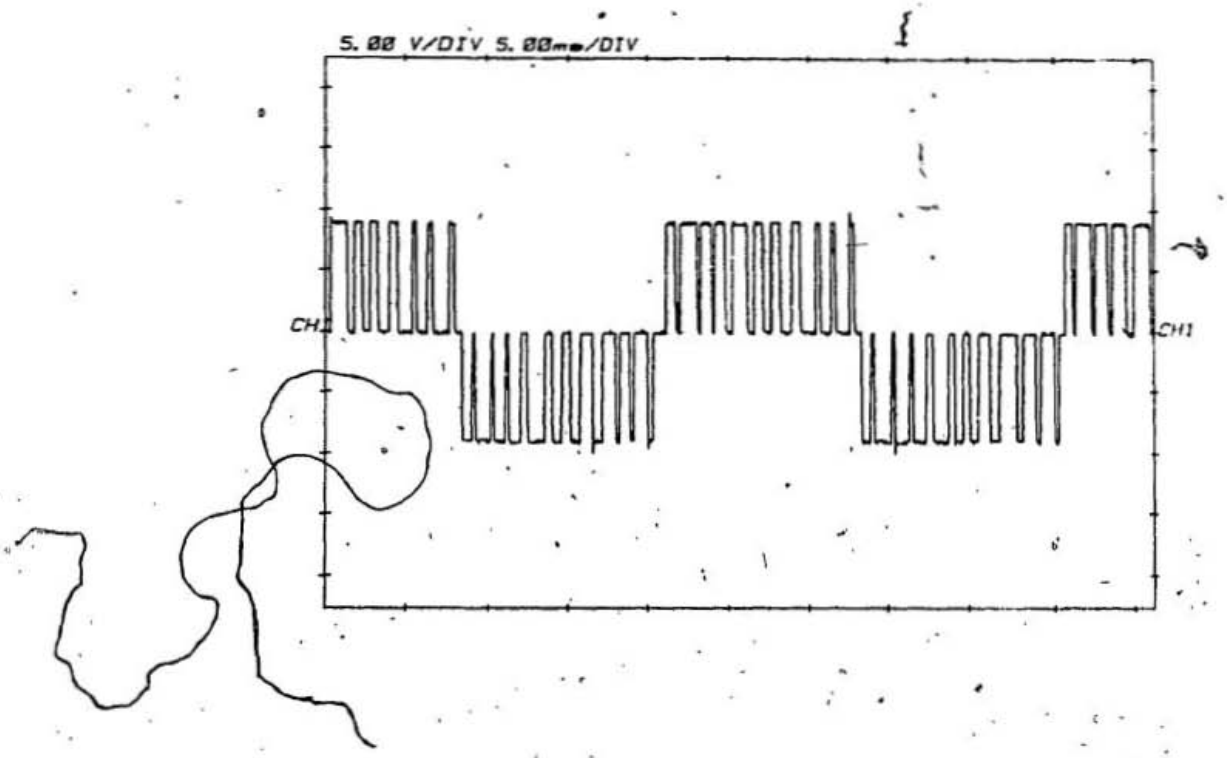


Fig. 5.11 Inverter Output Voltage and Power Spectrum of LDM for f = 20 Hz



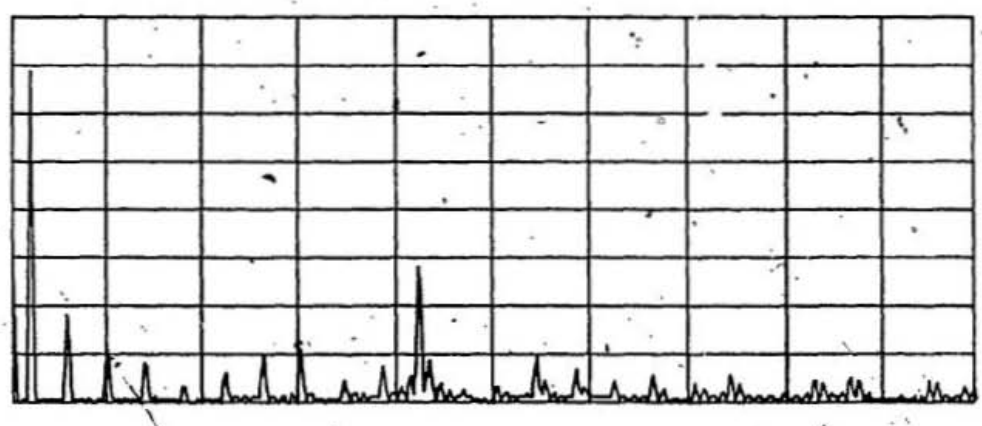
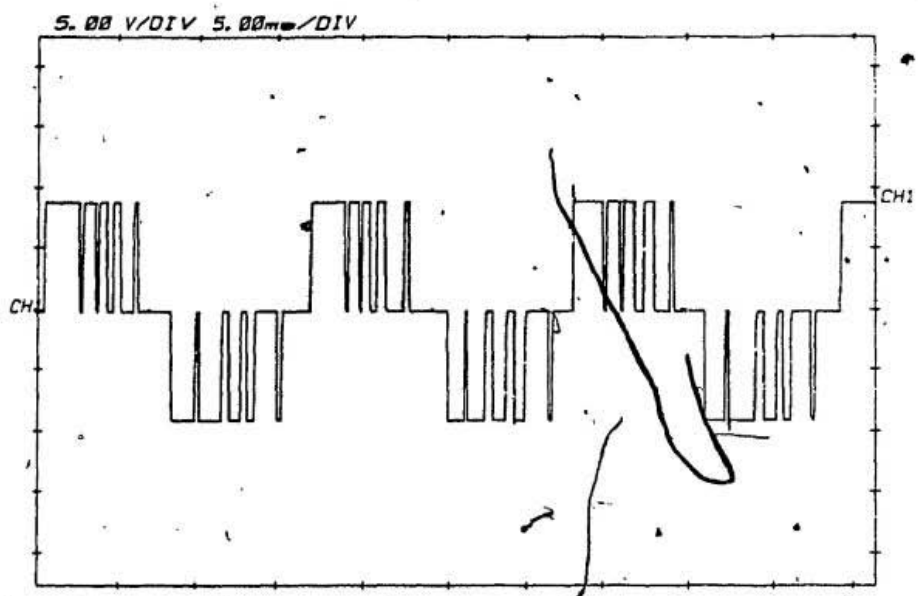


Fig. 5.12 Inverter Output Voltage and Power Spectrum of LDM for f = 40 Hz



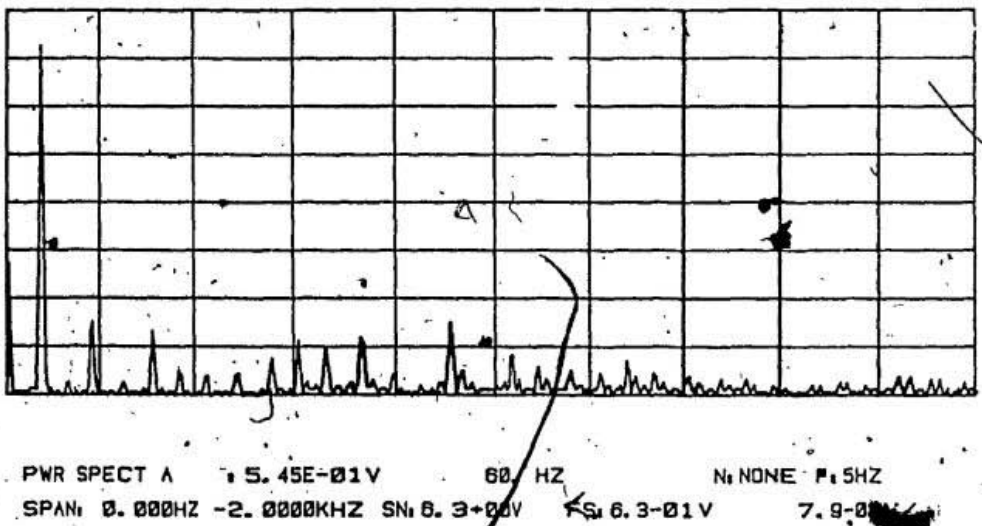
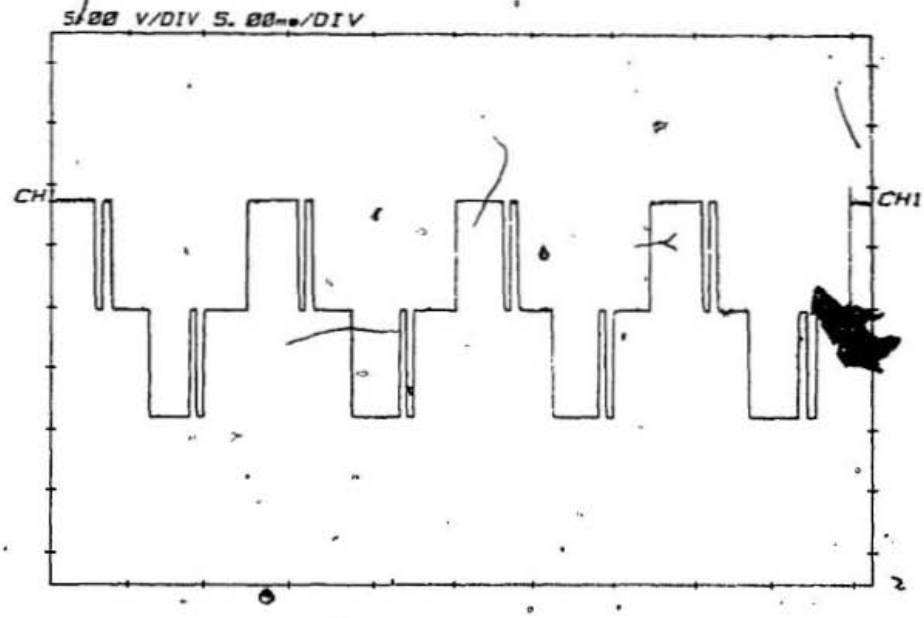
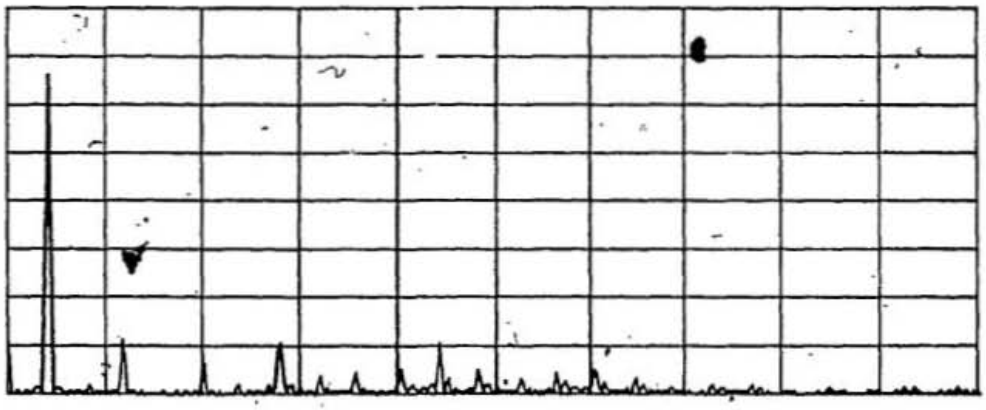


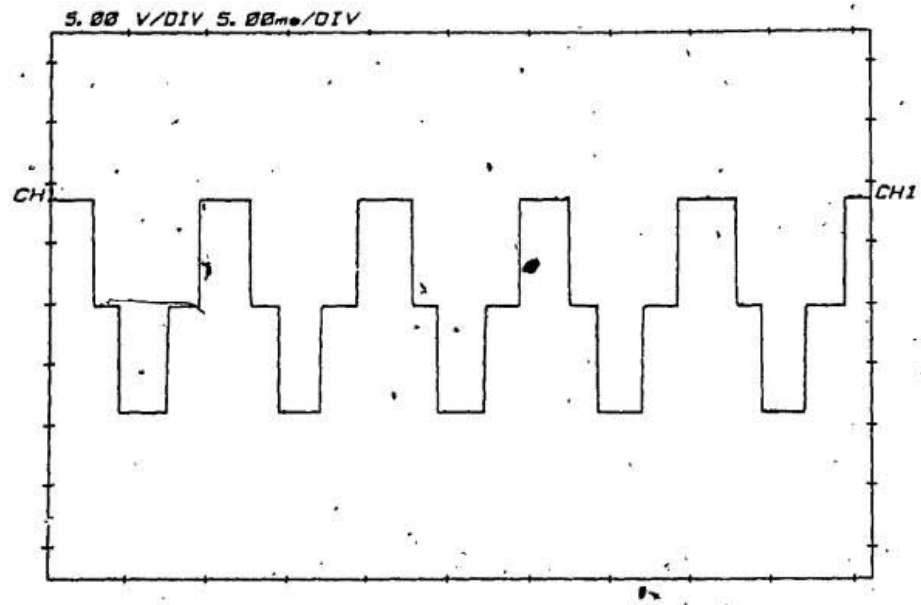
Fig. 5.13 Inverter Output Voltage and Power Spectrum of LDM for f = 60 Hz

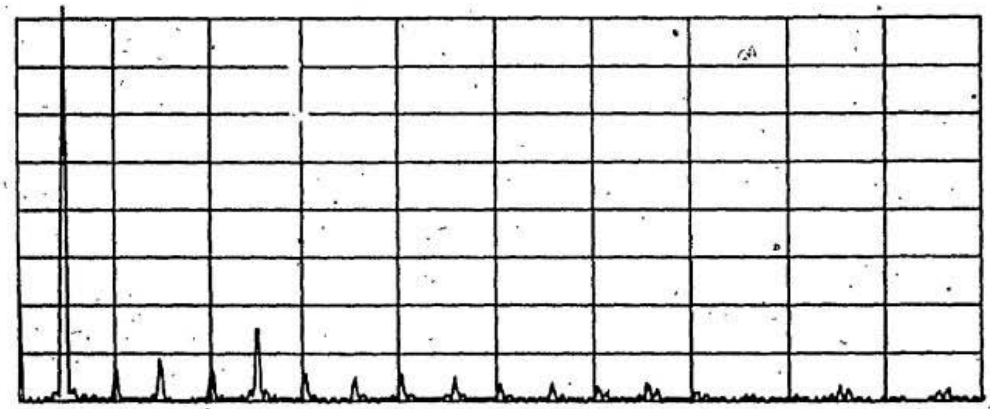




PWR SPECT A : 8.27E-01V 80. HZ N: NONE P: 5HZ
SPAN: 0.000HZ -2.0000KHZ SN: 4.0+00V FS: 8.0-01V 9.9-02V/

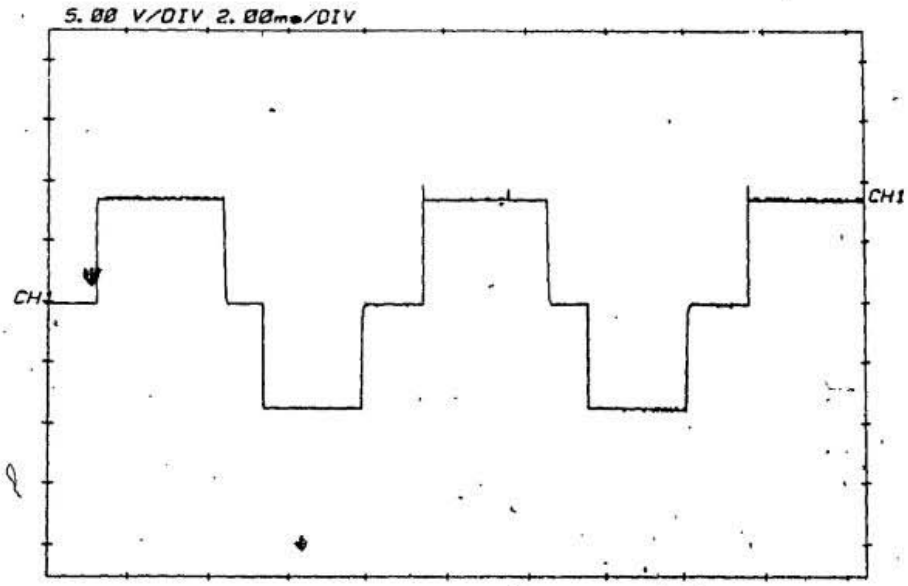
Fig. 5.14 Inverter Output Voltage and Power Spectrum of LDM for $f = 80$ Hz





PWR SPECT A : 8.95E-01V 100. HZ N: NONE F: 5HZ
SPAN: 0.000HZ -2.0000KHZ SN: 6.3+00V FS: 6.3-01V 7.9-02V/

Fig. 5.15 Inverter Output Voltage and Power Spectrum of LDM for f = 100 Hz



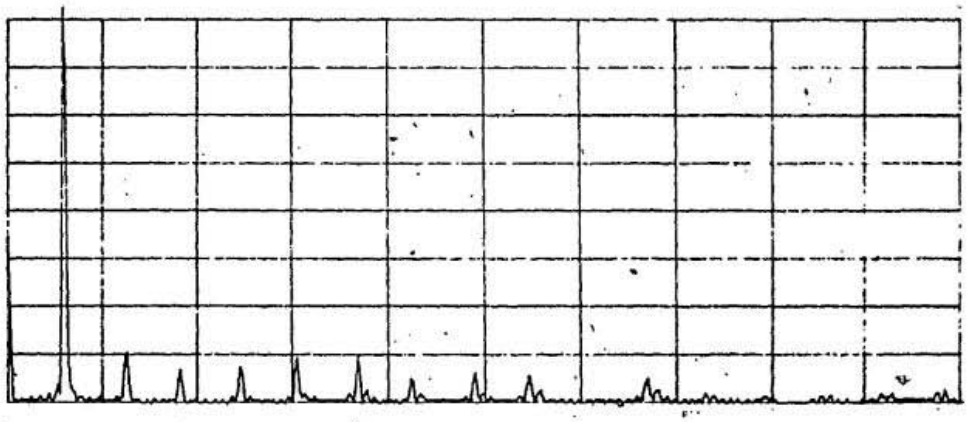
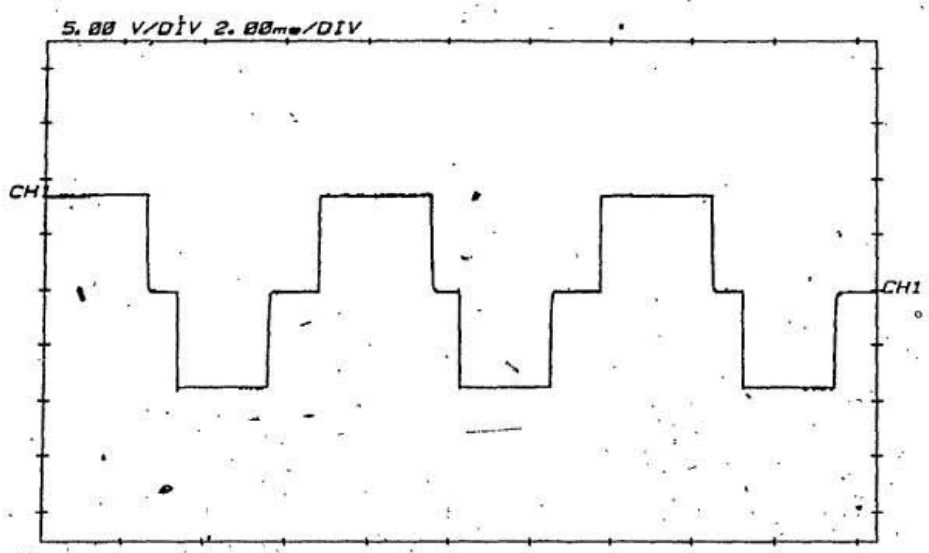


Fig. 5.16 Inverter Output Voltage and Power Spectrum of LDM for f = 120 Hz



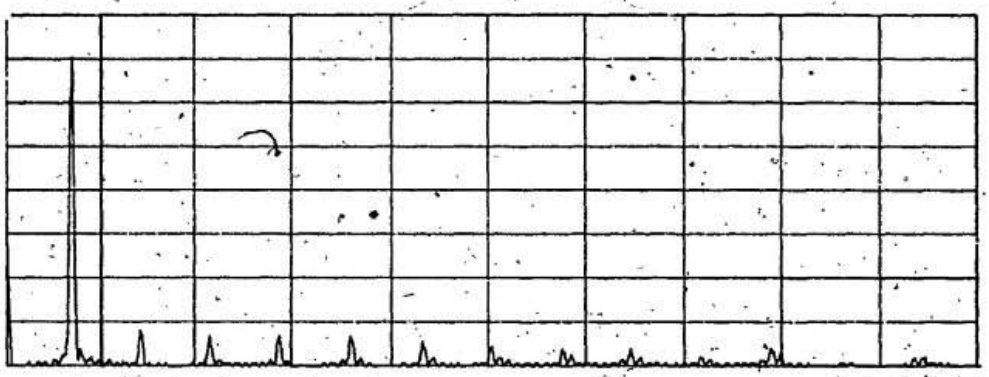
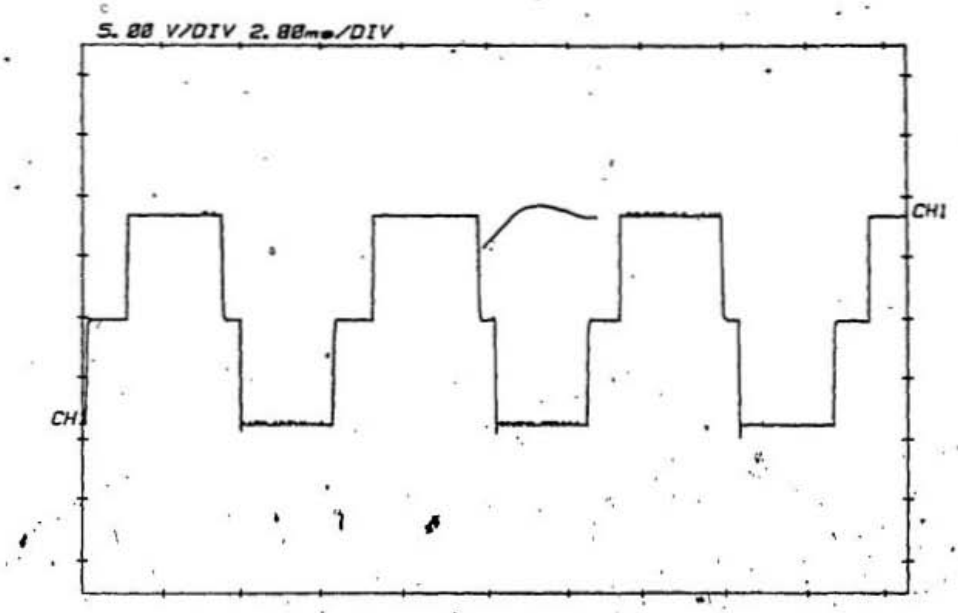
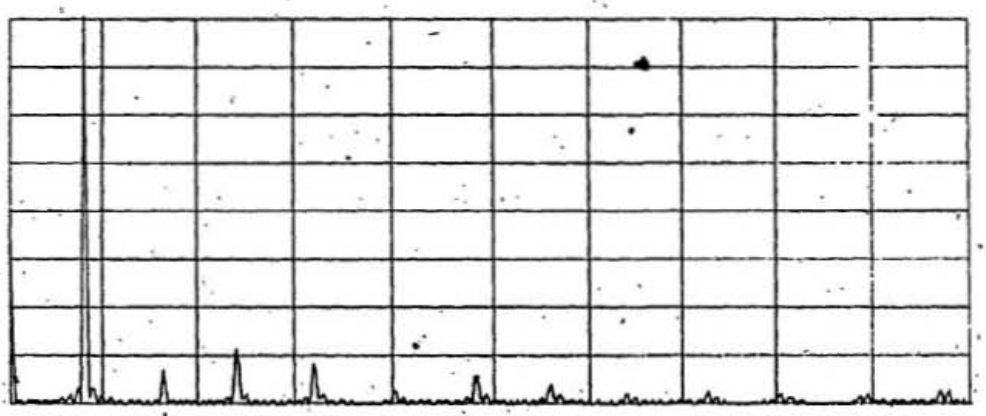


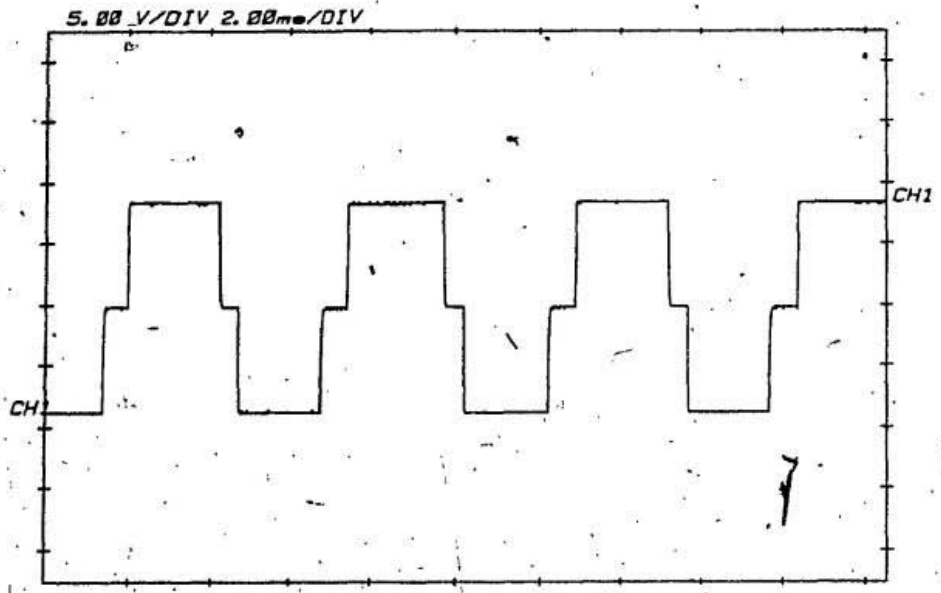
Fig. 5.17 Inverter Output Voltage and Power Spectrum of LDM for f = 140 Hz





PWR SPECT A : 7.71E-01V 160. HZ N: NONE F: 5HZ
SPAN: 0.000HZ -2.0000KHZ SN: 7.9+00V FS: 7.9-01V 9.9-02V/

Fig. 5.18 Inverter Output Voltage and Power Spectrum of LDM for f = 160 Hz



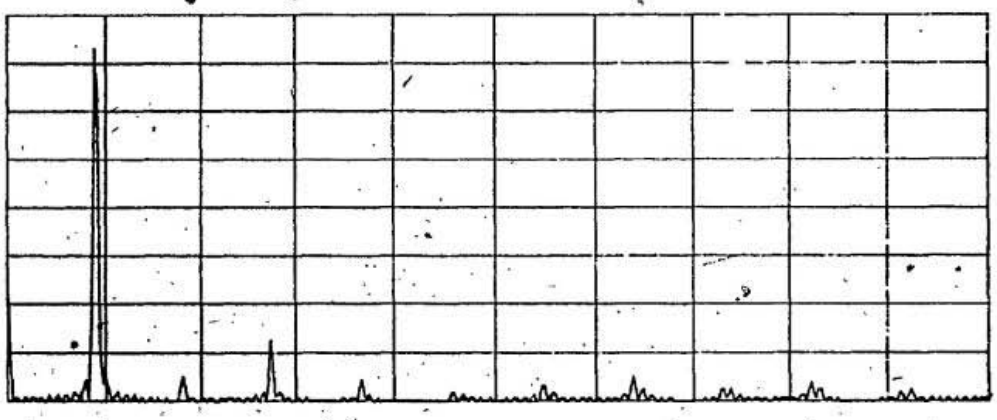
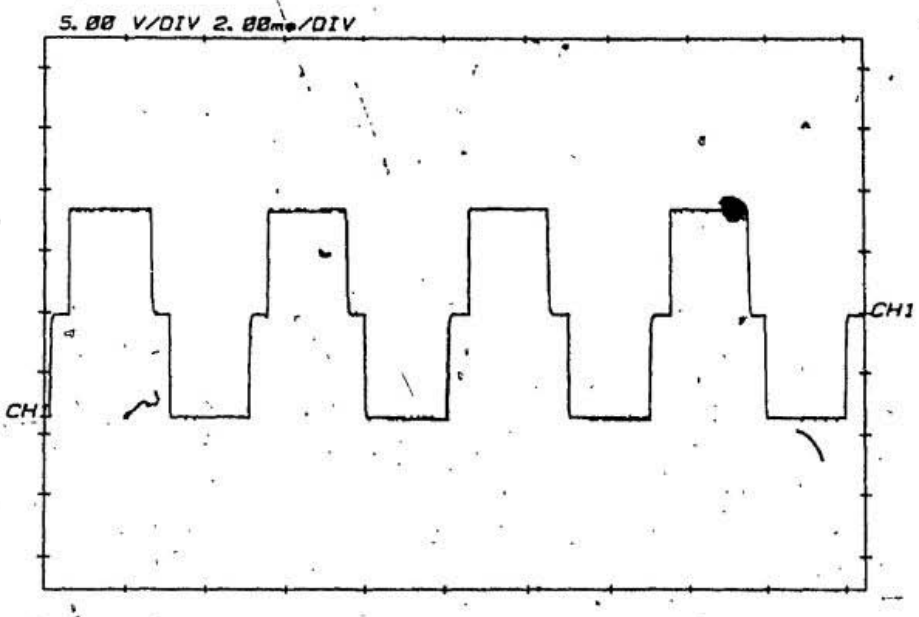


Fig. 5.19 Inverter Output Voltage and Power Spectrum of LDM for f = 180 Hz



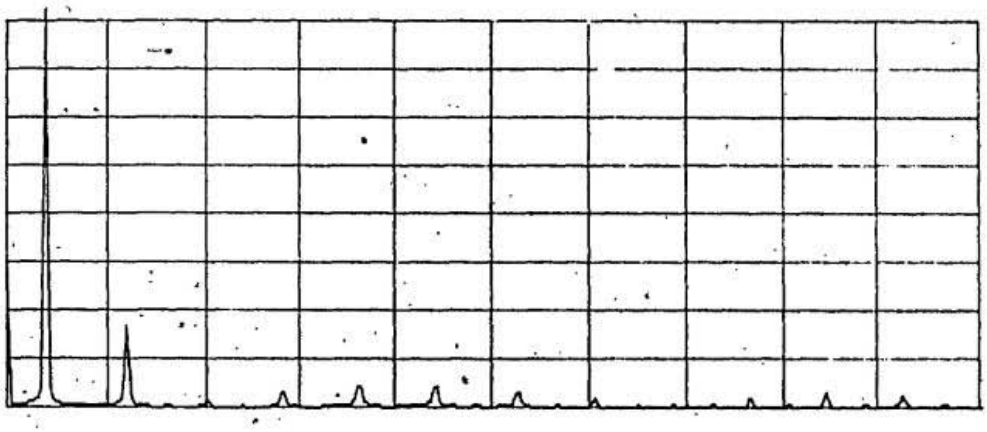
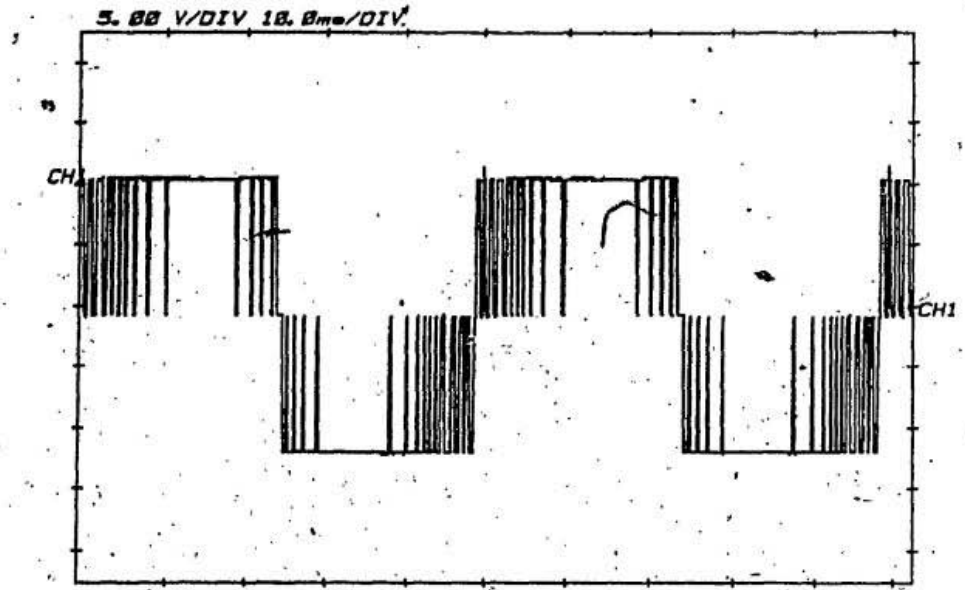


Fig. 5.20 Inverter Output Voltage and Power Spectrum of LDM for f = 200 Hz



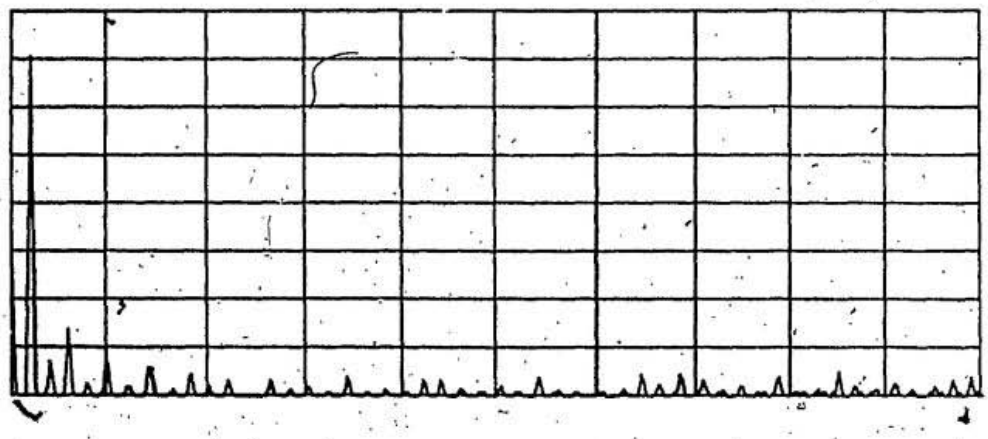
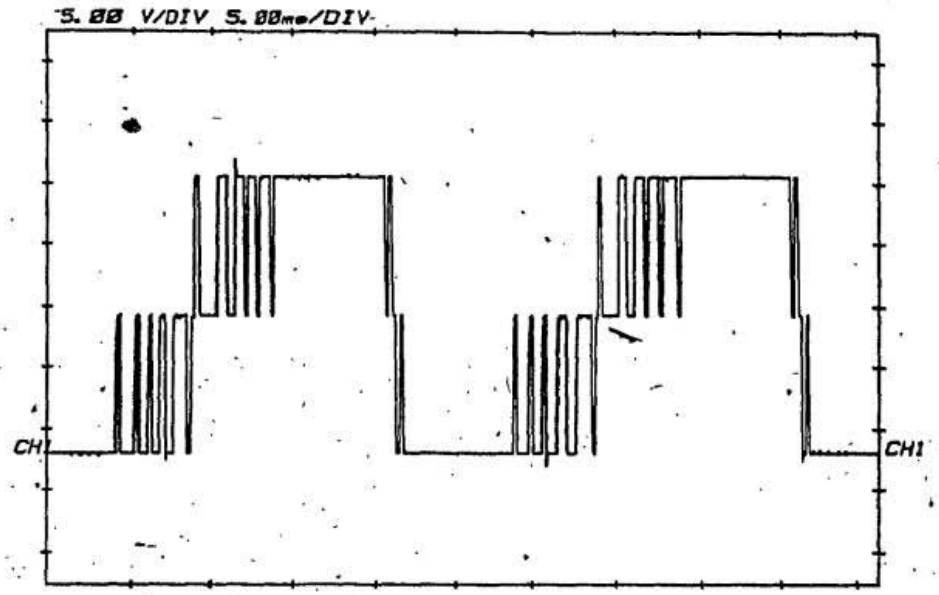


Fig. 5.21 Inverter Output Voltage and Power Spectrum of EDM for f = 20 Hz



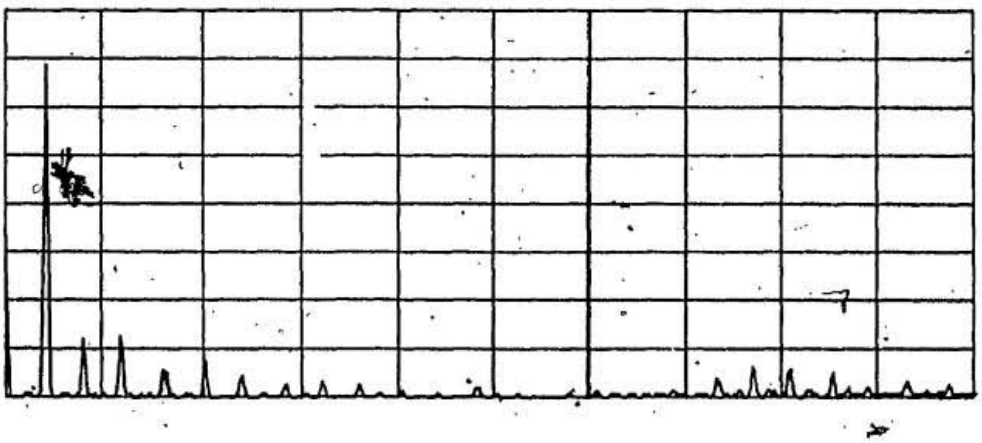
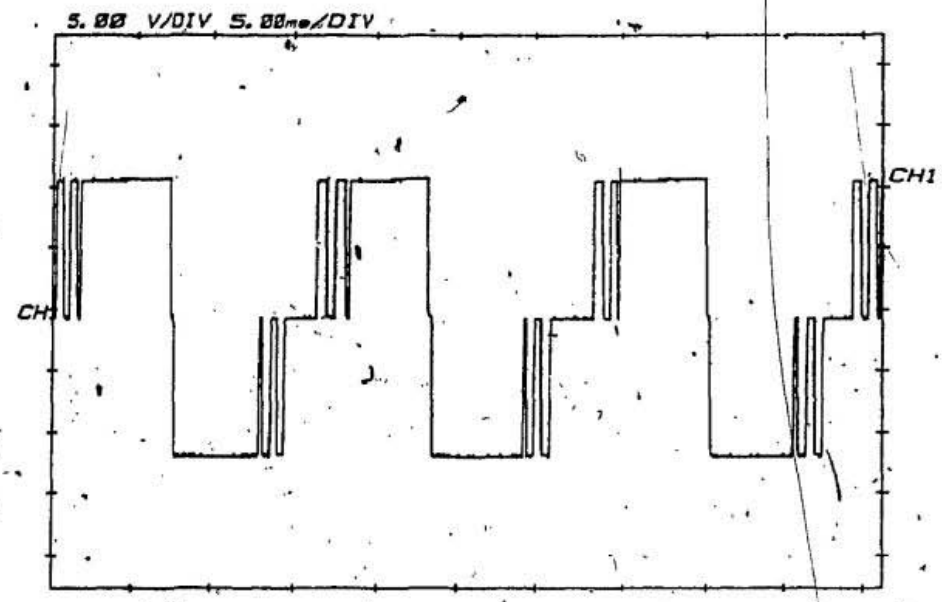


Fig. 5.22 Inverter Output Voltage and Power Spectrum of EDM for f = 40 Hz



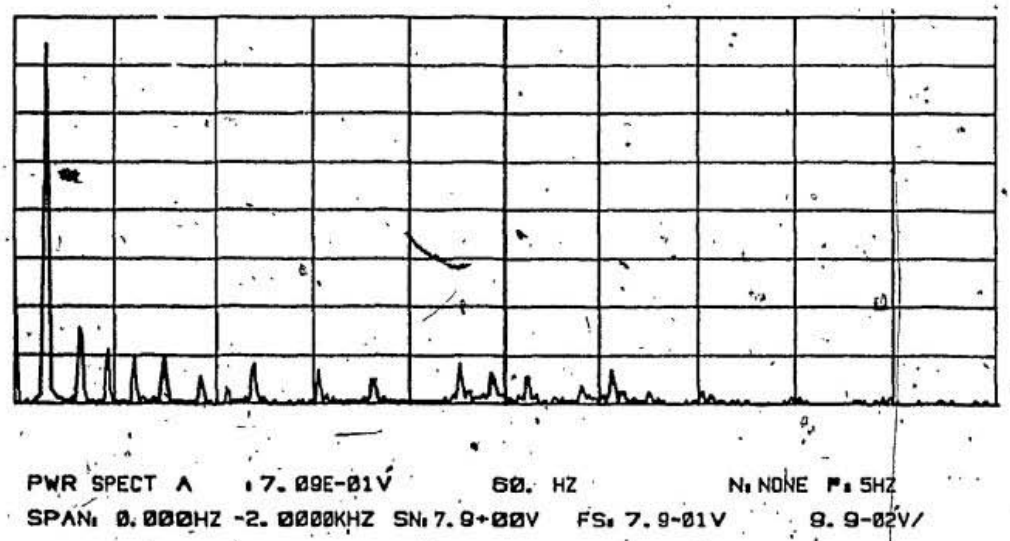
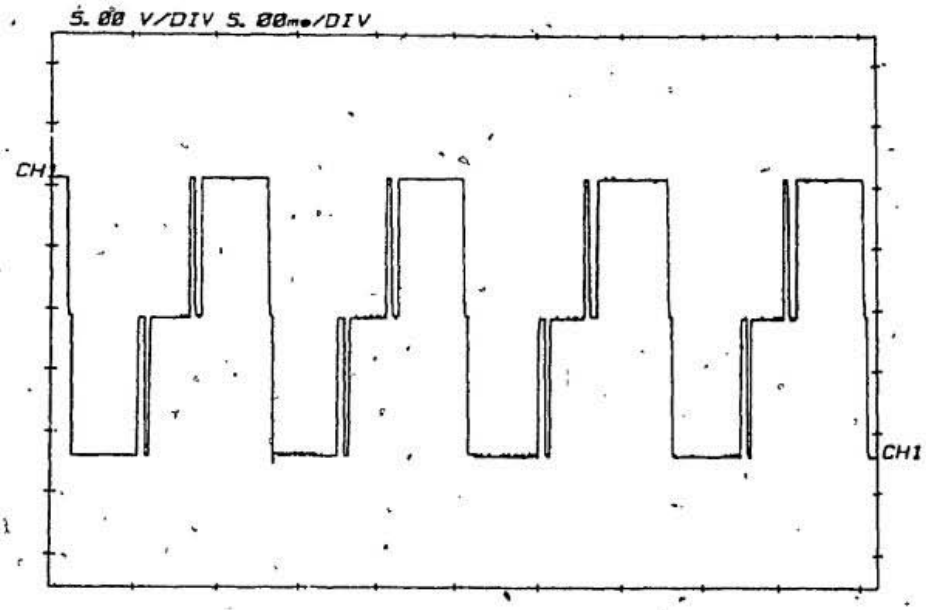
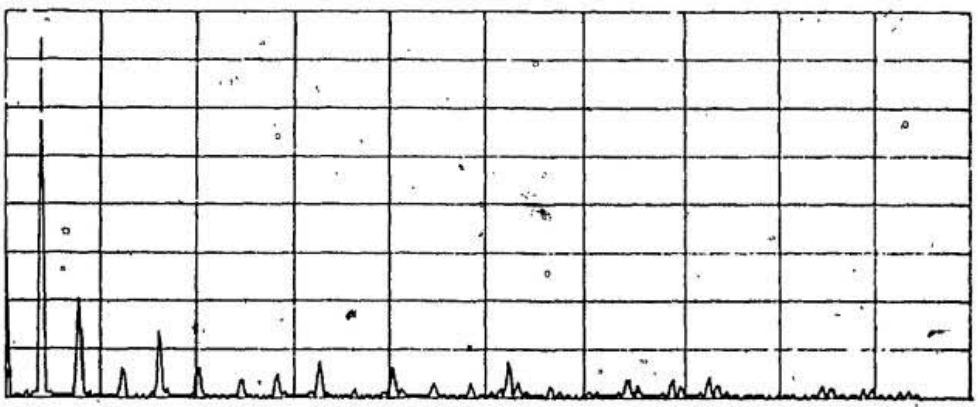


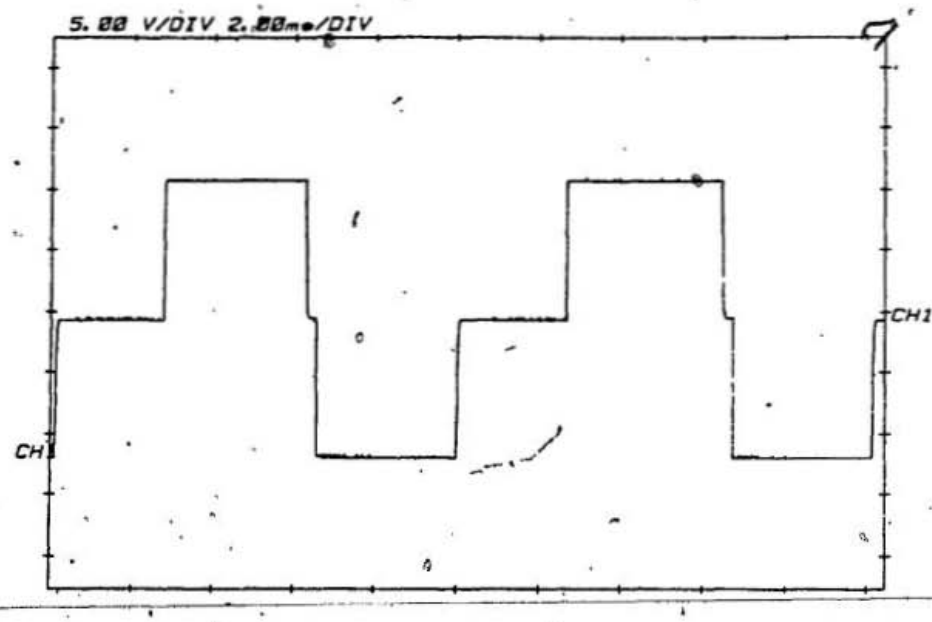
Fig. 5.23 Inverter Output Voltage and Power Spectrum of EDM for f = 60 Hz





PWR SPECT A : 7.07E-01V 80. HZ N: NONE F: 5HZ
SPAN: 0.000HZ -2.0000KHZ SN: 7.9+00V FS: 7.9-01V 9.9-02V/

Fig. 5.24 Inverter Output Voltage and Power Spectrum of EDM for f = 80 Hz



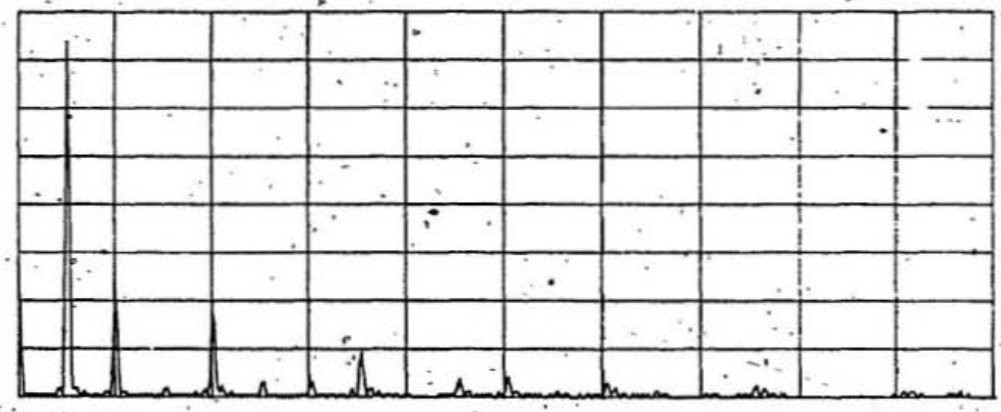
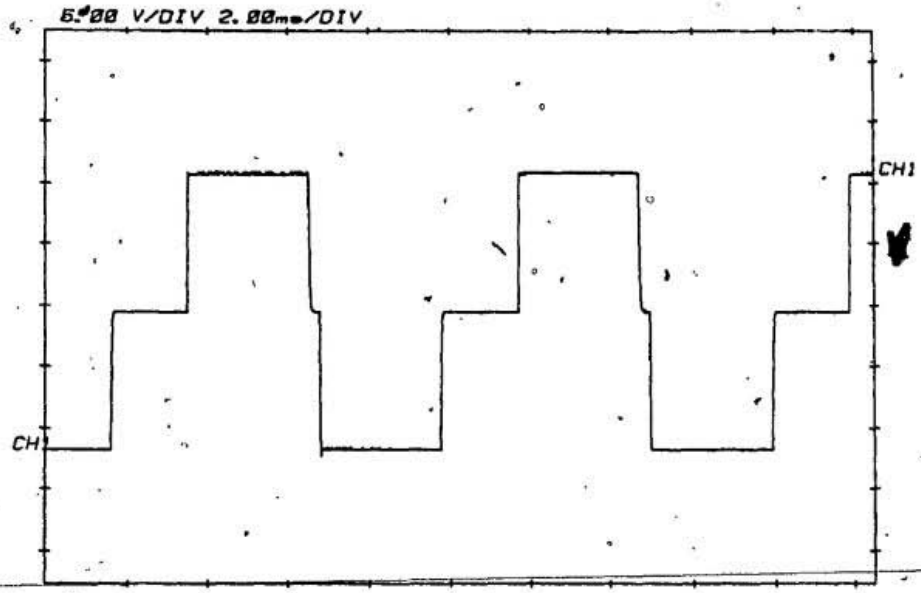


Fig. 5.25 Inverter Output Voltage and Power Spectrum of EDM for f = 100 Hz



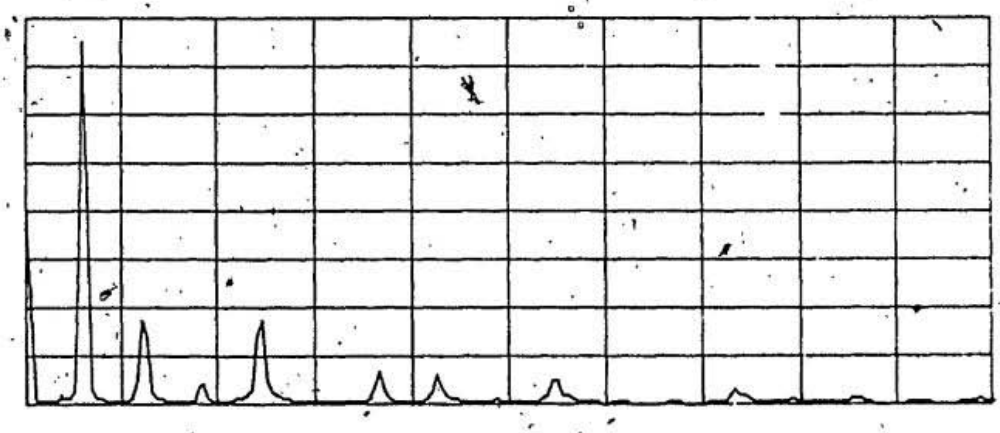
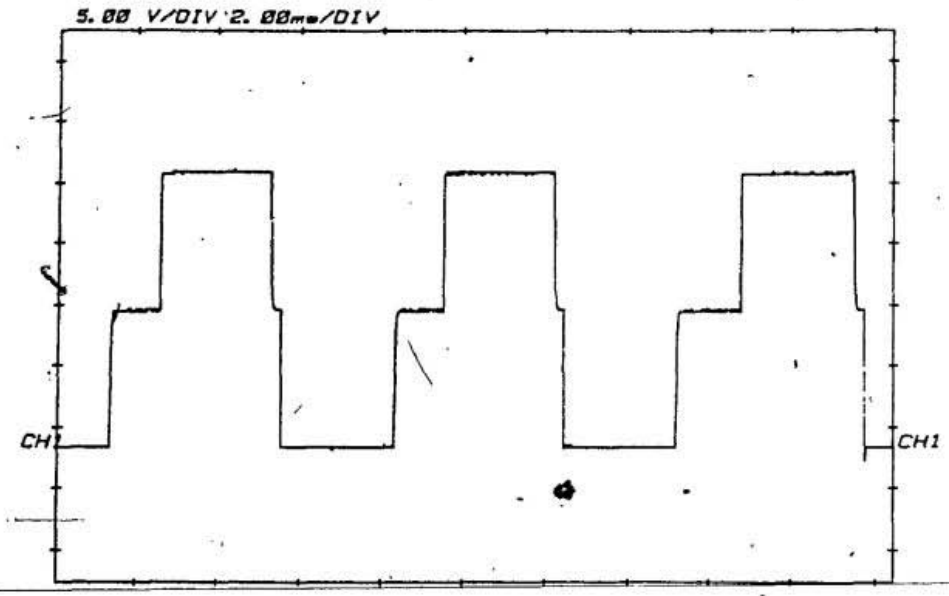


Fig. 5.26 Inverter Output Voltage and Power Spectrum of EDM for f = 120 Hz



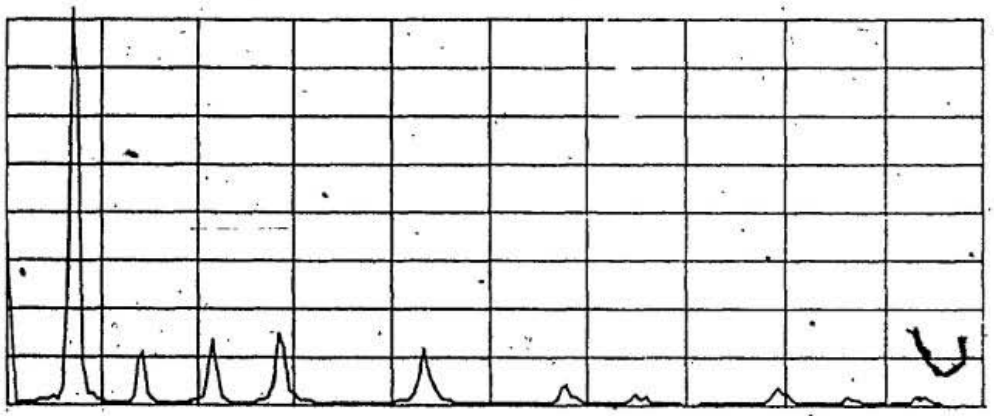
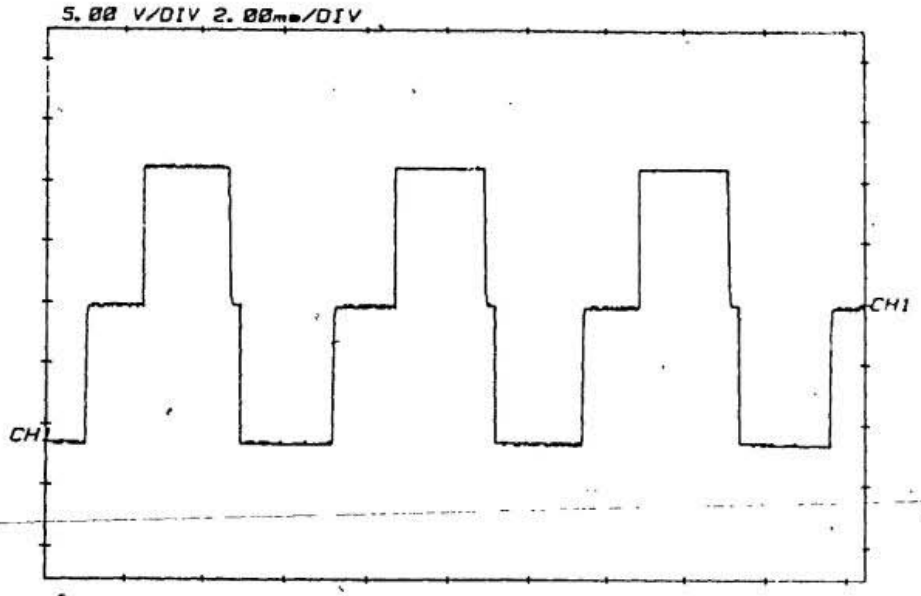


Fig. 5.27 Inverter Output Voltage and Power Spectrum of EDM for f = 140 Hz



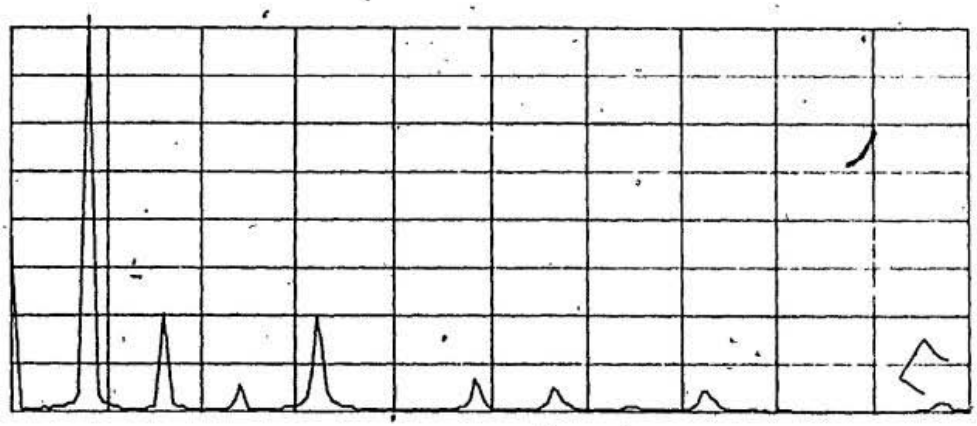
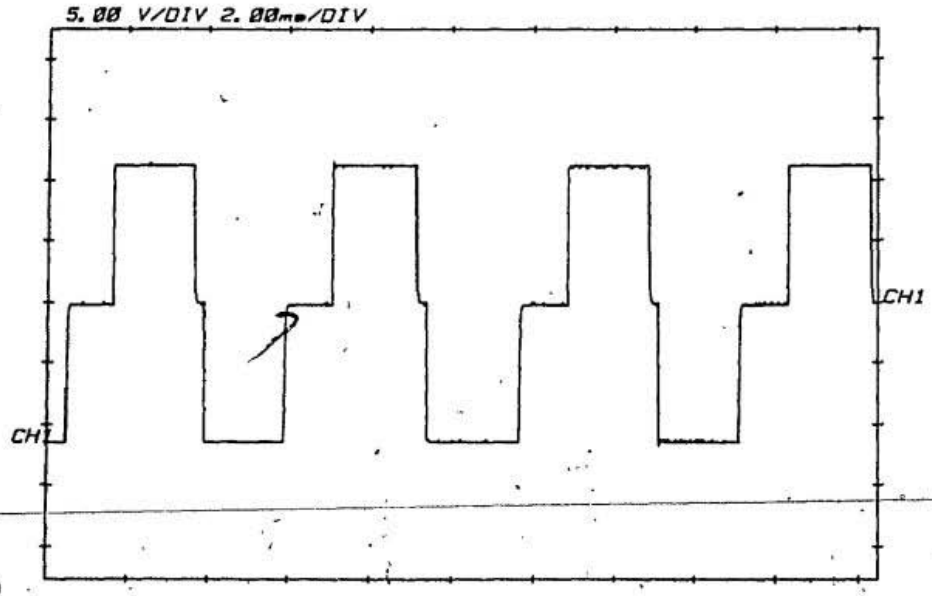


Fig. 5.28 Inverter Output Voltage and Power Spectrum of EDM for f = 160 Hz



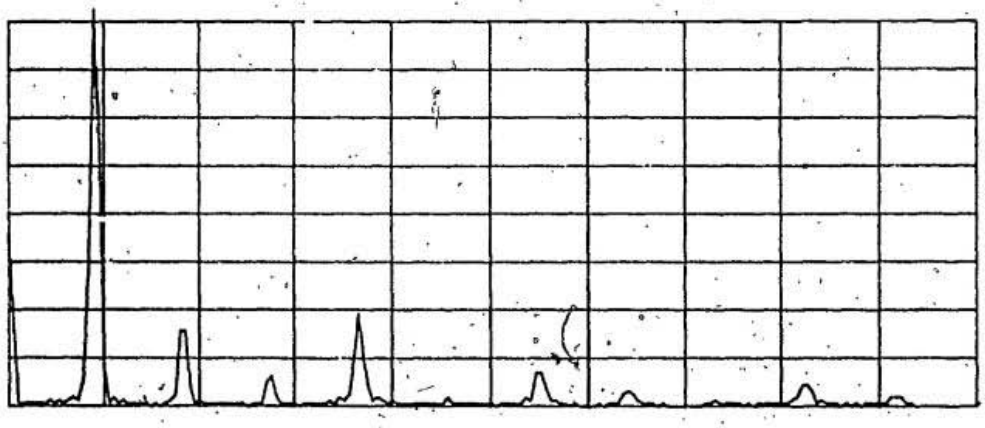
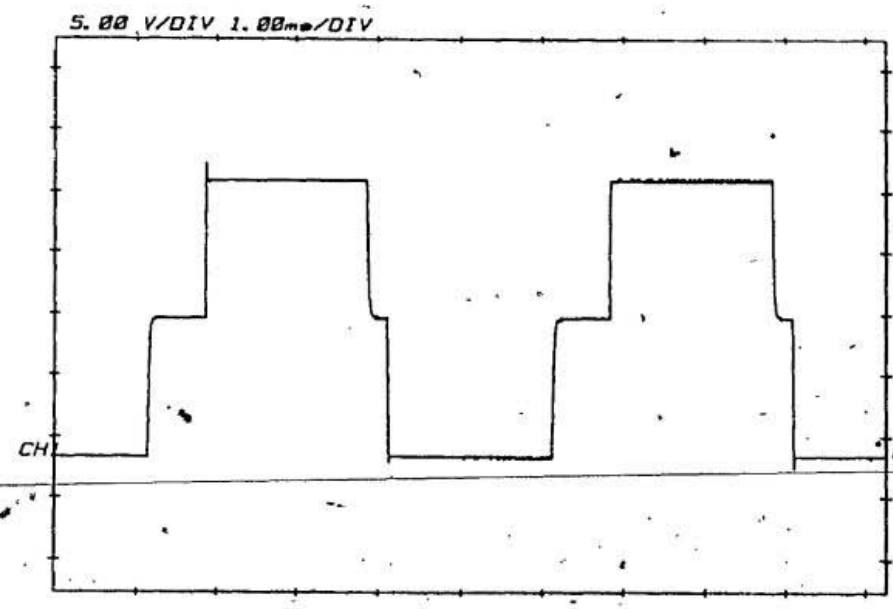


Fig. 5.29 Inverter Output Voltage and Power Spectrum of EDM for f = 180 Hz



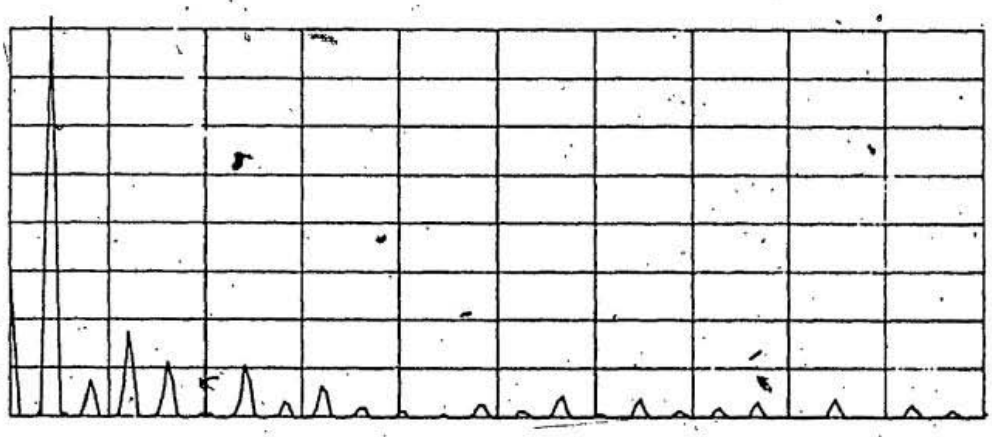
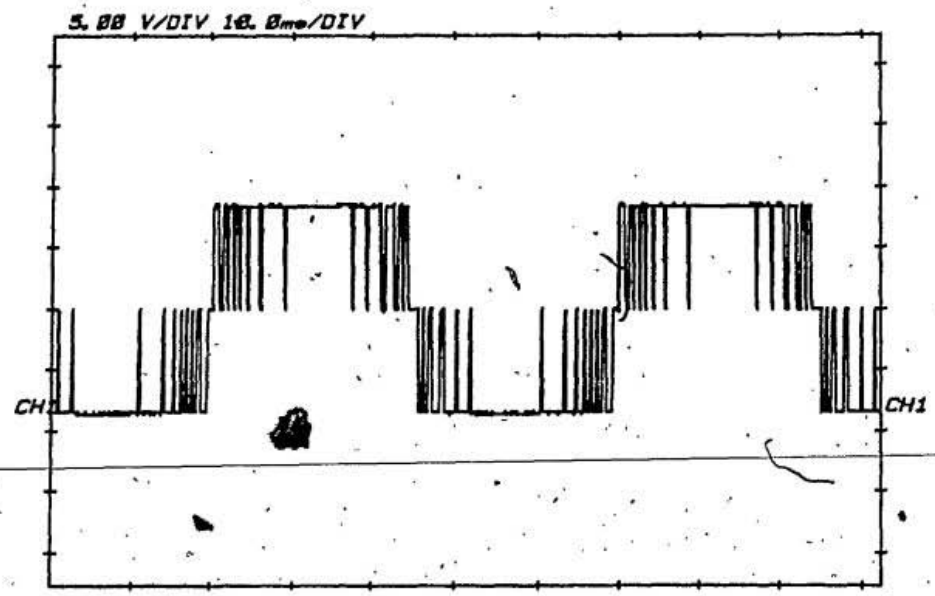


Fig. 5.30 Inverter Output Voltage and Power Spectrum of EDM for f = 200 Hz



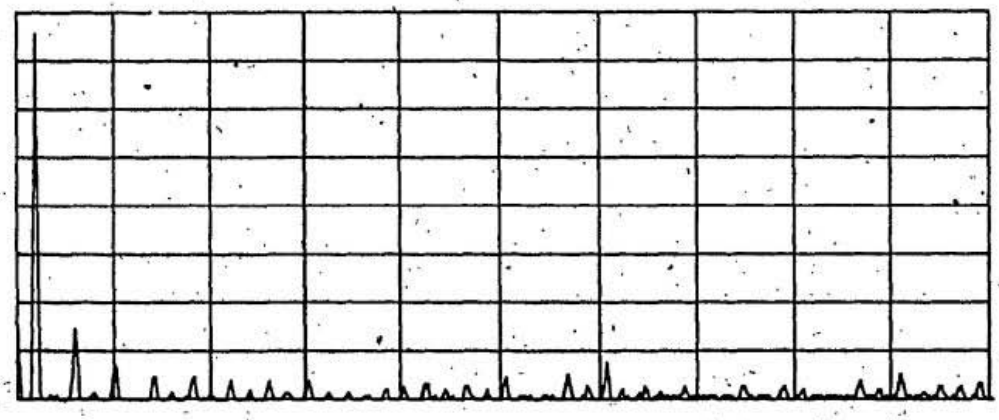
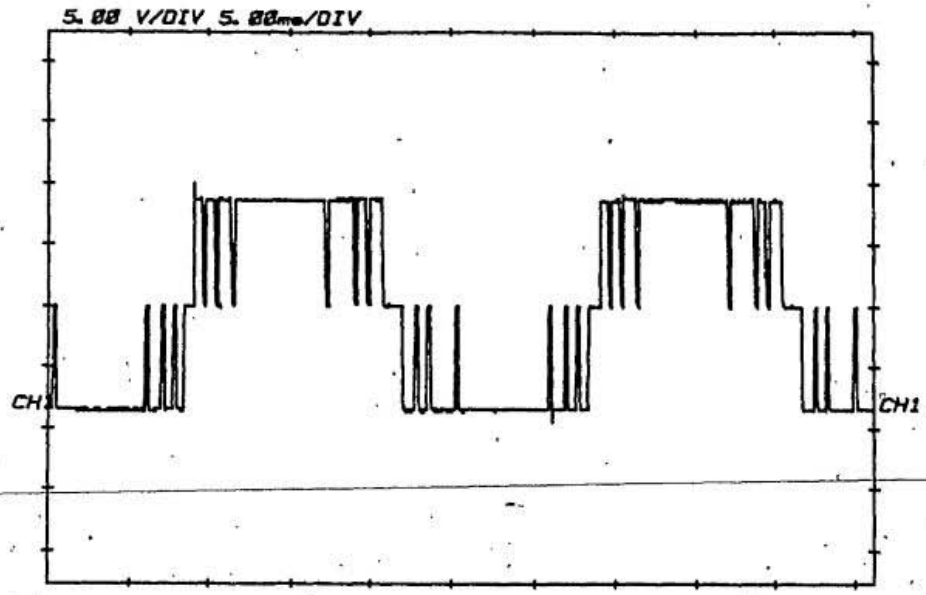


Fig. 5.31 Inverter Output Voltage and Power Spectrum of SDM for f = 20 Hz



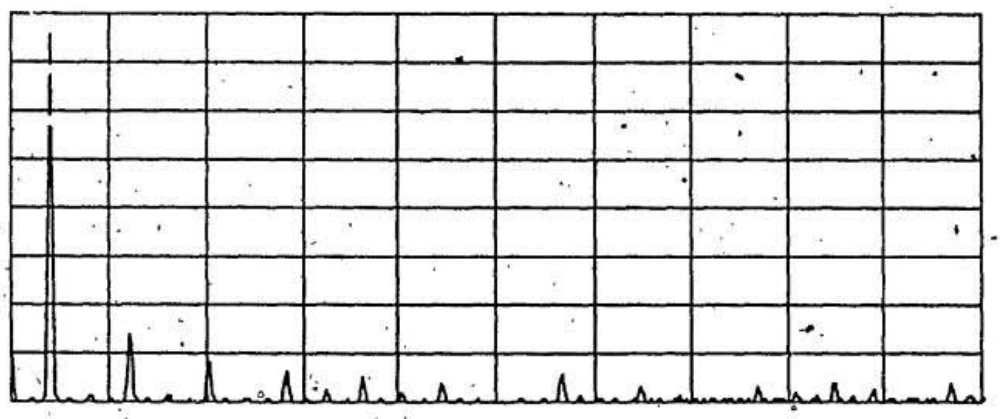
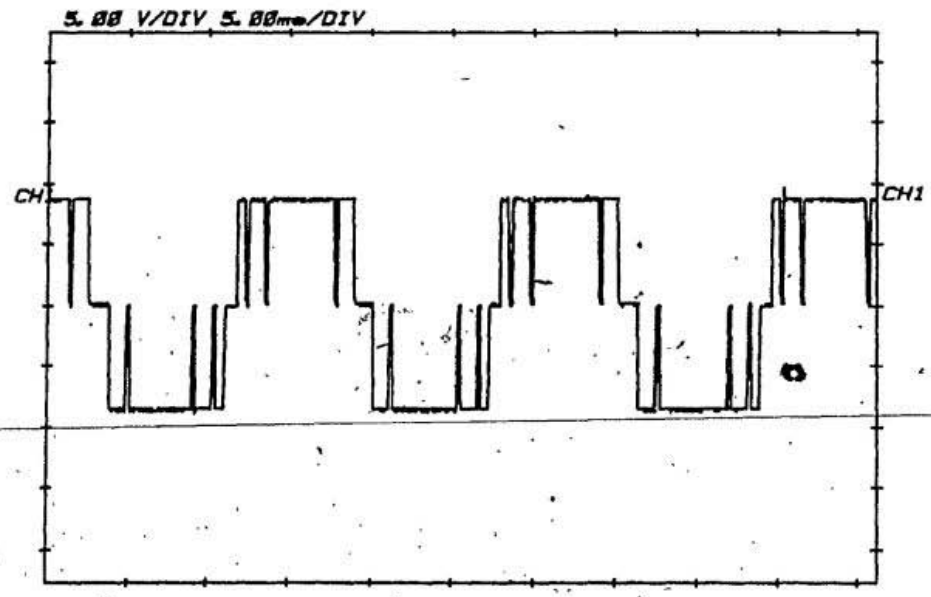


Fig. 5.32 Inverter Output Voltage and Power Spectrum of SDM for f = 40 Hz



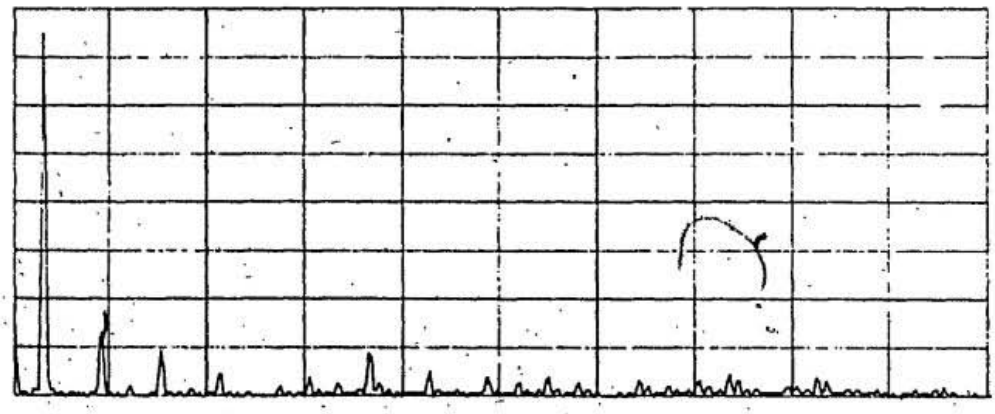
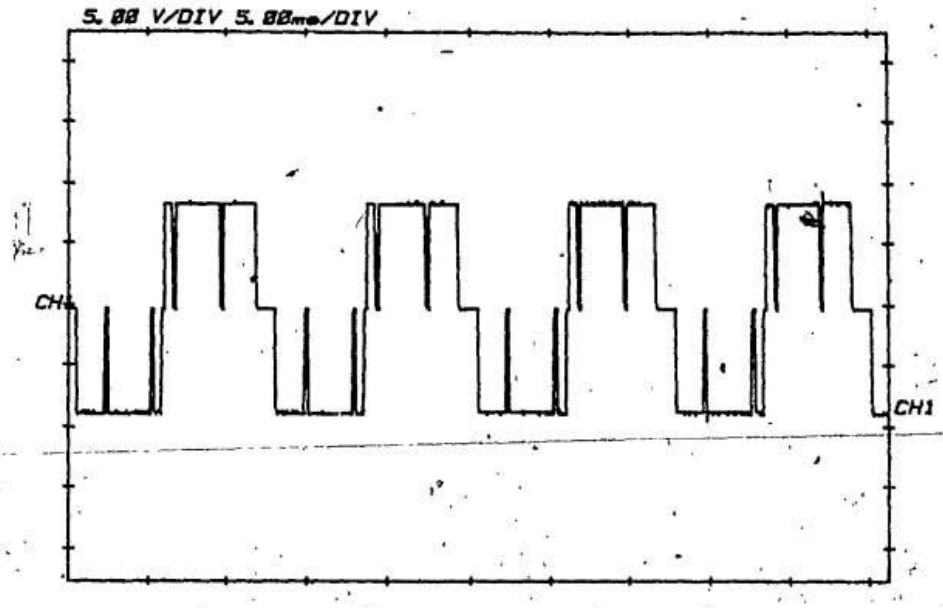


Fig. 5.33 Inverter Output Voltage and Power Spectrum of SDM for f = 60 Hz



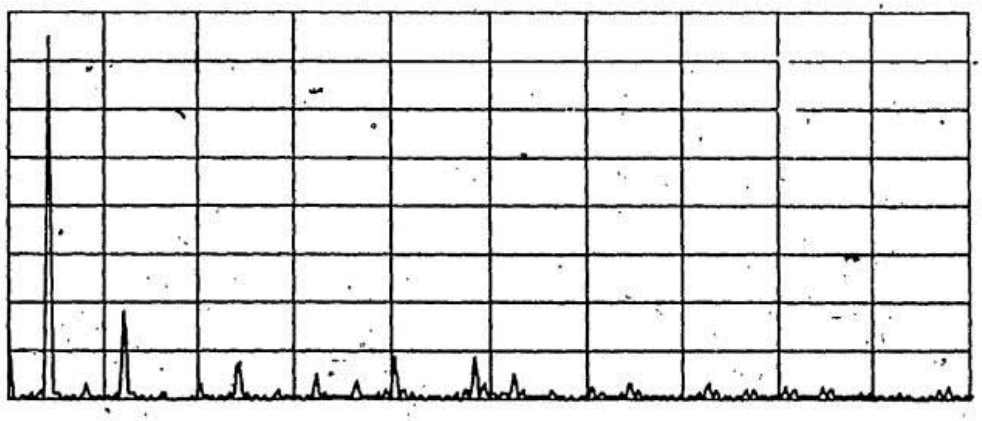
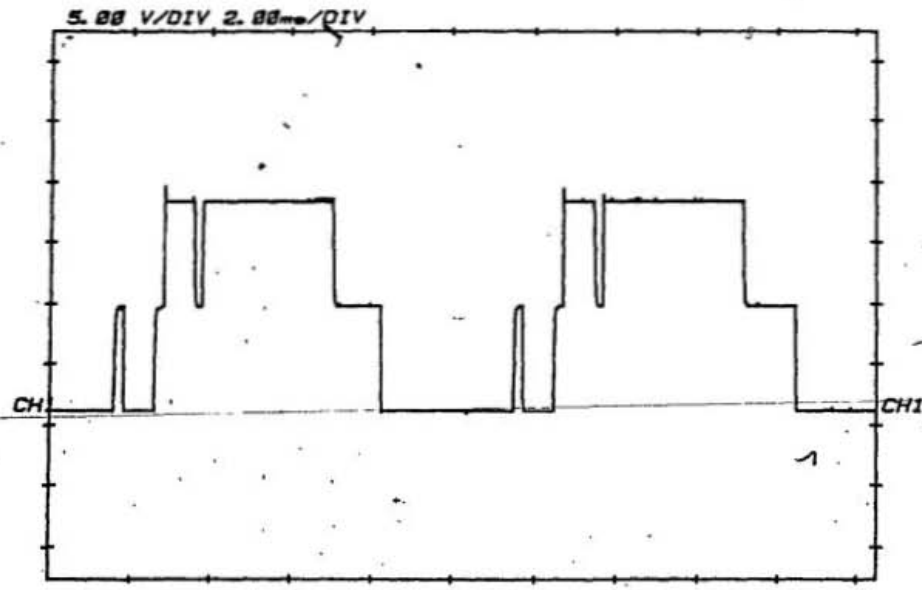


Fig. 5.34 Inverter Output Voltage and Power Spectrum of SDM for f = 80 Hz



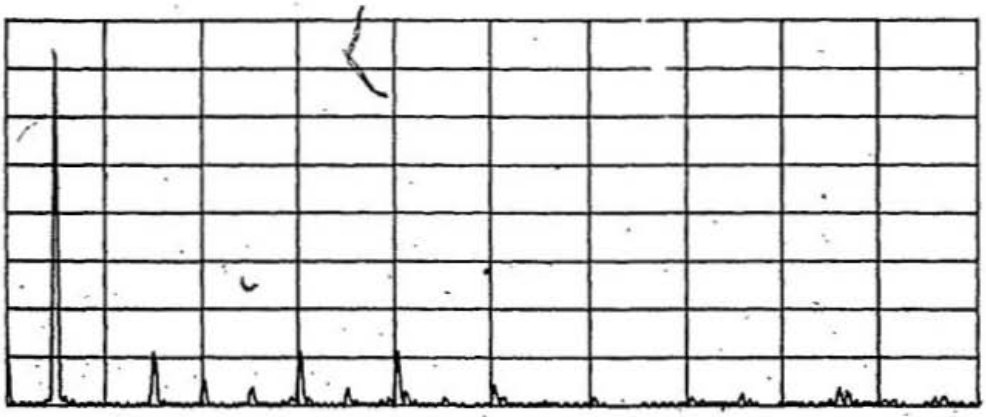
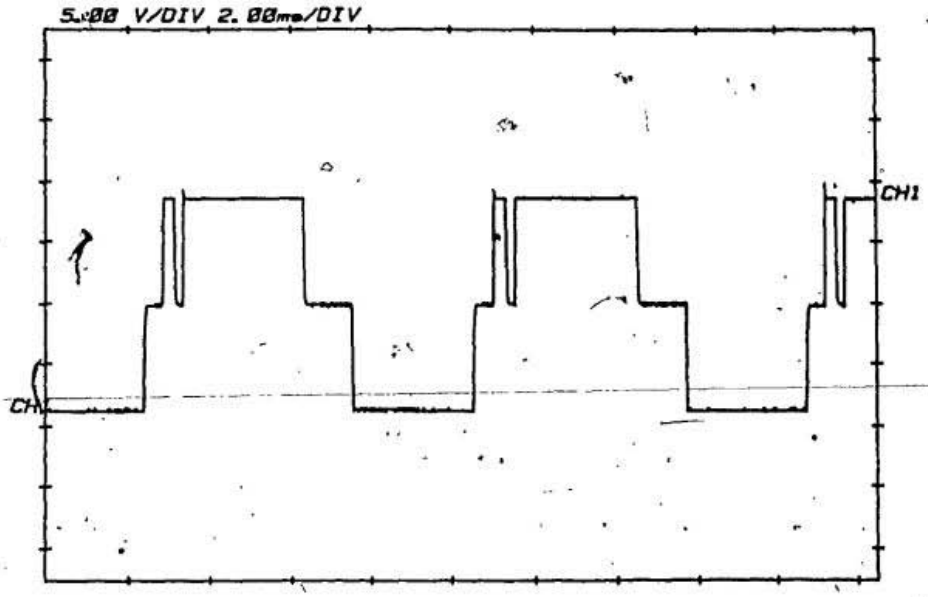


Fig. 5.35 Inverter Output Voltage and Power Spectrum of SDM for f = 100 Hz



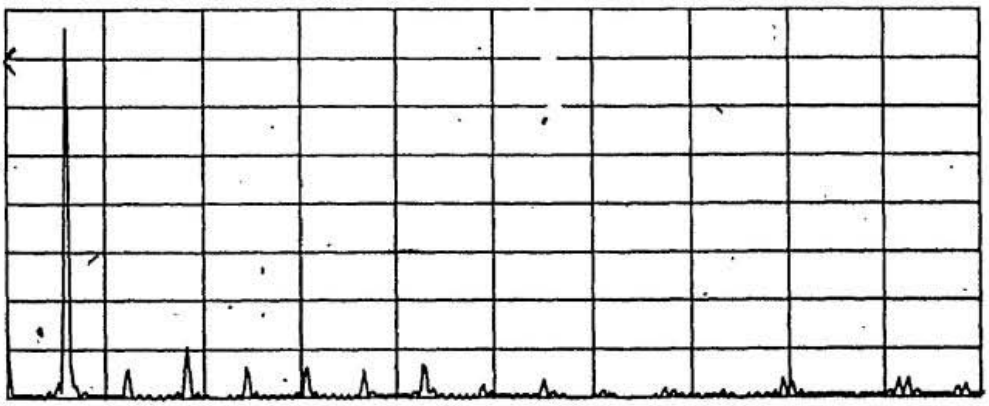
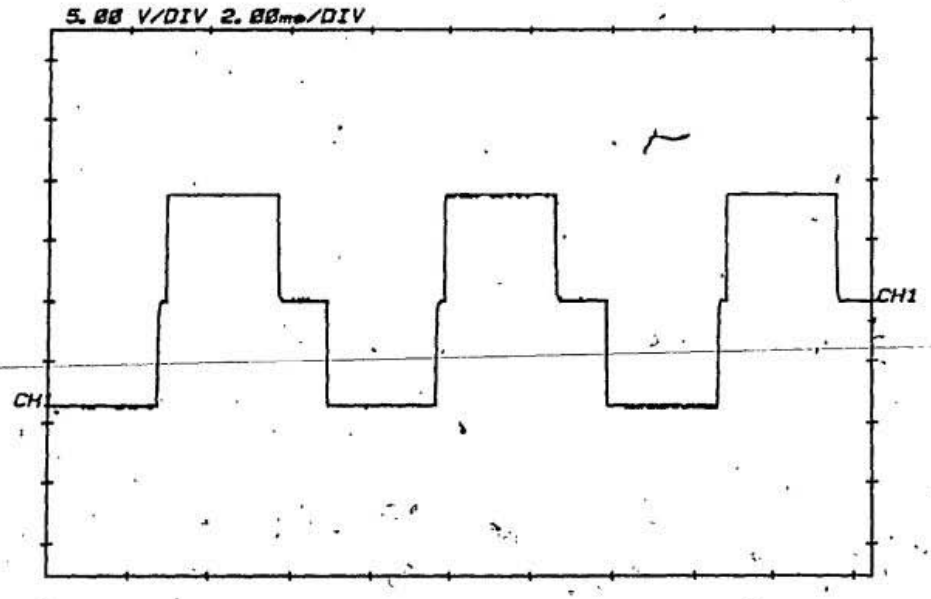
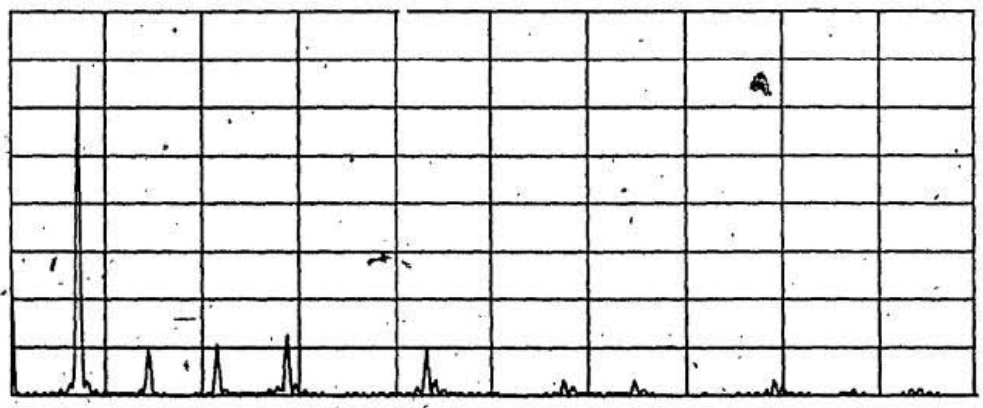


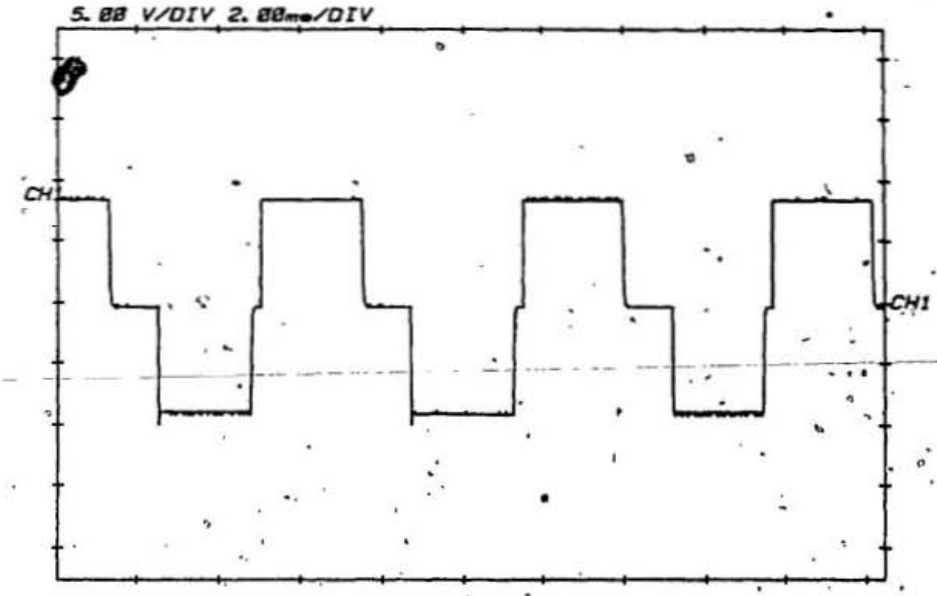
Fig. 5.36 Inverter Output Voltage and Power Spectrum of SDM for f = 120 Hz.





PWR SPECT-A , 7.32E-01V 145. HZ N: NONE F: 5HZ
SPAN: 0.000HZ -2.0000KHZ SN: 8.9+00V FS: 8.9-01V 1.1-01V/

Fig. 5.37 Inverter Output Voltage and Power Spectrum of SDM for f = 145 Hz



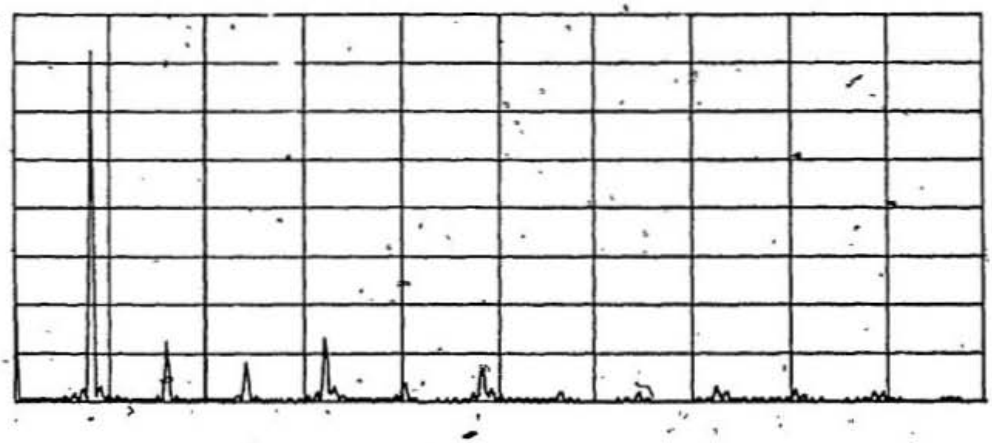
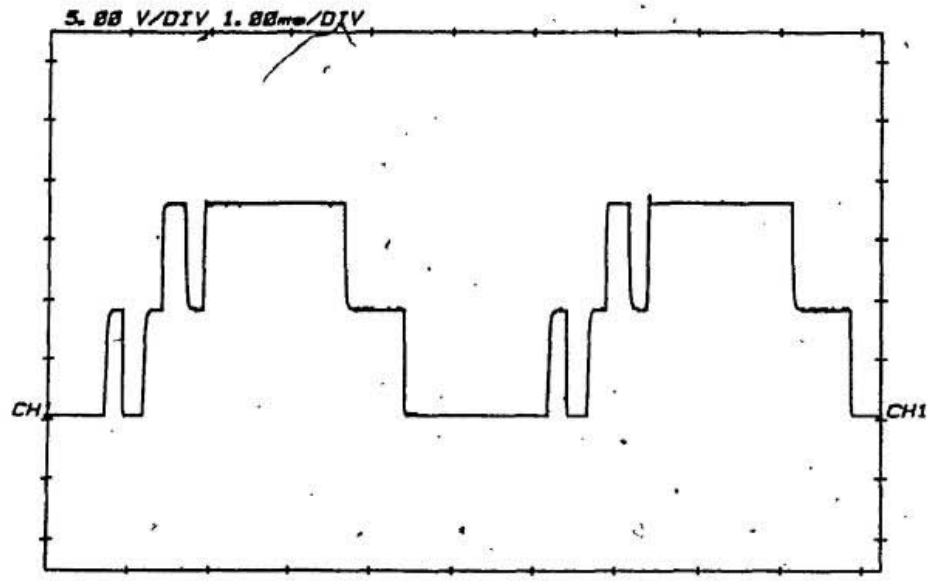


Fig. 5.38 Inverter Output Voltage and Power Spectrum of SDM for f = 160 Hz



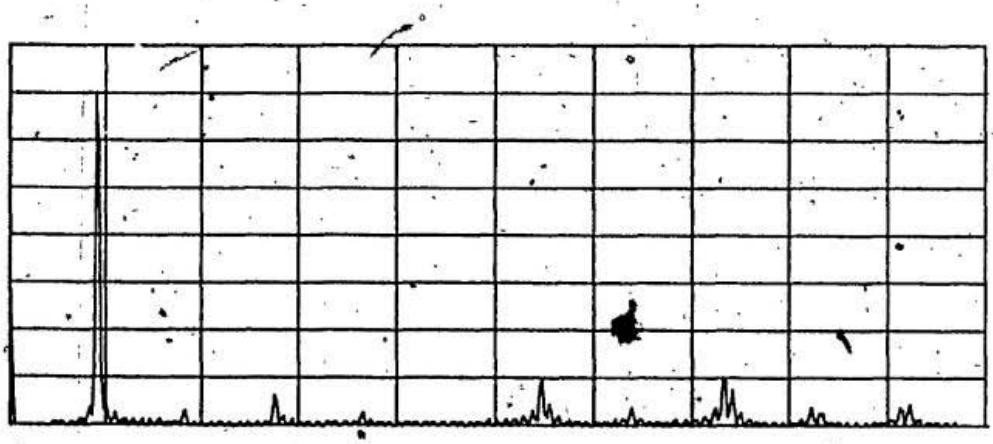
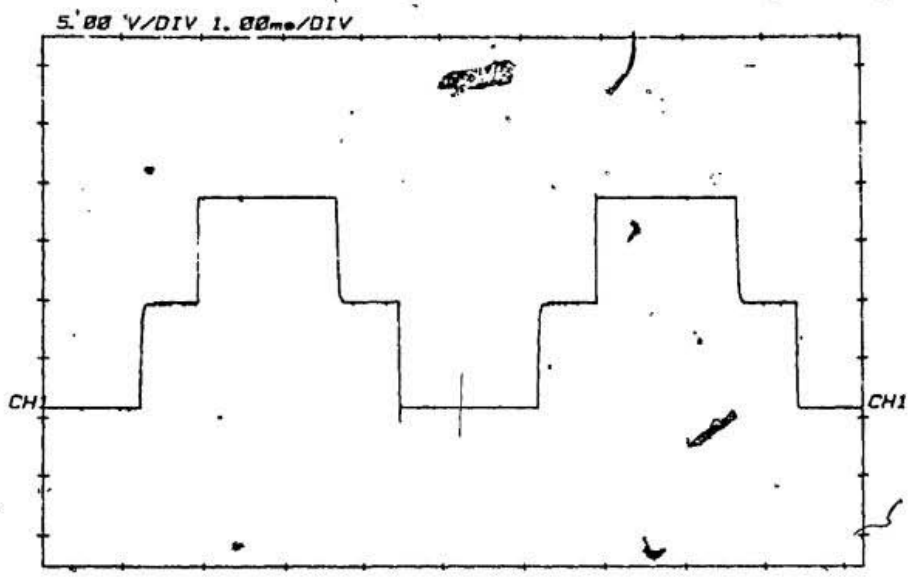


Fig. 5.39 Inverter Output Voltage and Power Spectrum of SDM for f = 180 Hz



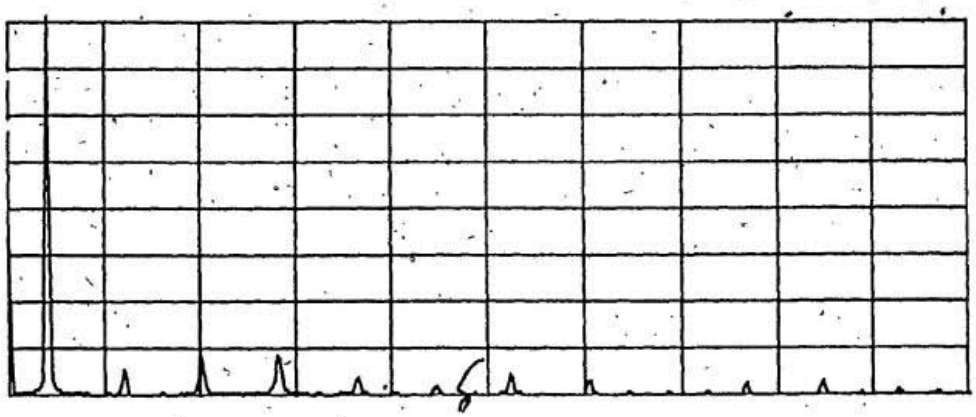


Fig. 5.40 Inverter Output Voltage and Power Spectrum of SDM for f = 200 Hz

For motor load, the output current of the DM inverter is non-sinusoidal and contains lower order harmonics. In Figs. 5.41 to 5.45 the voltage, current, and the power spectrum of the linear delta modulator (LDM) inverter output for motor load at various operating frequencies (f= 20, 40, 60, 80, and 100 Hz) are shown. The sampling frequency fs = 5 kHz, Δ = 1, R = 50 kohms and C = 0.05 microfarads were used. For simplicity the results of LDM inverter output with motor load are presented. However, the results of exponential delta modulator (EDM) and sigma ~~delta mo~~dulator (SDM) inverters under motor load are expected to be similar. These results are not included in this thesis.

Fundamental components of the power spectrum of output waveforms increase linearly with frequency up to base frequency. After base frequency, the magnitude of the fundamental component maintains a constant level. This supports the results obtained from LDM inverter for resistive load.

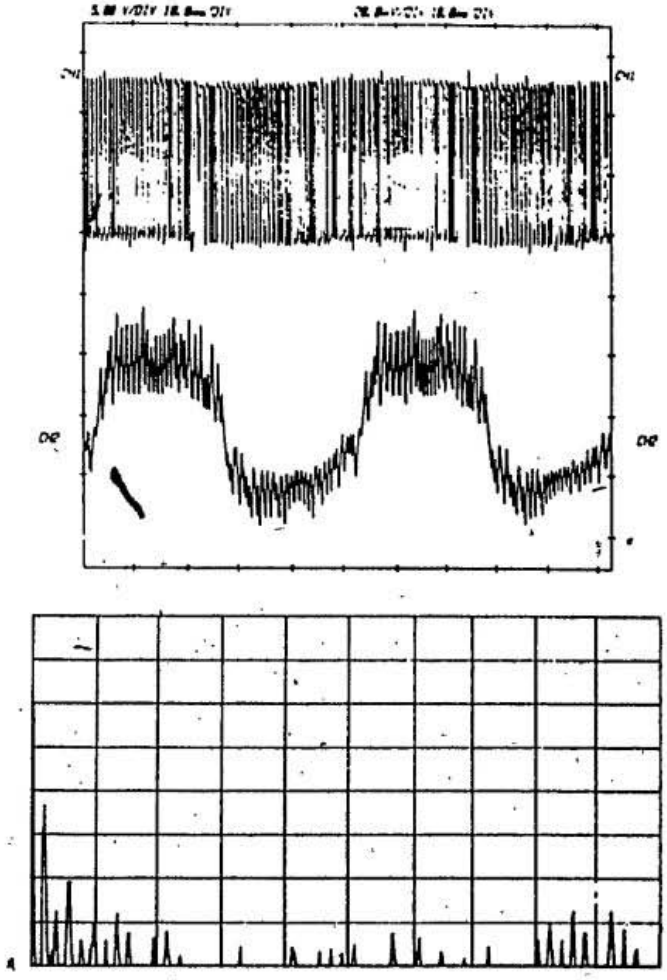


Fig. 5.41 LDM Inverter output voltage, current and power spectrum for motor load for $f = 20$ Hz

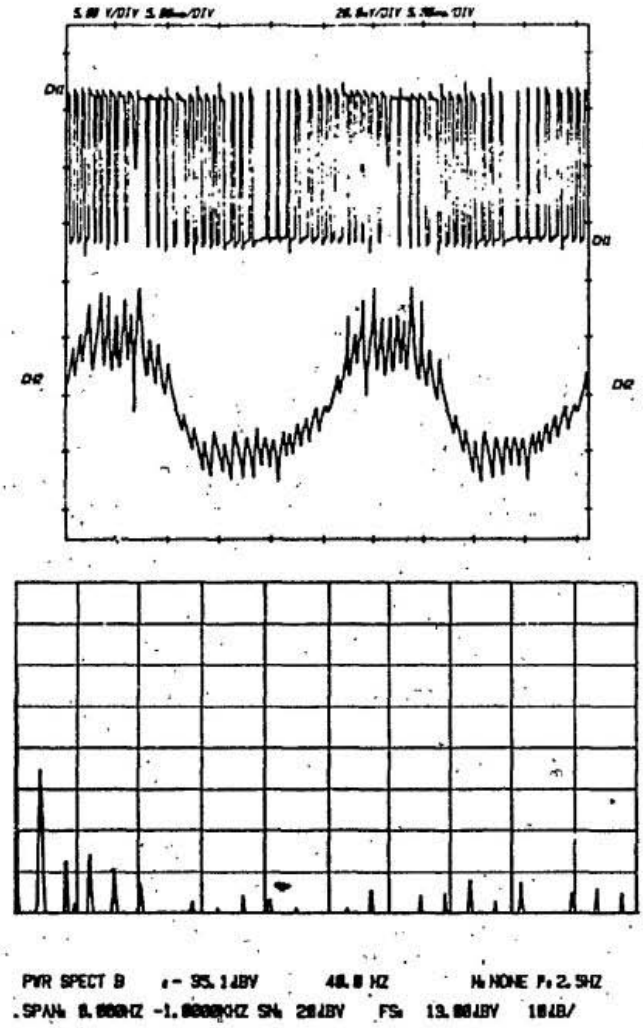


Fig. 5.42 LDM Inverter output voltage, current and power spectrum for motor load for f = 40 Hz

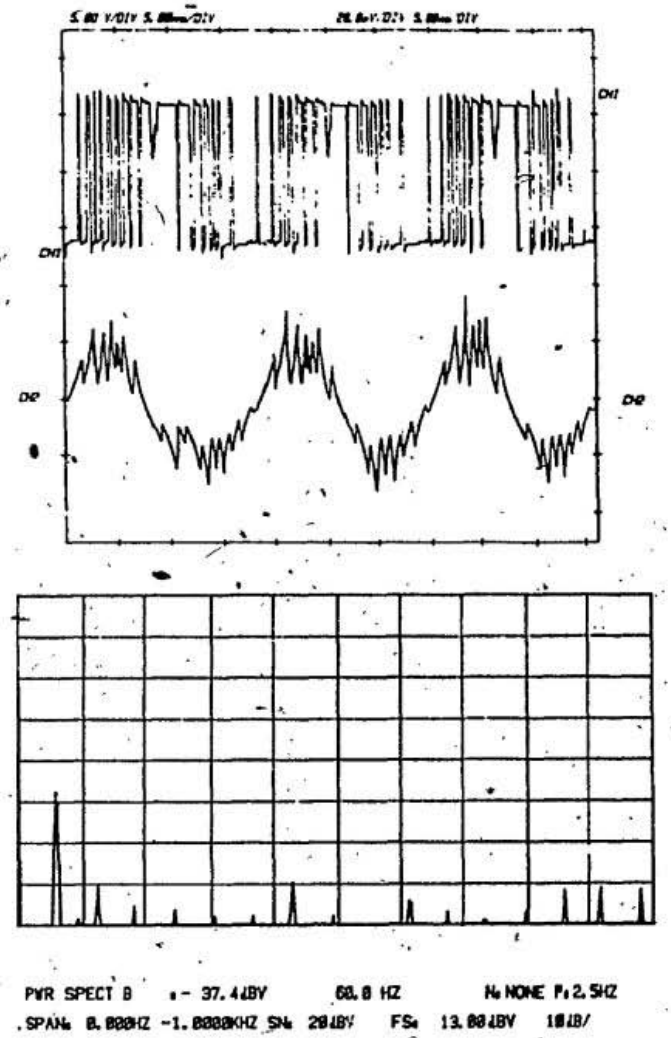


Fig. 5.43 LDM Inverter output voltage, current and power spectrum for motor load for f = 60 Hz

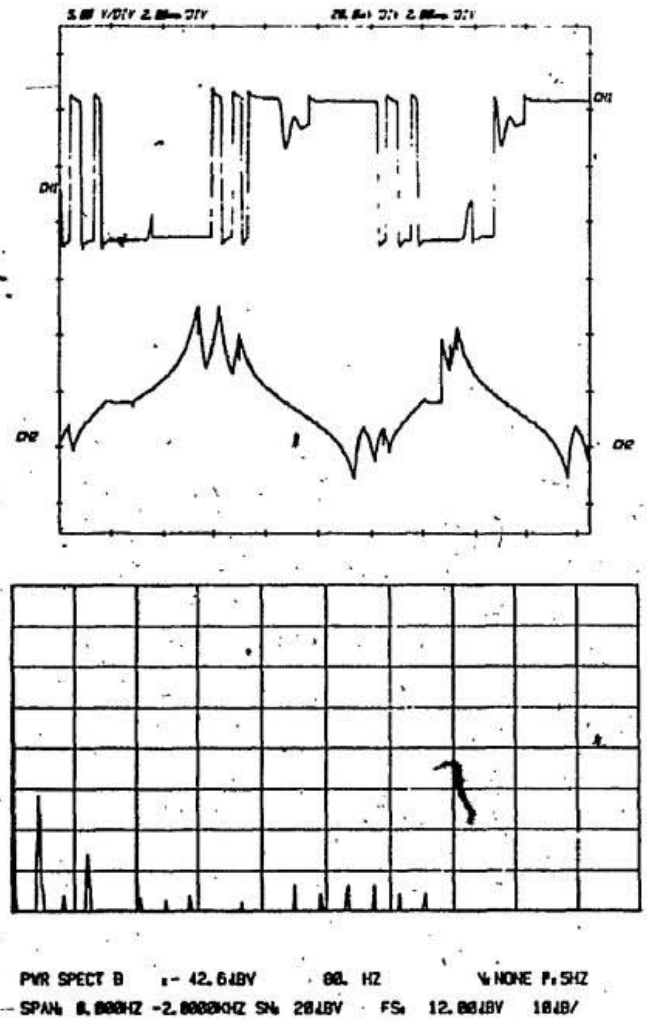


Fig. 5.44 LDM Inverter output voltage, current and power spectrum for motor load for f = 80 Hz

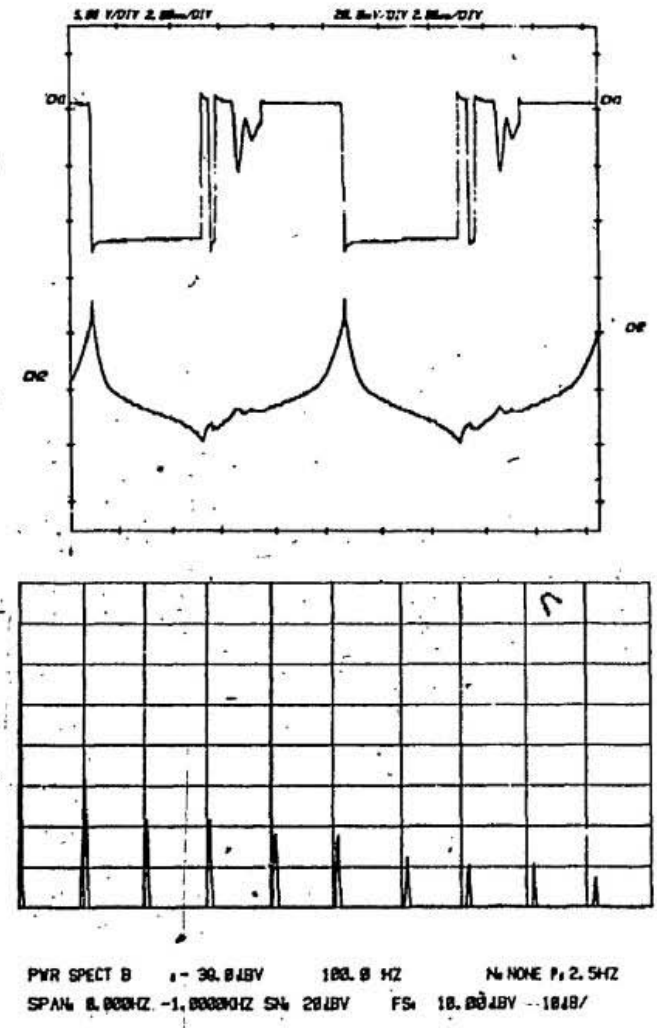


Fig. 5.45 LDM Inverter output voltage, current and power spectrum for motor load for f = 100 Hz

5.3 Merits of Software Controlled DM Inverters

Software control of delta modulated inverters offers a great deal of flexibility in parameter variation. The operation and performance of the inverter can be controlled by software merely by changing the parameter values. Easier implementation of various DM techniques in software and easier control of the operation are the main advantages of microprocessor based delta modulated inverter. Inherent V/f control, lower output harmonic content, and control of number of commutations are additional advantages of software controlled DM inverters.

Table 1 shows a comparison of the three types of delta modulation strategies. It has been found that the linear delta modulator has excellent linear V/f characteristics, whereas sigma delta modulator gives excellent spectral characteristics.

Table 1. Comparison of Three Different Types of Delta Modulation Strategies.

	MODULATION STRATEGY		
CHARACTERISTICS	Linear Delta Modulator	Exponential Delta Modulator	Sigma Delta Modulator
Idling Characteristic	101010...	101010...	101010...
Overload Characteristic	Flat up to base frequency and linearly decreases beyond base frequency	Flat up to base frequency and linearly decreases beyond base frequency	Independent of frequency
Power Shift in Output Spectrum	Present	Present	Present
V/f Characteristic	Linear increase up to base frequency and flat beyond base frequency	Flat at all Frequencies	Flat at all Frequencies
Output Voltage Harmonic Content	High	Medium	Low
Commutation Losses	High	Medium	Low

CHAPTER 6

SUMMARY AND CONCLUSIONS

6.1 Summary

In this thesis, the following objectives were accomplished:

(i) various delta modulation strategies namely LDM, EDM and SDM were implemented to generate switching signals under software control, and

(ii) effect of different delta modulation strategies on the performance of single phase bridge inverter under resistive (and dynamic) load conditions were studied.

In the software implementation of delta modulation techniques, a new approach based on discrete time and non-linear optimal control theory was developed. The integrator in the delta modulator was considered as a low pass digital filter and z-domain analysis of the modulator was carried out. This approach offers the potential for substantial improvement over classical or state space linear system controllers. For implementation, Linear Delta Modulator was considered first. Its input-output characteristics, output voltage harmonic content, and output power spectrum were studied. The work was then extended to other forms of delta modulation techniques, namely, exponential delta modulator and sigma delta modulator.

Software control of delta modulated inverters offers easier control of modulator parameters as well as the control of number of commutations, output voltage, and frequency of the inverter. The performance of the modulator and inverter can be optimised by varying system parameters. Parameter variation was easily achieved by software as opposed to hardware in which redesigning of the whole modulator and control circuit would have been required.

Inherent features of delta modulation such as constant V/f characteristics and lower output voltage harmonics were verified theoretically and experimentally for a single phase delta modulated bridge inverter. This is an important feature for the control of ac motor drives. Output of various delta modulation schemes were analyzed by using Fourier series method. From harmonic analysis of the DM output, it was found that harmonic voltage amplitudes were high at low frequency operation and low at high frequency operation. However, at low frequencies, the order of dominant harmonics was higher and at high frequencies, the order of dominant harmonics was low. Consequently, when DM inverters were used for motor loads, higher harmonics in the load current were attenuated. This was because the reactance for higher order harmonics at low frequency operation were high and for lower order harmonics at high frequency operation were low. The high reactance value at different dominant harmonics limits the harmonic load current. Theoretical results of the harmonic behaviour of various delta modulation systems were verified experimentally with a spectrum analyzer.

Experimentally, it was found that the output voltage of the linear delta modulator shows linear fundamental voltage to frequency variation, which is essential for the control of ac motors. This supported the theoretical expectations. The effect of variation of the modulator parameters such as input frequency, sampling frequency, filter coefficients, and step size on the modulator output was studied for these different types of delta modulators. For a constant sampling frequency, as the operating frequency was increased, the transition from PWM mode to square wave mode occurred in all three modulators. However, in linear delta modulator, mode transition occurred at lower base frequency whereas in exponential delta modulator and sigma delta modulator this mode transition occurred at relatively higher base frequencies. The base frequency at which mode transition occurred increased if the sampling frequency was increased or filter coefficients were decreased.

At low values of step size (Δ) and for constant operating frequency and sampling rate, all three modulators showed the overload condition. As delta was increased, quantization error decreased and modulators successfully decoded the input signal. However, for larger values of delta, quantization error started to increase again. For normal operation of delta modulators, it was found that delta must be comparable to the input signal amplitude.

For fixed values of operating frequency and delta, if the sampling frequency was gradually increased, the quantization error decreased and estimated signal approached the reference signal. However, the modulators produced a large number of output pulses. This increase in the number of output pulses increased

the number of commutations in the inverter and hence commutation losses.

From the power spectrum of the output of delta modulated systems and inverter output voltage, it was found that for linear delta modulator, the fundamental component of voltage and power increased with frequency up to base frequency, and beyond base frequency it became constant. However, in exponential delta modulator and sigma delta modulator, the fundamental component remained approximately constant for all input frequencies, thereby supporting the theoretical results.

To study the motor performances with delta modulated inverter supply, a single phase, 1/4 horse power induction motor was used as a load. The inverter was run at different operating frequencies, keeping other parameters constant. It was found that as the frequency of operation was increased, the speed of the motor also increased. The load current was found to be non-sinusoidal. Therefore, the harmonic content in the load current was large. The higher order harmonics present in the load current spectrum were attenuated, thus supporting the theoretical results.

6.2 Conclusions

The principle of delta modulation strategies and their software implementation, based on discrete time, non-linear optimal control theory, were outlined. It was seen that microprocessor based delta modulated inverter has essentially the characteristic of a uniformly sampled data system. It was found that delta

modulators with their zero-hysteresis, bang-bang type of control features were suited for the inverter systems under consideration. These modulators have shown good tracking capabilities and excellent spectral characteristics. From computer simulation and experimental results, the following conclusions can be made:

1. Software control offers an easier control of modulator and inverter parameters. By optimising parameter values, inverter performance can be optimised.

2. Low filter coefficients and higher sampling frequency result in low quantization error, low output voltage harmonic content, and improved output power spectrum. Therefore for good performance of delta modulated inverter systems, low filter coefficients and high sampling frequency are desired.

3. The delay of the sample and hold and filters in the feed forward and feedback paths of the modulator results in the phase shift of the power spectrum.

4. Linear delta modulation provides a linear voltage vs. frequency characteristic up to base frequency, and constant voltage characteristic beyond the base frequency. This feature of linear delta modulation is most suitable for speed control of ac motor drives under variable load conditions in industrial applications.

Sigma delta modulator has shown a flat output voltage vs. frequency characteristic. Thus sigma delta modulation is best suited for resonant link inverters where flat voltage frequency characteristic over a wide frequency range is required.

5. Due to finite turn-on and turn-off time and higher switching loss at higher sampling rate, switching frequency of delta modulated bridge inverter is limited. However, if zero switching loss inverter topology, instead of bridge inverter topology, is used, performance of the delta modulated inverter could be improved.

6.3 Recommendations for Further Research

This research could further be extended to 3-phase software controlled delta modulated inverters. In 3-phase modulation, the delta modulated output pattern obtained from 3-phase, variable frequency input sine wave can be stored in PROMs in the form of look up tables. Microprocessor could then retrieve the switching pattern corresponding to each phase from the memory and output to respective digital to analog converters. The analog switching signals could thus be used to control the operation of a 3-phase inverter.

The transition from PWM to square wave mode did not occur sharply at the desired base frequency. In this transition band, the behaviour of modulators was very unpredictable. Perhaps by parameter optimization, a sharp mode transition

could be achieved more effectively and sharply at the desired base frequency.

The frequency of the switching pattern was limited, typically 5 KHz, by the switching losses of the devices used in the bridge inverter. It was found that higher switching frequency resulted in better output spectral characteristics and lower output voltage harmonic content. Therefore, using zero switching loss inverter topologies, the switching frequency can be increased and hence the performance of delta modulated PWM inverters can be improved significantly.

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APPENDIX: PROGRAM LISTINGS

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C     ***************************************************
C     ***************************************************
C     **
C     **          "LINEAR DELTA MODULATOR "
C     **
C     **
C     **          PROGRAM TO GENERATE SYMMETRICAL
C     **         DELTA MODULATED SWITCHING WAVE-FORM
C     **            USING HALF-WAVE SYMMETRY
C     **              OF SINUSOIDAL INPUT
C     **
C     ***************************************************
C     ***************************************************
C     **
C     **          © RAJIV KUMAR SRIVASTAVA
C     **            DATE: OCTOBER 2, 1986
C     **
C     ***************************************************
C
C
C
      PROGRAM DELTA MODULATOR
      INTEGER N,NN
      REAL X(1000),Y(1000),XK1(1000),OP1(1000),EK1(1000),T(1000)
      REAL DELTA ,W,DEG,RAD,F,FS,TS,RESISTANCE,CAPACITANCE
      REAL A0,A1,OP,POP,YK,PYK,EK,XK
      OPEN(11,FILE='LDM.DAT',STATUS='NEW')
      PRINT*,'ENTER AMPLITUDE OF INPUT SIN SIGNAL'
      READ*, AMP
      PRINT*, 'ENTER THE FREQ. OF INPUT SINE SIGNAL IN HZ'
      READ*, F
      PRINT*,'ENTER DELTA'
      READ*,DELTA
      PI=3.141592654
      W=2.0*PI*F
      DEG=180.0/PI
      RAD=1.0/DEG
      PRINT*, 'ENTER SAMPLING FREQ. IN HZ'
      READ*,FS
      NN=INT(FS/F)
      TS=1.0/(FS)
      PRINT*, 'F= ',F, '  FS=',FS
      PRINT*,'NN=',NN, '  TS=',TS
      PRINT*,'ENTER THE VALUE OF RESISTANCE IN OHMS'
      READ*,RESISTANCE
      PRINT*,'ENTER THE VALUE OF CAPACITANCE IN MICRO-FARAD'
      READ*,CAPACITANCE
      A0=TS*1E0/(2*RESISTANCE*CAPACITANCE)
      A1=A0
      PRINT*,'A0=',A0,'A1=',A1
      WRITE(11,3)F,FS
3     FORMAT(2X,'INPUT FREQUENCY=',F6.2,2X,'SAMPLING FREQUENCY=',F8.2)
      WRITE(11,4)NN,TS
```

```
4     FORMAT(2X,'NO. OF POINTS=',I4,2X,'SAMPLING INTERVAL=',F8.5)
      WRITE(11,5)RESISTANCE,CAPACITANCE
5     FORMAT(2X,'RESISTANCE =',F8.2,2X,'CAPACITANCE =',F16.8)
      WRITE(11,*)' COEF-A0 = ',A0,'COEF-A1 = ',A1
      OP=0.0
      POP=0.0
      YK=0.0
      PYK=0.0
C     PRINT*,'I','    XX  ','    XK  ','   OP1(I)  ',' Y(I) '
      WRITE(11,7)'I','X(I)','XK1(I)','EK1(I)','OP1(I)','Y(I)','T(I)'
7     FORMAT(A5,2X,A10,2X,A10,2X,A10,2X,A10,2X,A10,2X,A10)
      DO 10 I=1,INT(NN/2)+1,1
       N=I-1
       XK=AMP*SIN(N*W*TS)
       XK1(I)=XK
       EK=XK-OP
       EK1(I)=EK
       OP1(I)=OP
       POP=OP
       IF (EK .GE. 0.0) THEN
        YK=DELTA
       ELSE
        YK= -DELTA
       END IF
       X(I)=N*TS*W*DEG
       T(I)=N*TS
       Y(I)=YK
       OP=A0*YK+ A1*PYK+ POP
       PYK = YK
       N=N+1
C      PRINT*,I,N,X(I),XK1(I),EK1(I),OP1(I),Y(I)
       WRITE(11,8)I,X(I),XK1(I),EK1(I),OP1(I),Y(I),T(I)
8      FORMAT(I5,4(2X,F10.4),2X,F10.2,2X,F10.6)
10    CONTINUE
C ***************************************************************
      DO 12 I=INT(NN/2)+2,NN+1,1
       II = I-1
       N1 = NN+1
       Y(I)= -Y(N1-II)
       X(I)=N*W*TS*DEG
       XK1(I)=-XK1(N1-II)
       EK1(I)=-EK1(N1-II)
       OP1(I)=-OP1(N1-II)
C      PRINT*, I,N,X(I),XK1(I),EK1(I),OP1(I),Y(I)
       WRITE(11,9)I,X(I),XK1(I),EK1(I),OP1(I),Y(I),T(I)
9      FORMAT(I5,4(2X,F10.4),2X,F10.2,2X,F10.6)
       N = N+1
12    CONTINUE
C ***************************************************************
      CALL DELPLOT(X,Y,XK1,OP1,EK1,NN,DELTA,AMP,F,FS,A0)
C ***************************************************************
      END
```

```
C ************************************************************
      SUBROUTINE DELPLOT(x,y,XK1,OP1,EK1,n,DELTA,AMP,F,FS,A0)
C ************************************************************
      REAL X(1),Y(1),XK1(1),OP1(1),EK1(1)
      INTEGER N
      XINC=6./N
      CALL PLOTS(53,0,-1)
      CALL ZPICK(3,0,ISTAT)
      CALL FACTOR(0.7)
      CALL ORIGIN(2.5,8.,0)
      DELVAL=X(2)*N/6.
      TINC = 1.0
      ASP = 1.0
      SZN = 0.1
      SZL = 0.12
      CALL HALAB2(0.,-2.5,0.,DELVAL,TINC,1,6.,1,SZN,ASP,1,-1,
     +          SZL,'WT (DEG.) -----')
      CALL VALAB2(0.,-1.,-DELTA,DELTA,TINC,1,2.,1,SZN,ASP,1,1,YP,
     +          SZL,' OUTPUT AMPLITUDE')
      CALL VALAB2(-1.0,-3.,-1.5*AMP,.5*AMP,TINC,1,6.,1,SZN,ASP,1,1,YP,
     +          SZL,'          INPUT AMPLITUDE')

      CALL PLOT(0.,0.,3)
      CALL DASHDF(0.,0.,0.,0)

      CALL PLABEL(XINC,XK1,N,AMP,.2,4.0,.15,'= INPUT SIGNAL',0.,0,2,11)
      CALL PLOT(6.,0.,2)
      CALL PLOT(0.,0.,3)
      CALL SYMB2(-0.4,-3.8,.15,'Coef_A0 = ',0.0,1)
      IF (A0.LT.1.0) CALL TYPNUM(999.,999.,.15,0.0,0.0,-1)
      CALL TYPNUM(999.,999.,.15,A0,0.0,3)
      CALL SYMB2(3.85,-3.8,.15,'Delta = ',0.0,1)
      IF (DELTA.LT.1.0) CALL TYPNUM(999.,999.,.15,0.0,0.0,-1)
      CALL TYPNUM(999.,999.,.15,DELTA,0.0,1)

      CALL SYMB2(3.03,-3.5,.15,'Samp. Freq. = ',0.0,1)
      CALL TYPNUM(999.,999.,.15,FS,0.0,1)
      CALL SYMB2(999.,999.,.15,' HZ',0.0,0)

      CALL SYMB2(-0.88,-3.5,.15,'Input Freq. = ',0.0,1)
      CALL TYPNUM(999.,999.,.15,F,0.0,1)
      CALL SYMB2(999.,999.,.15,' HZ',0.0,0)

C     CALL NEWPEN(2)
      CALL PSYMB(4.2,3.5,.15,'= OUTPUT SIGNAL',0.,0,2,-1)
      if (y(1) .ge. 0.) then
        YC = 1.
      else
        YC = -1.
      end if
      CALL PLOT(0.,0.,3)
      CALL PLOT(0.,YC,2)
      do 100 i=1,n
```

```
      if (y(i) .ge. 0.) then
       yd=1.
      else
       yd=-1.
      end if
      IF (YD.NE.YC) CALL PLOT(XD,YD,2)
      XD=I*XINC
      CALL PLOT(XD,YD,2)
      YC = YD
100   continue

C     CALL NEWPEN(3)
      CALL PLABEL(XINC,OP1,N,AMP,.2,3.5,.15,'= APPROX. SIGNAL',0.,0,2,2)
      CALL PLOT(XINC*N,0.,2)
      CALL PLOT(0.,0.,3)

C     CALL NEWPEN(4)
      CALL PLABEL(XINC,EK1,N,AMP,4.2,4.,.15,'= ERROR SIGNAL',0.,0,2,4)

      CALL PLOT(0.,0.,999)
      return
      end

C ***************************************************************
      SUBROUTINE PLABEL(XINC,YY,N,AMP,X,Y,SZ,LABEL,ANGL,ND,NLINE,NS)
C ***************************************************************
      CHARACTER*(*) LABEL
      DIMENSION YY(1)
      CALL PSYMB(X,Y,SZ,LABEL,ANGL,ND,NLINE,NS)
      NM = N/10
      DO 10 I=1,N+1
        CALL PLOT(XINC*(I-1),YY(I)*2./AMP,NLINE)
        IF (NM*((I+NS)/NM).EQ.(I+NS))
     +      CALL SYMBOL(XINC*(I-1),YY(I)*2./AMP,.08,NS,0.,-1)
10    CONTINUE
      call plot(0.,0.,3)
      RETURN
      END

C ***************************************************************
      SUBROUTINE PSYMB(X,Y,SZ,LABEL,ANGL,ND,NLINE,NS)
C ***************************************************************
      CHARACTER*(*) LABEL
      IF (NS.LT.0) THEN
        CALL PLOT(X-.7,Y,3)
        CALL PLOT(X-.48,Y,NLINE)
        CALL PLOT(X-.48,Y+.2,NLINE)
        CALL PLOT(X-.45,Y+.2,NLINE)
        CALL PLOT(X-.45,Y,NLINE)
        CALL PLOT(X-.2,Y,NLINE)
        CALL PLOT(0.,0.,3)
      ELSE
        CALL SYMBOL(X-.6,Y,.08,NS,0.,-1)
```

```
      CALL SYMBOL(X-.3,Y,.08,NS,0.,-1)
    ENDIF
    CALL SYMB2(X,Y,SZ,LABEL,ANGL,ND)
    CALL PLOT(0.,0.,3)
    RETURN
    END
```

```
C     ******************************************************
C     ******************************************************
C     **
C     **       "EXPONENTIAL DELTA MODULATOR"
C     **
C     **
C     **        PROGRAM TO GENERATE SYMMETRICAL
C     **       DELTA MODULATED SWITCHING WAVE-FORM
C     **          USING HALF-WAVE SYMMETRY
C     **            OF SINUSOIDAL INPUT
C     **
C     ******************************************************
C     ******************************************************
C     **          ©
C     **            RAJIV KUMAR SRIVASTAVA
C     **            DATE: APRIL 12, 1987
C     **
C     ******************************************************
C
C
C
      PROGRAM EXPONENTIAL DELTA MODULATOR
      INTEGER N,NN
      REAL X(1000),Y(1000),XK1(1000),OP1(1000),EK1(1000),T(1000)
      REAL DELTA ,W,DEG,RAD,F,FS,TS,RESISTANCE,CAPACITANCE
      REAL A0,A1,B1,OP,POP,YK,PYK,EK,XK,NUMR
      OPEN(11,FILE='EXP.DAT',STATUS='NEW')
      PRINT*,'ENTER AMPLITUDE OF INPUT SIN SIGNAL'
      READ*, AMP
      PRINT*, 'ENTER THE FREQ. OF INPUT SINE SIGNAL IN HZ'
      READ*, F
      PRINT*,'ENTER DELTA'
      READ*,DELTA
      PI=3.141592654
      W=2.0*PI*F
      DEG=180.0/PI
      RAD=1.0/DEG
      PRINT*, 'ENTER SAMPLING FREQ. IN HZ'
      READ*,FS
      NN=INT(FS/F)
      TS=1.0/(FS)
      PRINT*, 'F= ',F, '  FS=',FS
      PRINT*,'NN=',NN, '  TS=',TS
      PRINT*,'ENTER THE VALUE OF RESISTANCE IN OHMS'
      READ*,RESISTANCE
      PRINT*,'ENTER THE VALUE OF CAPACITANCE IN MICRO-FARAD'
      READ*,CAPACITANCE
      NUMR= 1E-6*(2*RESISTANCE*CAPACITANCE)
      A0=TS/(TS+ NUMR)
      A1=A0
      B1=(TS-NUMR)/(TS+ NUMR)
      PRINT*,'A0=',A0,'A1=',A1,' B1=',B1
      WRITE(11,3)F,FS
```

```
3     FORMAT(2X,'INPUT FREQUENCY=',F6.2,2X,'SAMPLING FREQUENCY=',F8.2)
      WRITE(11,4) NN,TS
4     FORMAT(2X,'NO. OF POINTS=',I4,2X,'SAMPLING INTERVAL=',F8.5)
      WRITE(11,5)RESISTANCE,CAPACITANCE
5     FORMAT(2X,'RESISTANCE =',F8.2,2X,'CAPACITANCE =',F16.8)
      WRITE(11,*)'  COEF-A0 & A1 = ',A0,'COEF-B1 = ',B1
      OP=0.0
      POP=0.0
      YK=0.0
      PYK=0.0
      N=0
      PRINT*,'I','     XX ',','     XK  ','    OP1(I) ','Y(I)  '
      WRITE(11,7)'I','X(I)','XK1(I)','EK1(I)','OP1(I)','Y(I)','T(I)'
7     FORMAT(A5,2X,A10,2X,A10,2X,A10,2X,A10,2X,A10,2X,A10)
      DO 10 I=1,INT(NN/2)+1,1
       XK=AMP*SIN(N*W*TS)
       XK1(I)=XK
       EK=XK-OP
       EK1(I)=EK
       OP1(I)=OP
       POP=OP
       IF (EK .GE. 0.0) THEN
        YK=DELTA
       ELSE
        YK= -DELTA
       END IF
       X(I)=N*TS*W*DEG
       T(I)=N*TS
       Y(I)=YK
       OP=A0*YK+ A1*PYK-B1*POP
       PYK = YK
       N=N+1
C      PRINT*,I,X(I),XK1(I),EK1(I),OP1(I),Y(I)
       WRITE(11,8)I,X(I),XK1(I),EK1(I),OP1(I),Y(I),T(I)
8      FORMAT(I5,4(2X,F10.4),2X,F10.2,2X,F10.6)
10    CONTINUE
C ***************************************************************
      N1=NN+1
      DO 12 I=INT(NN/2)+2,NN+1,1
         II=I-1
         Y(I)=-Y(N1-II)
         X(I)=N*W*TS*DEG
         XK1(I)=-XK1(N1-II)
         EK1(I)=-EK1(N1-II)
         OP1(I)=-OP1(N1-II)
         WRITE(11,9)I,X(I),XK1(I),EK1(I),OP1(I),Y(I),T(I)
9        FORMAT(I5,4(2X,F10.4),2X,F10.2,2X,F10.6)
12    CONTINUE
      CALL DELPLOT(X,Y,XK1,OP1,EK1,NN,DELTA,AMP,F,FS,A0)
      END
C
C ***************************************************************
    SUBROUTINE DELPLOT(x,y,XK1,OP1,EK1,n,DELTA,AMP,F,FS,A0)
```

```
C ***********************************************************
      REAL X(1),Y(1),XK1(1),OP1(1),EK1(1)
      INTEGER N
      XINC=6./N
      CALL PLOTS(53,0,-1)
      CALL ZPICK(3,0,ISTAT)
      CALL FACTOR(0.7)
      CALL ORIGIN(2.5,8.,0)
      DELVAL=X(2)*N/6.
      TINC = 1.0
      ASP = 1.0
      SZN = 0.1
      SZL = 0.12
      CALL HALAB2(0.,-2.5,0.,DELVAL,TINC,1,6.,1,SZN,ASP,1,-1,
     +          SZL,'WT (DEG) -----')
      CALL VALAB2(0.,-1.,-DELTA,DELTA,TINC,1,2.,1,SZN,ASP,1,1,YP,
     +          SZL,' OUTPUT AMPLITUDE')

      CALLVALAB2(-1.0,-3.,-1.5*AMP,.5*AMP,TINC,1,6.,1,SZN,ASP,1,1,YP,
     +          SZL,'          INPUT AMPLITUDE')

      CALL PLOT(0.,0.,3)
      CALL DASHDF(0.,0.,0.,0)

      CALL PLABEL(XINC,XK1,N,AMP,.2,4.0,.15,'= INPUT SIGNAL',0.,0,2,11)
      CALL PLOT(6.,0.,2)
      CALL PLOT(0.,0.,3)

      CALL SYMB2(-0.4,-3.8,.15,'Coef_A0 = ',0.0,1)
      IF (A0.LT.1.0) CALL TYPNUM(999.,999.,.15,0.0,0.0,-1)
      CALL TYPNUM(999.,999.,.15,A0,0.0,3)

      CALL SYMB2(1.8,-3.8,.15,'Coef_B1 = ',0.0,1)
C     IF (B1.LT.1.0) CALL TYPNUM(999.,999.,.15,0.0,0.0,-1)
      CALL TYPNUM(999.,999.,.15,B1,0.0,3)

      CALL SYMB2(4.05,-3.8,.15,'Delta = ',0.0,1)
      IF (DELTA.LT.1.0) CALL TYPNUM(999.,999.,.15,0.0,0.0,-1)
      CALL TYPNUM(999.,999.,.15,DELTA,0.0,1)

      CALL SYMB2(3.23,-3.5,.15,'Samp. Freq. = ',0.0,1)
      CALL TYPNUM(999.,999.,.15,FS,0.0,1)
      CALL SYMB2(999.,999.,.15,' HZ',0.0,0)

      CALL SYMB2(-0.88,-3.5,.15,'Input Freq. = ',0.0,1)
      CALL TYPNUM(999.,999.,.15,F,0.0,1)
      CALL SYMB2(999.,999.,.15,' HZ',0.0,0)

C     CALL NEWPEN(2)
      CALL PSYMB(4.2,3.5,.15,'= OUTPUT SIGNAL',0.,0,2,-1)
      if (y(1) .ge. 0.) then
        YC = 1.
      else
```

```
        YC = -1.
      end if
      CALL PLOT(0.,0.,3)
      CALL PLOT(0.,YC,2)
      do 100 i=1,n
        if (y(i) .ge. 0.) then
          yd=1.
        else
          yd=-1.
        end if
        IF (YD.NE.YC) CALL PLOT(XD,YD,2)
        XD=I*XINC
        CALL PLOT(XD,YD,2)
        YC = YD
100   continue

C     CALL NEWPEN(3)
      CALL PLABEL(XINC,OP1,N,AMP,.2,3.5,.15,'= ESTIMATED
     + SIGNAL',0.,0,2,2)
      CALL PLOT(XINC*N,0.,2)
      CALL PLOT(0.,0.,3)

C     CALL NEWPEN(4)
      CALL PLABEL(XINC,EK1,N,AMP,4.2,4.,.15,'= ERROR SIGNAL',0.,0,2,4)

      CALL PLOT(0.,0.,999)
      return
      end
C ***************************************************************
      SUBROUTINE PLABEL(XINC,YY,N,AMP,X,Y,SZ,LABEL,ANGL,ND,NLINE,NS)
C ***************************************************************
      CHARACTER*(*) LABEL
      DIMENSION YY(1)
      CALL PSYMB(X,Y,SZ,LABEL,ANGL,ND,NLINE,NS)
      NM = N/10
      DO 10 I=1,N+1
        CALL PLOT(XINC*(I-1),YY(I)*2./AMP,NLINE)
        IF (NM*((I+NS)/NM).EQ.(I+NS))
     +       CALL SYMBOL(XINC*(I-1),YY(I)*2./AMP,.08,NS,0.,-1)
10    CONTINUE
      call plot(0.,0.,3)
      RETURN
      END

C ***************************************************
      SUBROUTINE PSYMB(X,Y,SZ,LABEL,ANGL,ND,NLINE,NS)
C ***************************************************
      CHARACTER*(*) LABEL
      IF (NS.LT.0) THEN
        CALL PLOT(X-.7,Y,3)
        CALL PLOT(X-.48,Y,NLINE)
        CALL PLOT(X-.48,Y+.2,NLINE)
        CALL PLOT(X-.45,Y+.2,NLINE)
```

```
      CALL PLOT(X-.45,Y,NLINE)
      CALL PLOT(X-.2,Y,NLINE)
      CALL PLOT(0.,0.,3)
    ELSE
      CALL SYMBOL(X-.6,Y,.08,NS,0.,-1)
      CALL SYMBOL(X-.3,Y,.08,NS,0.,-1)
    END IF
    CALL SYMB2(X,Y,SZ,LABEL,ANGL,ND)
    CALL PLOT(0.,0.,3)
    RETURN
    END
```

```
C     ****************************************************
C     ****************************************************
C     **
C     **          "SIGMA DELTA MODULATOR"
C     **
C     **
C     **        PROGRAM TO GENERATE SYMMETRICAL
C     **       DELTA MODULATED SWITCHING WAVE-FORM
C     **         USING HALF-WAVE SYMMETRY
C     **           OF SINUSOIDAL INPUT
C     **
C     ****************************************************
C     ****************************************************
C     **
C     **          © RAJIV KUMAR SRIVASTAVA
C     **            DATE: MAY 19, 1987
C     **
C     ****************************************************
C
C
C
      PROGRAM SIGMA DELTA MODULATOR
      INTEGER N,NN,XK2(1000),XX(1000)
      REAL X(1000),Y(1000),XK1(1000),OP1(1000),EK1(1000),T(1000)
      REAL DELTA ,W,DEG,RAD,F,FS,TS,RESISTANCE,CAPACITANCE
      REAL A0,A1,B1,OP,POP,YK,PYK,EK,XK,NUMR
      OPEN(11,FILE='SIGMA.DAT',STATUS='NEW')
      PRINT*,'ENTER AMPLITUDE OF INPUT SIN SIGNAL'
      READ*, AMP
      PRINT*, 'ENTER THE FREQ. OF INPUT SINE SIGNAL IN HZ'
      READ*, F
      PRINT*,'ENTER DELTA'
      READ*,DELTA
      PI=3.141592654
      W=2.0*PI*F
      DEG=180.0/PI
      RAD=1.0/DEG
      PRINT*, 'ENTER SAMPLING FREQ. IN HZ'
      READ*,FS
      NN=INT(FS/F)
      TS=1.0/(FS)
      PRINT*, 'F= ',F, '  FS=',FS
      PRINT*,'NN=',NN, '  TS=',TS
      PRINT*,'ENTER THE VALUE OF RESISTANCE IN OHMS'
      READ*,RESISTANCE
      PRINT*,'ENTER THE VALUE OF CAPACITANCE IN MICRO-FARAD'
      READ*,CAPACITANCE
      A0=TS*1E6/(2*RESISTANCE*CAPACITANCE)
      A1=A0
      PRINT*,'  A0=',A0,'A1=',A1
      WRITE(11,3)F,FS
3     FORMAT(2X,'INPUT FREQUENCY=',F6.2,2X,'SAMPLING FREQUENCY=',F8.2)
      WRITE(11,4)NN,TS
```

```
4     FORMAT(2X,'NO. OF POINTS=',I4,2X,'SAMPLING INTERVAL=',F8.5)
      WRITE(11,5)RESISTANCE,CAPACITANCE
5     FORMAT(2X,'RESISTANCE =';F8.2,2X,'CAPACITANCE =',F16.8)
      WRITE(11,*)' COEF-A0 = ',A0,' COEF-A1 = ',A1
      OP=0.0
      POP=0.0
      YK=0.0
      EK=0.0
      PEK=0.0
C     PRINT*,'I','   XX ','    XK ','  OP1(I) ','Y(I) '
      WRITE(11,7)'I','X(I)','XK1(I)','EK1(I)','OP1(I)','Y(I)','T(I)'
7     FORMAT(A5,2X,A10,2X,A10,2X,A10,2X,A10,2X,A10,2X,A10)
      DO 10 I=1,INT(NN/2)+1,1
       N=I-1
       XK=AMP*SIN(N*W*TS)
       XK1(I)=XK
       XK2(I)=INT(2047*XK1(I))
       IF (XK1(I) .GE. 0.0) THEN
        XX(I) = 1
       ELSE
        XX(I) = -1
       END IF
       EK=XK-YK
       EK1(I)=EK
       OP=A0*EK+A1*PEK+POP
       OP1(I)=OP
       IF (OP .GE. 0.0) THEN
        YK=DELTA
       ELSE
        YK= -DELTA
       END IF
       X(I)=N*TS*W*DEG
       T(I)=N*TS
       Y(I)=YK
       POP=OP
       PEK = EK
       N=N+1
C      PRINT*,I,X(I),XK1(I),EK1(I),OP1(I),Y(I)
       WRITE(11,8)I,X(I),XK1(I),EK1(I),OP1(I),Y(I),T(I)
8      FORMAT(I5,4(2X,F10.4),2X,F10.2,2X,F10.6)
10    CONTINUE
C ***************************************************************
      DO 12 I=INT(NN/2)+2,NN+1,1
       II = I-1
       N1 = NN+1
       Y(I)= -Y(N1-II)
       X(I)=N*W*TS*DEG
       T(I)=N*TS
       XK1(I)=-XK1(N1-II)
       EK1(I)=-EK1(N1-II)
       OP1(I)=-OP1(N1-II)
       XK2(I)=INT(2047*XK1(I))
       IF (XK1(I) .GE. 0.0) THEN
```

```
        XX(I) =1
       ELSE
        XX(I) = -1
       END IF
C      PRINT*,I,N,X(I),XK1(I),EK1(I),OP1(I),Y(I)
       WRITE(11,9)I,X(I),XK1(I),EK1(I),OP1(I),Y(I),T(I)
9      FORMAT(I5,4(2X,F10.4),2X,F10.2,2X,F10.6)
       N = N+1
12     CONTINUE
C ***************************************************************
       CALL DELPLOT(X,Y,XK1,OP1,EK1,NN,DELTA,AMP,F,FS,A0)
C ***************************************************************
       END
C
C
C ***************************************************************
      SUBROUTINE DELPLOT(x,y,XK1,OP1,EK1,n,DELTA,AMP,F,FS,A0)
C ***************************************************************
      REAL X(1),Y(1),XK1(1),OP1(1),EK1(1)
      INTEGER N
      XINC=6./N
      CALL PLOTS(53,0,-1)
      CALL ZPICK(3,0,ISTAT)
      CALL FACTOR(0.7)
      CALL ORIGIN(2.5,8.,0)
      DELVAL=X(2)*N/6.
      TINC = 1.0
      ASP = 1.0
      SZN = 0.1
      SZL = 0.12
      CALL HALAB2(0.,-2.5,0.,DELVAL,TINC,1,6.,1,SZN,ASP,1,-1,
     +          SZL,'WT (DEG.) ----->')
      CALL VALAB2(0.,-1.,-DELTA,DELTA,TINC,1,2.,1,SZN,ASP,1,1,YP,
     +          SZL,' OUTPUT AMPLITUDE')
      CALL VALAB2(-1.0,-3.,-1.5*AMP,.5*AMP,TINC,1,6.,1,SZN,ASP,1,1,YP,
     +          SZL,'          INPUT AMPLITUDE')

      CALL PLOT(0.,0.,3)
      CALL DASHDF(0.,0.,0.,0)

      CALL PLABEL(XINC,XK1,N,AMP,.2,4.0,.15,'= INPUT SIGNAL',0.,0,2,11)
      CALL PLOT(6.,0.,2)
      CALL PLOT(0.,0.,3)
      CALL SYMB2(-0.4,-3.8,.15,'Coef_A0 = ',0.0,1)
      IF (A0.LT.1.0) CALL TYPNUM(999.,999.,.15,0.0,0.0,-1)
      CALL TYPNUM(999.,999.,.15,A0,0.0,3)
      CALL SYMB2(3.85,-3.8,.15,'Delta = ',0.0,1)
      IF (DELTA.LT.1.0) CALL TYPNUM(999.,999.,.15,0.0,0.0,-1)
      CALL TYPNUM(999.,999.,.15,DELTA,0.0,1)

      CALL SYMB2(3.03,-3.5,.15,'Samp. Freq. = ',0.0,1)
      CALL TYPNUM(999.,999.,.15,FS,0.0,1)
      CALL SYMB2(999.,999.,.15,' HZ',0.0,0)
```

```
      CALL SYMB2(-0.88,-3.5,.15,'Input Freq. = ',0.0,1)
      CALL TYPNUM(999.,999.,.15,F,0.0,1)
      CALL SYMB2(999.,999.,.15,' HZ',0.0,0)

C     CALL NEWPEN(2)
      CALL PSYMB(4.2,3.5,.15,'= OUTPUT SIGNAL',0.,0,2,-1)
      if (y(1) .ge. 0.) then
        YC = 1.
      else
        YC = -1.
      end if
      CALL PLOT(0.,0.,3)
      CALL PLOT(0.,YC,2)
      do 100 i=1,n
        if (y(i) .ge. 0.) then
          yd=1.
        else
          yd=-1.
        end if
        IF (YD.NE.YC) CALL PLOT(XD,YD,2)
        XD=I*XINC
        CALL PLOT(XD,YD,2)
        YC = YD
100   continue

C     CALL NEWPEN(3)
C     CALL PLABEL(XINC,OP1,N,AMP,.2,3.5,.15,'='ESTIMATED SIGNAL',0.,0,2,2)
      CALL PLABEL(XINC,OP1,N,AMP,.2,3.5,.15,'= INTEGRATED
     + ERROR',0.,0,2,2)
      CALL PLOT(XINC*N,0.,2)
      CALL PLOT(0.,0.,3)

C     CALL NEWPEN(4)
C     CALL PLABEL(XINC,EK1,N,AMP,4.2,4.,.15,'= ERROR SIGNAL',0.,0,2,4)

      CALL PLOT(0.,0.,999)
      RETURN
      END
C
C ***************************************************************
      SUBROUTINE PLABEL(XINC,YY,N,AMP,X,Y,SZ,LABEL,ANGL,ND,NLINE,NS)
C ***************************************************************
      CHARACTER*(*) LABEL
      DIMENSION YY(1)
      CALL PSYMB(X,Y,SZ,LABEL,ANGL,ND,NLINE,NS)
      NM = N/10
      DO 10 I=1,N+1
        CALL PLOT(XINC*(I-1),YY(I)*2./AMP,NLINE)
        IF (NM*((I+NS)/NM).EQ.(I+NS))
     +      CALL SYMBOL(XINC*(I-1),YY(I)*2./AMP,.08,NS,0.,-1)
10    CONTINUE
      call plot(0.,0.,3)
```

```
      RETURN
      END
C
C ***************************************************
      SUBROUTINE PSYMB(X,Y,SZ,LABEL,ANGL,ND,NLINE,NS)
C ***************************************************
      CHARACTER*(*) LABEL
      IF (NS.LT.0) THEN
        CALL PLOT(X-.7,Y,3)
        CALL PLOT(X-.48,Y,NLINE)
        CALL PLOT(X-.48,Y+ .2,NLINE)
        CALL PLOT(X-.45,Y+ .2,NLINE)
        CALL PLOT(X-.45,Y,NLINE)
        CALL PLOT(X-.2,Y,NLINE)
        CALL PLOT(0.,0.,3)
      ELSE
        CALL SYMBOL(X-.6,Y,.08,NS,0.,-1)
        CALL SYMBOL(X-.3,Y,.08,NS,0.,-1)
      ENDIF
      CALL SYMB2(X,Y,SZ,LABEL,ANGL,ND)
      CALL PLOT(0.,0.,3)
      RETURN
      END
```

```
C     ***********************************************
C     ***********************************************
C     **
C     **    CALCULATION OF NO. OF COMMUTATIONS
C     **      IN A LINEAR DELTA MODULATED
C     **            INVERTER
C     **
C     ***********************************************
C       ***************************************
C       **
C       **   © RAJIV KUMAR SRIVASTAVA
C       **     DATE: JUNE 21, 1987
C       **
C       ***************************************
C
      PROGRAM LINEAR DELTA MODULATOR
      INTEGER N,NN,M(1000),XO(1000),MO(1000),XO1(1000),MO1(1000)
      INTEGER MX(1000),MX1(1000),XK2(1000),XX(1000)
      INTEGER FMIN,FMAX,FINC,X1(1000)
      REAL X(1000),Y(1000),XK1(1000),OP1(1000),EK1(1000)
      REAL DELTA ,W,DEG,RAD,F,FS,TS,RESISTANCE,CAPACITANCE
      REAL A0,A1,OP,POP,YK,PYK,EK,XK
      OPEN(14,FILE='CDM.DAT',STATUS='NEW')
      PRINT*,'ENTER AMPLITUDE OF INPUT SIN SIGNAL'
      READ*, AMP
      PRINT*, 'ENTER LOWER FREQUENCY LIMIT'
      READ*, FMIN
      PRINT*, 'ENTER UPPER FREQUENCY LIMIT'
      READ*, FMAX
      PRINT*, 'ENTER FREQUENCY INCRIMENT'
      READ*, FINC
      PRINT*,'ENTER DELTA'
      READ*,DELTA
      PI=3.141592654
      DEG=180.0/PI
      RAD=1.0/DEG
      PRINT*, 'ENTER SAMPLING FREQ. IN HZ'
      READ*,FS
      TS=1.0/(FS)
      PRINT*,'  FS=',FS
      PRINT*,'  TS=',TS
      PRINT*,'ENTER THE VALUE OF RESISTANCE IN OHMS'
      READ*,RESISTANCE
      PRINT*,'ENTER THE VALUE OF CAPACITANCE IN MICRO-FARAD'
      READ*,CAPACITANCE
      A0=TS*1E6/(2*RESISTANCE*CAPACITANCE)
      A1=A0
      PRINT*,'A0=',A0,'A1=',A1
      OP=0.0
      POP=0.0
      YK=0.0
      PYK=0.0
      COUNT=1+(FMAX-FMIN)/FINC
```

```
      WRITE(14,*)COUNT
      DO 555 JJ=FMIN,FMAX,FINC
        F=FLOAT(JJ)
        NN=INT(FS/F)
        W=2.0*PI*F

      DO 10 I=1,INT(NN/2)+1,1
        N=I-1
        XK=AMP*SIN(N*W*TS)
        XK1(I)=XK
        XK2(I)=INT(2047*XK1(I))
        IF (XK1(I) .GE. 0.0) THEN
          XX(I) = 1
        ELSE
          XX(I) = -1
        END IF
        EK=XK-OP
        EK1(I)=EK
        OP1(I)=OP
        POP=OP
        IF (EK .GE. 0.0) THEN
          YK=DELTA
        ELSE
          YK='-DELTA
        END IF
        X(I)=N*TS*W*DEG
        Y(I)=YK
        OP=A0*YK+A1*PYK+POP
        PYK = YK
        N=N+1
10      CONTINUE
      DO 12 I=INT(NN/2)+2,NN+1,1
        II = I-1
        N1 = NN+1
        Y(I)= -Y(N1-II)
        X(I)=N*W*TS*DEG
        XK1(I)=-XK1(N1-II)
        XK2(I)=INT(2047*XK1(I))
        IF (XK1(I) .GE. 0.0) THEN
          XX(I) = 1
        ELSE
          XX(I) = -1
        END IF
        EK1(I)=-EK1(N1-II)
        OP1(I)=-OP1(N1-II)
        N = N+1
12      CONTINUE
      NN2 = INT(NN/2)+1
      NN3 = NN+1
      XX(1) = 0.0
      XX(NN2)=0.0
      XX(NN3)=0.0
```

```
      DO 20 I=1,NN+1
       M(I) = INT(Y(I))
20    CONTINUE
      DO 30 I = 1,NN+1
       IF ( XX(I) .GT. 0 ) THEN
         XO(I) = 1
       ELSE
         XO(I) = 0
       END IF
       IF ( M(I) .GE. 0 ) THEN
          MO(I) = 1
        ELSE
          MO(I) = 0
       END IF
30    CONTINUE
      DO 40 I = 1,NN+1
       IF ( XX(I) .GE. 0.0 ) THEN
          XO1(I) = 0
        ELSE
          XO1(I) = 1
       END IF
       IF ( MO(I) .EQ. 1 ) THEN
          MO1(I) = 0
        ELSE
          MO1(I) = 1
       END IF
40    CONTINUE
      DO 50 I = 1,NN+1
       IF ( (XO(I) .EQ. 1) .AND. (MO(I) .EQ. 1 )) THEN
          MX(I) = 1
        ELSE
          MX(I) = 0
       END IF
       IF ( (XO1(I) .EQ. 1) .AND. (MO1(I) .EQ. 1 )) THEN
          MX1(I) = 1
        ELSE
          MX1(I) = 0
       END IF
50    CONTINUE
      N=0
      N1=MX(1)
      DO 60 I=1,NN+1,1
       IF((N1 .NE. MX(I)) .AND. (MX(I) .EQ. 1))  N=N+1
      N1=MX(I)
60    CONTINUE
      N2=0
      N1=MX1(1)
      DO 70 I=1,NN+1,1
       IF((N1 .NE. MX1(I)) .AND. (MX1(I) .EQ. 1))  N2=N2+1
      N1=MX1(I)
70    CONTINUE
      NP=N+N2
C     PRINT*,'NO.OF COMMUTATIONS = ', NP
```

```
      WRITE(14,*) F,NP
      PRINT*,'FREQ = ',F,'N= ',N,'N2= ',N2,'NT = ',NP
555   CONTINUE
      END
```

```
C     ************************************************
C     ************************************************
C     **
C     **    CALCULATION OF NO. OF COMMUTATIONS IN AN
C     **        EXPONENTIAL-DELTA MODULATED
C     **              INVERTER
C     **
C     ************************************************
C        ***************************************
C        **
C        ** © RAJIV KUMAR SRIVASTAVA
C        **     DATE: JUNE 23, 1987
C        **
C        ***************************************
C
C
      PROGRAM EXPONENTIAL DELTA MODULATOR
      INTEGER N,NN,M(1000),XO(1000),MO(1000),XO1(1000),MO1(1000)
      INTEGER MX(1000),MX1(1000),XK2(1000),XX(1000)
      INTEGER FMIN,FMAX,FINC,X1(1000)
      REAL X(1000),Y(1000),XK1(1000),OP1(1000),EK1(1000),T(1000)
      REAL DELTA ,W,DEG,RAD,F,FS,TS,RESISTANCE,CAPACITANCE
      REAL A0,A1,B1,OP,POP,YK,PYK,EK,XK,NUMR
      OPEN(14,FILE='CEXP.DAT',STATUS='NEW')
      PRINT*,'ENTER AMPLITUDE OF INPUT SIN SIGNAL'
      READ*, AMP
      PRINT*, 'ENTER LOWER FREQUENCY LIMIT'
      READ*, FMIN
      PRINT*, 'ENTER UPPER FREQUENCY LIMIT'
      READ*, FMAX
      PRINT*, 'ENTER FREQUENCY INCRIMENT'
      READ*, FINC
      PRINT*,'ENTER DELTA'
      READ*,DELTA
      PI=3.141592654
      DEG=180.0/PI
      RAD=1.0/DEG
      PRINT*, 'ENTER SAMPLING FREQ. IN HZ'
      READ*,FS
      TS=1.0/(FS)
      PRINT*,' FS=',FS
      PRINT*,' TS=',TS
      PRINT*,'ENTER THE VALUE OF RESISTANCE IN OHMS'
      READ*,RESISTANCE
      PRINT*,'ENTER THE VALUE OF CAPACITANCE IN MICRO-FARAD'
      READ*,CAPACITANCE
      NUMR= 1E-6*(2*RESISTANCE*CAPACITANCE)
      A0=TS/(TS+ NUMR)
      A1=A0
      B1=(TS-NUMR)/(TS+ NUMR)
      PRINT*,'A0=',A0,'A1=',A1,' B1=',B1
      OP=0.0
      POP=0.0
```

```
      YK=0.0
      PYK=0.0
      N=0
      COUNT=1+(FMAX-FMIN)/FINC
      WRITE(14,*) COUNT
      DO 555 JJ=FMIN,FMAX,FINC
       F=FLOAT(JJ)
       NN=INT(FS/F)
       W=2.0*PI*F

      DO 10 I=1,INT(NN/2)+1,1
       XK=AMP*SIN(N*W*TS)
       XK1(I)=XK
       XK2(I)=INT(2047*XK1(I))
       IF (XK1(I) .GE. 0.0) THEN
        XX(I) = 1
       ELSE
        XX(I) = -1
       END IF
       EK=XK-OP
       EK1(I)=EK
       OP1(I)=OP
       POP=OP
       IF (EK .GE. 0.0) THEN
        YK=DELTA
       ELSE
        YK= -DELTA
       END IF
       X(I)=N*TS*W*DEG
       T(I)=N*TS
       Y(I)=YK
       OP=A0*YK+A1*PYK-B1*POP
       PYK = YK
       N=N+1
10     CONTINUE

      N1=NN+1
      DO 12 I=INT(NN/2)+2,NN+1,1
        II=I-1
        Y(I)=-Y(N1-II)
        X(I)=N*W*TS*DEG
        XK1(I)=-XK1(N1-II)
        XK2(I)=INT(2047*XK1(I))
        IF (XK1(I) .GE. 0.0) THEN
         XX(I) = 1
        ELSE
         XX(I) = -1
        END IF
        EK1(I)=-EK1(N1-II)
        OP1(I)=-OP1(N1-II)
12     CONTINUE

       NN2 = INT(NN/2)+1
```

```
      NN3 = NN+1
      XX(1) = 0.0
      XX(NN2)=0.0
      XX(NN3)=0.0

      DO 20 I=1,NN+1
       M(I) = INT(Y(I))
20    CONTINUE

      DO 30 I = 1,NN+1
       IF ( XX(I) .GT. 0 ) THEN
         XO(I) = 1
        ELSE
         XO(I) = 0
       END IF
       IF ( M(I) .GE. 0 ) THEN
         MO(I) = 1
        ELSE
         MO(I) = 0
       END IF
30    CONTINUE

      DO 40 I = 1,NN+1
       IF ( XX(I) .GE. 0.0 ) THEN
         XO1(I) = 0
        ELSE
         XO1(I) = 1
       END IF
       IF ( MO(I) .EQ. 1 ) THEN
         MO1(I) = 0
        ELSE
         MO1(I) = 1
       END IF
40    CONTINUE

      DO 50 I = 1,NN+1
       IF ( (XO(I) .EQ. 1) .AND. (MO(I) .EQ. 1 )) THEN
         MX(I) = 1
        ELSE
         MX(I) = 0
       END IF
       IF ( (XO1(I) .EQ. 1) .AND. (MO1(I) .EQ. 1 )) THEN
         MX1(I) = 1
        ELSE
         MX1(I) = 0
       END IF
50    CONTINUE

      N=0
      N1=MX(1)
      DO 60 I=1,NN+1,1
       IF((N1 .NE. MX(I)) .AND. (MX(I) .EQ. 1))  N=N+1
      N1=MX(I)
```

```
60    CONTINUE

      N2=0
      N1=MX1(1)
      DO 70 I=1,NN+1,1
       IF((N1 .NE. MX1(I)) .AND. (MX1(I) .EQ. 1)) N2=N2+1
      N1=MX1(I)
70    CONTINUE

      NP=N+N2
C     PRINT*,'NO.OF COMMUTATIONS = ', NP
      WRITE(14,*) F,NP
      PRINT*,'N= ',N,'N2 =',N2,'FREQ.= ',F,' NP = ',NP
555   CONTINUE
      END
```

```
C     ************************************************
C     ************************************************
C     **
C     **    CALCULATION OF NO. OF COMMUTATIONS
C     **      IN A SIGMA-DELTA MODULATED
C     **            INVERTER
C     **
C     ************************************************
C        ****************************************
C        **
C        ** © RAJIV KUMAR SRIVASTAVA
C        **    DATE: JUNE 23, 1987
C        **
C        ****************************************
C
C
      PROGRAM SIGMA DELTA MODULATOR
      INTEGER FMIN,FMAX,FINC,X1(1000)
      INTEGER N,NN,M(1000),XO(1000),MO(1000),XO1(1000),MO1(1000)
      INTEGER MX(1000),MX1(1000),XK2(1000),XX(1000)
      REAL X(1000),Y(1000),XK1(1000),OP1(1000),EK1(1000),T(1000)
      REAL DELTA ,W,DEG,RAD,F,FS,TS,RESISTANCE,CAPACITANCE
      REAL A0,A1,OP,POP,YK,PYK,EK,XK
      OPEN(14,FILE='CSIGMA.DAT',STATUS='NEW')
      PRINT*,'ENTER AMPLITUDE OF INPUT SIN SIGNAL'
      READ*, AMP
      PRINT*, 'ENTER LOWER FREQUENCY LIMIT'
      READ*, FMIN
      PRINT*, 'ENTER UPPER FREQUENCY LIMIT'
      READ*, FMAX
      PRINT*, 'ENTER FREQUENCY INCRIMENT'
      READ*, FINC
      PRINT*,'ENTER DELTA'
      READ*,DELTA
      PI=3.141592654
      DEG=180.0/PI
      RAD=1.0/DEG
      PRINT*, 'ENTER SAMPLING FREQ. IN HZ'
      READ*,FS
      TS=1.0/(FS)
      PRINT*,'  FS=',FS
      PRINT*,'  TS=',TS
      PRINT*,'ENTER THE VALUE OF RESISTANCE IN OHMS'
      READ*,RESISTANCE
      PRINT*,'ENTER THE VALUE OF CAPACITANCE IN MICRO-FARAD'
      READ*,CAPACITANCE
      A0=TS*1E6/(2*RESISTANCE*CAPACITANCE)
      A1=A0
      PRINT*,'  A0=',A0,'A1=',A1
      OP=0.0
      POP=0.0
      YK=0.0
      EK=0.0
```

```
      PEK=0.0
      N=0
      COUNT=1+(FMAX-FMIN)/FINC
      WRITE(14,*) COUNT

      DO 555 JJ=FMIN,FMAX,FINC
       F=FLOAT(JJ)
       NN=INT(FS/F)
       W=2.0*PI*F
      DO 10 I=1,INT(NN/2)+1,1
      N=I-1
       XK=AMP*SIN(N*W*TS)
       XK1(I)=XK
       XK2(I)=INT(2047*XK1(I))
       IF (XK1(I) .GE. 0.0) THEN
        XX(I) = 1
       ELSE
        XX(I) = -1
       END IF
      EK=XK-YK
       EK1(I)=EK
       OP=A0*EK+A1*PEK+POP
       OP1(I)=OP
       IF (OP .GE. 0.0) THEN
        YK=DELTA
       ELSE
        YK= -DELTA
       END IF
       X(I)=N*TS*W*DEG
      T(I)=N*TS
       Y(I)=YK
       POP=OP
       PEK = EK
       N=N+1
10     CONTINUE

      DO 12 I=INT(NN/2)+2,NN+1,1
       II = I-1
       N1 = NN+1
       Y(I)= -Y(N1-II)
       X(I)=N*W*TS*DEG
       T(I)=N*TS
       XK1(I)=-XK1(N1-II)
       EK1(I)=-EK1(N1-II)
       OP1(I)=-OP1(N1-II)
       XK2(I)=INT(2047*XK1(I))
       IF (XK1(I) .GE. 0.0) THEN
        XX(I) = 1
       ELSE
        XX(I) = -1
       END IF
      N = N+1
12     CONTINUE
```

```
      NN2 = INT(NN/2)+1
      NN3 = NN+1
      XX(1) = 0.0
      XX(NN2)=0.0
      XX(NN3)=0.0

      DO 20 I=1;NN+1
       M(I) = INT(Y(I))
20    CONTINUE

      DO 30 I = 1;NN+1
       IF ( XX(I) .GT. 0 ) THEN
         XO(I) = 1
        ELSE
         XO(I) = 0
       END IF
       IF ( M(I) .GE. 0 ) THEN
         MO(I) = 1
        ELSE
         MO(I) = 0
       END IF
30    CONTINUE

      DO 40 I = 1,NN+1
       IF ( XX(I) .GE. 0.0 ) THEN
         XO1(I) = 0
        ELSE
         XO1(I) = 1
       END IF
       IF ( MO(I) .EQ.-1 ) THEN
         MO1(I) = 0
        ELSE
         MO1(I) = 1
       END IF
40    CONTINUE

      DO 50 I = 1,NN+1
       IF ( (XO(I) .EQ. 1) .AND. (MO(I) .EQ. 1 )) THEN
         MX(I) = 1
        ELSE
         MX(I) = 0
       END IF
       IF ( (XO1(I) .EQ. 1) .AND. (MO1(I) .EQ. 1 )) THEN
         MX1(I) = 1
        ELSE
         MX1(I) = 0
       END IF
50    CONTINUE

      N=0
      N1=MX(1)
      DO 60 I=1,NN+1,1
      IF((N1 .NE. MX(I)) .AND. (MX(I) .EQ. 1))  N=N+1
```

```
      N1=MX(1)
60     CONTINUE

      N2=0
      N1=MX1(1)
      DO 70 I=1,NN+1,1
       IF((N1 .NE. MX1(I)) .AND. (MX1(I) .EQ. 1)) N2=N2+1
      N1=MX1(I)
70     CONTINUE

      NP=N+N2
C     PRINT*,'NO. OF COMMUTATIONS = ',NP
      WRITE(14,*)F,NP
      PRINT*,'N= ',N,'N2= ',N2,' FREQ.= ',F,' NP = ',NP
555    CONTINUE
      END
```

```
C     ****************************************
C     ****************************************
C     **
C     **       FOURIER SERIES ANALYSIS
C     **         OF THE OUTPUT WAVEFORM
C     **              OF A
C     **         LINEAR-DELTA MODULATOR
C     **
C     ****************************************
C     ****************************************
C       **********************************
C       ** © RAJIV KUMAR SRIVASTAVA
C       **    DATE JULY 2, 1987
C       **********************************
C This program analyses the output waveforms of a LINEAR DELTA
C MODULATOR using FOURIER SERIES ANALYSIS method.
C
      PROGRAM DELTA MODULATOR
      INTEGER N,N1,N2,N3,NN,YC,YD,K,NW,IWK(2000),Z1(1000)
      REAL X(1000),Y(1000),XK1(1000),OP1(1000),EK1(1000),T(1000)
      REAL ASUM,BSUM,AK,BK,A1SUM(5000),B1SUM(5000),VO(500),YO(5000)
      REAL DELTA ,W,DEG,RAD,F,FS,TS,RESISTANCE,CAPACITANCE,DD(300)
      REAL A0,A1,OP,POP,YK,PYK,EK,XK,D1,KK,Z(1000),XK4(1000),WK(2000)
      REAL VH(1000)
      COMPLEX Q(1000),P(1000),XK2(1000),XK3(1000),Q1(1000)
      OPEN(11,FILE='SPECTRADM.DAT',STATUS='NEW')
      OPEN(14,FILE='FFTDM.DAT',STATUS='NEW')
      OPEN(15,FILE='FFTSIN.DAT',STATUS='NEW')
      PRINT*,'ENTER AMPLITUDE OF INPUT SIN SIGNAL'
      READ*,AMP
      PRINT*, 'ENTER THE FREQ. OF INPUT SINE SIGNAL IN HZ'
      READ*, F
      PRINT*,'ENTER DELTA'
      READ*,DELTA
      PI=3.141592654
      W=2.0*PI*F
      DEG=180.0/PI
      RAD=1.0/DEG
      PRINT*, 'ENTER SAMPLING FREQ. IN HZ'
      READ*,FS
      NN=INT(FS/F)
      TS=1.0/(FS)
      PRINT*, 'F= ',F, ' FS=',FS
      PRINT*,'NN=',NN, ' TS=',TS
      PRINT*,'ENTER THE VALUE OF RESISTANCE IN OHMS'
      READ*,RESISTANCE
      PRINT*,'ENTER THE VALUE OF CAPACITANCE IN MICRO-FARAD'
      READ*,CAPACITANCE
      A0=TS*1E6/(2*RESISTANCE*CAPACITANCE)
      A1=A0
      PRINT*,'A0=',A0,'A1=',A1
      WRITE(11,3)F,FS
3     FORMAT(2X,'INPUT FREQUENCY=',F6.2,2X,'SAMPLING FREQUENCY=',F8.2)
```

```
      WRITE(11,4)NN,TS
4     FORMAT(2X,'NO. OF POINTS=',I4,2X,'SAMPLING INTERVAL=',F8.5)
      WRITE(11,5)RESISTANCE,CAPACITANCE
5     FORMAT(2X,'RESISTANCE =',F8.2,2X,'CAPACITANCE =',F16.8)
      WRITE(11,*)' COEF-A0 = ',A0,'COEF-A1 = ',A1
      OP=0.0
      POP=0.0
      YK=0.0
      PYK=0.0
      N=0
      WRITE(11,7)'I','X(I)','XK1(I)','EK1(I)','OP1(I)','Y(I)','T(I)'
7     FORMAT(A5,2X,A10,2X,A10,2X,A10,2X,A10,2X,A10,2X,A10,2X,A10)
C
      DO 10 I=1,INT(NN/2)+1,1
       N=I-1
       XK=AMP*SIN(N*W*TS)
       XK1(I)=XK
       EK=XK-OP
       EK1(I)=EK
       OP1(I)=OP
       POP=OP
       IF (EK .GE. 0.0) THEN
        YK=DELTA
       ELSE
        YK= -DELTA
       END IF
       X(I)=N*TS*W*DEG
       T(I)=N*TS
       Y(I)=YK
       OP=A0*YK+A1*PYK+POP
       PYK = YK
       N=N+1
       WRITE(11,8)I,X(I),XK1(I),EK1(I),OP1(I),Y(I),T(I)
8      FORMAT(I5,4(2X,F10.4),2X,F10.2,2X,F10.6)
10    CONTINUE
C
      DO 12 I=INT(NN/2)+2,NN+1,1
       II = I-1
       N1 = NN+1
       Y(I)= -Y(N1-II)
       X(I)=N*W*TS*DEG
       XK1(I)=-XK1(N1-II)
       EK1(I)=-EK1(N1-II)
       OP1(I)=-OP1(N1-II)
       WRITE(11,9)I,X(I),XK1(I),EK1(I),OP1(I),Y(I),T(I)
9      FORMAT(I5,4(2X,F10.4),2X,F10.2,2X,F10.6)
       N = N+1
12    CONTINUE
C
C     ************************************
C     **      HARMONIC ANALYSIS
C     ************************************
C
```

```
      N=1
      DD(N)=0.0
      IF (Y(1) .GE. 0.) THEN
        YC = 1.
      ELSE
        YC = -1.
      END IF
      DO 100 I=1,NN+1
        IF (Y(I) .GE. 0.) THEN
          YD=1.
        ELSE
          YD=-1.
        END IF
        IF (YD.NE.YC) THEN
          N=N+1
          DD(N)=(I-1)*TS*W
        END IF
        IF ( DD(N) .GE. 3.14159) DD(N) = PI
        YC = YD
      WRITE(11,90)I,Y(I),N,DD(N)
90    FORMAT(2X,I5,F6.2,2X,I5,F10.6)
100   CONTINUE
C
      D1=DD(1)
      DO 200 I=2,N
        IF ( (DD(I)-D1) .LE. 0.0001) THEN
          K=I-1
          GOTO 210
        END IF
        D1 = DD(I)
200   CONTINUE
210   N=K
C
      DO 300 I=1,N
C       PRINT*, I,DD(I)
        WRITE(11,290) I,DD(I)
290   FORMAT(2X,I5,F10.6)
300   CONTINUE
C
C       ************************************
C       **  COMPUTE F.S. COEFFICIENTS
C       ************************************
C
      AMPP= 2*DELTA/PI
C     FIRST COEF.(DC COMPONENT) is 0
      NW = 100
      VH(1) = 0.0
      Z1(1) = 0
C
      DO 400 K=1,NW,1
        KK=K+1
        ASUM=0.0
        BSUM=0.0
```

```
      DO 500 I=2,2*N,1
        AK=(-1)**(I+1)*(SIN(K*DD(I))-SIN(K*DD(I-1)))
        BK=(-1)**(I+1)*(COS(K*DD(I-1))-COS(K*DD(I)))
        ASUM=ASUM+AK
        BSUM=BSUM+BK
500     CONTINUE
      A1SUM(K)=ASUM
      B1SUM(K)=BSUM
      VO(K)=AMPP*SQRT(A1SUM(K)**2+B1SUM(K)**2)/K
      VH(KK)=VO(K)
      Z1(KK) =K
400   CONTINUE

    AMP1=VH(2)
C*************************************************************
C**     SUBROUTINE CALL TO PLOT HARMONIC CONTENT
C*************************************************************

      CALL HPLOT(Z1,VH,NW,DELTA,AMP1,F,FS,A0,B1)

C*************************************************************
C**          PERFORM FFT ON DM OUTPUT
C*************************************************************

    N1=NN+1
    WRITE(14,*) N1
    WRITE(15,*) N1
    DO 600 I=1,N1,1
      Q(I)=CMPLX(Y(I))
      XK2(I)=CMPLX(XK1(I))
600   CONTINUE
    CALL FFTCF(N1,Q,Q1)
    CALL FFTCF(N1,XK2,XK3)
    X(1)=-F
    N3=INT(N1/2)+1
    X(N3)=0.0
    XINC=(2*F)/NN
C
    DO 610 I=2,INT(N1/2),1
      X(I)=X(1)+(I-1)*XINC
610   CONTINUE
C
      I1=0
    DO 620 I=INT(N1/2)+2,N1,1
      I1=I1+1
      X(I)=X(N3)+I1*XINC
C       PRINT*,I,X(I)
620   CONTINUE
    Q(N3)=Q1(1)
    XK2(N3)=XK3(1)
    DO 640 I=1,INT(N1/2),1
      XK2(I)=XK3(I+1)
      Q(I)=Q1(I+1)
```

```
640  CONTINUE
     DO 650 I=INT(N1/2)+2,N1,1
       XK2(I)=XK3(I)
       Q(I)=Q1(I)
650  CONTINUE
     DO 660 I=1,N1,1
       XK2(I)=XK2(I)*CONJG(XK2(I))
       Q(I)=Q(I)*CONJG(Q(I))
660  CONTINUE
     DO 700 I=1,N1,1
       Z(I)=CABS(Q(I))
       XK4(I)=CABS(XK2(I))
       WRITE(14,*)X(I),Z(I)
       WRITE(15,*)X(I),XK4(I)
700  CONTINUE
     END
C*************************************************************
     SUBROUTINE HPLOT(Z1,VH,N,DELTA,AMP1,F,FS,A0,B1)
C*************************************************************
     REAL VH(1),VH1(1000)
     INTEGER N,Z1(1)
     XINC=6./N
     CALL PLOTS(53,0,-1)
     CALL ZPICK(3,0,ISTAT)
     CALL ORIGIN(2.5,7.,0)
     CALL FACTOR(0.7)
     DELVAL=Z1(2)*N/6.
     VINC=1.25/5
     TINC = 1.0
     ASP = 1.0
     SZN = 0.1
     SZL = 0.12
     CALL HALAB2(0.,0.,0.,DELVAL,TINC,1,6.,1,SZN,ASP,1,-1,
    +          SZL,' ORDER OF HARMONIC ( N ) -----')
     CALL VALAB2(0.,0.,0.0,VINC,TINC,1,5.,1,SZN,ASP,1,1,YP,
    +          SZL,'          AMPLITUDE ( P.U. )')
C
C       ***************************************
C       **    PLOT FOURIER COMPONENTS
C       ***************************************
     DO 800 I=1,N+1
       VH1(I)= VH(I)/(VINC*VH(2))
800  CONTINUE
     DO 1000 I=1,N+1
       XD=(I-1)*XINC
       CALL PLOT(XD,VH1(I),3)
       CALL PLOT(XD,0.,2)
1000  continue
     CALL PLOT(0.,0.,3)
C
     CALL SYMB2(-0.4,-1.8,.15,'Coef_A0 = ',0.0,1)
     IF (A0.LT.1.0) CALL TYPNUM(999.,999.,.15,0.0,0.0,-1)
     CALL TYPNUM(999.,999.,.15,A0,0.0,3)
```

```
C
      CALL SYMB2(4.05,-1.8,.15,'Delta = ',0.0,1)
      IF (DELTA.LT.1.0) CALL TYPNUM(999.,999.,.15,0.0,0.0,-1)
      CALL TYPNUM(999.,999.,.15,DELTA,0.0,1)
C
      CALL SYMB2(3.23,-1.5,.15,'Samp. Freq. = ',0.0,1)
      CALL TYPNUM(999.,999.,.15,FS,0.0,1)
      CALL SYMB2(999.,999.,.15,' HZ',0.0,0)
C
      CALL SYMB2(-0.88,-1.5,.15,'Input Freq. = ',0.0,1)
      CALL TYPNUM(999.,999.,.15,F,0.0,1)
      CALL SYMB2(999.,999.,.15,' HZ',0.0,0)
C
      CALL PLOT(0.,0.,999)
      return
      end
```

```
C     ********************************************
C     ********************************************
C     **
C     **      FOURIER SERIES ANALYSIS
C     **        OF THE OUTPUT WAVEFORM
C     **              OF AN
C     **     EXPONENTIAL-DELTA MODULATOR
C     **
C     ********************************************
C     ********************************************
C       ***********************************
C       ** © RAJIV KUMAR SRIVASTAVA
C       **      DATE JULY 28, 1987
C       ***********************************
C This program analyses the output waveforms of an EXPONENTIAL
C DELTA MODULATOR using FOURIER SERIES ANALYSIS method.
C
      PROGRAM EXPONENTIAL DELTA MODULATOR
      INTEGER N,N1,N2,N3,NN,YC,YD,K,NW,IWK(2000),Z1(1000)
      REAL X(1000),Y(1000),XK1(1000),OP1(1000),EK1(1000),T(1000)
      REAL ASUM,BSUM,AK,BK,A1SUM(5000),B1SUM(5000),VO(500),YO(5000)
      REAL DELTA,W,DEG,RAD,F,FS,TS,RESISTANCE,CAPACITANCE,DD(300)
      REAL A0,A1,OP,POP,YK,PYK,EK,XK,D1,KK,Z(1000),XK4(1000),WK(2000)
      REAL VH(1000),B1,NUMR
      COMPLEX Q(1000),P(1000),XK2(1000),XK3(1000),Q1(1000)
      OPEN(11,FILE='SPECTRAEXP.DAT',STATUS='NEW')
      OPEN(14,FILE='FFTEXP.DAT',STATUS='NEW')
      OPEN(15,FILE='FFTSIN.DAT',STATUS='NEW')
      PRINT*,'ENTER AMPLITUDE OF INPUT SIN SIGNAL'
      READ*, AMP
      PRINT*, 'ENTER THE FREQ. OF INPUT SINE SIGNAL IN HZ'
      READ*, F
      PRINT*,'ENTER DELTA'
      READ*,DELTA
      PI=3.141592654
      W=2.0*PI*F
      DEG=180.0/PI
      RAD=1.0/DEG
      PRINT*, 'ENTER SAMPLING FREQ. IN HZ'
      READ*,FS
      NN=INT(FS/F)
      TS=1.0/(FS)
      PRINT*, 'F= ',F,'  FS=',FS
      PRINT*,'NN=',NN,'  TS=',TS
      PRINT*,'ENTER THE VALUE OF RESISTANCE IN OHMS'
      READ*,RESISTANCE
      PRINT*,'ENTER THE VALUE OF CAPACITANCE IN MICRO-FARAD'
      READ*,CAPACITANCE
      NUMR= 1E-6*(2*RESISTANCE*CAPACITANCE)
      A0=TS/(TS+NUMR)
      A1=A0
      B1=(TS-NUMR)/(TS+NUMR)
      PRINT*,'A0=',A0,'A1=',A1,'B1=',B1
```

```
      WRITE(11,3)F,FS
3     FORMAT(2X,'INPUT FREQUENCY=',F6.2,2X,'SAMPLING FREQUENCY=',F8.2)
      WRITE(11,4)NN,TS
4     FORMAT(2X,'NO. OF POINTS=',I4,2X,'SAMPLING INTERVAL=',F8.5)
      WRITE(11,5)RESISTANCE,CAPACITANCE
5     FORMAT(2X,'RESISTANCE =',F8.2,2X,'CAPACITANCE =',F16.8)
      WRITE(11,*)'  COEF-A0 & A1 = ',A0,'COEF-B1 = ',B1
      OP=0.0
      POP=0.0
      YK=0.0
      PYK=0.0
      N=0
C     PRINT*,'I','    XX   ','     XK   ','    OP1(I)  ',' Y(I)  '
      WRITE(11,7)'I','X(I)','XK1(I)','EK1(I)','OP1(I)','Y(I)','T(I)'
7     FORMAT(A5,2X,A10,2X,A10,2X,A10,2X,A10,2X,A10,2X,A10)
      DO 10 I=1,INT(NN/2)+1,1
       XK=AMP*SIN(N*W*TS)
       XK1(I)=XK
       EK=XK-OP
       EK1(I)=EK
       OP1(I)=OP
       POP=OP
       IF (EK .GE. 0.0) THEN
        YK=DELTA
       ELSE
        YK=-DELTA
       END IF
       X(I)=N*TS*W*DEG
       T(I)=N*TS
       Y(I)=YK
       OP=A0*YK+A1*PYK-B1*POP
       PYK = YK
       N=N+1
       WRITE(11,8)I,X(I),XK1(I),EK1(I),OP1(I),Y(I),T(I)
8      FORMAT(I5,4(2X,F10.4),2X,F10.2,2X,F10.6)
10    CONTINUE
      N1=NN+1
      DO 12 I=INT(NN/2)+2,NN+1,1
         II=I-1
         Y(I)=-Y(N1-II)
         X(I)=N*W*TS*DEG
         XK1(I)=-XK1(N1-II)
         EK1(I)=-EK1(N1-II)
         OP1(I)=-OP1(N1-II)
         WRITE(11,9)I,X(I),XK1(I),EK1(I),OP1(I),Y(I),T(I)
9        FORMAT(I5,4(2X,F10.4),2X,F10.2,2X,F10.6)
12    CONTINUE
C     ************************************
C     **      HARMONIC ANALYSIS
C     ************************************
      N=1
      DD(N)=0.0
      IF (Y(1) .GE. 0.) THEN
```

```
        YC = 1.
      ELSE
        YC = -1.
      END IF
      DO 100 I=1,NN+1
       IF (Y(I) .GE. 0.) THEN
        YD=1.
       ELSE
        YD=-1.
       END IF
       IF (YD.NE.YC) THEN
        N=N+1
        DD(N)=(I-1)*TS*W
       END IF
       IF ( DD(N) .GE. 3.14159) DD(N) = PI
       YC = YD
      WRITE(11,90)I,Y(I),N,DD(N)
90    FORMAT(2X,I5,F6.2,2X,I5,F10.6)
100   CONTINUE
      D1=DD(1)
      DO 200 I=2,N
       IF ( (DD(I)-D1) .LE. 0.0001) THEN
        K=I-1
        GOTO 210
       END IF
       D1 = DD(I)
200   CONTINUE
210   N=K
      DO 300 I=1,N
C       PRINT*, I,DD(I)
       WRITE(11,290) I,DD(I)
290    FORMAT(2X,I5,F10.6)
300    CONTINUE
C       ****************************************
C       **      FOURIER SERIES ANALYSIS
C       ****************************************
      AMPP= 2*DELTA/PI
C     FIRST COEF.(DC COMPONENT) is 0
      NW = 100
      VH(1) = 0.0
      Z1(1)  = 0
      DO 400 K=1,NW,1
       KK=K+1
       ASUM=0.0
       BSUM=0.0
       DO 500 I=2,2*N,1
        AK=(-1)**(I+1)*(SIN(K*DD(I))-SIN(K*DD(I-1)))
        BK=(-1)**(I+1)*(COS(K*DD(I-1))-COS(K*DD(I)))
        ASUM=ASUM+AK
        BSUM=BSUM+BK
500    CONTINUE
       A1SUM(K)=ASUM
       B1SUM(K)=BSUM
```

```
      VO(K)=AMPP*SQRT(A1SUM(K)**2+ B1SUM(K)**2)/K
      VH(KK)=VO(K)
      Z1(KK) =K
400   CONTINUE
     AMP1=VH(2)
C*****************************************************
C**     SUBROUTINE CALL TO PLOT HARMONIC CONTENT
C*****************************************************
      CALL HPLOT(Z1,VH,NW,DELTA,AMP1,F,FS,A0,B1)
C*****************************************************
C**          PERFORM FFT ON DM OUTPUT
C*****************************************************
     N1=NN+1
     WRITE(14,*) N1
     WRITE(15,*) N1
     DO 600 I=1,N1,1
       Q(I)=CMPLX(Y(I))
       XK2(I)=CMPLX(XK1(I))
600   CONTINUE
     CALL FFTCF(N1,Q,Q1)
     CALL FFTCF(N1,XK2,XK3)
      X(1)=-F
      N3=INT(N1/2)+1
      X(N3)=0.0
     XINC=(2*F)/NN
C     PRINT*,XINC
      DO 610 I=2,INT(N1/2),1
        X(I)=X(1)+(I-1)*XINC
C       PRINT*,I,X(I)
610   CONTINUE
       I1=0
     DO 620 I=INT(N1/2)+2,N1,1
       I1=I1+1
       X(I)=X(N3)+I1*XINC
C      PRINT*,I,X(I)
620   CONTINUE
     Q(N3)=Q1(1)
     XK2(N3)=XK3(1)
     DO 640 I=1,INT(N1/2),1
       XK2(I)=XK3(I+1)
       Q(I)=Q1(I+1)
640   CONTINUE
     DO 650 I=INT(N1/2)+2,N1,1
       XK2(I)=XK3(I)
       Q(I)=Q1(I)
650   CONTINUE
     DO 660 I=1,N1,1
       XK2(I)=XK2(I)*CONJG(XK2(I))
       Q(I)=Q(I)*CONJG(Q(I))
660   CONTINUE
     DO 700 I=1,N1,1
C      PRINT*, 'I=',I,'XK2(I)=',XK2(I),'Q(I)=',Q(I)
       Z(I)=CABS(Q(I))
```

```
      XK4(I)=CABS(XK2(I))
      WRITE(14,*)X(I),Z(I)
      WRITE(15,*)X(I),XK4(I)
C       PRINT*, 'I= ',I,'X(I)= ',X(I),' Z(I)=',Z(I)
700   CONTINUE
      END
C*************************************************************
      SUBROUTINE HPLOT(Z1,VH,N,DELTA,AMP1,F,FS,A0,B1)
C*************************************************************
      REAL VH(1),VH1(1000)
      INTEGER N,Z1(1)
      XINC=6./N
      CALL PLOTS(53,0,-1)
      CALL ZPICK(3,0,ISTAT)
      CALL ORIGIN(2.5,7.,0)
      CALL FACTOR(0.7)
      DELVAL=Z1(2)*N/6.
      VINC=1.25/5
      TINC = 1.0
      ASP = 1.0
      SZN = 0.1
      SZL = 0.12
      CALL HALAB2(0.,0.,0.,DELVAL,TINC,1,6.,1,SZN,ASP,1,-1,
     +          SZL,' ORDER OF HARMONIC ( N ) -----')
      CALL VALAB2(0.,0.,0.0,VINC,TINC,1,5.,1,SZN,ASP,1,1,YP,
     +          SZL,'          AMPLITUDE ( P.U. )')
C
C       ************************************
C       **    PLOT FOURIER COMPONENTS
C       ************************************
      DO 800 I=1,N+1
        VH1(I)= VH(I)/(VINC*VH(2))
800   CONTINUE
      DO 1000 I=1,N+1
        XD=(I-1)*XINC
        CALL PLOT(XD,VH1(I),3)
        CALL PLOT(XD,0.,2)
1000    continue
      CALL PLOT(0.,0.,3)
C
      CALL SYMB2(-0.4,-1.8,.15,'Coef_A0 = ',0.0,1)
      IF (A0.LT.1.0) CALL TYPNUM(999.,999.,.15,0.0,0.0,-1)
      CALL TYPNUM(999.,999.,.15,A0,0.0,3)
C
      CALL SYMB2(1.8,-1.8,.15,'Coef_B1 = ',0.0,1)
      CALL TYPNUM(999.,999.,.15,B1,0.0,3)
C
      CALL SYMB2(4.05,-1.8,.15,'Delta = ',0.0,1)
      IF (DELTA.LT.1.0) CALL TYPNUM(999.,999.,.15,0.0,0.0,-1)
      CALL TYPNUM(999.,999.,.15,DELTA,0.0,1)
C
      CALL SYMB2(3.23,-1.5,.15,'Samp. Freq. = ',0.0,1)
      CALL TYPNUM(999.,999.,.15,FS,0.0,1)
```

```
      CALL SYMB2(999.,999.,.15,' HZ',0.0,0)
C
      CALL SYMB2(-0.88,-1.5,.15,'Input Freq. = ',0.0,1)
      CALL TYPNUM(999.,999.,.15,F,0.0,1)
      CALL SYMB2(999.,999.,.15,' HZ',0.0,0)
C
      CALL PLOT(0.,0.,999)
      return
      end
```

```
C     ******************************************
C     ******************************************
C     **
C     **      FOURIER SERIES ANALYSIS
C     **       OF THE OUTPUT WAVEFORM
C     **           OF A
C     **       SIGMA-DELTA MODULATOR
C     **
C     ******************************************
C     ******************************************
C       **********************************
C       ** (C) RAJIV KUMAR SRIVASTAVA
C       **     DATE JULY 28, 1987
C       **********************************
C This program analyses the output waveforms of a SIGMA DELTA
C MODULATOR using FOURIER SERIES ANALYSIS method.
C
      PROGRAM SIGMA DELTA MODULATOR
      INTEGER N,N1,N2,N3,NN,YC,YD,K,NW,IWK(2000),Z1(1000),XX(1000)
      REAL X(1000),Y(1000),XK1(1000),OP1(1000),EK1(1000),T(1000)
      REAL ASUM,BSUM,AK,BK,A1SUM(5000),B1SUM(5000),VO(500),YO(5000)
      REAL DELTA ,W,DEG,RAD,F,FS,TS,RESISTANCE,CAPACITANCE,DD(300)
      REAL A0,A1,OP,POP,YK,PYK,EK,XK,D1,KK,Z(1000),XK4(1000),WK(2000)
      REAL VH(1000)
      COMPLEX Q(1000),P(1000),XK2(1000),XK3(1000),Q1(1000)
      OPEN(11,FILE='SPECTSIGMA.DAT',STATUS='NEW')
      OPEN(14,FILE='FFTSIGMA.DAT',STATUS='NEW')
      OPEN(15,FILE='FFTSIN.DAT',STATUS='NEW')
      PRINT*,'ENTER AMPLITUDE OF INPUT SIN SIGNAL'
      READ*, AMP
      PRINT*, 'ENTER THE FREQ. OF INPUT SINE SIGNAL IN HZ'
      READ*, F
      PRINT*,'ENTER DELTA'
      READ*,DELTA
      PI=3.141592654
      W=2.0*PI*F
      DEG=180.0/PI
      RAD=1.0/DEG
      PRINT*, 'ENTER SAMPLING FREQ. IN HZ'
      READ*,FS
      NN=INT(FS/F)
      TS=1.0/(FS)
      PRINT*, 'F= ',F, '  FS=',FS
      PRINT*,'NN=',NN, '  TS=',TS
      PRINT*,'ENTER THE VALUE OF RESISTANCE IN OHMS'
      READ*,RESISTANCE
      PRINT*,'ENTER THE VALUE OF CAPACITANCE IN MICRO-FARAD'
      READ*,CAPACITANCE
      A0=TS*1E6/(2*RESISTANCE*CAPACITANCE)
      A1=A0
      PRINT*,'  A0=',A0,'A1=',A1
      WRITE(11,3)F,FS
3     FORMAT(2X,'INPUT FREQUENCY=',F6.2,2X,'SAMPLING FREQUENCY=',F8.2)
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      WRITE(11,4)NN,TS
4     FORMAT(2X,'NO. OF POINTS=',I4,2X,'SAMPLING INTERVAL=',F8.5)
      WRITE(11,5)RESISTANCE,CAPACITANCE
5     FORMAT(2X,'RESISTANCE =',F8.2,2X,'CAPACITANCE =',F16.8)
      WRITE(11,*)' COEF-A0 = ',A0,' COEF-A1 = ',A1
      OP=0.0
      POP=0.0
      YK=0.0
      EK=0.0
      PEK=0.0
C     PRINT*,'I',' XX ',' XK ',' OP1(I) ',' Y(I) '
      WRITE(11,7)'I','X(I)','XK1(I)','EK1(I)','OP1(I)','Y(I)','T(I)'
7     FORMAT(A5,2X,A10,2X,A10,2X,A10,2X,A10,2X,A10,2X,A10)
      DO 10 I=1,INT(NN/2)+1,1
       N=I-1
       XK=AMP*SIN(N*W*TS)
       XK1(I)=XK
       XK2(I)=INT(2047*XK1(I))
       IF (XK1(I) .GE. 0.0) THEN
        XX(I) = 1
       ELSE
        XX(I) = -1
       END IF
       EK=XK-YK
       EK1(I)=EK
       OP=A0*EK+A1*PEK+POP
       OP1(I)=OP
       IF (OP .GE. 0.0) THEN
        YK=DELTA
       ELSE
        YK= -DELTA
       END IF
       X(I)=N*TS*W*DEG
       T(I)=N*TS
       Y(I)=YK
       POP=OP
       PEK = EK
       N=N+1
C      PRINT*,I,X(I),XK1(I),EK1(I),OP1(I),Y(I)
       WRITE(11,8)I,X(I),XK1(I),EK1(I),OP1(I),Y(I),T(I)
8      FORMAT(I5,4(2X,F10.4),2X,F10.2,2X,F10.6)
10    CONTINUE
      DO 12 I=INT(NN/2)+2,NN+1,1
       II = I-1
       N1 = NN+1
       Y(I)= -Y(N1-II)
       X(I)=N*W*TS*DEG
       T(I)=N*TS
       XK1(I)=-XK1(N1-II)
       EK1(I)=-EK1(N1-II)
       OP1(I)=-OP1(N1-II)
       XK2(I)=INT(2047*XK1(I))
       IF (XK1(I) .GE. 0.0) THEN
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          XX(I) = 1
         ELSE
          XX(I) = -1
         END IF
C        PRINT*,I,N,X(I),XK1(I),EK1(I),OP1(I),Y(I)
         WRITE(11,9)I,X(I),XK1(I),EK1(I),OP1(I),Y(I),T(I)
9        FORMAT(I5,4(2X,F10.4),2X,F10.2,2X,F10.6)
         N = N+1
12       CONTINUE
C         ************************************
C         **      HARMONIC ANALYSIS
C         ************************************
       N=1
       DD(N)=0.0
       IF (Y(1) .GE. 0.) THEN
         YC = 1.
       ELSE
         YC = -1.
       END IF
       DO 100 I=1,NN+1
         IF (Y(I) .GE. 0.) THEN
          YD=1.
         ELSE
          YD=-1.
         END IF
         IF (YD.NE.YC) THEN
          N=N+1
          DD(N)=(I-1)*TS*W
         END IF
         IF ( DD(N) .GE. 3.14159) DD(N) = PI
         YC = YD
       WRITE(11,90)I,Y(I),N,DD(N)
90     FORMAT(2X,I5,F6.2,2X,I5,F10.6)
100    CONTINUE
       D1=DD(1)
       DO 200 I=2,N
         IF ( (DD(I)-D1) .LE. 0.0001) THEN
          K=I-1
          GOTO 210
         END IF
         D1 = DD(I)
200    CONTINUE
210    N=K
       DO 300 I=1,N
C        PRINT*, I,DD(I)
         WRITE(11,290) I,DD(I)
290    FORMAT(2X,I5,F10.6)
300    CONTINUE
C         ****************************************
C         **      FOURIER SERIES ANALYSIS
C         ****************************************
       AMPP=2*DELTA/PI
C      FIRST COEF.(DC COMPONENT) is 0
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      NW = 100
      VH(1) = 0.0
      Z1(1)  = 0
      DO 400 K=1,NW,1
        KK=K+1
        ASUM=0.0
        BSUM=0.0
        DO 500 I=2,2*N,1
          AK=(-1)**(I+1)*(SIN(K*DD(I))-SIN(K*DD(I-1)))
          BK=(-1)**(I+1)*(COS(K*DD(I-1))-COS(K*DD(I)))
          ASUM=ASUM+AK
          BSUM=BSUM+BK
500     CONTINUE
        A1SUM(K)=ASUM
        B1SUM(K)=BSUM
        VO(K)=AMPP*SQRT(A1SUM(K)**2+B1SUM(K)**2)/K
        VH(KK)=VO(K)
        Z1(KK) =K
400   CONTINUE
      AMP1=VH(2)
C*********************************************************
C**     SUBROUTINE CALL TO PLOT HARMONIC CONTENT
C*********************************************************
      CALL HPLOT(Z1,VH,NW,DELTA,AMP1,F,FS,A0,B1)
C*********************************************************
C**          PERFORM FFT ON DM OUTPUT
C*********************************************************
      N1=NN+1
      WRITE(14;*) N1
      WRITE(15,*) N1
      DO 600 I=1,N1,1
        Q(I)=CMPLX(Y(I))
        XK2(I)=CMPLX(XK1(I))
600   CONTINUE
      CALL FFTCF(N1,Q,Q1)
      CALL FFTCF(N1,XK2,XK3)
      X(1)=-F
      N3=INT(N1/2)+1
      X(N3)=0.0
      XINC=(2*F)/NN
      DO 610 I=2,INT(N1/2),1
        X(I)=X(1)+(I-1)*XINC
610   CONTINUE
      I1=0
      DO 620 I=INT(N1/2)+2,N1,1
        I1=I1+1
        X(I)=X(N3)+I1*XINC
620   CONTINUE
      Q(N3)=Q1(1)
      XK2(N3)=XK3(1)
      DO 640 I=1,INT(N1/2),1
        XK2(I)=XK3(I+1)
        Q(I)=Q1(I+1).
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640   CONTINUE
      DO 650 I=INT(N1/2)+2,N1,1
        XK2(I)=XK3(I)
        Q(I)=Q1(I)
650   CONTINUE
      DO 660 I=1,N1,1
        XK2(I)=XK2(I)*CONJG(XK2(I))
        Q(I)=Q(I)*CONJG(Q(I))
660   CONTINUE
      DO 700 I=1,N1,1
C       PRINT*, 'I=',I,'XK2(I)=',XK2(I),'Q(I)=',Q(I)
        Z(I)=CABS(Q(I))
        XK4(I)=CABS(XK2(I))
        WRITE(14,*)X(I),Z(I)
        WRITE(15,*)X(I),XK4(I)
700   CONTINUE
      END
C*************************************************************
      SUBROUTINE HPLOT(Z1,VH,N,DELTA,AMP1,F,FS,A0,B1)
C*************************************************************
      REAL VH(1),VH1(1000)
      INTEGER N,Z1(1)
      XINC=6./N
      CALL PLOTS(53,0,-1)
      CALL ZPICK(3,0,ISTAT)
      CALL ORIGIN(2.5,7.,0)
      CALL FACTOR(0.7)
      DELVAL=Z1(2)*N/6.
      VINC=1.25/5
      INC = 1.0
      ASP = 1.0
      SZN = 0.1
      SZL = 0.12
      CALL HALAB2(0.,0.,0.,DELVAL,TINC,1,6.,1,SZN,ASP,1,-1,
     +          SZL,' ORDER OF HARMONIC ( N ) -----')
      CALL VALAB2(0.,0.,0.0,VINC,TINC,1,5.,1,SZN,ASP,1,1,YP,
     +          SZL,'          AMPLITUDE ( P.U. )')
C
C       ****************************************
C       **    PLOT FOURIER COMPONENTS
C       ****************************************
      DO 800 I=1,N+1
        VH1(I)= VH(I)/(VINC*VH(2))
C     PRINT*,VH(I),VH1(I)
800   CONTINUE
      DO 1000 I=1,N+1
        XD=(I-1)*XINC
        CALL PLOT(XD,VH1(I),3)
        CALL PLOT(XD,0.,2)
1000  continue
      CALL PLOT(0.,0.,3)
C
      CALL SYMB2(-0.4,-1.8,.15,'Coef_A0 = ',0.0,1)
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      IF (A0.LT.1.0) CALL TYPNUM(999.,999.,.15,0.0,0.0,-1)
      CALL TYPNUM(999.,999.,.15,A0,0.0,3)
C
      CALL SYMB2(4.05,-1.8,.15,'Delta = ',0.0,1)
      IF (DELTA.LT.1.0) CALL TYPNUM(999.,999.,.15,0.0,0.0,-1)
      CALL TYPNUM(999.,999.,.15,DELTA,0.0,1)
C
      CALL SYMB2(3.23,-1.5,.15,'Samp. Freq. = ',0.0,1)
      CALL TYPNUM(999.,999.,.15,FS,0.0,1)
      CALL SYMB2(999.,999.,.15,' HZ',0.0,0)
C
      CALL SYMB2(-0.88,-1.5,.15,'Input Freq. = ',0.0,1)
      CALL TYPNUM(999.,999.,.15,F,0.0,1)
      CALL SYMB2(999.,999.,.15,' HZ',0.0,0)
C
      CALL PLOT(0.,0.,999)
      return
      end
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