ANALYSIS AND DESIGN OF DELTA PWM STATIC AC TO DC CONVERTERS

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by

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Abstract

In this thesis, the modelling, analysis and implementation of the delta modulation technique as used in controlled ac-to-dc converters are presented. The proposed modulation scheme, fundamentally differs from conventional PWM techniques, by virtue of its self-carrier generating ability. This intrinsic feature provides the added advantages of ease of implementation, continuous converter voltage control and more importantly, a direct control on the line harmonic contents.

An analytical model is developed, which provides key information on the maximum converter switching frequency, location of dominant harmonics and the PWM switching instances. Optimization of the delta modulator parameters is also carried out by means of parametric variations on a single-phase converter.

The delta PWM technique is implemented in both a single-phase and three-phase transistor bridge converter. In each case, theoretical harmonic analysis of the converter waveforms are presented based on the discrete Fourier transform approach. The pertinent converter waveforms are described in terms of generalized switching functions and the harmonic components are evaluated using an FFT algorithm. Attention has been given to the design of the power and logic circuits conforming to the delta modulator switching specifications. Theoretical results are substantiated by experimental results conducted on prototype single-phase and three-phase transistor converters.

Performance of the three-phase delta modulated converter with typical R-L and dynamic motor loads are also considered. The results indicate the enhanced

performance of the delta modulated converter yielding improved power-factor, near sinusoidal line currents and minimum filtering requirements.

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Chapter 1

Introduction

Optimum performance achievable by Pulse Width Modulation (PWM) techniques has revolutionized the field of static ac to dc converters. Implementation of these techniques has been facilitated by the advent of power transistors offering outstanding characteristics of high power handling capabilities, fast switching and most significantly, the absence of commutation circuitry in converter topologies. Consequently, conventional thyristor-based converters are gradually being replaced by solid state PWM controlled transistor converters.

Traditional phase angle controlled converters proved particularly attractive due to the inherent ruggedness, simplicity, low maintenance and ease of control afforded by the natural commutation of thyristors. However, they have undesirable properties and impose certain disadvantages on the power network. The two chief demerits of these converters are:

- low operating power factor (especially at light loads)
- generation of low order harmonics in the ac line current and ripple in the output.

Moreover, as the output voltage is decreased, the input power factor decreases, necessitating the ac source to supply reactive power. The harmonics generated tend to pollute the power network and cause interference with other equipment in close proximity. In dc drives, the ripple causes overheating and a general derating of the motor.

To compensate the poor performance and enhance the conversion efficiency, various methods have been proposed. Principal schemes for power factor improvement include:

1. Reactive compensation
2. Multiphase rectification
3. Sequential control
4. PWM techniques

1. Reactive Compensation: [1,2]

Basically, this method is a filtering approach, utilizing shunt inductor - capacitor (LC) filters at the ac side and a smoothing reactor in series at the output dc stage. The LC filter located at the harmonic source is tuned to resonance at low order characteristic harmonics. The filter serves as a low impedance path for the harmonic current to flow, virtually eliminating their presence in the ac system. Although the scheme results in a definite improvement in the current waveform, it has the following disadvantages: (1) a separate filter is required for every major harmonic component, or alternatively, continuous tuning is essential to eliminate troublesome harmonic orders, (2) due to the large magnitude of current and low

harmonic components, large sized inductors and capacitors are required, (3) the filter causes voltage fluctuations, and (4) it results in increased losses.

2. Multiphase Rectification: [2,3]

Since harmonic currents are a function of converter pulses, improvement in power factor can be obtained by increasing the number of output pulses. In general, an n-pulse converter generates harmonic components of orders $nk \pm 1$, where k is any integer. As for example, a six pulse converter contains harmonics of orders $5^{th}, 7^{th}, 11^{th}, 13^{th}, \ldots$, and correspondingly, a twelve pulse converter is characterized by $11^{th}, 13^{th}, 23^{th}, 25^{th}, \ldots$ harmonic orders. This procedure, using a higher number of phases for low order harmonic cancellation is referred to as phase multiplication. Multiphase rectification is restricted to high power ac to dc converters such as high voltage dc transmission (HVDC) systems where the cost of additional power apparatus and complex circuitry are justified.

3. Sequential Control: [4,5]

Improvement in power factor is achieved by cascading two converter bridges and using sequential control. In this process, one bridge is maintained in full advance (rectifying) or full retard (inverting) and the other bridge is controlled. Since one converter operates as a diode bridge, the cascade connection simulates a semi converter in both the motoring as well as the regenerating modes, resulting in an improvement in displacement angle. The sequential control method is complicated, expensive and only partially effective, and hence it has found limited uses.

4. PWM Techniques:

The line commutation method offers little flexibility in controlling thyristor switching due to the natural commutation of thyristors by line voltages and subsequent conduction of thyristors on different phases. Hence, the phase angle control technique is more or less restricted as the only control parameter is thyristor turn-on instants with turn-off dictated by converter operation. In contrast, the forced commutation principle allows thyristor commutation at any desired instant by providing each thyristor with its own commutation circuit. In other words, the use of forced commutation increases the versatility of the converter and permits a direct control of thyristor switching to improve performance.

Initially, control schemes incorporating forced commutation were based on a single pulse approach to symmetrically trigger thyristor pairs per half cycle. Various single pulse control schemes have been reported in the literature [5 – 7] and moreover, when used in conjunction with the aforementioned schemes, resulted in a general improvement in converter performance. However, it was soon realized that maximum power factor and reduction in low order harmonics could be achieved by using multiple pulses per half cycle. This opened the avenue for PWM techniques, where thyristor switchings are governed by certain modulation laws such that the ac waveform closely resembles a sinusoid.

PWM techniques have gained considerable attention in recent years due to the optimum performance attainable with a simple converter topology. The salient features of a PWM controlled ac/dc converter are:

- High operating power factor
- Unity displacement factor

- Negligible lower order harmonics
- Controllability
- Reduced filter size

Limitations of the process are:

- Complex control circuits
- Auxiliary commutation circuits
- Increased losses due to high switching frequency

1.1 Review of PWM Techniques

Various types of PWM techniques exist and can be categorized as

1. Natural Sampling
2. Uniform Sampling
3. Optimal PWM and
4. Adaptive control PWM

1. Natural Sampling:

In the natural sampling technique as shown in Fig. 1.1(a), the switching points are determined by the crossings of the modulating waveform, typically a sine wave and an isosceles triangle carrier wave. This technique, most commonly referred to as Sinusoidal PWM [7 – 9], has the modulated waveform containing harmonics as a function of the frequency ratio. The frequency ratio or modulation index is

defined as the ratio of the carrier frequency to modulating frequency. The higher the frequency ratio, the more distant the dominant harmonics are from the fundamental component. Another version of the carrier modulated PWM technique described above, uses a triangular wave and a constant dc reference waveform. In this case, variation in the dc level controls the pulse widths. Similar to the Sinusoidal PWM method, the harmonic content is a function of the triangular wave frequency [10]. High carrier frequency causes the dominant harmonics to appear in the upper frequency spectrum.

2. Uniform Sampling:

This PWM technique is based on a sample and hold principle, with the modulating wave represented by piecewise linear segments. The uniform sampling approach as shown in Fig. 1.1(b), is essentially a derivative of the natural sampling process, with the continuous sine wave replaced by an equivalent stepped version. It has the advantage that the sampling pulse can be made symmetrical about the trough of the carrier. This results in a significant reduction of low frequency harmonics and elimination of subharmonics at non-integer frequency ratios. The technique is particularly suitable for microprocessor implementation.

3. Optimal PWM:

Optimal PWM strategies are based on the minimization of certain criteria [11,12]; for example, elimination or minimization of particular harmonics, harmonic current distortion, peak current, etc. As opposed to the natural or uniform sampling methods, optimal PWM techniques require the PWM waveform to be defined a priori in terms of the desired switching instances and followed by their determina-

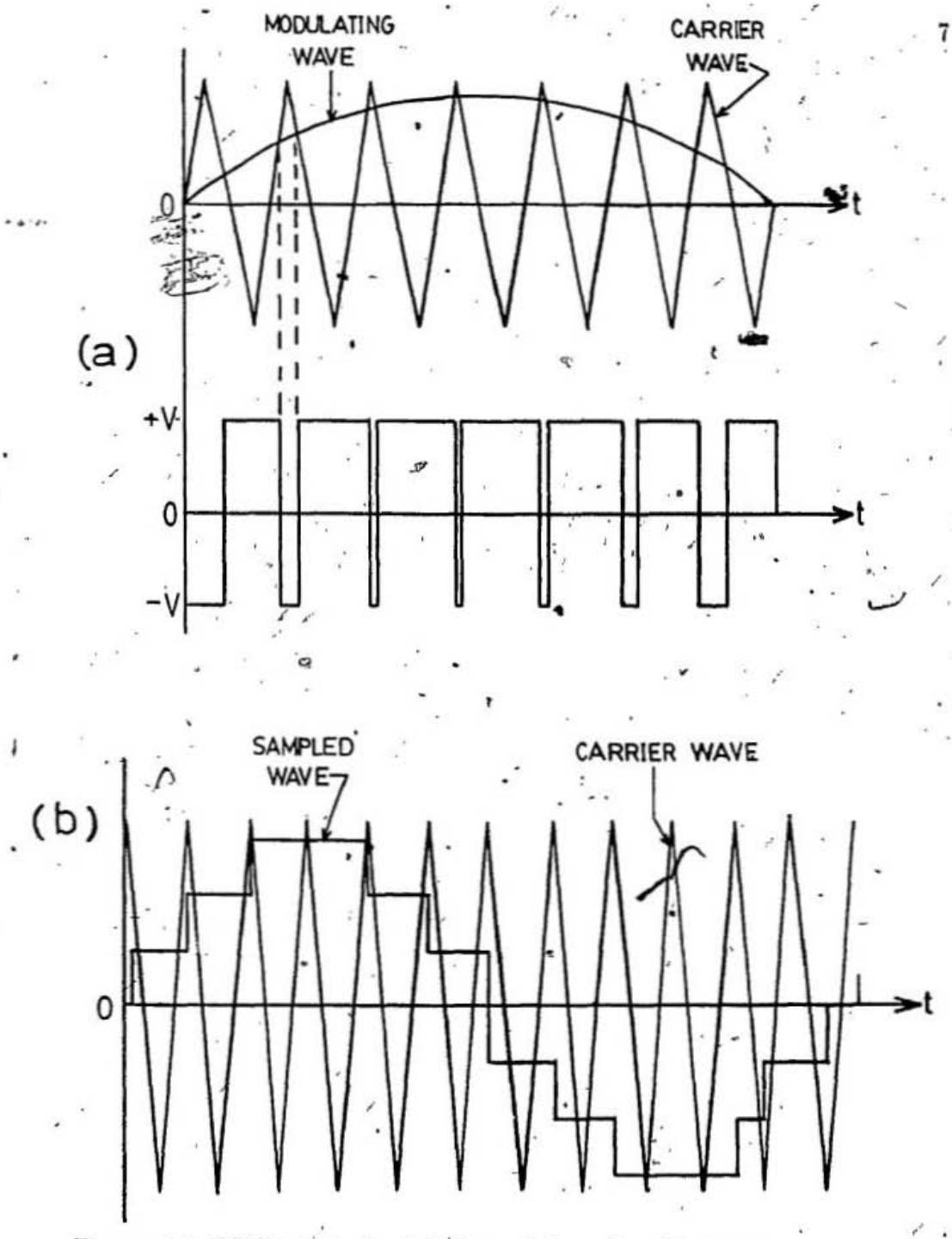


Figure 1.1: PWM strategies (a) Natural Sampling (b) Uniform Sampling

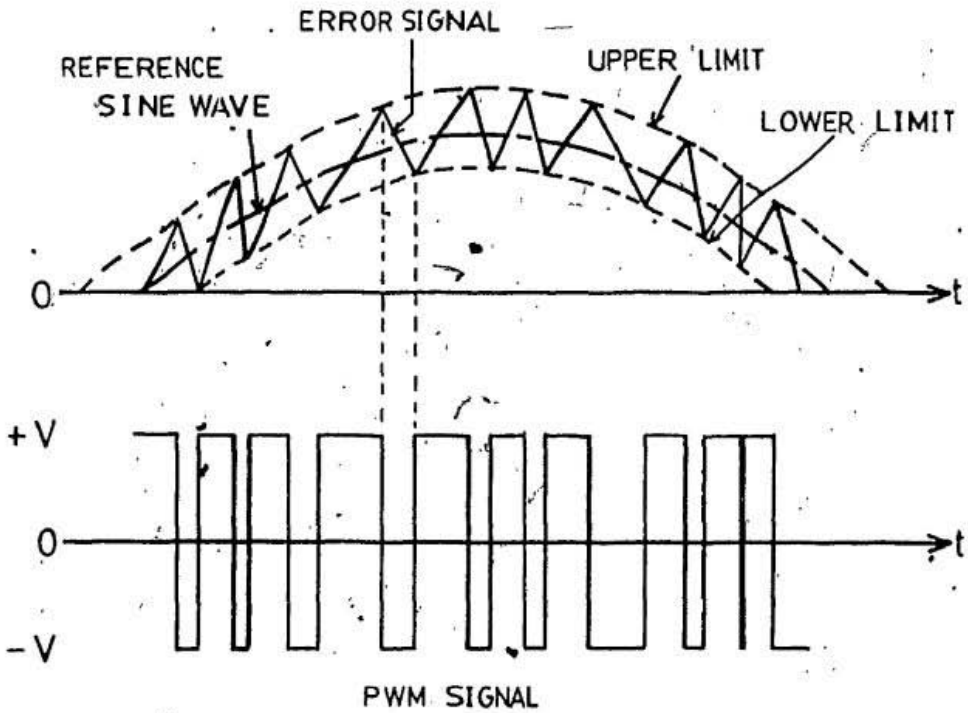


Figure 1.2: Adaptive control PWM

tion through numerical techniques. Optimal PWM techniques are computational intensive and require dedicated microprocessors for successful implementation.

4. Adaptive Control PWM:

In principle, adaptive PWM techniques utilize a "bang - bang" hysteresis control approach to minimize a desired signal (usually an error signal) within certain critical limits. In this approach, as shown Fig. 1.2, the switching instances are intrinsically determined by the intersection of the error signal with the upper and lower hysteresis boundaries. For a sinusoidal reference signal, the modulated waveform has a fundamental frequency component equal to the reference frequency and the dominant harmonics appear at the ripple frequencies. Therefore, by adjusting the hysteresis limits, dominant harmonics can be laterally shifted towards the higher end of the frequency spectrum. The adaptive PWM technique has a dual advantage: (1) it allows a closed loop control process, and (2) the modulation process inherently eliminates lower order harmonics.

The present work utilizes an adaptive control PWM technique to generate the switching waveforms for ac to dc converters. The proposed PWM technique, referred to as delta modulation in communication terminology, has been used extensively in digital signal transmission. Recently, the modulation technique has been successfully incorporated in inverter and ac motor drive applications [11,13 – 19]. However, its use in controlled rectifier applications has not been addressed. This thesis is directed towards a comprehensive study of the delta modulation technique as applied to ac to dc converters.

1.2 Objectives of the Present Work

The objectives of this thesis are to:

1. Investigate the characteristics of the delta modulation technique and develop an analytical model to accurately describe the modulation process.

2. Undertake a quantitative analysis with the perspective of predicting the performance of delta PWM single-phase and three-phase ac to dc converters.

3. Provide experimental results to validate the predicted results.

Chapter 2 covers the essentials of the modulation technique. An analytical model is presented along with a methodology for determining the switching characteristics of the modulator.

Chapter 3 is devoted to the study of the single-phase Delta Modulated (DM) converter. The procedure for simulating the converter is explained and theoretical results of the converter performance with a resistive load are presented. Implementation aspects of the converter are discussed and experimental results are also included. An equitable comparison of the DM converter with other noted PWM converters, although desirable, is beyond the scope of this thesis. However, the latter part of this chapter compares the performance of the DM converter with the conventional phase angle controlled converter.

In Chapter 4, the three-phase DM converter is studied in detail. The analysis procedure for predicting converter performance is presented. Implementation of the three phase logic circuit and the power converter topology are described. Experimental results of the converter with resistive loads are provided.

Performance of the three-phase DM converter with passive R-L and motor loads is investigated in Chapter 5. The analysis presented is based on continuous current mode of operation. Experimental results of a 1/4 hp, 120 volt, dc motor are provided.

Conclusions and suggestions for future work are outlined in Chapter 6.

Chapter 2

Delta PWM Technique

This chapter is devoted to the study of the delta PWM technique as applied to ac to dc converters. The principle of operation, method of control and an analytical model describing the modulation process are presented. At the outset, the family of delta modulators is introduced, leading to the development of the rectangular wave delta modulator. A practical circuit to realize the modulator is presented along with the control scheme used to vary the output voltage. The delta PWM system is modelled and a numerical approach for determining the switching instances is provided. Finally, inherent features of the PWM scheme are outlined.

2.1 Introduction to Delta Modulation

In communication systems, the most prominent digital encoding technique of continuous signals is pulse code modulation (PCM). Several variant or alternate techniques [19,20] have been proposed, the most important class comprising delta modulation and allied differential encoding methods.

Classical PCM entails the sampling, quantization and coding of an analog

signal to a series of pulses. The process is initiated by sampling the analog signal followed by quantization, in which each sample is represented by a discrete value chosen from a fixed number of possible levels. The quantized samples are then converted into a series of binary digits forming the code word. In contrast, the basic principle of differential encoding is to quantize and encode changes in the signal, rather than instantaneous sample values.

In the case of delta modulation, a single binary digit is used to describe the change from one sample value to the next. This digit is derived by comparing the signal amplitude at one sampling instant with the value obtained by reconstructing the signal from the previous digits. Hence, delta modulation can be viewed as a simple type of predictive quantizing system and is essentially a 1-digit, (2-level) differential pulse code modulation system. Relative to PCM, delta modulation is the simplest known method for analog to digital and digital to analog conversion. The salient features of the delta modulation technique are summarized [20 – 22] as

- a high resolution A/D interface since quantizing accuracy depends on a single well defined step, not a series of threshold levels as in conventional A/D converters.
- low complexity resulting in inexpensive implementation.
- robustness to transmission errors, and
- simple filtering requirements.

In addition to these features, the modulation technique offers the option of either a digital or analog circuit implementation. These promising attributes of the

delta modulation technique make it a potential candidate for power electronic applications.

2.1.1 Types of Delta Modulators

Since the discovery of delta modulation in the early 1950's, various modifications to the single integrator delta modulator have evolved. The family of delta modulators, from a broader perspective, can be categorized into the following three classes as [23]

1. Linear delta modulator
2. Asynchronous delta modulator
3. Adaptive delta modulator

1. Linear delta modulator

The chief components of a linear delta modular are a quantizer or hard-limiter, sample and hold circuitry and a filter. Depending on the configuration of these elements and the type of filter employed, various modulators have been developed. Figure 2.1(a) depicts a single integrator delta modulator [24] in which the filter consists of an ideal integrator placed in the feedback path. An alternate configuration Fig. 2.1(b), designated as sigma delta modulator [21,24] uses an ideal integrator in the feedforward path with unity feedback close loop arrangement. In the case of the exponential delta modulator [23] as shown in Fig. 2.1(c), the ideal integrator is replaced by an RC combination serving as a low-pass filter. Though the topology of each modulator is unique, their outputs are characterized by pulses quantized both in time and amplitude. Hence, from the power electronic

viewpoint, this class of modulators is adaptable for microprocessor control.

2. Asynchronous delta modulator

Asynchronous delta modulation schemes [23] are characterized by their output pulses quantized only in amplitude and not in time. Consequently, no sampling processes are involved. This class of modulators derives its name by virtue of the nonlinear characteristics of the quantizer. Fig. 2.2(a) illustrates a typical asynchronous delta modulator consisting of a hysteresis quantizer and an ideal integrator. The particular configuration termed as a rectangular wave delta modulator [22] allows continuous encoding of the reference signal. Since in this system, information is contained in the varying pulse widths, only the zero crossings of the pulses need be transmitted. As a result, asynchronous delta modulators are ideally suited for analog circuit implementation.

3. Adaptive delta modulators

Complexity of the delta modulator incorporating adaptive schemes is far greater than the linear or asynchronous modulators. This is due to the fact that the modulator is designed to encode signals having wide bandwidth characteristics and hence improve resolution of the encoded signal. Various adaptive schemes have been proposed, most common among which are based on an optimal control strategy such as the use of a multilevel quantizer or multistage delta modulator [23]. An adaptive delta modulator using a multilevel quantizer is shown in Fig. 2.2(b). The quantizer level is inherently selected by the modulator and therefore, it can accommodate abrupt changes in the slope of the input signal. A multistage encoder contains a number of delta modulation stages, where each delta

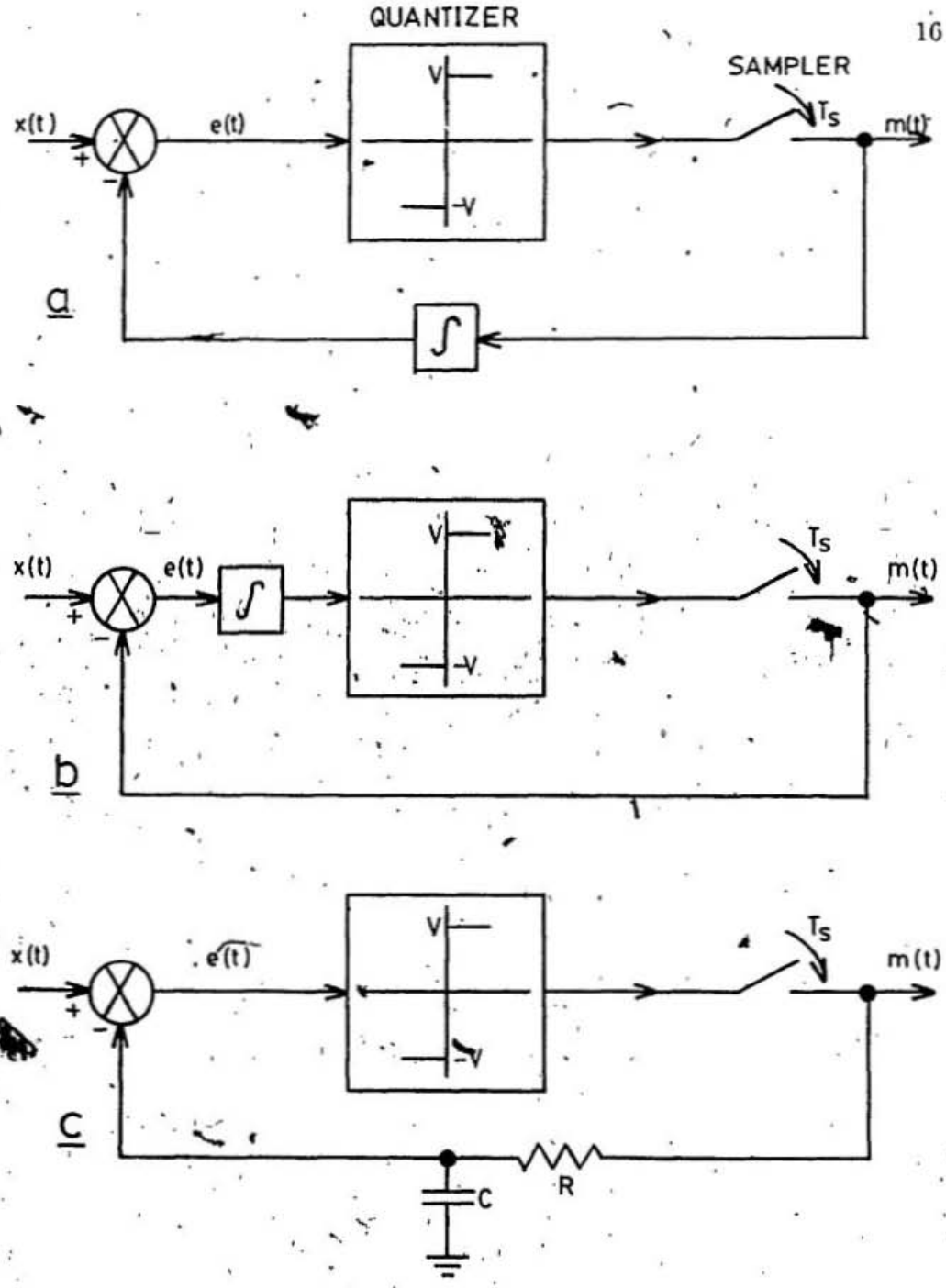


Figure 2.1: Linear delta modulators: (a) single integrator DM (b) sigma DM (c) exponential DM

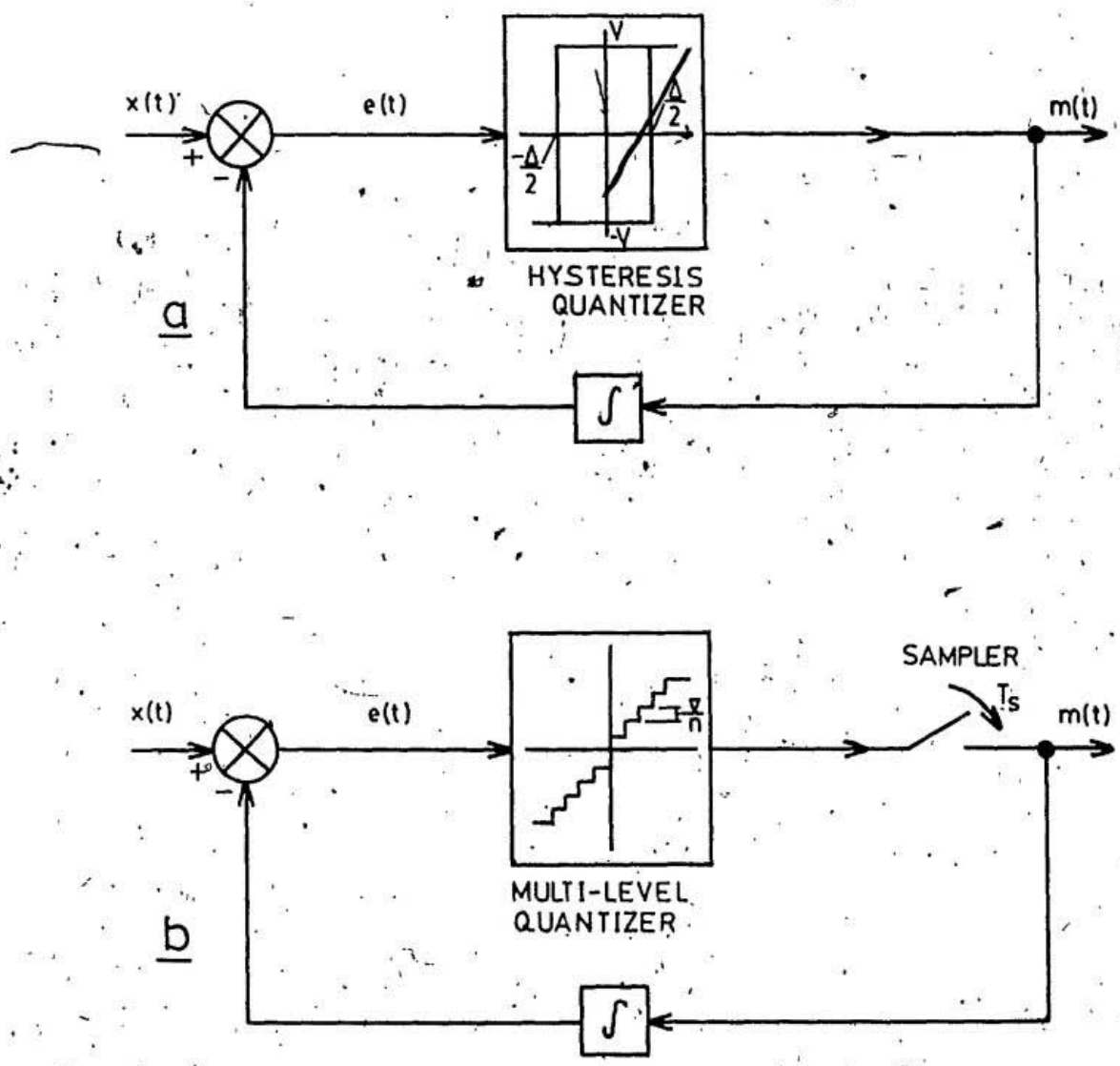


Figure 2.2: (a) Asynchronous DM (b) Adaptive DM

modulator encodes the bandlimited error signal of the previous delta modulator.

Of the wide array of delta modulators available, the most suitable one for a power electronic application is determined by factors such as the power conversion scheme, either ac to dc (rectifier) or dc to ac (inverter) and, the implementation and control schemes (microprocessor – base or analog – base). In inverter applications, the output frequency (either fixed or variable) also dictates the choice of the delta modulation scheme.

2.1.2 Survey of Delta Modulation Strategies in Power Electronics

Recently, the delta modulation technique has gained considerable attention as a potential PWM scheme for control of power converters. Most of the literature on the subject pertains to the implementation of inverters and adjustable speed ac drives. Characteristic of these applications are output parameters such as variable- voltage,variable - frequency operation or variable - voltage, constant - frequency operation which must be afforded by the modulator.

Ziogas [13] has implemented a free running rectangular wave delta modulator to control a voltage source inverter. Rahman, et al [14,15] have made use of the inherent V/f (voltage/frequency) characteristics of the symmetrical hysteresis delta modulator to control the speed of induction and permanent-magnet synchronous motors. Manias, et al [16] have suggested its use in current control of a switch mode rectifier (SMR), though provision for controlling the output voltage is not accounted for by the modulation circuit. Its use in uninterruptible power supplies (UPS) for controlling both the rectifier stage as well as inverter switching has also been reported [17].

Kheraluwala, et al [18] have employed the Sigma delta modulator for a resonant dc link inverter. The sampled data nature of the delta modulation strategy has been exploited to realize the switchings at the zero crossings of the link voltage.

An optimal control strategy incorporating a multistage delta modulator has been reported by Rahman, et al [11] to improve the performance of a single phase inverter. The modulation system consists of a rectangular wave delta modulator followed by an active filter network, the output of which is fed to another rectangular wave delta modulator.

Although the Sigma delta modulator has been used in resonant link inverters, its application in motor drives is restricted due to the absence of a V/f control strategy. High sampling frequency demanded by the digital encoding process results in substantial transistor switching losses. On the other hand, the rectangular wave delta modulator, besides providing the desired V/f characteristic, offers good current tracking ability. It is, therefore suited for applications such as inverters, drives as well as non-linear control systems.

2.1.3 Requirements of Delta PWM Converter

For PWM control of a rectifier by the delta modulation technique, the modulator must be instrumental in providing the following features:

- continuous control of the output voltage over the entire operating range.
- reduce and/or eliminate lower order harmonics
- minimize output voltage ripple

- ease of implementation.

To meet the first criterion, it is necessary to have an indirect control of the pulse widths of the modulated pulses such that the ratio of "on" pulses to "off" pulses determines the output voltage. Clearly, the family of Linear delta modulators are unable to satisfy this requirement due to the fact that the pulses are a function of sampling frequency and a preset step size.

One approach in overcoming this limitation in Linear delta modulators is to adopt a different scheme of controlling the output voltage. Rather than having a filter of preset characteristics, the time constant associated with the "on" pulse is maintained different from that of the "off" pulse. Consequently, control of the output voltage is achieved by continuously changing the two time constants. Needless to say, the procedure substantially complicates the circuit implementation.

Rectangular wave delta modulator has the inherent ability to track the reference signal within a well defined boundary established by the hysteresis threshold levels. The modulator can therefore be used for either voltage or current control depending on the reference signal. Another attribute of this modulator concerns the switching frequency. Switching frequency and hence harmonic control can be achieved in three unique ways; (1) by adjusting the integrator parameters, (2) by changing the amplitude of the reference signal, and (3) by controlling the hysteresis threshold levels.

The use of adaptive schemes for converter applications is debatable considering that the modulator is responsible for encoding a well defined sinusoidal signal of constant frequency. Again, for control purposes, the adaptive scheme must

incorporate a hysteresis comparator. Undoubtedly, adaptive delta modulators provide superior performance but at the expense of a substantially complex circuit. The same quality performance can be obtained by a single rectangular wave delta modulator using a simple filter network.

In light of the arguments presented, rectangular wave delta modulator is capable of meeting the controlled rectifier criteria. The intrinsic feature of the asynchronous modulator is classified as an adaptive PWM technique as mentioned earlier. As such, the modulator serves a dual purpose of encoding a typical sinusoidal reference signal as well as controlling the output voltage.

2.2 Delta Modulation Technique

Rectangular wave delta modulation is a differential encoding technique. The modulated pulses are produced by the interaction of the reference signal and a locally reconstructed signal. As applied in signal processing, the rectangular delta modulation process can be illustrated with the aid of Fig. 2.3

The input signal, $x(t)$, is compared with the reconstructed signal, $y(t)$. The difference is examined by the comparator circuit. In this system, the comparator consists of a hysteresis quantizer with symmetrical quantization levels $\pm\Delta$. The binary waveform $z_i(t)$ at the output of the modulator consists of pulses of equal magnitude $\pm V$, but of varying widths. The pulses are integrated in the feedback path to establish the carrier waveform $y(t)$, consisting of linear segments having alternative positive and negative slopes of equal magnitude Δ. Depending on the polarity of the error $e(t)$ defined as $[x(t) - y(t)]$, the hysteresis comparator either maintains or changes states causing the output pulse to similarly maintain

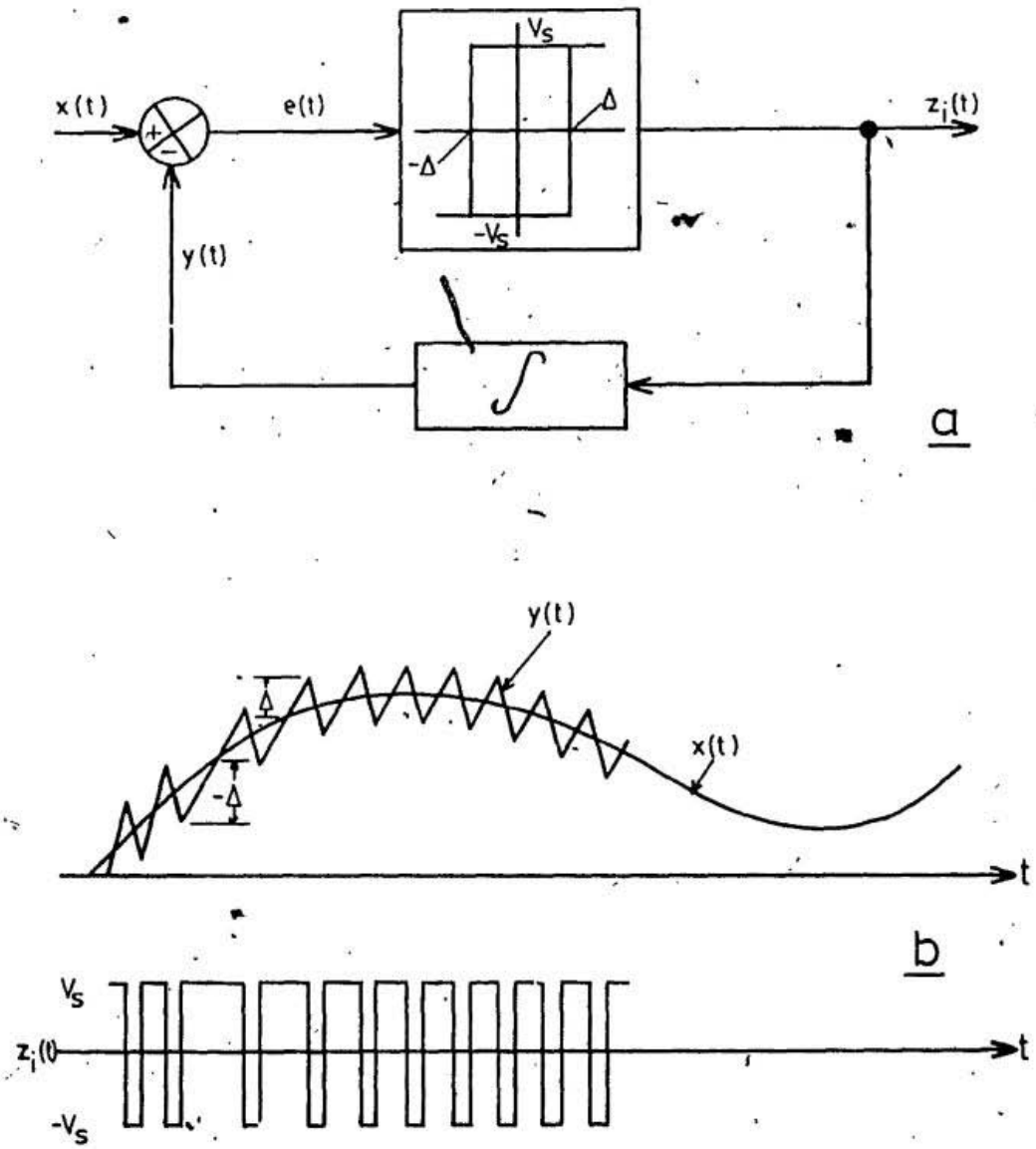


Figure 2.3: Rectangular wave delta modulation: (a) schematic of encoder (b) typical waveforms of the modulation process

or change polarity. The closed loop arrangement ensures that the carrier faithfully tracks the input signal and the modulator in turn gives output information corresponding to the differentiation of the $x(t)$ signal.

Mathematically, the sampled modulated switching waveform $z_i(t)$ can be expressed as [23]

$$z_i(t) = V_s \sum_k \Delta sgn[x(kT_s) - y(kT_s)] \qquad (2.1)$$

where:

$\pm\Delta$	=	quantization level
$\pm V_s$	=	level of switching pulses
$x(kT_s)$	=	modulating signal
$y(kT_s)$	=	predicted signal at kT_s
sgn	=	indicates the sign of $[x(kT_s) - y(kT_s)]$
T_s	=	sampling time

The equal slope approximation as illustrated in Fig. 2.3(b) is implemented in an efficient manner with a simple differentiation of the linear segments resulting in a positive or negative pulse of equal height but of varying width and frequency. The delta modulation process is essentially continuous, providing a digital representation of the input signal as long as the input signal does not change at a rate greater than the maximum average slope of the carrier waveform. If this occurs, the carrier wave is unable to track the reference signal and the modulation process fails. The phenomenon termed as slope overload [21 - 24] is the limiting case of the delta modulation technique. Because the modulator encodes information corresponding to the derivative of the message function, the overload characteristics

are a function of the signal slope instead of the amplitude. In the absence of an input signal, a condition commonly referred to as the idle channel condition, the modulator outputs a square wave signal indicating the oscillatory nature of the circuit.

The switching frequency of the modulator can be controlled in three different ways: by changing the amplitude of the reference signal, by changing the slope of the triangular carrier wave or by changing the magnitude of the window widths ($\pm\Delta$ quantization levels). The flexibility offered by the rectangular delta modulation system has made it very attractive for converter applications.

2.2.1 Delta Modulated Converter

The asynchronous operation of the rectangular DM circuit yields the modulated pulses quantized in amplitude with the pulse widths determined by the positive and negative slope transitions in the carrier wave. For rectifier implementation it is necessary to control the output dc voltage via the modulated pulses which govern the transistor 'on–off' switching action. With a constant frequency modulating signal, the inherent self-carrier generating feature of the DM technique allows a simple control process for varying the output dc voltage of the converter.

The modified rectangular wave delta modulator shown in Fig. 2.4 permits the voltage to be controlled via an asymmetrical hysteresis quantizer. The quantizer threshold levels (Fig. 2.4) or alternately, the delta window widths, designated Δ_p and Δ_n, control the output voltage such that, maintaining Δ_p greater than Δ_n leads to an increase in the output dc level. Conversely, if Δ_n is greater than Δ_p the output voltage decreases.

The simple control process through the *asymmetrical delta control* (ADC) procedure is graphically illustrated in Fig. 2.5. In this case, the modulated switching pulses $v_M(t)$ are obtained by the interaction of the reference sine wave $v_R(t)$ and the triangular carrier wave $v_C(t)$ generated in the feedback path. The carrier is allowed to oscillate within the delta window defined by Δ_p and Δ_n located about the reference sinusoid. Whenever the magnitude of the carrier wave reaches the boundary of either Δ_p or Δ_n it reverses its slope and the output switching pulses accordingly change polarity. Since the reference input signal to the modulator is a sinusoidal signal of fixed frequency, the PWM switching signal generated at the output of the modulator has a sinusoidally varying average value. This characteristic feature of the modulator, in essence, is the principle behind PWM techniques [5 – 10], which aim to attenuate the low order harmonic components present in the converter waveforms.

2.2.2 Delta Modulator Circuit Implementation

A practical circuit which realizes the DM scheme is shown in Fig. 2.6. Comparator A_1 configured as a Schmitt trigger serves as a hysteresis comparator and outputs pulses of magnitude proportional to its saturation voltages of $+V_s$ and $-V_s$. The sinusoidal reference or modulating wave $v_R(t)$ is applied to the input of comparator A_1 and the carrier $v_C(t)$ is generated in the following manner; whenever the output voltage of A_3 exceeds the threshold limits of comparator A_1, it reverses the polarity of $v_M(t)$ at the output of A_1. This reverses the slope of $v_C(t)$ at the output of A_3. It forces the carrier wave $v_C(t)$ to oscillate around the reference waveform $v_R(t)$ at ripple frequency f_r.

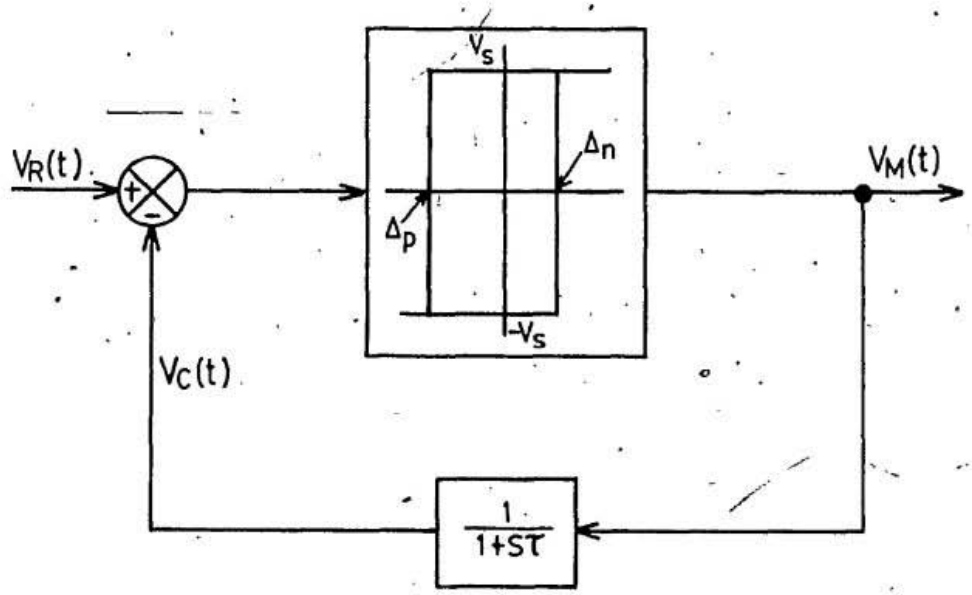


Figure 2.4: Schematic diagram of the modified delta modulator with asymmetrical hysteresis

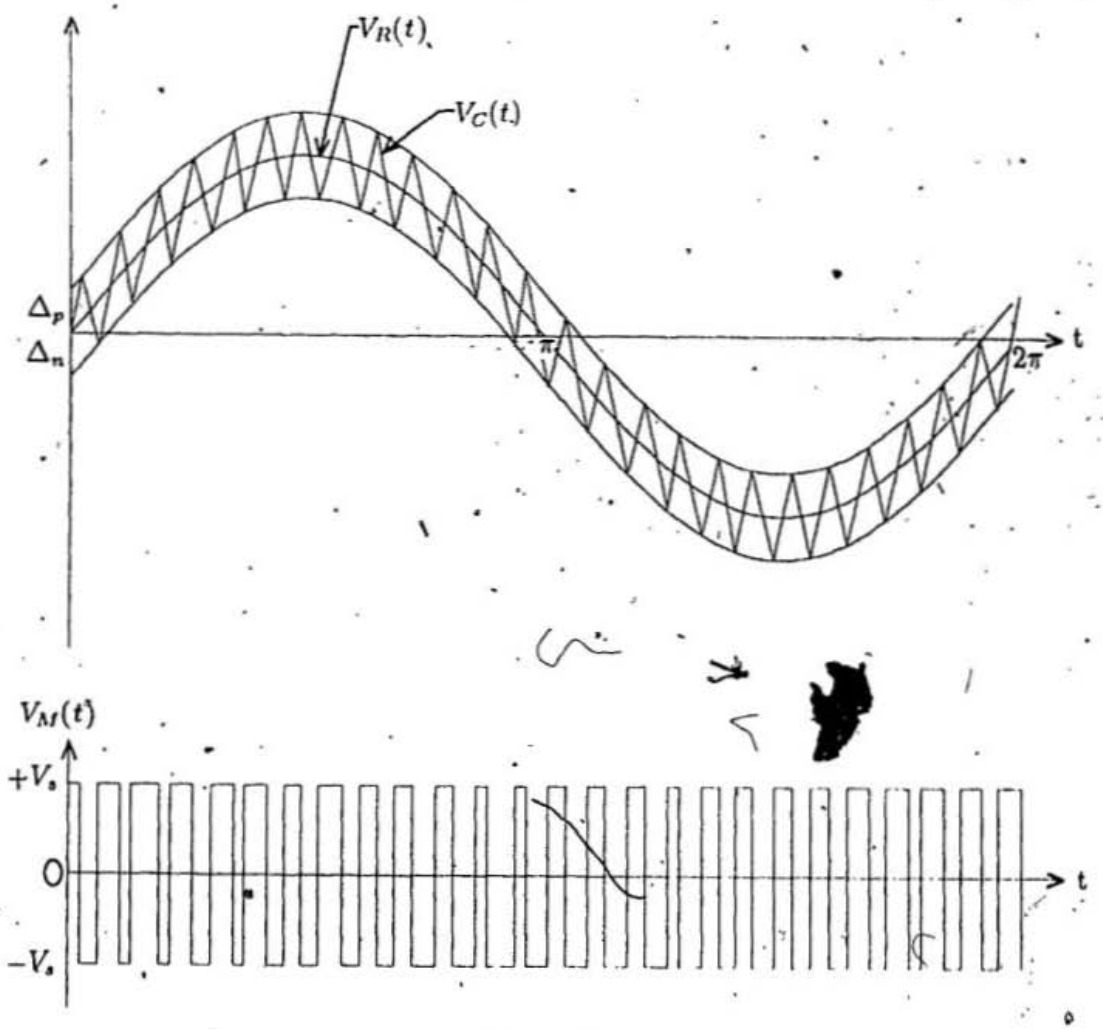


Figure 2.5: Graphical illustration of the DM technique for converters

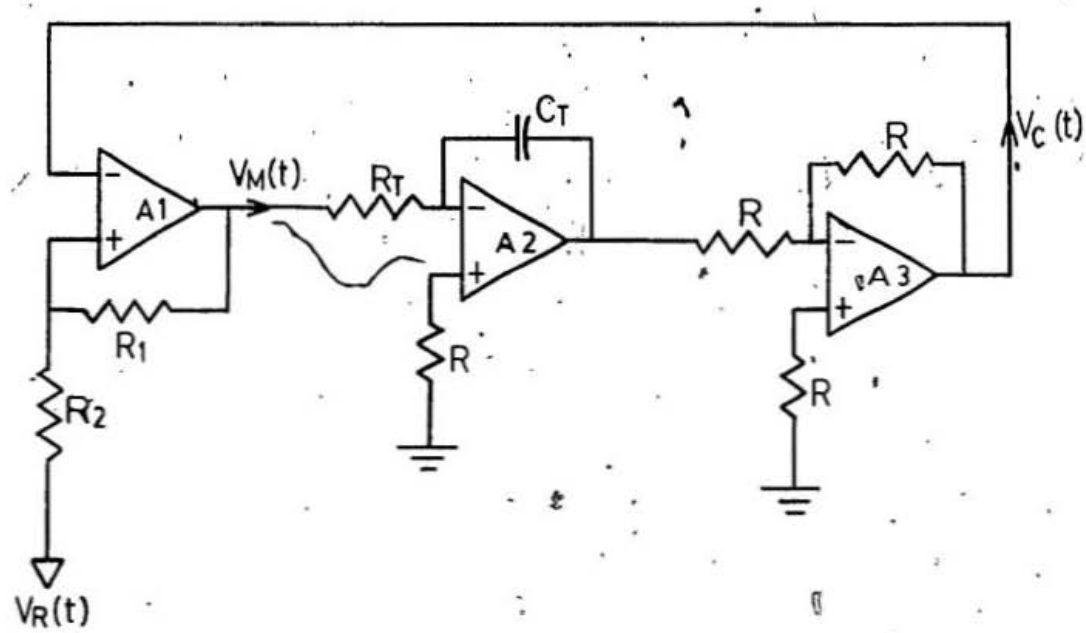


Figure 2.6: A practical DM circuit for producing single phase switching signals

The hysteresis comparator threshold limits or alternatively the delta window widths are established by the arms ratio R_1/R_2 such that:

$$\Delta_p = \frac{R_1}{R_2}|+V_s| \tag{2.2}$$

$$\Delta_n = \frac{R_1}{R_2}|-V_s| \tag{2.3}$$

The frequency of the modulated waveform is determined by the $R_T\,C_T$ combination of integrator A_2. The rising and falling slopes of the carrier wave are given by:

$$M_p = \frac{1}{R_T C_T}|+V_s| \tag{2.4}$$

$$M_n = \frac{1}{R_T C_T}|-V_s| \tag{2.5}$$

where:

M_p = positive slope of $v_C(t)$

M_n = negative slope of $v_C(t)$

$R_T C_T$ = time constant of integrator A_2

In the circuit, the ratio R_1/R_2 is set at a constant value giving Δ_p and Δ_n directly proportional to the comparator's saturation voltages. This allows the ADC scheme to be implemented in an efficient manner by the pertinent parameters $+V_s$ and $-V_s$. By independently controlling $+V_s$ and $-V_s$, the converter's output voltage can be controlled over the entire range of operation. Since the slopes of the carrier waveform are directly proportional to the pulse magnitudes ($+V_s$ or $-V_s$), the control scheme is similar to the dual integration [25] control process.

However, with the ADC scheme expanding over the control range, particular attention must be given to the slope overload limitation of the modulator. In this case, slope overload occurs when the slope of either the positive or negative segments of $v_C(t)$ is less than the maximum slope of the reference sinusoid. For a constant amplitude modulating sine wave $v_R(t) = V_R \sin(\omega t)$, the maximum slope is

$$\frac{dv_R}{dt}|_{max} = 2\pi f V_R$$

and therefore slope overload occurs when the instantaneous slopes of either M_p or M_n goes below the minimum limit of $2\pi f V_R$. Mathematically, the condition for slope overload is given by

$$\left.\begin{array}{ll} M_p \leq 2\pi f V_R & \text{for rising slope in } v_C(t) \\ M_n \leq 2\pi f V_R & \text{for falling slope in } v_C(t) \end{array}\right\} \qquad (2.6)$$

This sets the limitation on M_p and M_n and consequently, on the time constant of the integrator with $+V_s$ and $-V_s$ being the control variables.

Another factor which has been taken into consideration in designing the delta modulator is synchronizing the carrier wave with the reference sinusoidal signal. For a particular Δ_p and Δ_n setting, a situation may arise where the fundamental frequency of the carrier wave may deviate from that of the reference sine wave. To ensure synchronization between these two signals, the capacitor C_T is momentarily shorted to ground at each zero crossing of the reference signal. This permits the capacitor to discharge, forcing the carrier wave to be synchronized with the sinusoidal reference signal for all Δ_p and Δ_n values. The differential encoding principle of the delta modulator results in the modulated waveform being displaced by 90 degrees with respect to the sinusoidal input. The problem is

circumvented by passing the sinusoidal signal to a basic integrator circuit, which provides the necessary phase shift and then to the modulator input. Although not significant for converter applications, the presence of the integrator permits the modulator to encode time-invariant signals, which otherwise cannot be digitally represented by delta modulation schemes.

2.3 DM System Modelling

The DM system, though conceptually simple, is difficult to analyse due to the presence of the non-linear element in the feedforward path. The intrinsic self generating carrier feature of the modulator affords a viable control mechanism, but substantially complicates the task of modelling and analytically predicting system behavior.

An analytical model describing the DM process is of prime importance to: (1) enable the selection of circuit parameters, (2) predict the performance of the converter, and (3) optimize the converter performance. Selection of the circuit parameters must be given due consideration as the modulator is instrumental in controlling the output voltage as well as reducing harmonics.

The switching frequency of the converter is not fixed, but varies as the window widths are varied in accordance with the ADC scheme. The modulator responds to a variation in Δ_p and Δ_n and inherently determines the converter's switching instances corresponding to the positive and negative transitions in the carrier wave. However, as the magnitudes of the window widths are varied, the pulse widths vary and consequently, the number of pulses per half cycle change as the output voltage is controlled. This results in the converter power transistors being

switched over a wide frequency range. Prediction of the maximum switching frequency, is therefore, essential to maintain transistor switching losses within reasonable limits.

Many types of delta modulators have been successfully used in digital communication systems. From the communications viewpoint, typical performance parameters such as signal to noise ratio (SNR), quantization noise, idle channel noise, spectral density function and the like are detailed in the literature. Johnson [21] has quantitatively described the performance of a single-integrator delta modulator in terms of its overload characteristics. Flood, et al [24] have proposed an open loop mathematical model which generates a pulse waveform identical to a single-integrator delta modulator. Sharma [22,26] has outlined a methodology for calculating the various parameters of the rectangular wave delta modulator with symmetrical hysteresis. Gotz, et al [27] have considered the effects of step-size imbalance and quantizer threshold hysteresis on the idle channel noise characteristics of the delta modulator.

Such parameters, though relevant for predicting the modulator's performance in digital communication systems, do not convey the performance of the controlled rectifier. Of more interest in power electronic applications, are factors such as output signal spectral content and harmonic distribution. Determination of these parameters entails the development of an analytical model which provides a mathematical foundation for calculating the converter's switching instances and number of pulses per half cycle. Once the switching instances are known, a study of the spectral contents in the voltage and in the current waveforms can be conducted using the Fourier series approach.

2.3.1 Analytical Model

A prerequisite in aiding the development of an analytical model is an understanding of the intrinsic behavior of the delta modulator with the ADC scheme. The control scheme suggests that the window widths be varied asymmetrically if the output voltage is to be controlled.

To generalize the model over the entire control range, consider the encoding of an arbitrary sinusoidal reference signal $v_R(t)$ with an asymmetrical Δ setting of Δ_p and Δ_n, such that $\Delta_p > \Delta_n$. The waveforms of the delta modulator under the specified conditions, over successive positive levels in $v_M(t)$ are illustrated in Fig. 2.7. If T_{DR} and T_{DF} denote the rising and successive falling edges of the carrier wave $v_C(t)$, then the total time duration T_D, between successive positive (or negative) levels in $v_M(t)$ is given by:

$$T_D = T_{DR} + T_{DF} \tag{2.7}$$

From the geometry in Fig. 2.7

$$T_{DR} = \frac{\Delta_p + \Delta_n}{M_p - \bar{v}_R(t)|_{t_i,t_{i+1}}} \tag{2.8}$$

$$T_{DF} = \frac{\Delta_p + \Delta_n}{M_n + \bar{v}_R(t)|_{t_i,t_{i+1}}} \tag{2.9}$$

substituting into (2.7), yields

$$T_D = \frac{\Delta_p + \Delta_n}{M_p - \bar{v}_R(t)|_{t_i,t_{i+1}}} + \frac{\Delta_p + \Delta_n}{M_n + \bar{v}_R(t)|_{t_i,t_{i+1}}} \tag{2.10}$$

Replacing the instantaneous values of $\bar{v}_R(t)|_{t_i}$ and $\bar{v}_R(t)|_{t_{i+1}}$ by their long term average slope of $v_R(t)$, Equation (2.10) can be expressed as

$$T_{Davg} = \frac{(\Delta_p + \Delta_n)(M_p + M_n)}{M_p M_n + (M_p - M_n)\bar{v}_R(t) - \{\bar{v}_R(t)\}^2} \tag{2.11}$$

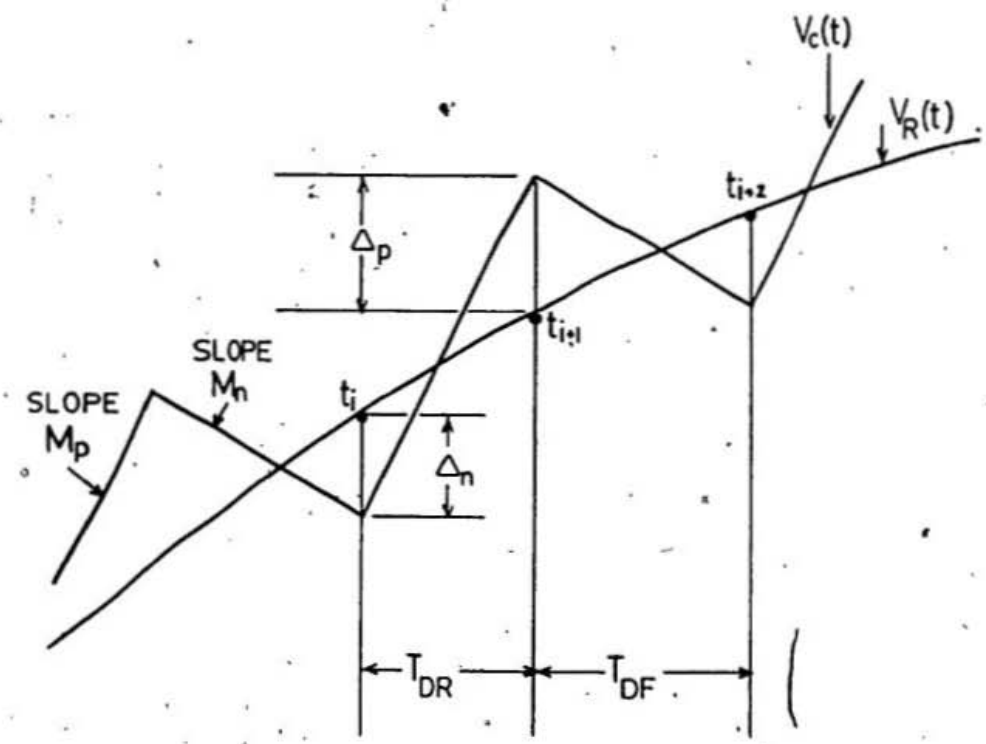


Figure 2.7: Output of delta modulator over successive switching intervals

where:

Δ_p	=	positive window width
Δ_n	=	negative window width
M_p	=	rising slope of carrier $v_C(t)$
M_n	=	falling slope of $v_C(t)$
$\bar{v}_R(t)$	=	deriyative of reference signal $v_R(t)$

Maximum switching occurs when the modulator is in the idle channel condition; when $v_R(t) =$ constant. Hence,

$$T_{max} = \frac{(\Delta_p + \Delta_n)(M_p + M_n)}{M_p M_n} \tag{2.12}$$

For a sinusoidal input, $v_R(t) = V_R \sin \omega_m(t)$, the ripple frequency of the carrier waveform is obtained from (2.11) as

$$\begin{aligned} f_r &= \frac{1}{2\pi} \int_0^{2\pi} \frac{M_p M_n + (M_p - M_n)\bar{v}_R(t) - \{\bar{v}_R(t)\}^2}{(\Delta_p + \Delta_n)(M_p + M_n)} d(\omega_m t) \\ &= \frac{M_p M_n}{(\Delta_p + \Delta_n)(M_p + M_n)} \left\{ 1 - \frac{\omega_m^2 V_R^2}{2 M_p M_n} \right\} \\ &= f_{r_{max}} \left\{ 1 - \frac{\omega_m^2 V_R^2}{2 M_p M_n} \right\} \end{aligned} \tag{2.13}$$

where:

ω_m	=	frequency of reference signal $v_R(t)$
V_R	=	amplitude of $v_R(t)$, and

$$f_{r_{max}} = \frac{M_p M_n}{(\Delta_p + \Delta_n)(M_p + M_n)} \tag{2.14}$$

is the maximum ripple frequency of the carrier in the absence of a reference signal and is the reciprocal of (2.12).

The values of Δ_p, Δ_n,M_p and M_n are found from the circuit implementation of the delta modulator given by Equations (2.2) – (2.5). The arms ratio $R1/R2$ is set to a typical value in the range 0.05 to 0.1 [28], so that the time constant of integrator A_2 determines the slopes of the carrier wave. It is important to note that as the threshold level of the hysteresis quantizer reaches a maximum value, corresponding to a maximum in Δ_p or Δ_n, the encoding process is not truly representative of the reference sinusoid. To enhance the resolution of the modulator, time constant of integrator A_2 must be sufficiently small to give a steep transition in the carrier waveform. The lower limiting values of M_p and M_n are specified by the slope overload criterion (Equation 2.6), while the upper values are determined by the maximum transistor switching frequency.

In order to complete the analytical description of the DM process, it is necessary to establish a methodology for determining the switching instances, $t_i, t_{i+1}\ldots$. This is discussed in the following section.

2.3.2 Determination of Switching Points

The procedure for analytically determining the switching instances in the modulated waveform is facilitated by examining the actual working of the DM circuit. A graphical illustration of the encoding process in Fig. 2.6 indicates that the carrier wave, $v_C(t)$ oscillates about the reference sinusoid and is bounded by the upper and lower windows. Each intersection of $v_C(t)$ with the Δ_p and Δ_n boundary locates a switching point, with a positive transition in $v_C(t)$ giving an 'on'

pulse and a negative transition an 'off' pulse. Hence, it is possible to express the pulse positions in terms of the carrier slopes, amplitude of the reference signal and the window widths.

Detailed derivation of the generalized expressions for individual switching instances, t_i are given in Appendix A.

For even switching instances $i = 2, 4, 6, \ldots$

$$t_i = \frac{1}{M_n} \{(\Delta_p + \Delta_n) + M_n t_{i-1} + V_R \sin\omega_m t_{i-1} - V_R \sin\omega_m t_i\} \tag{2.15}$$

For odd values, $i = 3, 5, 7, \ldots$

$$t_i = \frac{1}{M_p} \{(\Delta_p + \Delta_n) + M_p t_{i-1} - V_R \sin\omega_m t_{i-1} + V_R \sin\omega_m t_i\} \tag{2.16}$$

with the first switching point described by

$$t_1 = \frac{\Delta_p + V_R \sin\omega_m t_1}{M_p} \tag{2.17}$$

The transcendental nature of the Equations (2.15) – (2.17) suggest the use of numerical techniques for their solution. A FORTRAN program incorporating an IMSL subroutine [29], is used to compute the switching times. Equations (2.15) - (2.17) are defined by external functions and successive switching times are calculated by the subroutine. Depending on the input parameters, the program checks the slope overload criterion, before proceeding with the computations. Switching instances are computed for the first half cycle of the reference signal and the last switching point is terminated at $T/2$. This ensures that the modulated waveform is synchronized with the reference signal for all Δ_p and Δ_n values. Switching instances for the remaining half cycle are obtained by displacing the computes points by $T/2$. A listing of the program is included in Appendix B.

2.4 Concluding Remarks

In this chapter, various delta modulators are investigated from the viewpoint of selecting the most appropriate modulator for ac to dc converter applications. A close examination of the characteristics of each modulator suggests that the rectangular wave delta modulator with asymmetrical hysteresis meets the criteria for controlled rectifier implementation. The fundamental principles of operation and the ADC scheme used to vary the output voltage are described in detail. An analytical model to calculate the ripple frequency of the modulated wave is presented. Generalized expressions to determine the switching instances are derived and the numerical approach adopted to compute the switching times are discussed.

The key features of the rectangular wave delta modulator are summarized as:

- PWM switching waveforms generated by the modulator have a sinusoidal average value. Hence, the modulation process results in attenuation of lower order harmonics.
- The self generating carrier feature, tremendously reduces circuit complexity compared to other carrier modulated PWM techniques such as sinusoidal PWM, trapezoidal PWM, etc.
- Asymmetrical control of the window widths enables the converter output voltage to be controlled without additional circuit requirements.
- Implementation of the modulator is relatively simple with a minimum number of components.

Chapter 3

Single Phase Delta PWM Converter

In the preceding chapter, theoretical aspects of the delta modulator were presented with an emphasis on the numerical approach for defining the PWM switching waveform. Having established the necessary mathematical foundation, the following sections investigate the performance of the ac/dc converter switched with the delta PWM scheme. In this chapter, the analysis procedure used for determining the harmonics at both the input and output stages of the single-phase converter is first addressed. This is followed by a parametric study of the delta modulator. The objective of the study is to establish preferred modulator parameters which optimize the performance of the delta PWM converter. The performance of the converter is evaluated for various operating conditions. The predicted results are verified experimentally. Finally, the performance of the DM converter is compared with the conventional phase angle control converter. It is shown that the DM technique provides significant improvement in converter performance.

3.1 Analysis of Single Phase Converter

The general approach used in the harmonic analysis of PWM ac/dc converter circuits is to express the PWM input current and output voltage waveforms in terms of general Fourier series. By evaluating the Fourier coefficients, the spectral contents of the waveform can then be determined.

Figure 3.1 shows the single-phase controlled bridge rectifier and the associated waveforms of the converter when switched in the delta PWM scheme. Analysis of the steady state converter performance for all operating conditions requires a general Fourier series expansion of the complex PWM waveforms. Rather than solving for the Fourier coefficients, the analysis procedure followed here is based on a discrete Fourier transform (DFT) approach and utilizes an efficient fast Fourier transform (FFT) algorithm to compute the DFT coefficients.

The DFT approach tremendously simplifies the harmonic analysis process, as it does not require analytical expressions describing individual converter waveforms. The advantage of this approach is further illustrated when considering the analysis of the three-phase converter, by virtue of the symmetry exhibited in the waveforms.

The single-phase DM converter was simulated on a digital computer in standard FORTRAN. The simulation process is mathematically described as follows:

Firstly, to obtain the correct converter switching sequence, the delta modulator waveform is represented in terms of a general gating function defined by

$$g(t, t_i, t_{i+1}) = U(t, t_i) - U(t, t_{i+1}) \tag{3.1}$$

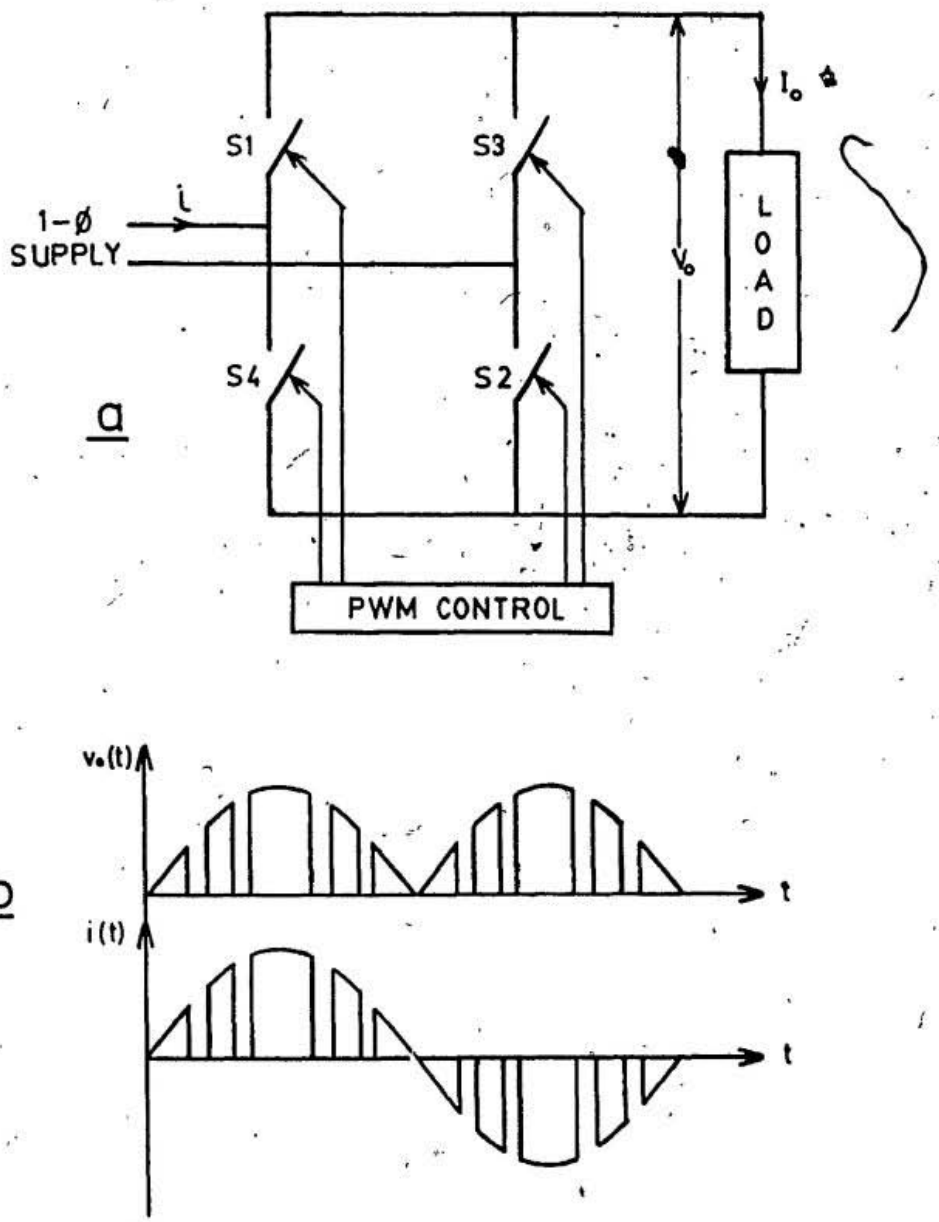


Figure 3.1: Single phase DM converter (a) schematic of converter (b) typical waveforms for a resistive load

where $U(t, t_i)$ is a unit step function

$$U(t,t_i) = \begin{cases} 0 & t < t_i \\ 1 & t \geq t_i \end{cases} \tag{3.2}$$

The process of defining the single-phase converter waveforms is pictorially depicted in Fig. 3.2, where $M(t)$ is the delta modulator output waveform and $G(t)$ is the converter switching function described in terms of the gating function. The converter switching function is defined by:

$$G(t) = \sum_{i=1,3,5,}^{N_p/2} g(t,t_i,t_{i+1}) - \sum_{\frac{N_p}{2},\frac{N_p}{2}+2,}^{N_p} g(t,t_i,t_{i+1}) \tag{3.3}$$

where N_p is the number of pulses per cycle and t_i are the switching instances, obtained by solving Equations (2.15)-(2.17).

The output voltage waveform is readily obtained as a switched sinusoid, and is given by

$$v_o(t) = G(t) \cdot v(t) \tag{3.4}$$

where $v(t) = V \sin\omega t$ is the input line voltage.

The continuous time periodic $v_o(t)$ waveform can be represented in the form of a Fourier series as

$$v_o(t) = \frac{1}{T} \sum_{-\infty}^{\infty} c_n \, e^{jn\omega_o t} \tag{3.5}$$

$$\begin{aligned} c_n &= \int_0^T v_o(t) \, e^{-jn\omega_o t} \, d(t) \\ &= \sum_{i=1}^{N_p} \int_{i=1,3,5,} G(t) \cdot v(t) \, e^{-jn\omega_o t} \, d(t) \end{aligned} \tag{3.6}$$

where c_n is the n^{th} Fourier coefficient and $\omega_o = 2\pi/T$ is the fundamental frequency in radian/sec.

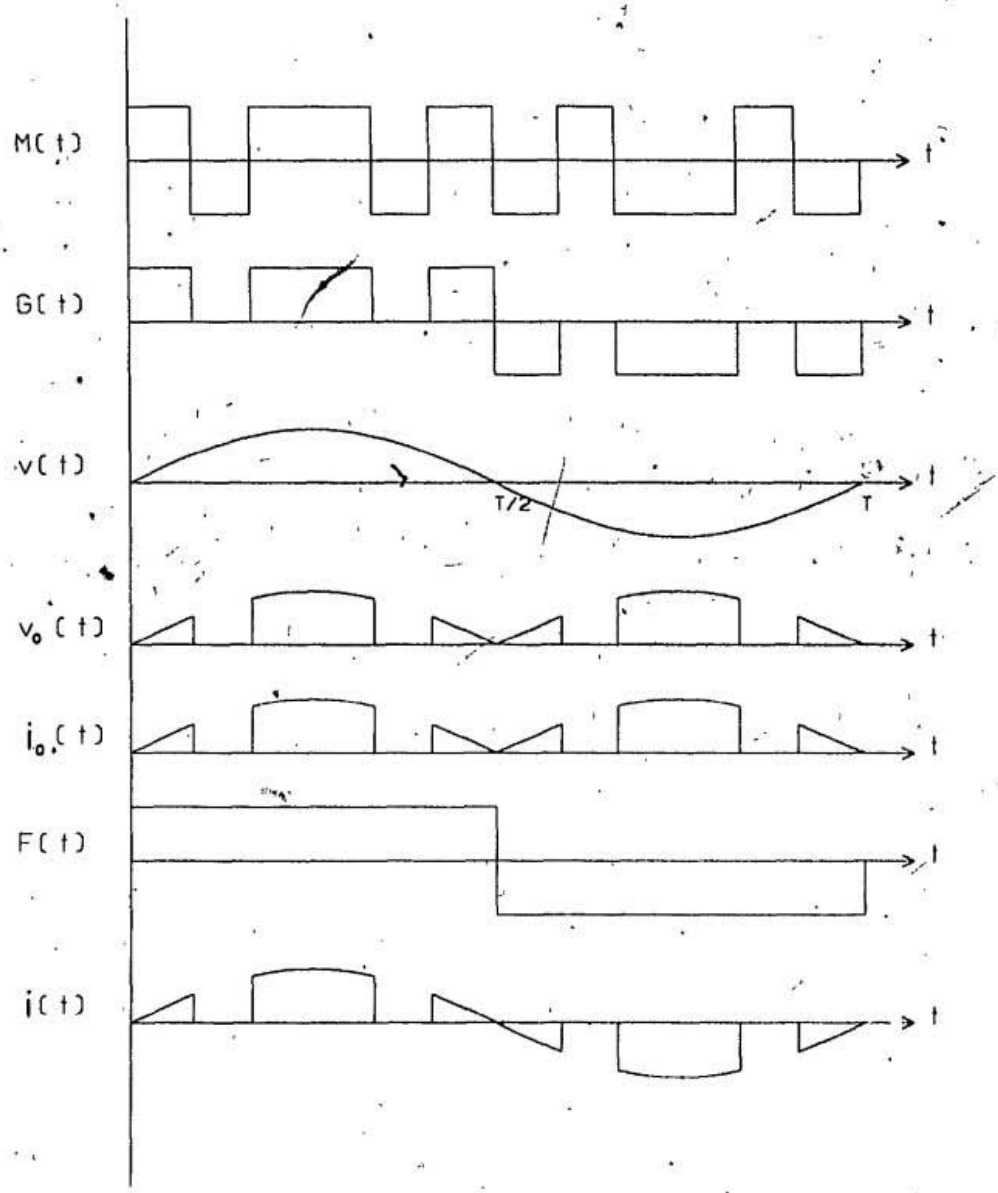


Figure 3.2: Graphical illustration for defining converter waveforms in terms of general switching functions

The Fourier series expression for the output current $i_o(t)$ is given by

$$i_o(t) = \frac{1}{T} \sum_{-\infty}^{\infty} d_n \, e^{jn\omega_o t} \tag{3.7}$$

$$d_n = \frac{c_n(\omega t)}{Z(\omega t)} \tag{3.8}$$

with $Z(\omega t)$ denoting the load impedance.

The input current waveform is defined in terms of the output current waveform and a squaring function $F(t)$,

$$i(t) = i_o(t) \cdot F(t) \tag{3.9}$$

where $F(t)$ serves the purpose of describing $i(t)$ in accordance with the converter switching function $G(t)$. The Fourier series representation of $i(t)$ is then obtained as

$$i(t) = \frac{1}{T} \sum_{-\infty}^{\infty} h_n \, e^{jn\omega_o t} \tag{3.10}$$

$$where \qquad h_n = \sum_{i=1}^{N_p} \int_{i=1,3,5,} i_o(t) \cdot F(t) \, e^{-jn\omega_o t} \tag{3.11}$$

To use the DFT approach, the converter waveforms have to be represented as discrete time sampled signals. This is accomplished by sampling $v_o(t)$ and $i_o(t)$ at a sufficiently high sampling frequency in conformance with the Nyquist sampling criterion [19]. The process results in the discrete Fourier transform representation of Equation (3.6) and (3.11) as

$$C(n) = \sum_{m=0}^{N-1} v_o(m) \, W^{mn} \qquad 0 \le n \le N-1 \tag{3.12}$$

$$H(n) = \sum_{m=0}^{N-1} i(m) \, W^{mn} \qquad 0 \le n \le N-1 \tag{3.13}$$

where

$v_o(m)$ is the sampled sequence representing $v_o(t)$ in the interval $0 \leq t \leq T$ and is bounded by $0 \leq m \leq N-1$

$i(m)$ is the sampled sequence representing $i(t)$ in the interval $0 \leq t \leq T$ and is bounded by $0 \leq m \leq N-1$

W is the root of unity $= e^{-j2\pi/N}$

$C(n)$ is the n^{th} DFT coefficient of $v_o(m)$

$H(n)$ is the n^{th} DFT coefficient of $i(m)$

The DFT coefficients are numerically computed using a Fast Fourier Transform (FFT) algorithm [30]. Solution of the FFT algorithm appropriately conveys information of the spectral contents in the waveforms. A listing of the program is provided in Appendix B.

3.2 Single Phase DM Converter with Resistive Load

Simulated results of the DM converter for a resistive load and an average output voltage of $V_o = .5$ pu are shown in Figs. 3.3(A) and 3.3(B) for two switching frequencies. It is evident that the converter performance is strictly related to the delta modulator switching pattern. Since the same load demands can be met by different modulator parameters, it becomes imperative to optimize the delta modulator parameters before proceeding to analyse the performance of the controlled rectifier.

In order to optimize the delta modulator a parametric variation of the DM circuit and its effects on the single-phase converter are investigated. The objective of the parametric study is to investigate the spectral contents of the converter

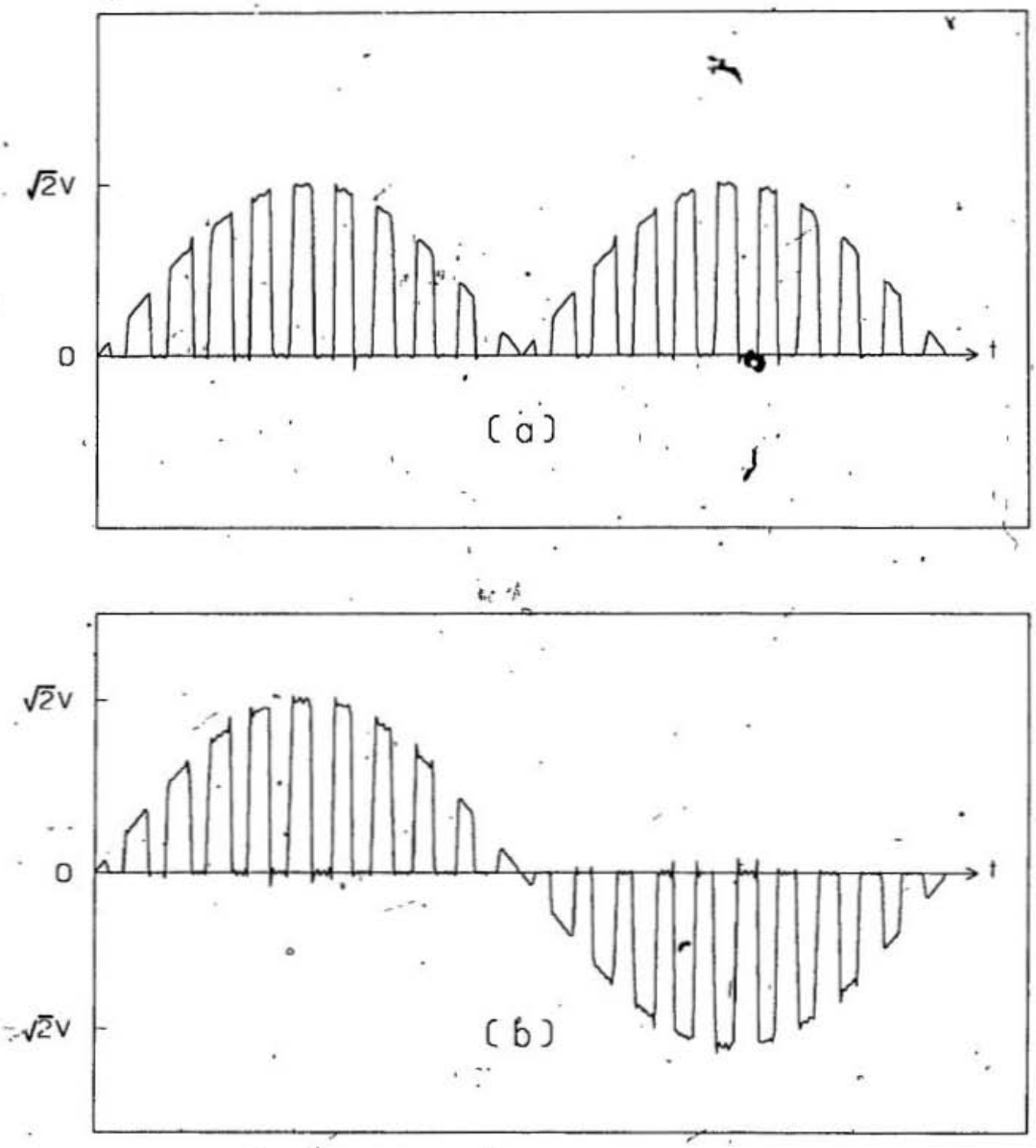


Figure 3.3: (A) Simulated converter waveforms: V_o =.5 pu, switching frequency = 1 kHz. (a) output voltage (b) input current

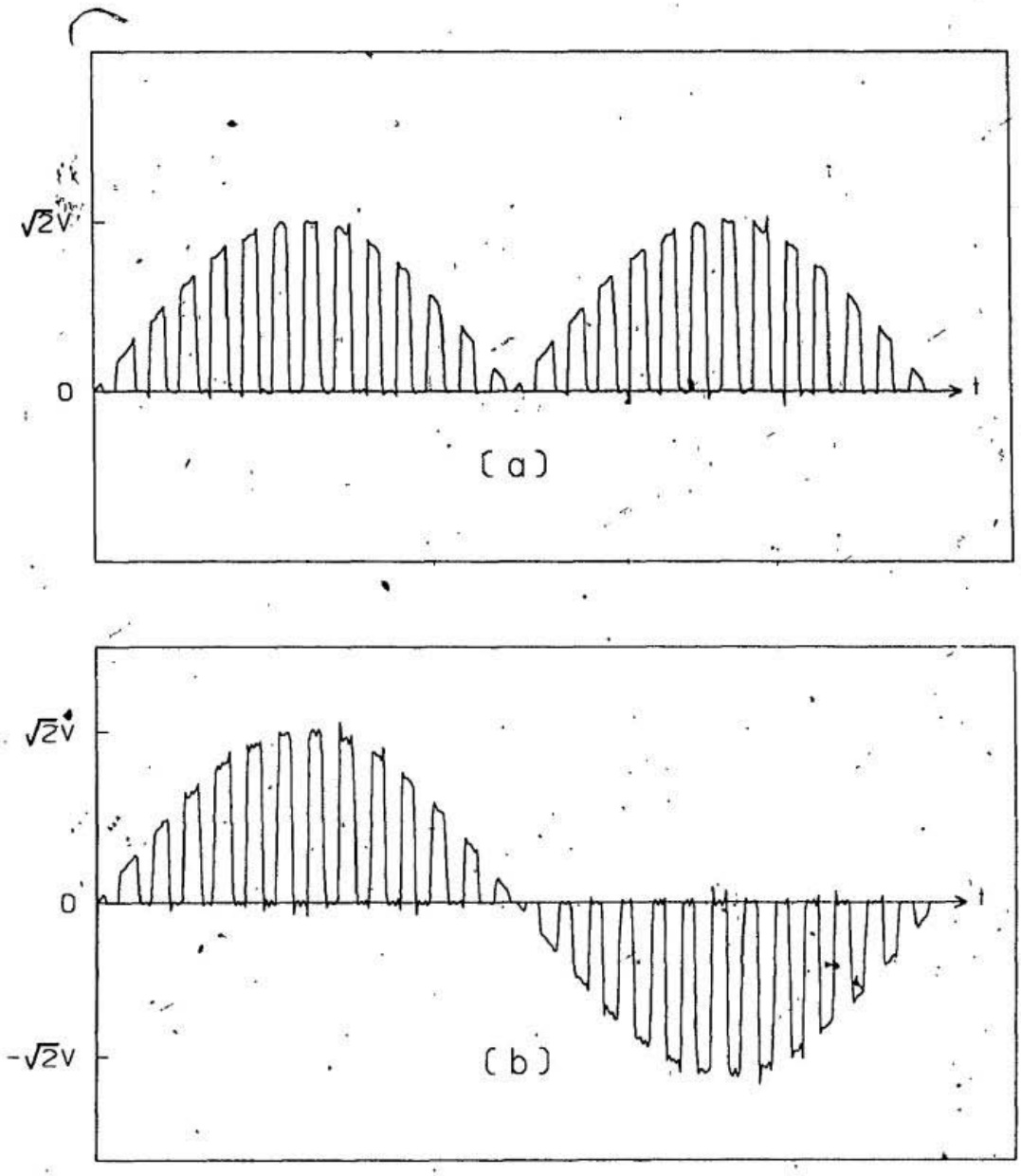


Figure 3.3: (B) Simulated converter waveforms: V_o =.5 pu, switching frequency = 1.5 kHz. '(a) output voltage (b) input current

waveforms for various modulator parameters. It is to be noted that the primary advantage of the PWM strategy is the improvement in the power factor. This study focuses on the spectral content and harmonic distribution in the input current waveform for the following conditions:

1. Variation in time constant
2. Variation in reference signal amplitude

Adaptive control PWM technique realized by the delta modulator results in the switching frequency of the modulated waveform being a function of the carrier ripple frequency. This is due to the fact that the carrier wave $v_C(t)$ is forced to oscillate within the hysteresis boundary, with each intersection of $v_C(t)$ and either the Δ_p or Δ_n boundary locating a switching pulse. As a result, the switching frequency of the converter is a function of the carrier slopes, amplitude of the reference signal and the window widths. Moreover, as is characteristic of PWM systems, the dominant harmonics in the modulated switching waveform appear near the ripple frequency of the carrier wave. This phenomenon is investigated for the DM system from the view point of being able to predict the spectral contents of the converter waveforms for various modulator parameters.

3.2.1 Variation in Time Constant

In the circuit implementation of the delta modulator as shown in Fig.2.6, the positive and negative slopes of $v_C(t)$ are determined by the time constant, $\tau = R_T C_T$ of integrator A_2 for fixed Δ_p and Δ_n values. Variation in τ has the desired effect of changing the slopes of $v_C(t)$, which in turn determine the ripple frequency of the carrier waveform. The analysis implicitly assumes that the ripple frequency

is synchronized with the sinusoidal reference signal. However, it should be noted that absolute synchronization between the two signals does not exist for all operating conditions. As Δ_p and Δ_n are controlled in the ADC scheme, the fundamental period of the carrier waveform may deviate from that of the sinusoidal reference signal. Nevertheless the modulated switching waveform is periodic and exhibits half wave symmetry for all Δ_p and Δ_n values. To ensure synchronization i.e. equal periodicity between the carrier and sinusoidal reference signals, time constant τ must be sufficiently small allowing the carrier ripple frequency to be much greater than the nominal 60 Hz. reference signal frequency.

The range of variation of τ is determined by the slope overload condition and optimum converter performance. The maximum value of τ is dictated by the slope overload condition such that $\tau = \tau_{max}$; when

$$\left.\begin{array}{ll} M_p = \omega_m V_R & \text{for rising slope in } v_C(t) \\ M_n = \omega_m V_R & \text{for falling slope in } v_C(t) \end{array}\right\} \tag{3.14}$$

where ω_m = radian frequency of $v_R(t)$.

V_R = amplitude of $v_R(t)$

The lower limit of τ can be set to a desired value to obtain optimum converter performance.

Figures 3.4(a)–(d) depict the harmonic distribution in the input current waveform as τ is varied from the maximum value to lower values with all other parameters held constant. The pu value of τ is expressed as:

$$\tau_{pu} = \frac{R_T C_T}{T_m} \tag{3.15}$$

where $T_m = 2\pi/\omega_m$. Parametric variation in τ results in the following observation:

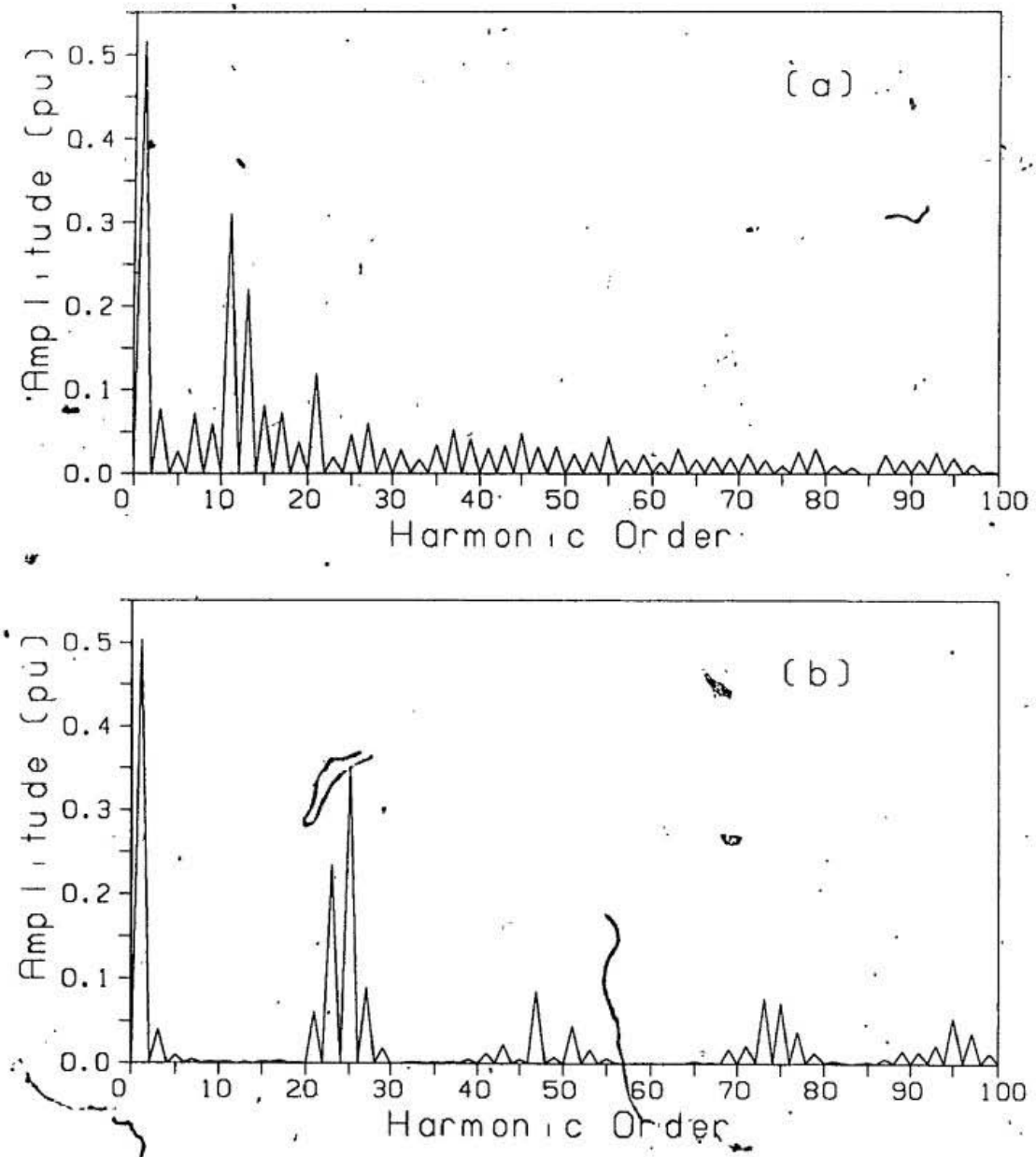


Figure 3.4: Simulated input line current spectrum of single phase DM converter. $\Delta_p = .5V$, $\Delta_n = .5V$, $V_R = 2.5V$ (a) parameter $\tau = .2$ pu (b) parameter $\tau = .1$ pu

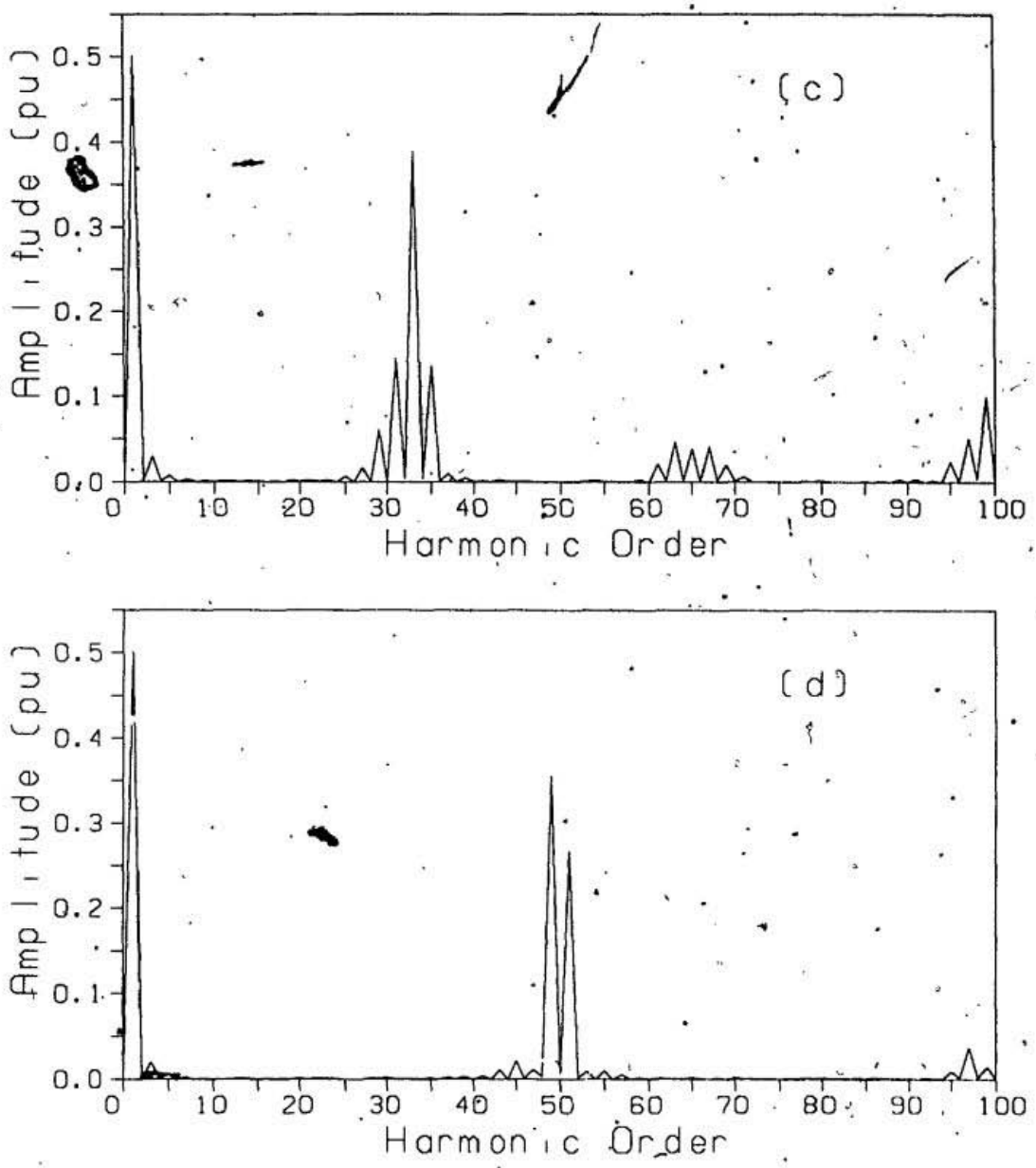


Figure 3.4: continued: (c) parameter $\tau = .075$ pu (d) parameter $\tau = .05$ pu

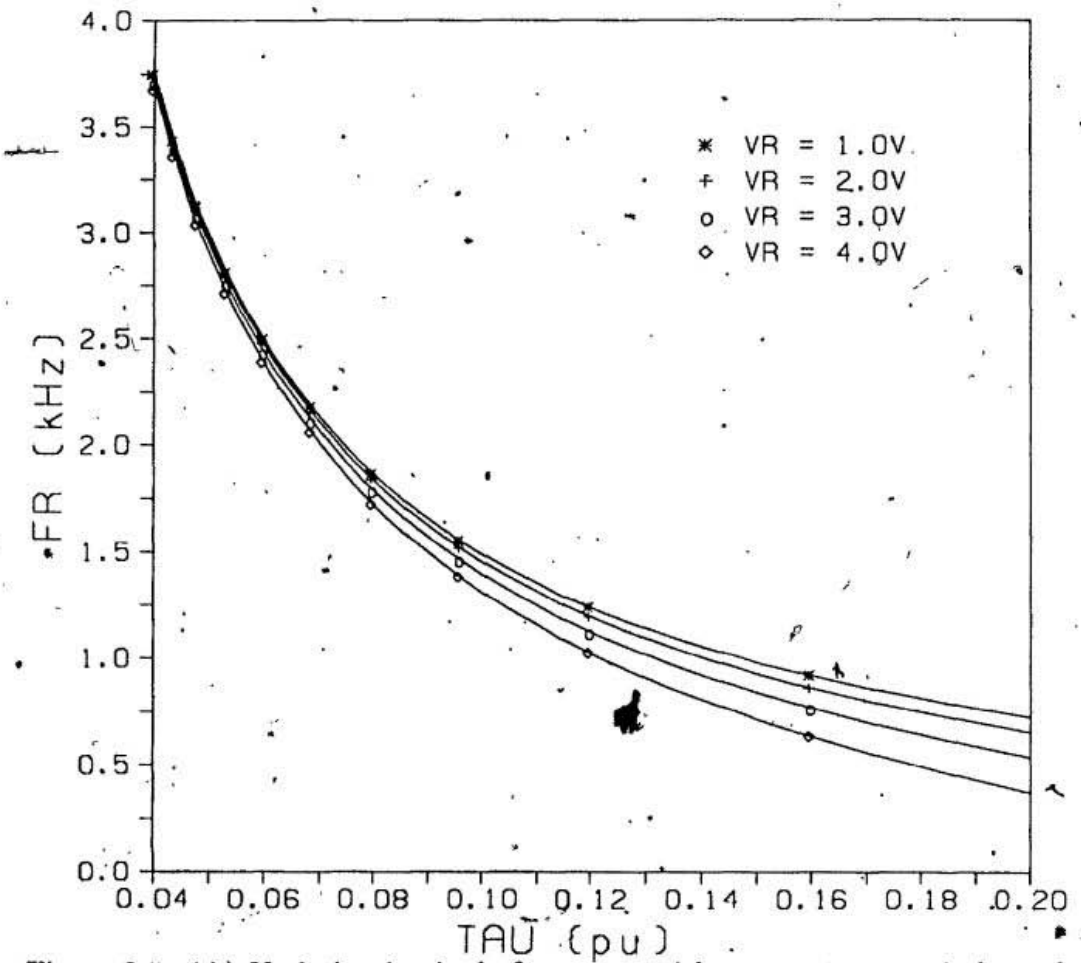


Figure 3.5: (A) Variation in ripple frequency with parameter τ as independent variable

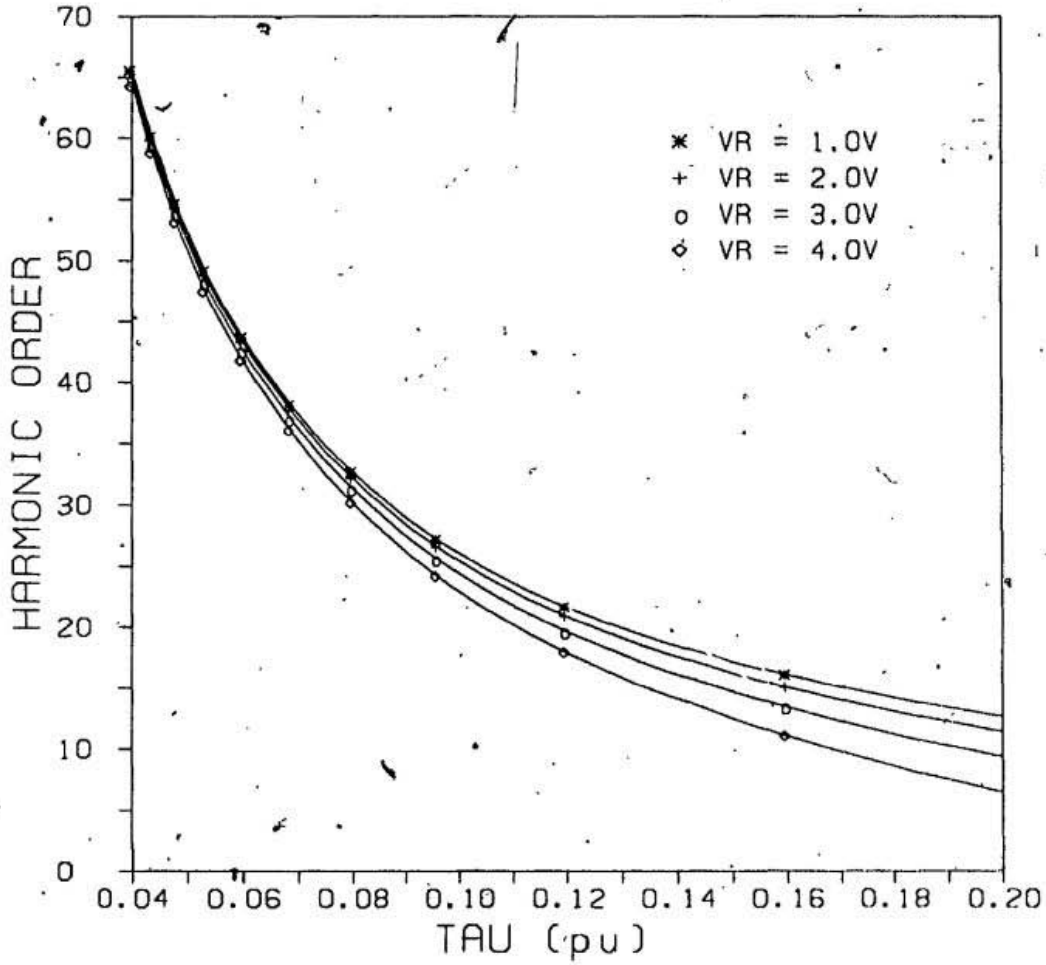


Figure 3.5: (B) Input current harmonic order as a function of parameter τ

1. As τ is decreased the dominant harmonics after the fundamental are shifted to higher frequencies. The amplitude of the fundamental component, however, remains constant for all τ.

2. Since the input current waveforms exhibits odd symmetry, only odd harmonics are present.

3. With decreasing τ, the ripple frequency of $v_C(t)$ increases.

The relationship between ripple frequency and τ, given by Equation (2.13) is shown in Fig. 3.5(A) for different reference signal amplitudes. The graph is indicative of the fact that for low τ values, variation in reference signal amplitude, V_R, has little effect on converter switching frequency. However, for large τ values, the magnitude of V_R has a more dramatic influence on converter switching frequency. Since dominant harmonics components are a function of converter switching frequency, it is possible to corelate the appearance of dominant harmonic components as a function of parameter τ for different V_R amplitudes. This is illustrated in Fig. 3.5(B) which shows the relationship between harmonic components in the input current waveform as a function of τ for different V_R amplitudes. Indeed, the order of dominant harmonic components can be predetermined from Fig. 3.5(B) for any value of τ. As a result, it is possible to select the ripple frequency by simply altering τ and in doing so, a direct control on the dominant harmonic component locations can be realized. By appropriately setting the value of the modulator time constant, lower order harmonics in the input current waveform can be eliminated. Although operating at high ripple frequencies result in high order dominant harmonics, the power conversion efficiency is adversely affected.

This is due to the fact that the switching frequency of the modulated waveform increases resulting in increased switching losses.

3.2.2 Variation in Reference Signal Amplitude

As seen in the previous section, the dominant harmonics are directly related to the ripple frequency of the carrier wave. Maximum ripple frequency occurs when the modulator is in the idle channel state, with the ripple frequency progressively decreasing with increasing reference signal amplitude. Figures 3.6(a)-(d) show the spectral contents in the input current waveform when V_R is increased from the idle channel condition to the slope overload condition. It is evident that the harmonic amplitudes after the fundamental component are related to V_R; higher V_R giving higher harmonic amplitudes, particularly in lower order harmonics. Figure 3.7 shows the relationship between V_R and ripple frequency for fixed Δ_p, Δ_n and τ values.

Increasing the reference amplitude has a detrimental effect on the harmonic content of the input current waveform owing to the decrease in the ripple frequency. Consequently, the input power factor is expected to be low, necessitating the use of a large filter to suppress low order harmonics. On the other hand, by the appropriate choice of τ, dominant low order harmonics can be shifted to higher frequencies. The strong coherence between ripple frequency and dominant harmonics obtained by the parameter τ, allows an easy optimization of the DM modulator. In fact, by maintaining V_R constant, the DM modulator can be designed to yield optimum performance for a preset value of time constant.

In PWM converter systems, it is customary to select the ripple frequency on

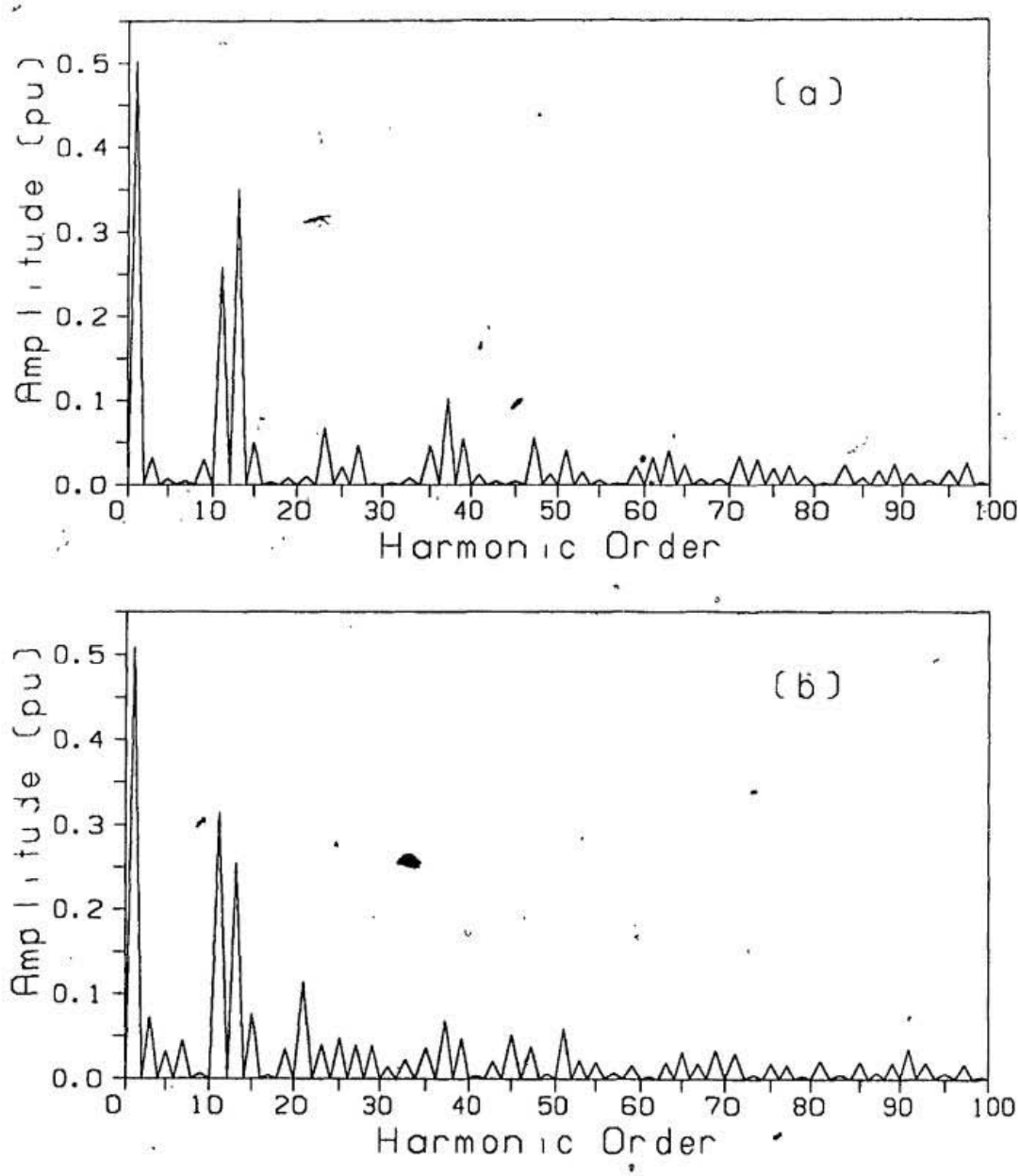


Figure 3.6: Simulated input line current spectrum of single phase DM converter. $\Delta_p = .5$V, $\Delta_n = .5$V, $\tau = .2$ pu (a) parameter $V_R = 1$V (b) parameter $V_R = 2$V

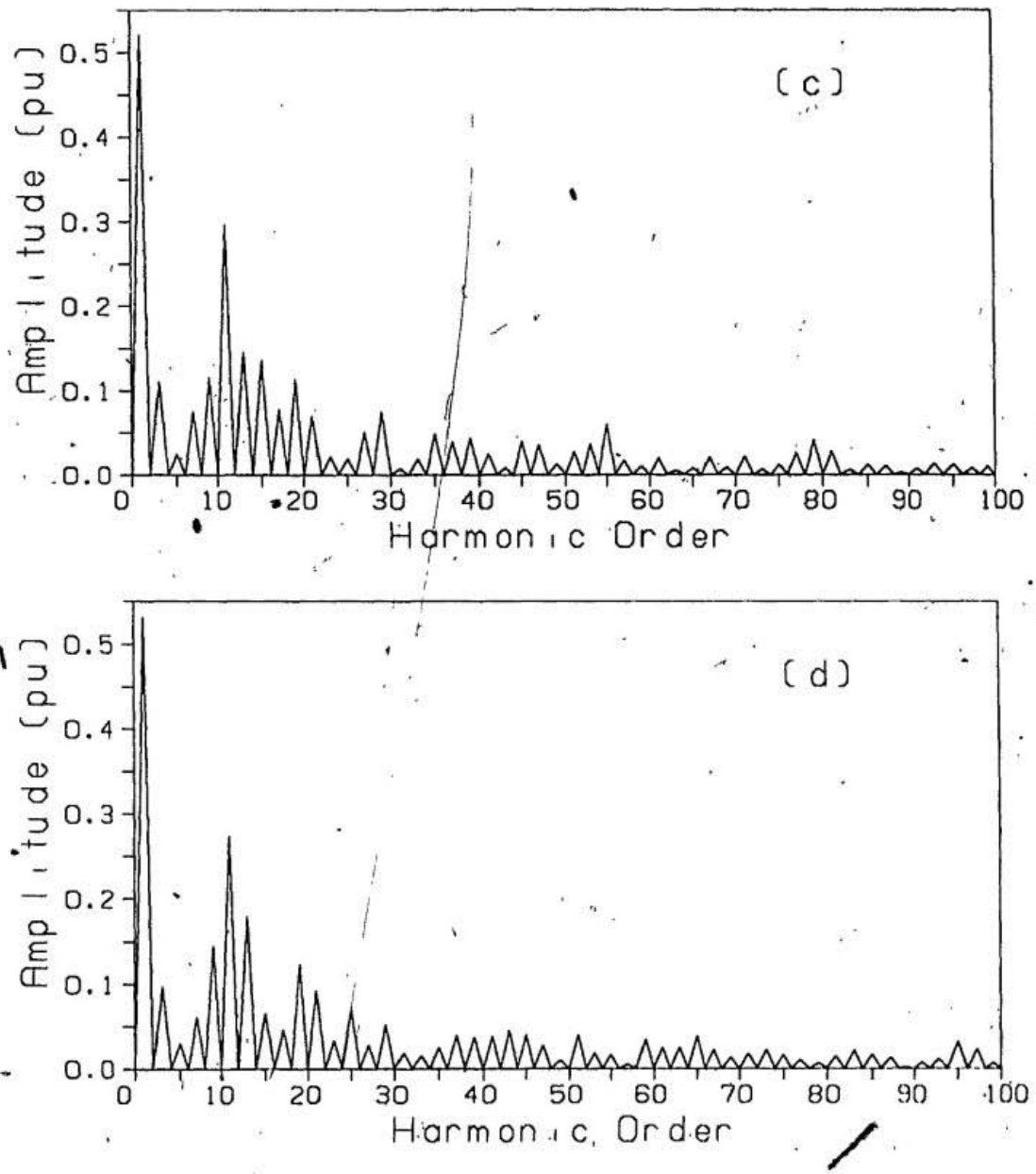


Figure 3.6: continued: (c) parameter $V_R = 3$V (d) parameter $V_R = 3.5$V

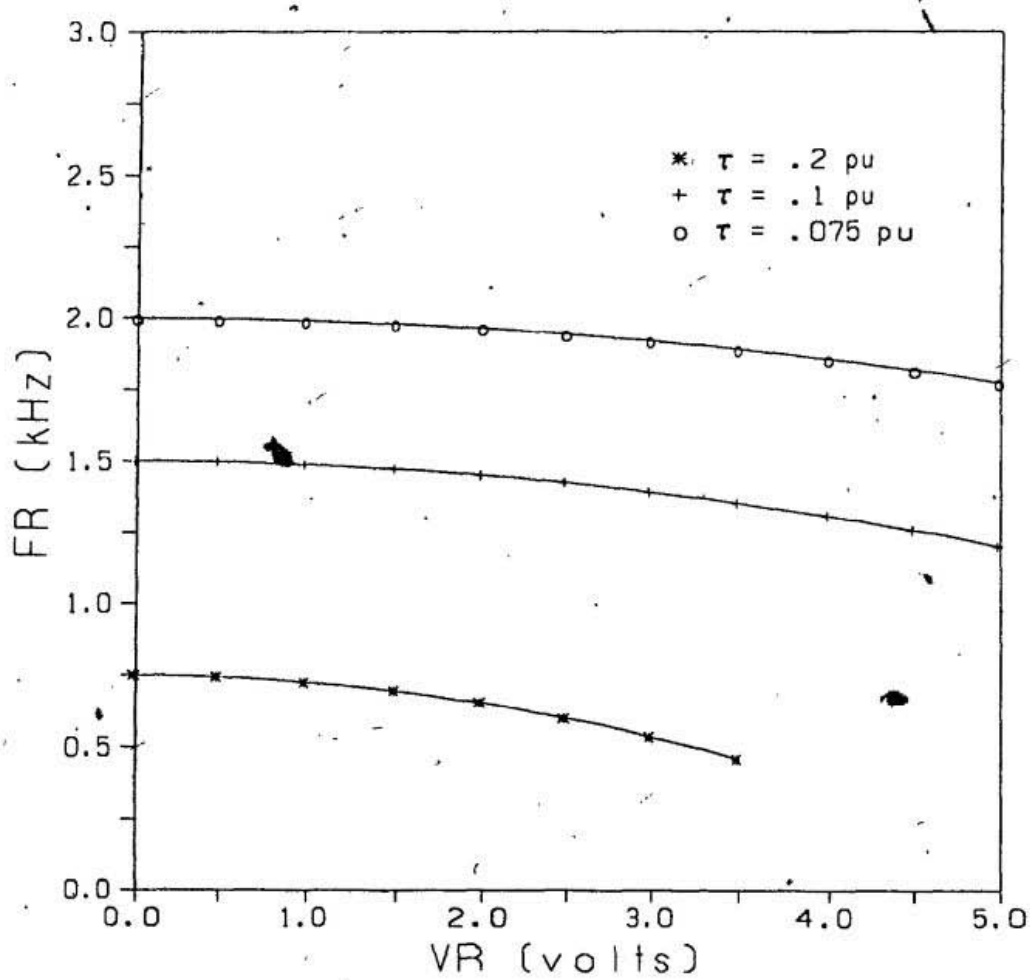


Figure 3.7: Ripple frequency as a function of reference signal amplitude

the basis of maximum allowable converter switching frequency. The number of commutations is an important parameter in any PWM system as an increase in commutation results in an increase in switching losses in the converter. Some applications, such as UPS systems, require the converter switching frequency to be as low as possible. Like other PWM strategies, the number of commutations in delta modulation depends on the ripple frequency of the carrier wave. Because each ripple cycle corresponds to two transitions in the modulated wave, each of these transition points specifies a commutation instant. This allows the modulator to be designed to operate at a specified ripple frequency. Since the dominant harmonics in the supply current are easily determined by the harmonic analysis procedure, the input filter can also be designed to eliminate troublesome harmonics appearing near the ripple frequency.

3.3 Converter Performance

A theoretical analysis of the performance of the DM converter is undertaken using the DFT harmonic analysis procedure. Performance of the ac to dc conversion process is evaluated on the basis of harmonic currents injected into the ac supply line and the displacement between the voltage and current waveforms resulting from converter switching. Conventional parameters to assess the converter performance are defined as [3,5]

Input power factor:

$$PF = \frac{I_1}{\sqrt{I_1^2 + \sum_{n=2}^{\infty} I_n^2}} \cos\phi_1 \tag{3.16}$$

Distortion factor:

$$DTF = \frac{I_1}{\sqrt{I_1^2 + \sum_{n=2}^{\infty} I_n^2}} \tag{3.17}$$

Displacement factor:

$$DSF = \cos\phi_1 \tag{3.18}$$

where I_1 = rms fundamental component of phase current

I_n = rms value of n^{th} harmonic component

ϕ_1 = phase angle between supply voltage and I_1

In the DM converter, control of the output voltage is achieved by the ADC scheme, in which the window widths are set at different levels. Figure 3.8 shows the normalized values of Δ_p and Δ_n required to control the output voltage. The window widths are normalized with respect to the reference signal amplitude.

As Δ_p and Δ_n are controlled, the ripple frequency of the carrier wave changes. For any value of τ, maximum converter switching frequency occurs when Δ_p and Δ_n are symmetrical about the reference signal. For $\Delta_p = \Delta_n$, the converter gives a characteristic output voltage of 0.5 pu. However, as the output voltage is decreased ($\Delta_p < \Delta_n$) or increased ($\Delta_p > \Delta_n$) from the mid point value, the ripple frequency decreases. Hence, the number of commutations over the control range does not remain fixed but changes in accordance with the ripple frequency. Figure 3.9 shows the relationship between number of commutations per cycle with output voltage for various values of time constant.

The parameters given in Equations (3.16) – (3.18) are evaluated over the control range of the output voltage. In calculating the converter parameters, all harmonics up to the maximum ripple frequency are taken into consideration.

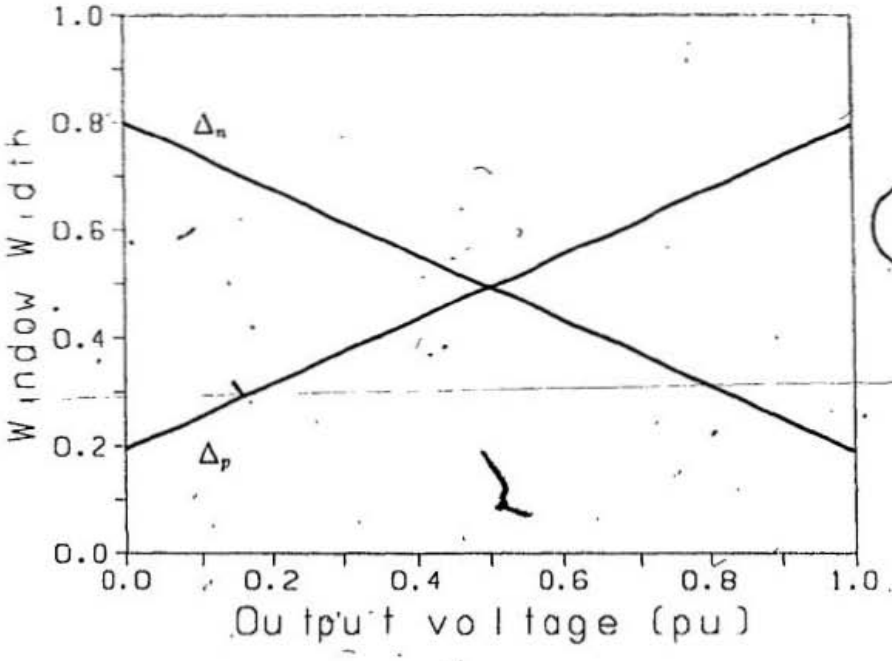


Figure 3.8: Normalized Δ settings required to control output voltage

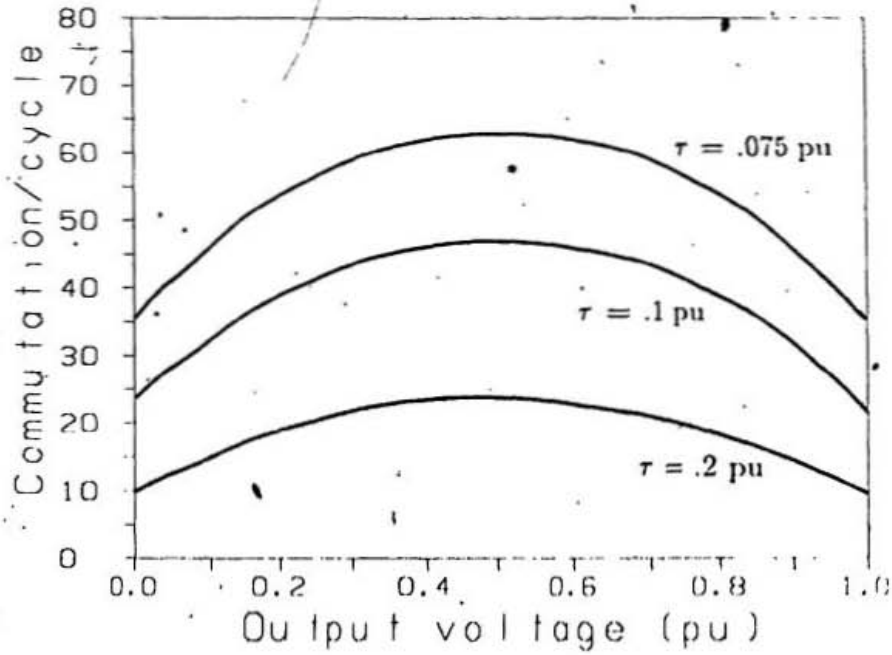


Figure 3.9: Number of commutations per cycle versus average output voltage with τ as a parameter

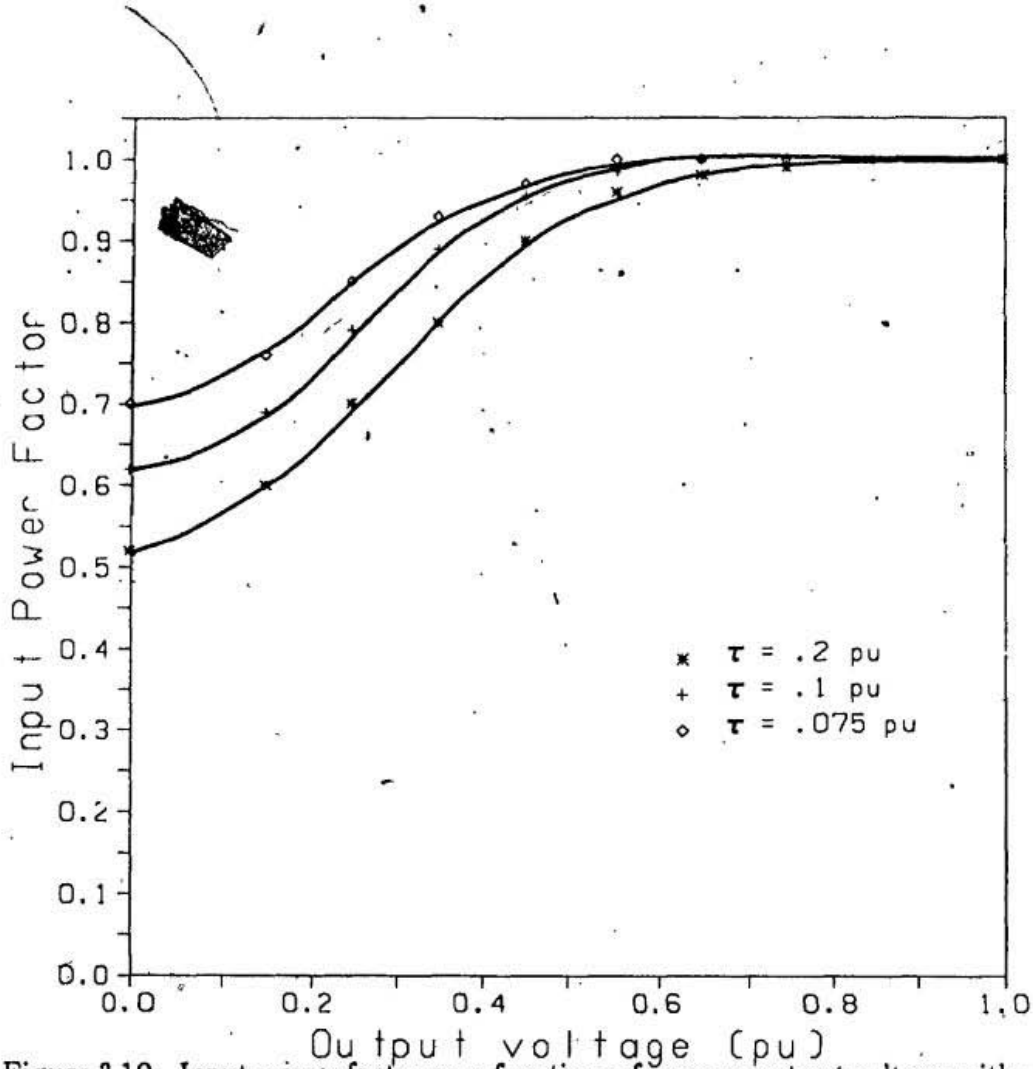


Figure 3.10: Input power factor as a function of average output voltage with τ as a parameter (single phase DM converter)

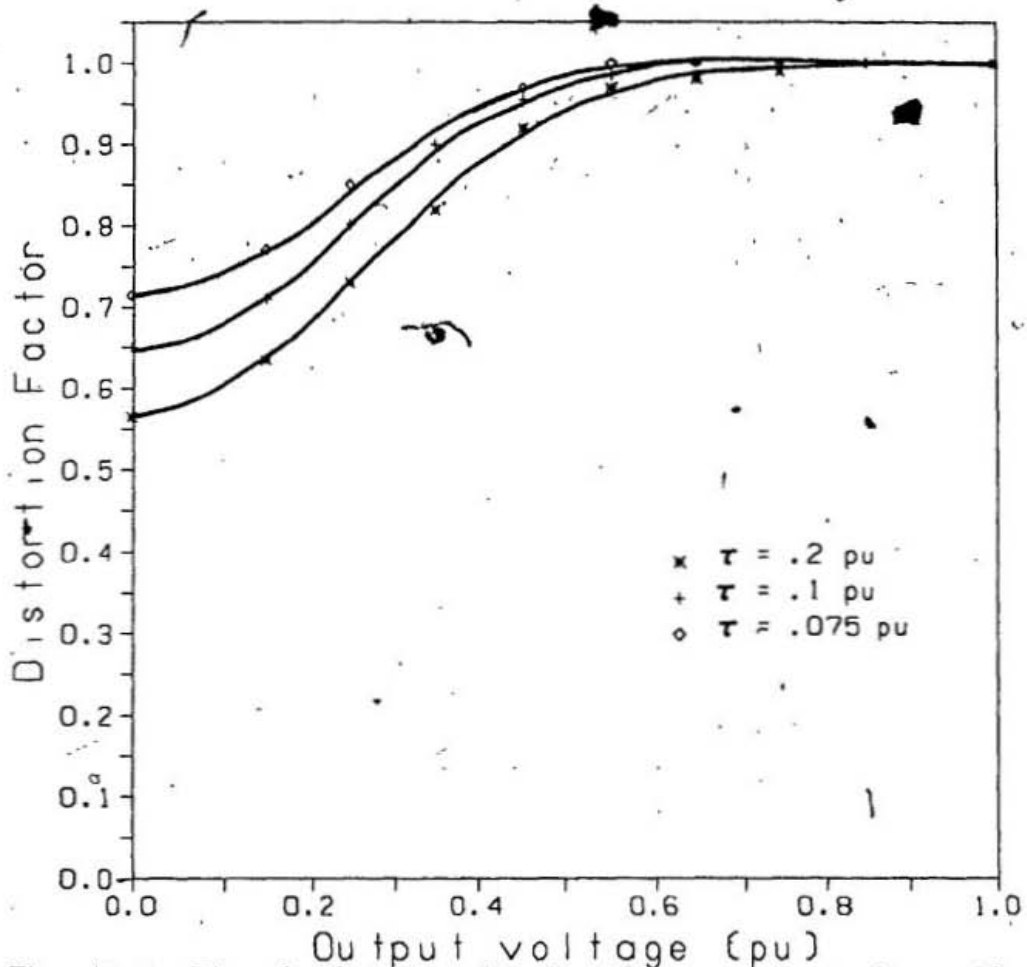


Figure 3.11: Distortion factor as a function of average output voltage with τ as a parameter (single phase DM converter)

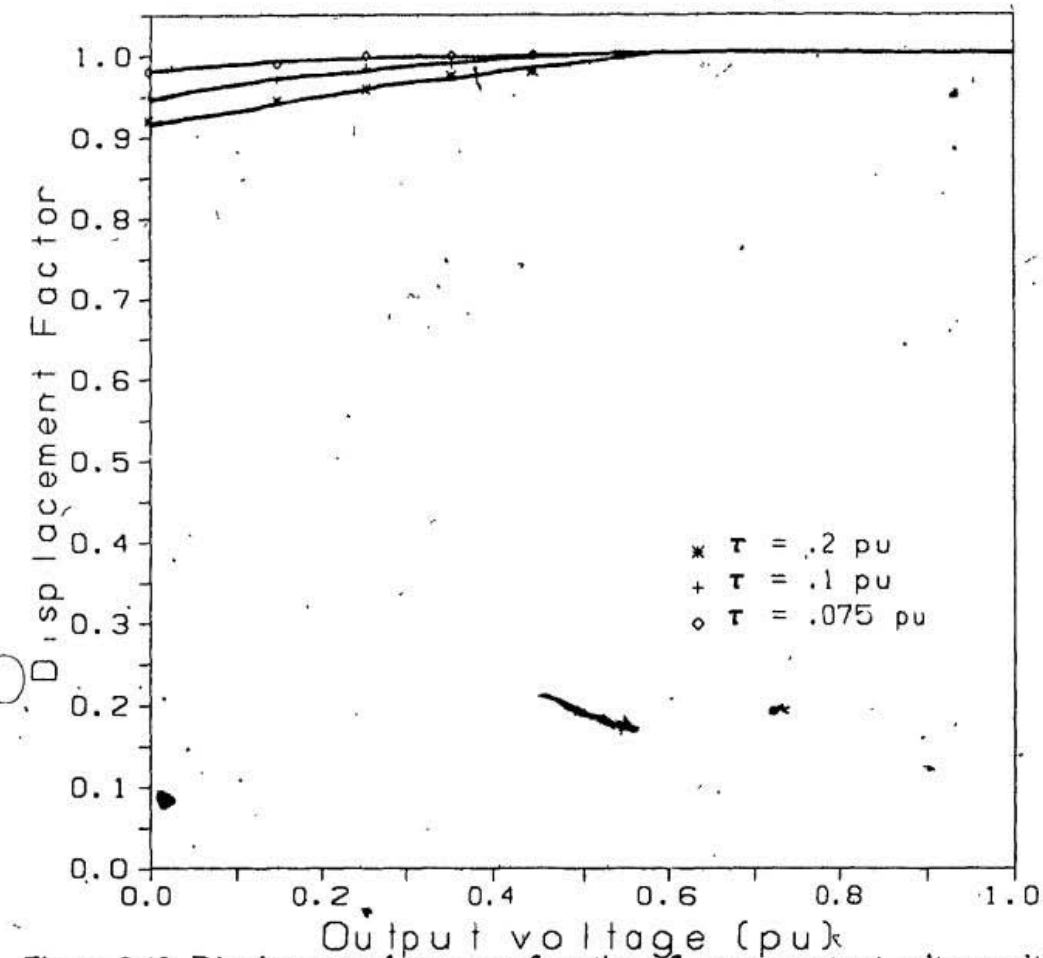


Figure 3.12: Displacement factor as a function of average output voltage with τ as a parameter (single phase DM converter)

Theoretical results of input power factor of the DM converter for three cases of maximum ripple frequency specified by modulator time constant settings of τ = .2 pu, .1 pu and 0.075 pu are shown in Fig. 3.10. The maximum ripple frequency corresponding to the three subject cases are 725 Hz, 1.45 kHz and 1.95 kHz respectively. As expected, superior performance is attainable at low τ values due to the high ripple frequency and virtually no harmonics present in the input current below the ripple frequency. Figure 3.11 shows the variation in distortion factor as a function of average output voltage. At low output voltage levels, the ripple frequency decreases and consequently, the input current harmonic content increases. Hence, the distortion factor is low but progressively improves as the output voltage increases. Again, minimum τ results in substantial improvement in distortion factor over the control range. However, the displacement factor is close to unity for all cases as shown in Fig. 3.12.

3.4 Experimental Verification of Converter Performance

In this section the validity of the predicted results presented in the previous section is verified experimentally. Implementation of the logic circuit and the delta modulator parameters selected are described in detail. Harmonics in the input current waveform are analysed with the aid of a spectrum analyser and the converter performance parameters for various operating conditions are tabulated.

3.4.1 Implementation of the Logic Circuit

Figure 3.13 shows the schematic diagram of the experimental single-phase DM converter. Before the output of the modulator can be fed to the bridge converter, it has to be processed via appropriate logic circuit to obtain the correct gating signals for the converter switching elements. A logic circuit was designed to accomplish the task of processing the DM switching signal and providing the transistor gating signals synchronized with the ac supply line. The block diagram of the logic circuit is illustrated in Fig. 3.14 and the resulting transistor timing diagram is shown in Fig. 3.15.

The circuit parameters of the basic delta modulator of Fig. 2.6 are set at

$$R_1 = 10K\Omega$$

$$R_2 = 100K\Omega$$

$$C_T = 0.068\mu F.$$

the value of R_T is adjusted to give maximum number of commutations per cycle of 25, 50 and 65 obtained when $\tau = 0.2, 0.1, 0.075$ pu, respectively. The output

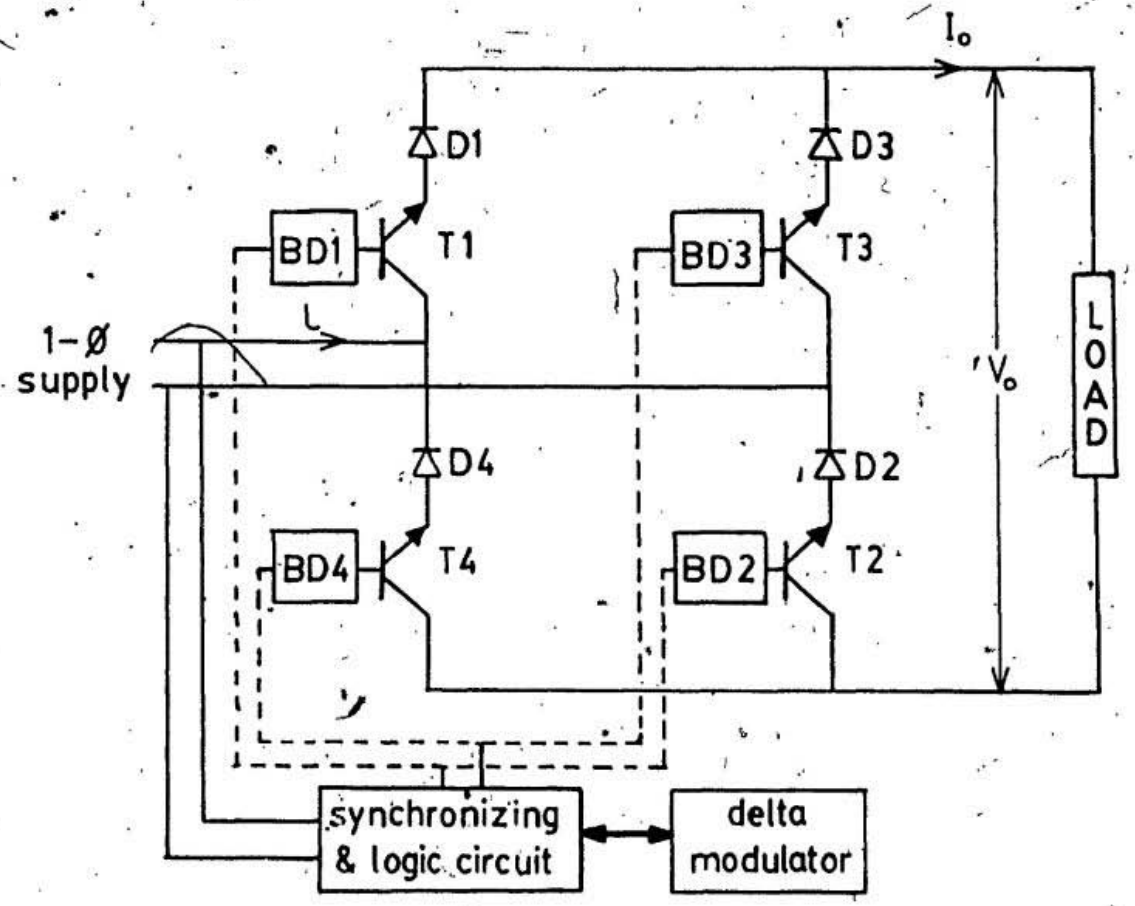


Figure 3.13: Single phase transistor DM converter

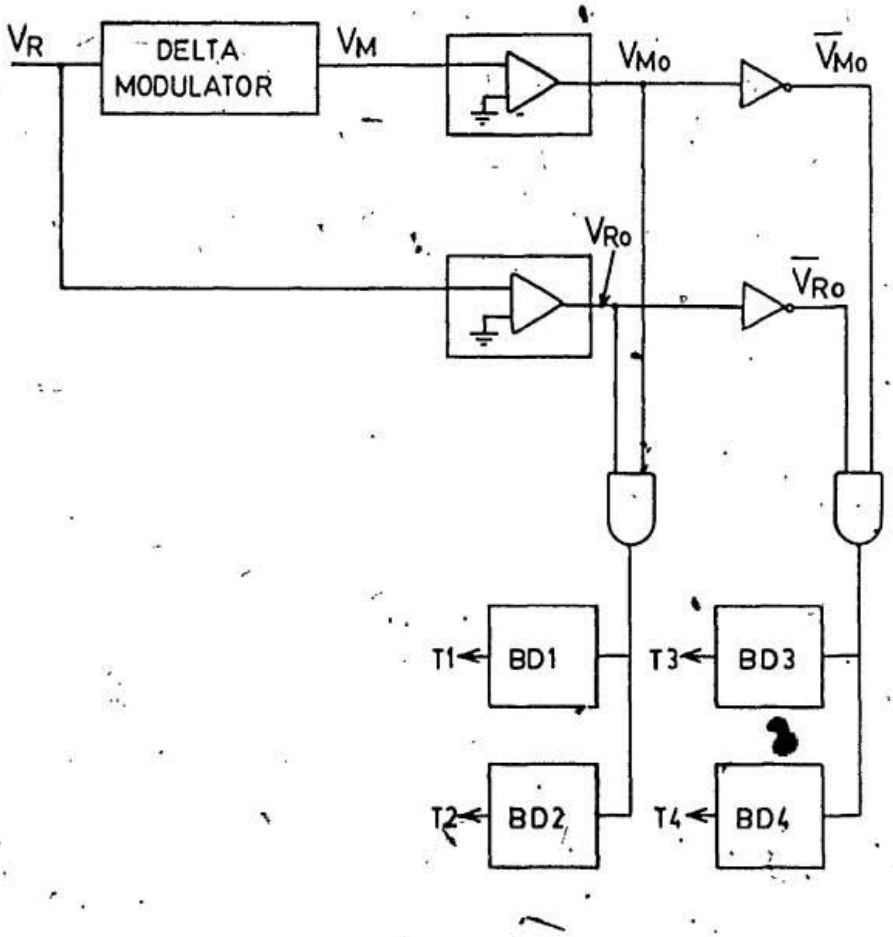


Figure 3.14: Block diagram of logic circuit for single phase DM converter

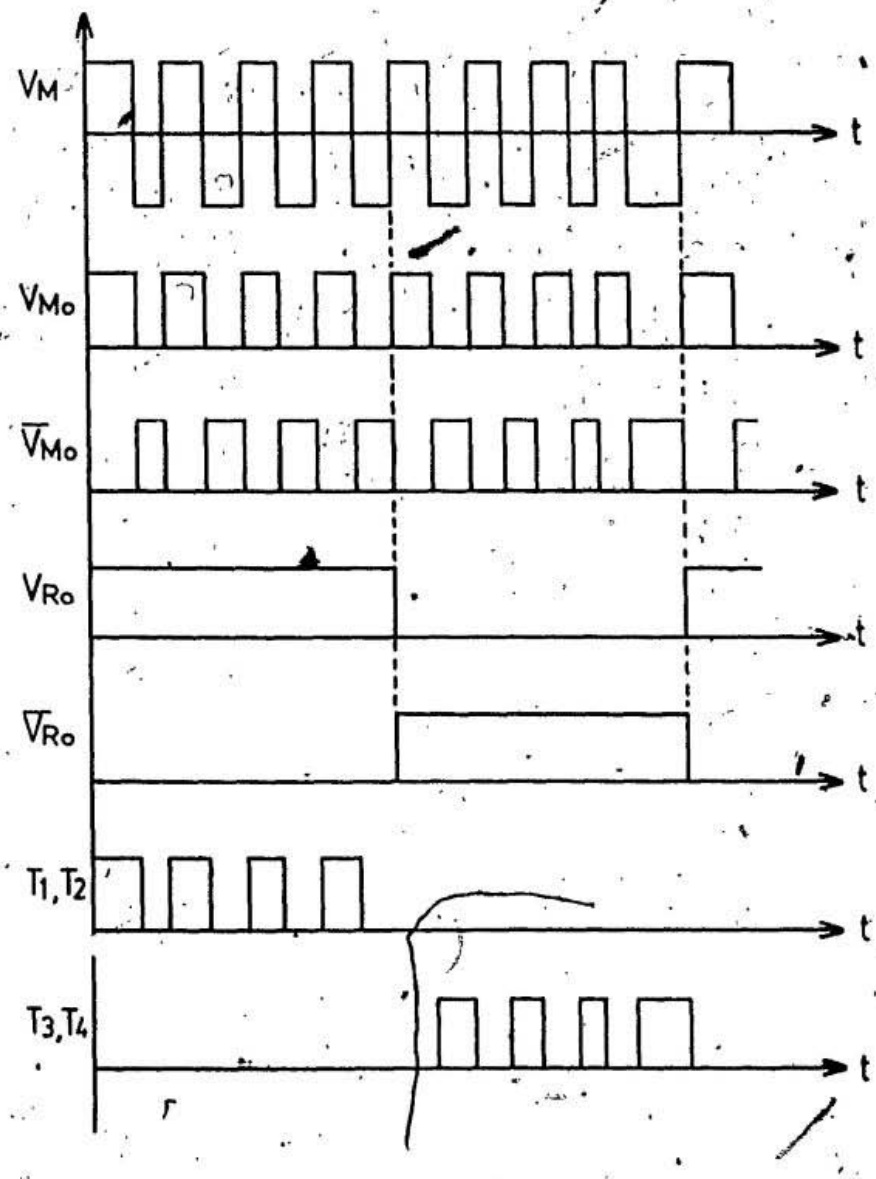


Figure 3.15: Timing diagram of single phase DM logic circuit

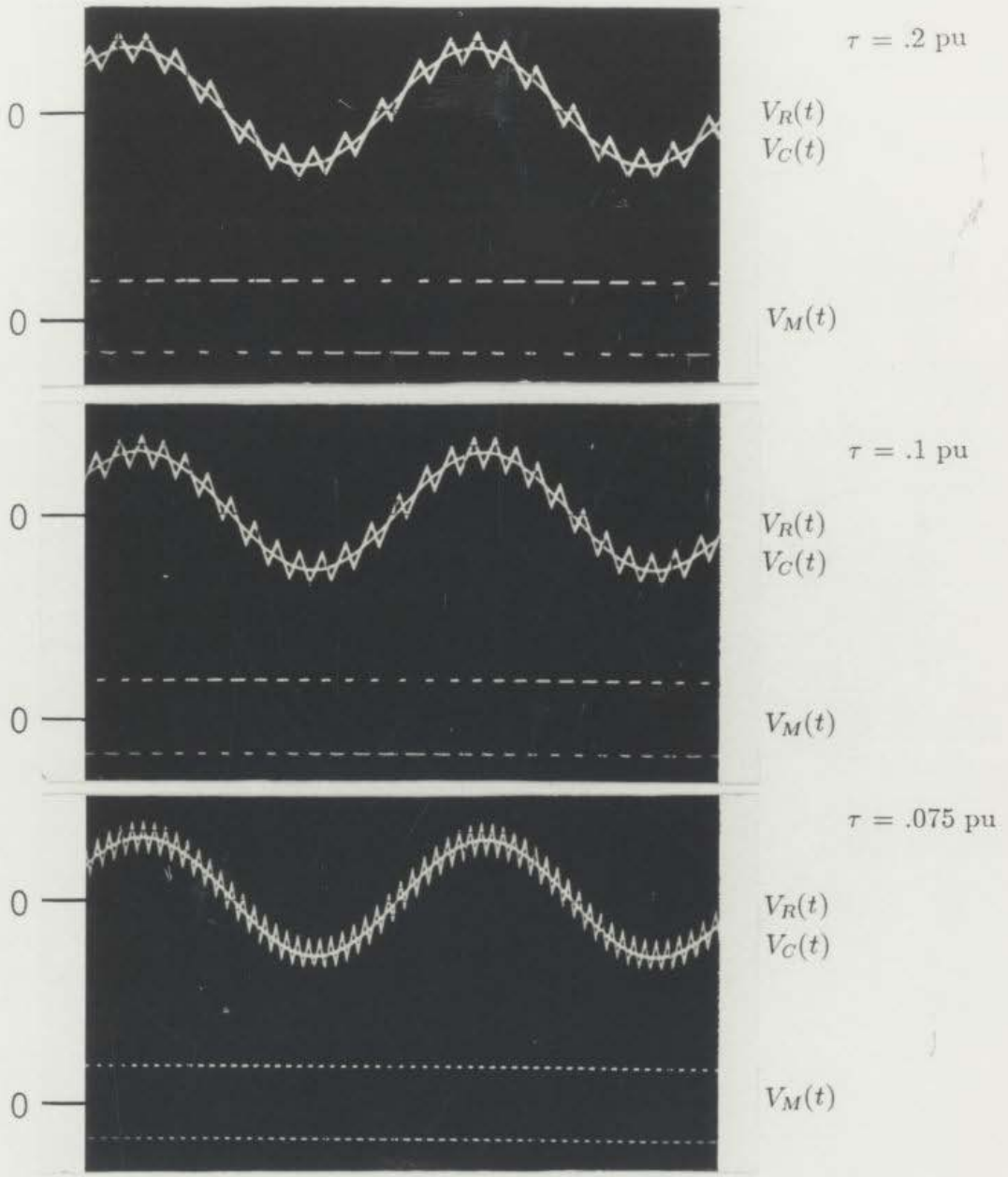


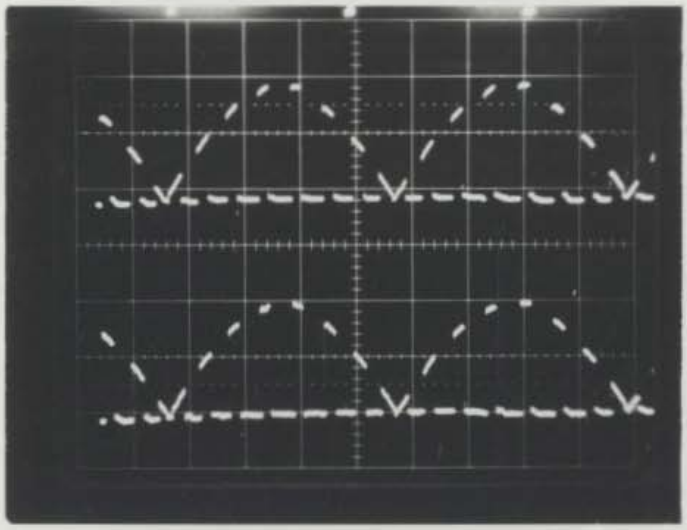
Figure 3.16: Experimental oscillograms illustrating key waveforms of delta modulator (based on 60 Hz. operation). $V_R = 1.5$V peak, $\Delta_p = \Delta_n = .5$V

of the modulator for the three cases of maximum number of commutations with $\Delta_p = \Delta_n$ are depicted in the oscilloscope pictures of Fig. 3.16.

3.4.2 Experimental Results

The power module of the single-phase DM converter prototype consists of four bipolar power transistors configured in a bridge. Detail design parameters of the power circuit are given in Appendix D. The supply voltage was maintained at 50 volts (rms). The load consisted of a resistive bank with an equivalent load impedance of 250Ω. The converter waveforms for a modulator setting of $\tau = 0.1$ pu. are exhibited in the following oscillograms. Figs 3.17(a)–(f) pertain to the converter output voltage waveforms for different load voltage values. Experimentally, it was found that the delta modulator allowed continuous control of the output voltage in the range 0.2 pu to 0.95 pu. Typical oscillograms for the input current waveform are illustrated in Figs. 3.18(a)–(f).

Harmonics in the input current waveform were analysed with a digital spectrum analyser (Wavetek, model: 5820A). The harmonic profile at various average output voltage values are given in oscillograms of Figs. 3.19(a)–(f). The experimental oscillograms substantiate the theoretical analysis and the predicted frequency range of dominant harmonic components.

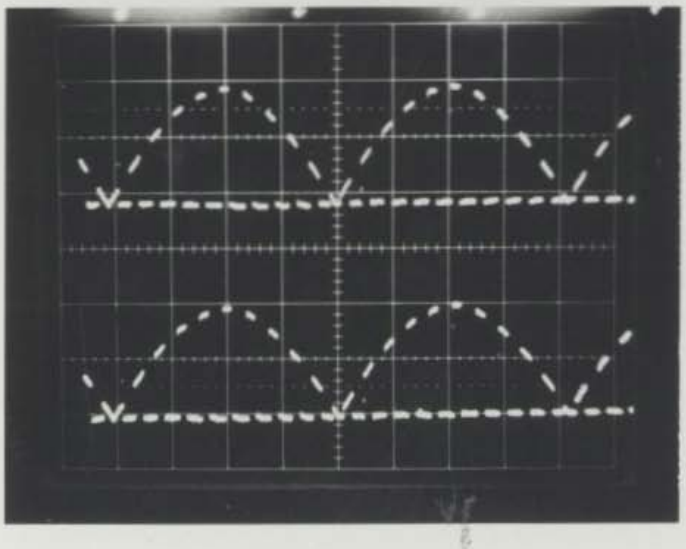


Vo = 0.2 pu

Output Voltage:
25 V/div

(a)

Output Current:
.1 A/div



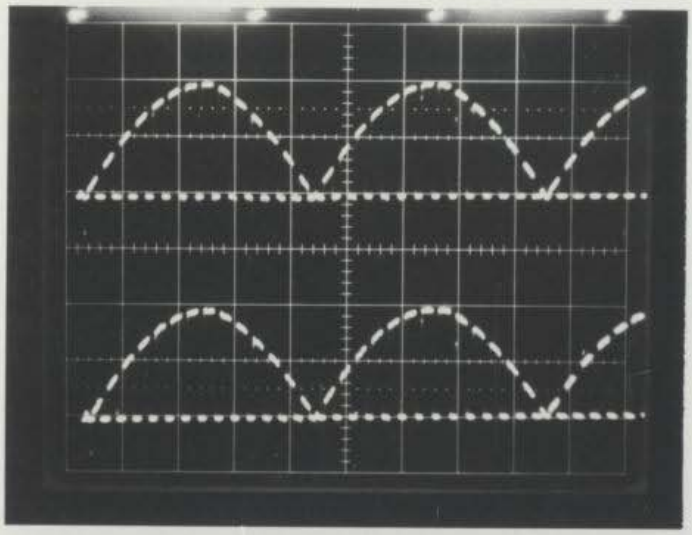
Vo = 0.4 pu

Output Voltage:
25 V/div

(b)

Output Current:
.1 A/div

Figure 3.17: Experimental oscillograms of single phase DM converter: Output voltage and output current waveforms

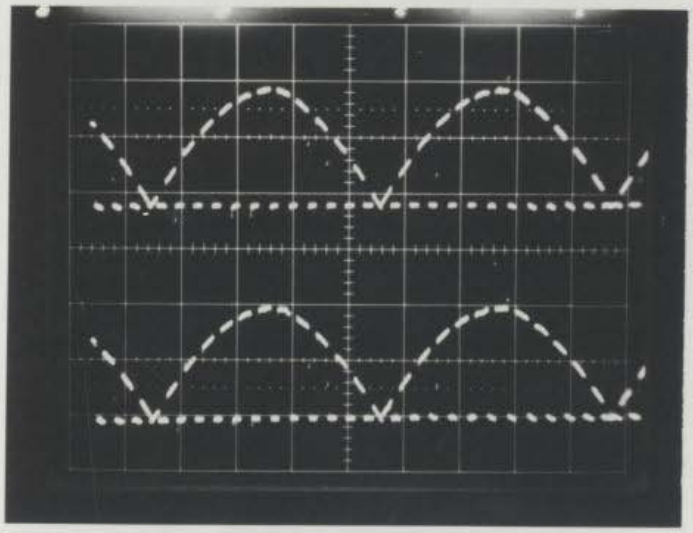


Vo = 0.5 pu

Output Voltage:
25 V/div

(c)

Output Current:
.1 A/div



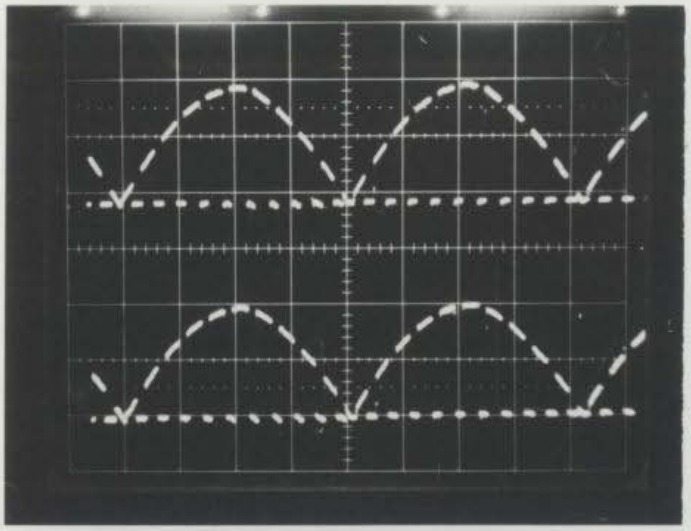
Vo = 0.6 pu

Output Voltage:
25 V/div

(d)

Output Current:
.1 A/div

Figure 3.17: continued

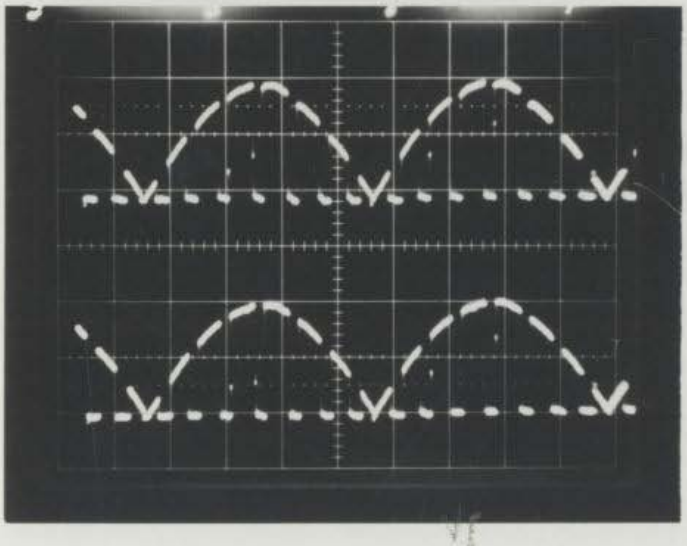


Vo = 0.7 pu

Output Voltage:
25 V/div

(e)

Output Current:
.1 A/div



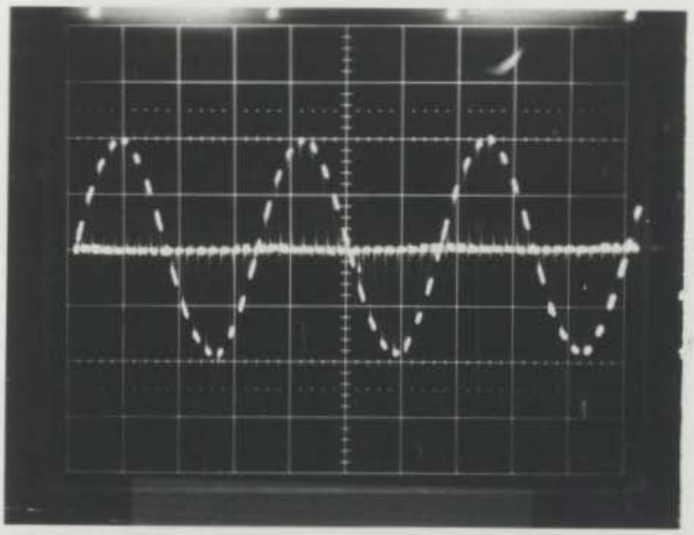
Vo = 0.8 pu

Output Voltage:
25 V/div

(f)

Output Current:
.1 A/div

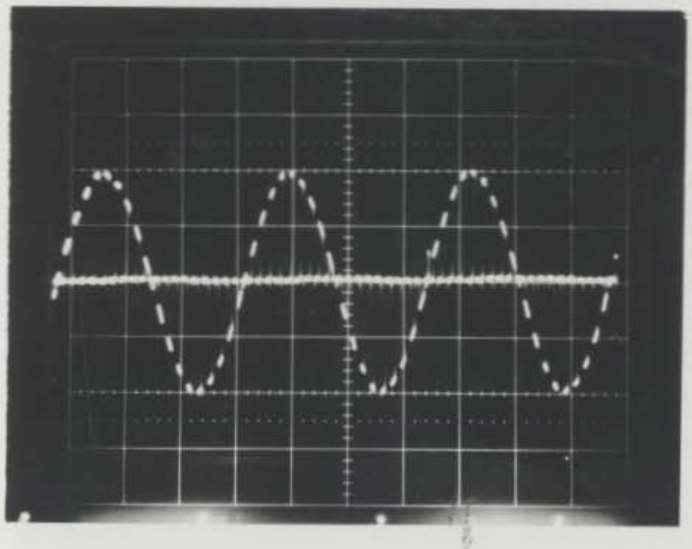
Figure 3.17: continued



For Io = 0.2 pu

Vertical scale:
.1 A/div

(a)

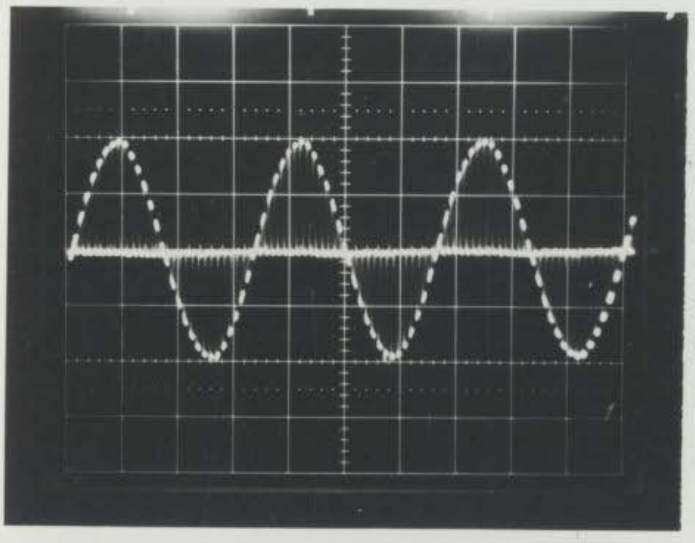


For Io = 0.4 pu

Vertical scale:
.1 A/div

(b)

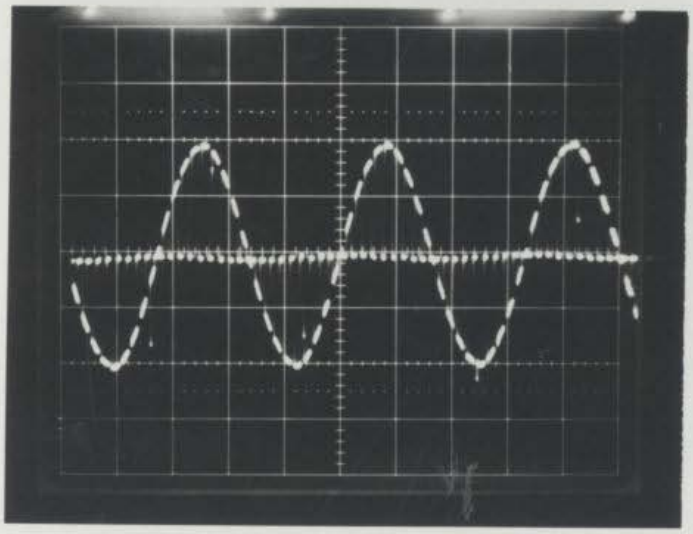
Figure 3.18: Experimental oscillograms of single phase DM converter: Input current waveforms



For Io = 0.5 pu

Vertical scale:
.1 A/div

(c)

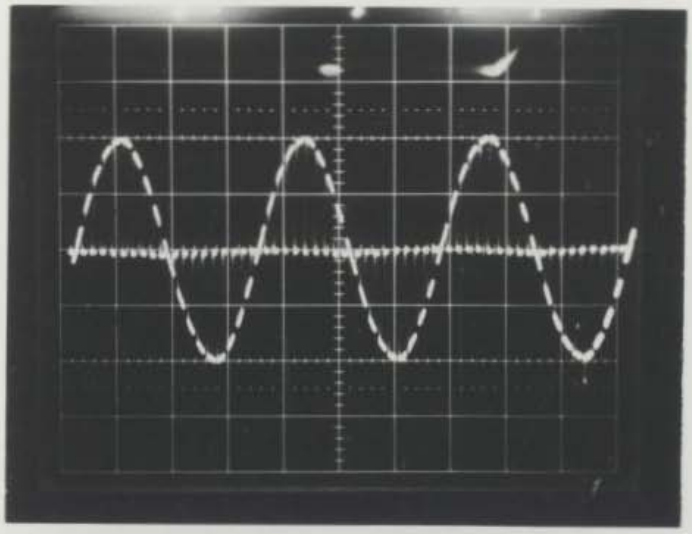


For Io = 0.6 pu

Vertical scale:
.1 A/div

(d)

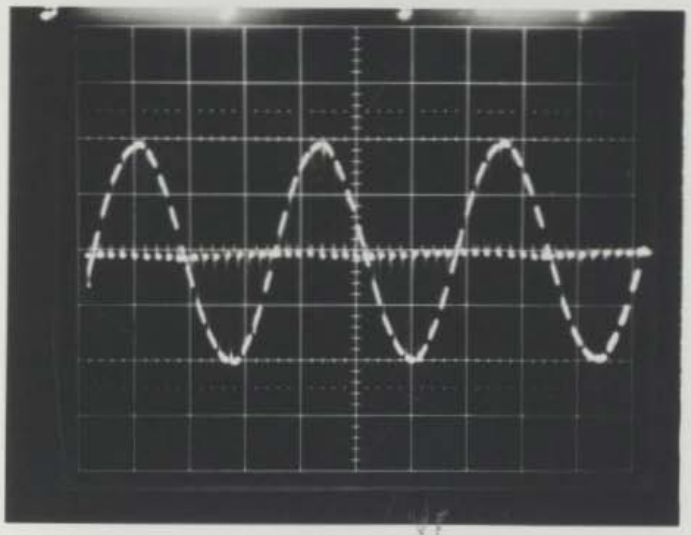
Figure 3.18: continued



For Io = 0.7 pu

Vertical scale:
.1 A/div

(e)

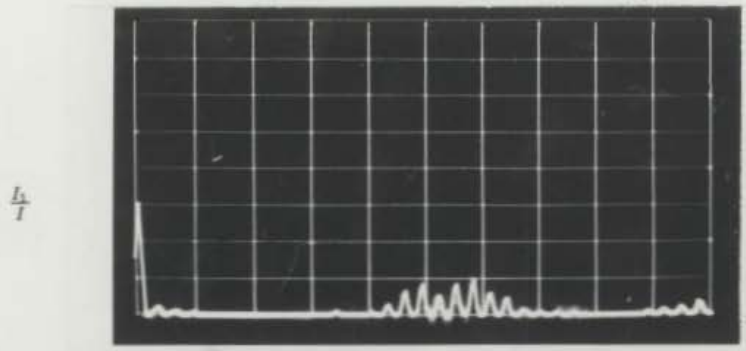


For Io = 0.8 pu

Vertical scale:
.1 A/div

(f)

Figure 3.18: continued

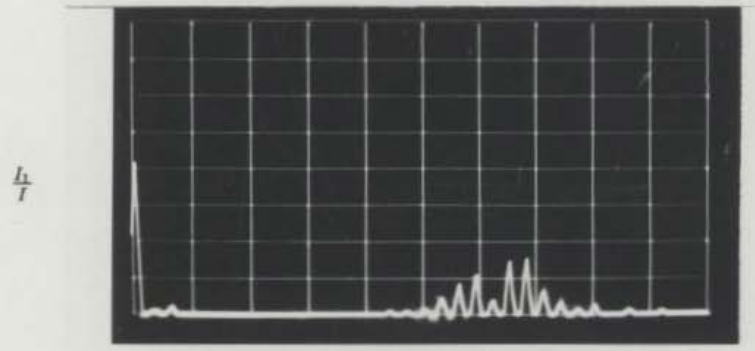


For Io = 0.3 pu

(a)

$\frac{I_1}{I}$

span: 50 - 2050 Hz

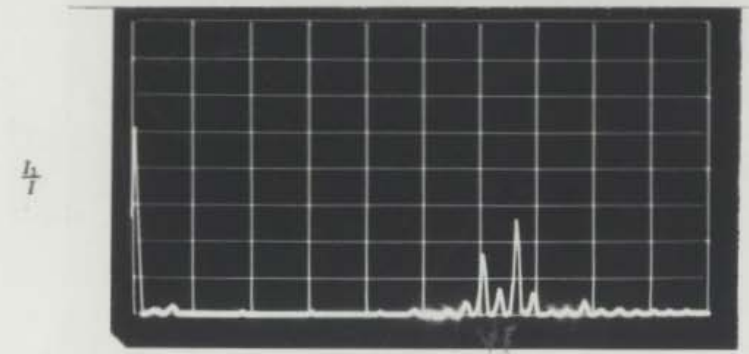


For Io = 0.4 pu

(b)

$\frac{I_1}{I}$

span: 50 - 2050 Hz



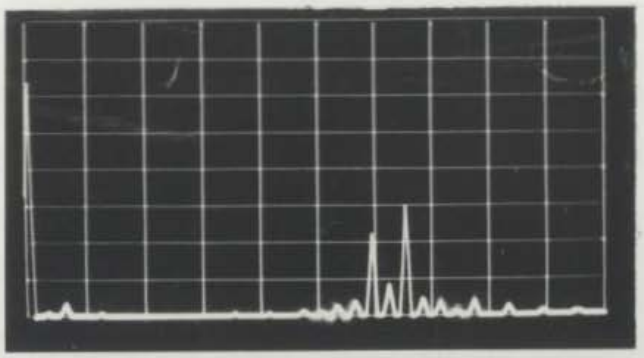
For Io = 0.5 pu

(c)

$\frac{I_1}{I}$

span: 50 - 2050 Hz

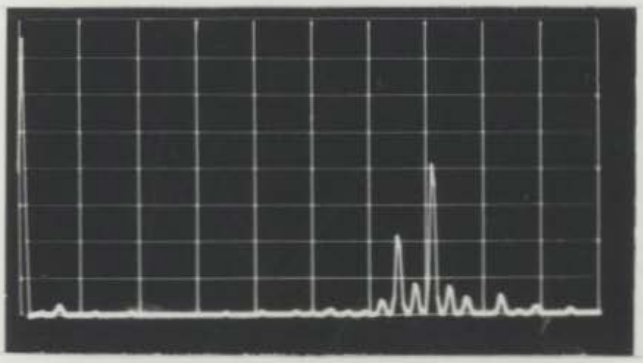
Figure 3.19: Experimental oscillograms of single phase DM converter: Input current harmonic spectra



For Io = 0.6 pu

(d)

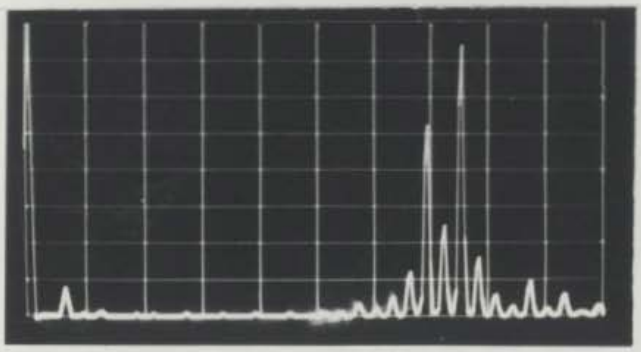
span: 50 - 2050 Hz



For Io = 0.75 pu

(e)

span: 50 - 2050 Hz



For Io = 0.8 pu

(f)

span: 50 - 2050 Hz

Figure 3.19: continued

3.4.3 Experimental Performance of Single Phase Converter

The single-phase DM converter was subjected to a series of experimental tests for different modulator settings of $\tau = .2, .1, .075$ pu., so as to investigate the actual performance of the converter for various switching frequencies.

The harmonic profile of the input current waveform for each experimental test with the pertinent modulator settings are recorded in Tables 3.1, 3.2 and 3.3 respectively. Performance parameters; input power factor, distortion factor and displacement factor based on experimental results are given in the following tables.

Table 3.1: Experimental frequency spectra and calculated performance parameters of single phase DM converter for $\tau = .2$ pu

Average Output Voltage (pu)	Harmonic Current (pu)						DTF	DSF	PF
	1	3	5	7	9	11			
.20	.201	.008	.03	.18	.19	.004	.63	.94	.59
.30	.303	.02	.01	.05	.18	.26	.70	.97	.68
.40	.40	.04	.02	.03	.06	.31	.77	.98	.75
.50	.50	.03	.008	.005	.03	.25	.90	.99	.89
.60	.601	.026	.009	.012	.046	.30	.90	1.00	.90
.70	.70	.025	.016	.04	.11	.28	.91	1.00	.91
.80	.801	.016	.031	.18	.26	.11	.93	1.00	.93
.90	.905	.07	.10	.21	.07	.09	.94	.98	.92
.95	.95	.04	.09	.23	.19	.10	.94	1.00	.94

Table 3.2: Experimental frequency spectra and calculated performance parameters of single phase DM converter for $\tau = .1$ pu

Average Output Voltage (pu)	Harmonic Current (pu)										DTF	DSF	PF
	1	3	5	9	11	13	15	17	19	21			
.20	.202	.03		.01	.01	.02	.16	.08	.01	.01	.76	0.98	.74
.30	.30	.03		.01		.03	.085	.10	.07	.09	.84	1.0	.84
.40	.41	.03			.01	.02	.05	.09	.12	.08	.90	1.0	.90
.50	.51	.03			.005	.01	.02	.05	.18	.09	.94	1.0	.94
.62	.62	.04				.01	.03	.04	.22	.10	.94	1.0	.94
.75	.75	.03				.01	.03	.21	.09	.09	.94	1.0	.94
.80	.80	.06				.01	.04	.28	.10	.08	.95	1.0	.95
.90	.90	.08	.02				.04	.06	.14	.31	.94	1.0	.94
.96	.96	.07	.03					.09	.11	.36	.94	1.0	.94

Table 3.3: Experimental frequency spectra and calculated performance parameters of single phase DM converter for $\tau = .075$ pu

Average Output Voltage (pu)	Harmonic Current (pu)											DTF	DSF	PF
	1	3	15	17	19	21	23	25	27	29	31			
.20	.20	.006	.006	.02	.06	.14	.11	.04	.01	.005	.003	.75	1.0	.75
.30	.302	.007				.004	.012	.06	.15	.09	.03	.85	1.0	.85
.40	.40	.01					.002	.007	.02	.07	.16	.92	1.0	.92
.50	.502	.01						.005	.01	.02	.08	.98	1.0	.98
.60	.60	.009							.009	.05	.15	.97	1.0	.97
.70	.70	.007						.006	.20	.13	.007	.96	1.0	.96
.80	.80	.004			.04	.20	.11	.03				.96	1.0	.96
.90	.901	.003		.12	.02	.11	.05	.08	.08			.97	1.0	.97
.96	.96	.003	.004	.09	.10	.13	.06	.03	.005			.97	1.0	.97

The experimental results demonstrate that the DM converter performs according to the theoretically predicted results. Dominant harmonics after the fundamental component are directly related to the converter switching frequency. Therefore, for $\tau = 0.075$ pu, which gives a switching frequency of approximately 2 kHz, dominant harmonic components are of higher orders compared with the case of $\tau = 0.2$ pu where the switching frequency is only 0.725 kHz. Correspondingly, the converter performance is better for $\tau = 0.075$ pu than for either case of $\tau = 0.1$ pu or $\tau = 0.2$ pu, respectively. These results suggest that the analytical model can be used to accurately determine converter performance.

3.5 Comparative Evaluation of DM Converter with Phase Controlled Converter

Phase angle control technique has been extensively used in many ac/dc converter configurations due to the simplicity and ease of control afforded by the natural commutation of thyristors. The performance of the phase controlled bridge rectifier is investigated and compared with the single-phase DM converter.

In the phase angle control (PAC) technique, control of the output voltage is achieved by varying the turn - on time at which the diagonally opposite thyristor pairs are allowed to conduct. The thyristors conduct for certain time segments of the ac waveform and are naturally commutated when the incoming ac voltage has a higher instantaneous value than the outgoing wave.

The thyristor turn - on time is commonly referred to in the literature [3,5] as the delay angle α. For the converter with a resistive load, the delay angle α can vary from 0 to π, with $\alpha = 0$ denoting the case of a full rectified sine wave. The

pertinent equations required to evaluate the performance of the bridge converter with a resistive load are given below [3]

average output voltage

$$V_o = \frac{\sqrt{2}V}{\pi}[1 + \cos\alpha] \tag{3.19}$$

rms value of input current

$$I = \frac{V}{R}\left[\frac{1}{\pi}\left[(\pi - \alpha) + \frac{1}{2}\sin 2\alpha\right]\right]^{\frac{1}{2}} \tag{3.20}$$

rms value of fundamental component I_1

$$I_1 = \frac{1}{\sqrt{2}}\left[a_1^2 + b_1^2\right]^{\frac{1}{2}} \tag{3.21}$$

$$a_1 = \frac{\sqrt{2}V}{\pi R}\left[(\pi - \alpha) + \frac{1}{2}\sin 2\alpha\right] \tag{3.22}$$

$$b_1 = \frac{\sqrt{2}V}{2\pi R}[\cos 2\alpha - 1] \tag{3.23}$$

fundamental displacement angle

$$\phi_1 = \tan^{-1}\left[\frac{b_1}{a_1}\right] \tag{3.24}$$

The performance parameters such as power factor, distortion factor and displacement factor of the phase controlled converter as α is controlled in the range $0 \leq \alpha \leq \pi$ are numerically computed using Equations (3.19)-(3.24). The results obtained are graphically illustrated in the subsequent figures along with typical results of the DM converter.

Power factor as a function of average output voltage for both converter systems under consideration is plotted in Fig. 3.20. In the case of the phase controlled

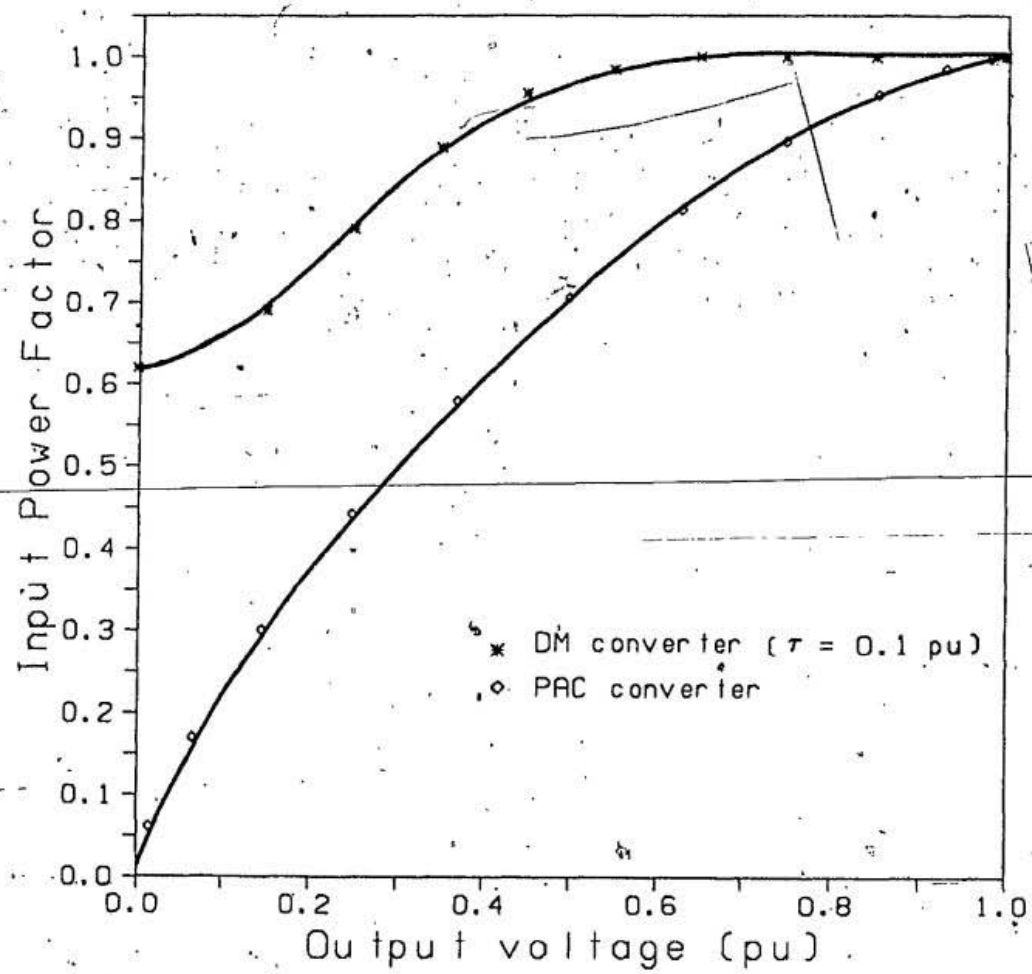


Figure 3.20: Comparison of power factor versus average output voltage for phase controlled bridge converter and DM converter

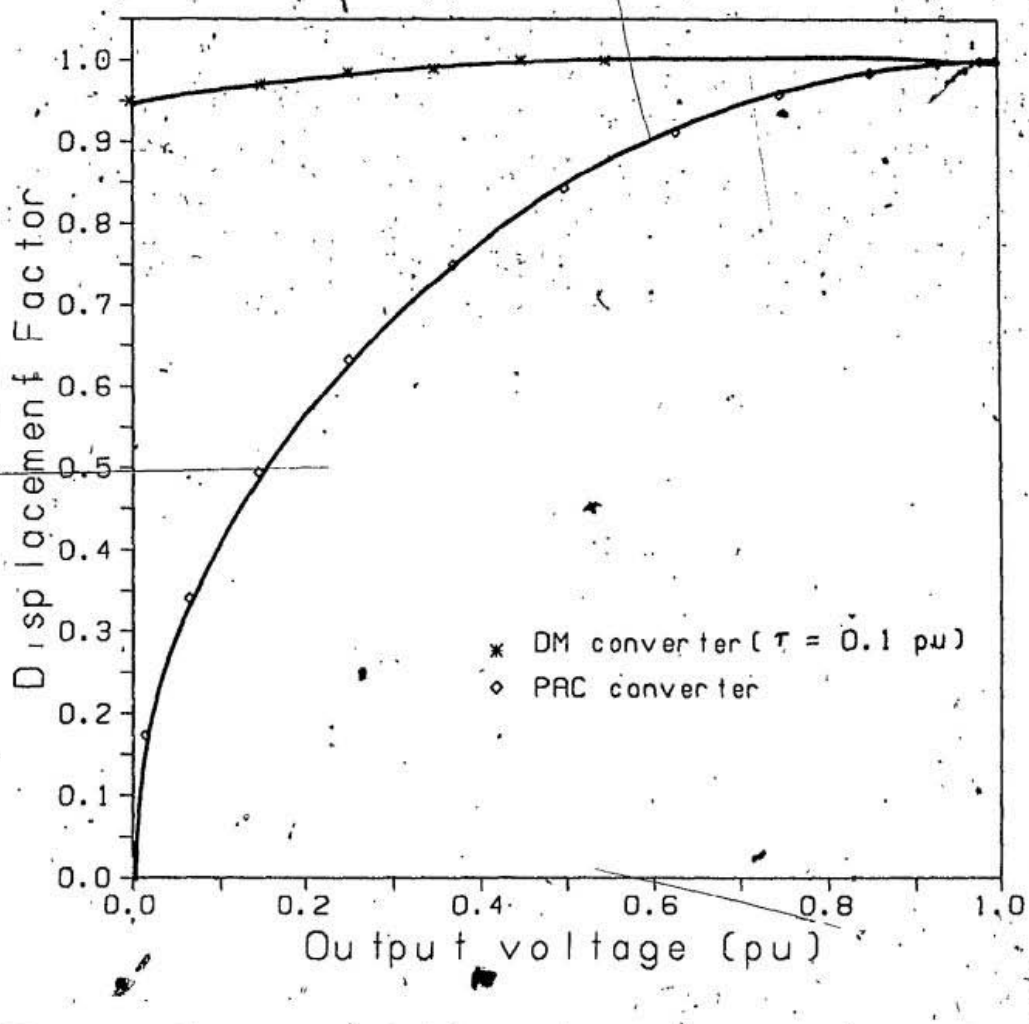


Figure 3.21: Comparison of displacement factor versus average output voltage for phase controlled bridge converter and DM converter

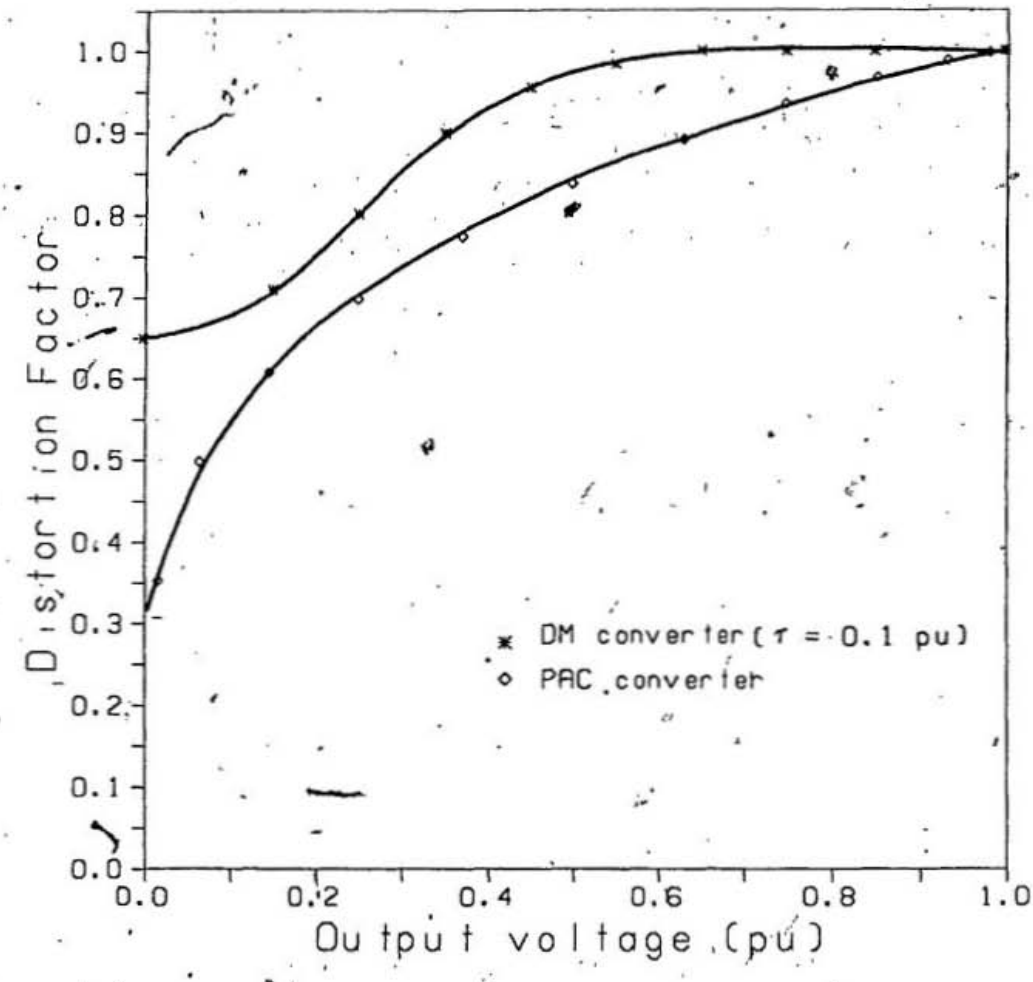


Figure 3.22: Distortion factor as a function of average output voltage for phase controlled and DM converter systems

converter, power factor substantially deteriorates as the delay angle α is increased. The poor power factor in phase controlled converters stems from the fact that the displacement angle between the supply current and the fundamental component of supply current increases as α increases. It is evident from Fig. 3.21 that the displacement factor decreases as the output voltage is decreased, indicating the large reactive power which must be supplied by the ac source. The relationship between the distortion factor and average output voltage is illustrated in Fig. 3.22., which confirms the high harmonic content in the input current waveform at low operating output voltage levels.

Since the distortion factor is less than unity, the power factor in phase controlled converter is less than the displacement factor. However, in the DM converter, the displacement factor is close to unity for all values of output voltage and this results in the power factor being approximately equal to the distortion factor.

In this context, it should be emphasized that with the phase angle control scheme, considerable amount of low order harmonics are present in the input current. Thus, a large filter is needed to correct the power factor, adding to the size, weight and cost of the converter system. In contrast, dominant harmonics beyond the fundamental component in the DM rectifier are clustered around the ripple frequency or at the multiple of the ripple frequency. This in effect reduces the filter requirements of the converter.

3.6 Concluding Remarks

A detailed study of the single-phase DM converter was undertaken and the performances of the converter for various operating conditions were analysed. The converter waveforms were described in terms of general switching functions, which permitted a harmonic analysis to be conducted using an efficient FFT algorithm. As-such, the harmonic analysis procedure followed here can be extended to any PWM system. Simulation results of the DM converter for different modulator settings indicated a strong dependence of dominant harmonic distribution with modulator ripple frequency. This enables the modulator to be designed to eliminate harmonic components up to a critical harmonic order, at the expense of increased number of commutations. Performance of the DM converter with a resistive load was presented for three different cases of maximum switching frequency. An experimental prototype was built, details of the logic circuit have been outlined. A close agreement was found between the predicted and experimental results. Comparative study of the performances of the conventional phase controlled converter and the DM converter revealed that the DM converter offers the advantages of higher power factor, lower harmonic distortion and reduced reactive power requirements.

Chapter 4

Three Phase DM Converter

The single-phase full wave controlled rectifier is restricted to applications requiring moderate to low power levels. The characteristic two pulse output of the single-phase bridge converter has a high proportion of ripple voltage at the dc terminals. Another feature of this converter is the frequently encountered discontinuous current mode of operation for loads having small inductance. Hence, it is mandatory to include large size filters at the dc side to obtain satisfactory performance or an additional choke to ensure continuous load current.

By using three-phase converters some of these problems can be alleviated. Three-phase converters are more suitable for industrial applications due to the avaliability of three-phase supply and their ability to accomodate loads requiring high power levels. Typically, three-phase bridge converters have six pulses at their output which leads to lower ripple content and consequently small filter requirements. The range of continuous current operation is also larger compared to the single-phase counterpart.

In this chapter, the delta modulation technique is extended to control the operation of three-phase ac to dc full wave converter. In the begining, analysis of

the converter with a resistive load is presented together with theoretical results. This is followed by a detailed explanation of the three-phase circuit implementation. Design of the logic circuit and the power circuit topology are subsequently discussed in the latter part of the chapter. Finally, the study of the DM technique as applied to multiphase converter topologies is complemented with experimental results of the three-phase transistor converter subjected to resistive loads.

4.1 Analysis of Three Phase DM Converter With Resistive Load

The general configuration of the bridge converter used in converting three-phase ac voltages to a dc level is shown in Fig. 4.1. Control of the output voltage is achieved by the modulation circuit which dictates the manner in which the switches are to be operated. Operation of the three-phase bridge converter using power - transistors as the switching devices is discussed in section 4.3.2.

Typical expected waveforms of the converter when switched in the delta PWM scheme are illustrated in Fig. 4.2. The basic equations which quantitatively determine the converter operation under a resistive load are given by

average output voltage

$$V_o = \frac{6}{2\pi} \sum_{i=1}^{N_p} \int_{\alpha_i}^{\beta_i} \sqrt{2}\, V_L \sin(\omega t + \frac{\pi}{3})\, d(\omega t)$$

$$= \frac{3\sqrt{2}\, V_L}{\pi} \sum_{i=1}^{N_p} \left[\frac{1}{2}(\cos\alpha_i - \cos\beta_i) + \frac{\sqrt{3}}{2}(\sin\beta_i - \sin\alpha_i) \right] \qquad (4.1)$$

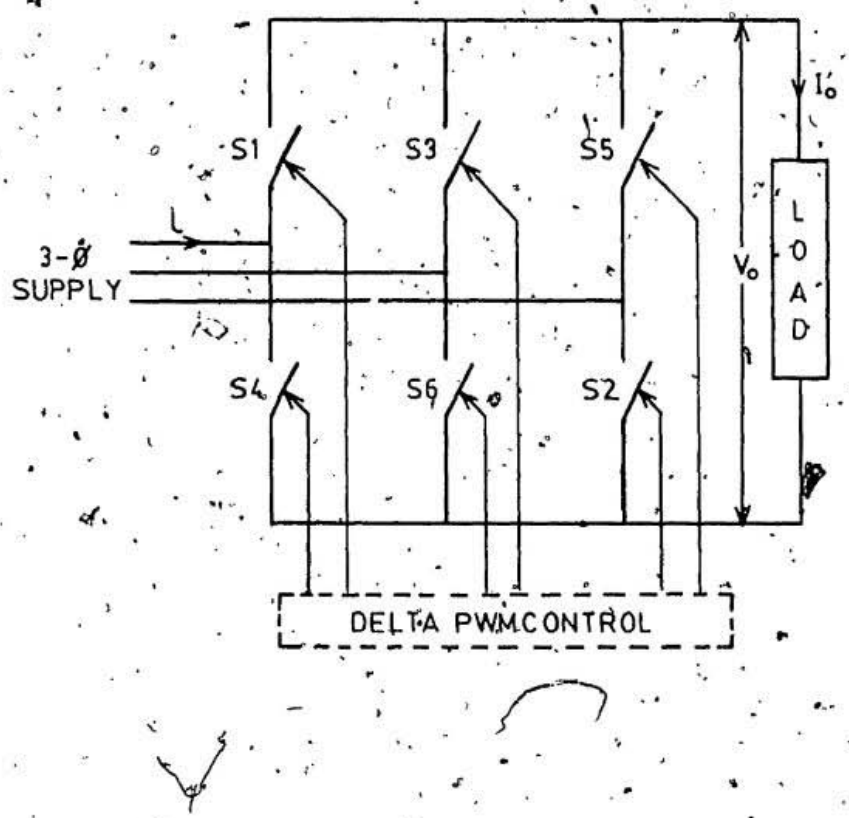


Figure 4.1: General three phase bridge converter topology

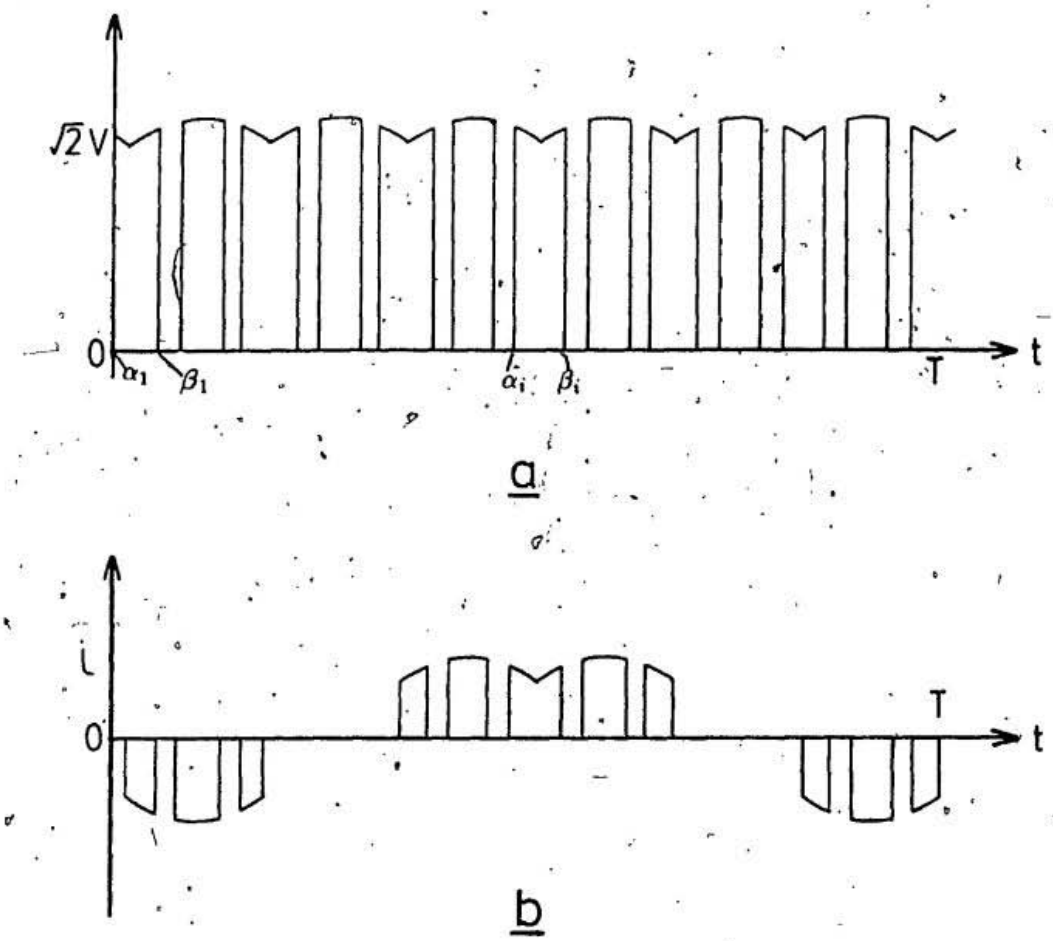


Figure 4.2: Typical waveforms of three phase DM converter (a) output voltage (b) input current of one phase

rms value of the output voltage

$$V = \left[\frac{6}{2\pi}\sum_{i=1}^{N_p}\int_{\alpha_i}^{\beta_i}\left[\sqrt{2}\,V_L\sin(\omega t+\frac{\pi}{3})\right]^2 d(\omega t)\right]^{\frac{1}{2}}$$

$$= \left[\frac{3\sqrt{2}\,V_L}{2\pi}\sum_{i=1}^{N_p}\int_{\alpha_i}^{\beta_i}\left\{(\beta_i-\alpha_i)-\frac{1}{4}(\sin 2\alpha_i-\sin 2\beta_i)\right.\right.$$

$$\left.\left.+\frac{\sqrt{3}}{4}(\cos 2\beta_i-\cos 2\alpha_i)\right\}\right]^{\frac{1}{2}} \qquad (4.2)$$

where

N_p = number of pulses per 1/6 cycle

α_i = turn-on instant in radians

β_i = turn-off instant in radians

V_L = line to line supply voltage

average output current is then obtained as

$$I_o = \frac{V_o}{R} \qquad (4.3)$$

and the rms value of output current is given by

$$I = \frac{V}{R} \qquad (4.4)$$

The rms value of input line current is obtained by making use of the fact that each phase current consists of 4 out of the six pulses, hence

$$I_i = \sqrt{\frac{4}{6}}\cdot I \qquad (4.5)$$

Investigations of the harmonic components generated by the converter are analysed using the discrete Fourier transform method described in chapter 3. In this case the converter waveforms are redefined in terms of general switching functions taking into consideration the operation of the three-phase bridge. In defining the output voltage and current waveforms, the delta PWM switching waveform is synchronized with the the 60 degree segment of the input line to line voltages to ensure the correct condition pattern. A similar approach is used in defining the input line current waveform. The process of defining the converter waveforms is accomplished by two FORTRAN programs, one dedicated for the input stage and the other for the output voltage and current waveforms. Detailed listing of the subroutines are provided in Appendix B.

Simulation results of the DM converter with a resistive load are illustrated in Figs. 4.3 – 4.5. The maximum switching frequency of the converter is set at 1.8 kHz. Figure 4.3(a) indicates the output voltage waveform for $V_o = 0.3$ pu. Since the load is purely resistive, the output current waveform resembles the voltage waveform with the magnitude of the current determined by the value of the load resistance. Figure 4.3(b) shows the input current waveform of one phase. Results for average output voltage levels of 0.5 and 0.7 pu for the same converter switching frequency of 1.8 kHz are illustrated in Figs. 4.4 and 4.5, respectively. It is apparant that the converter switching frequency changes as the output voltage is controlled, indicating the similar switching pattern of the three-phase DM converter as exhibited by the single-phase DM converter.

In retrospect, the harmonic profile of the converter waveforms also changes as a function of output voltage level. Figures 4.6 to 4.8 illustrate the simulated line

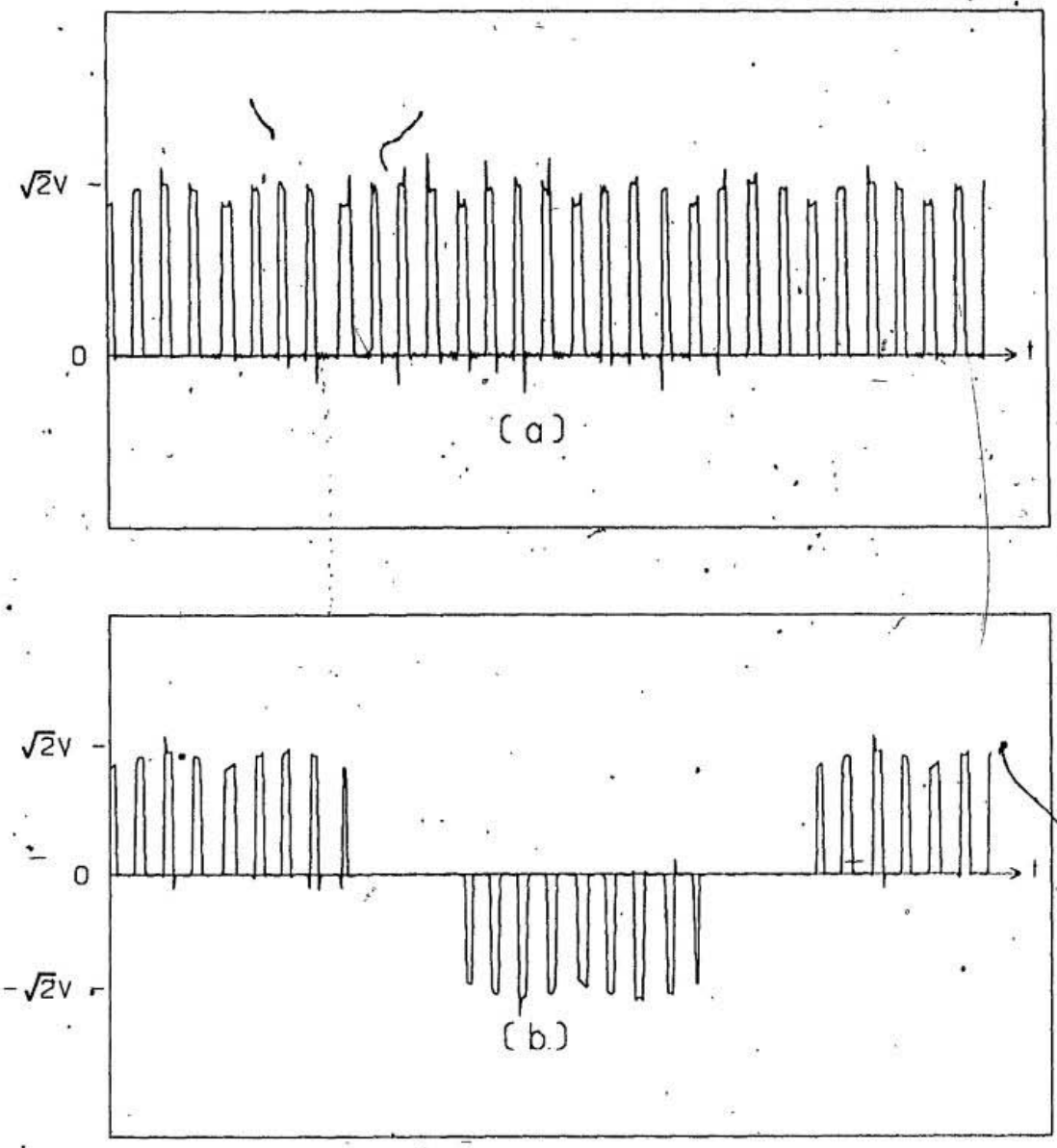


Figure 4.3: Simulated three phase DM converter waveforms for switching frequency = 1.8 kHz: $V_o = 0.3$ pu; (a) output voltage (b) input current

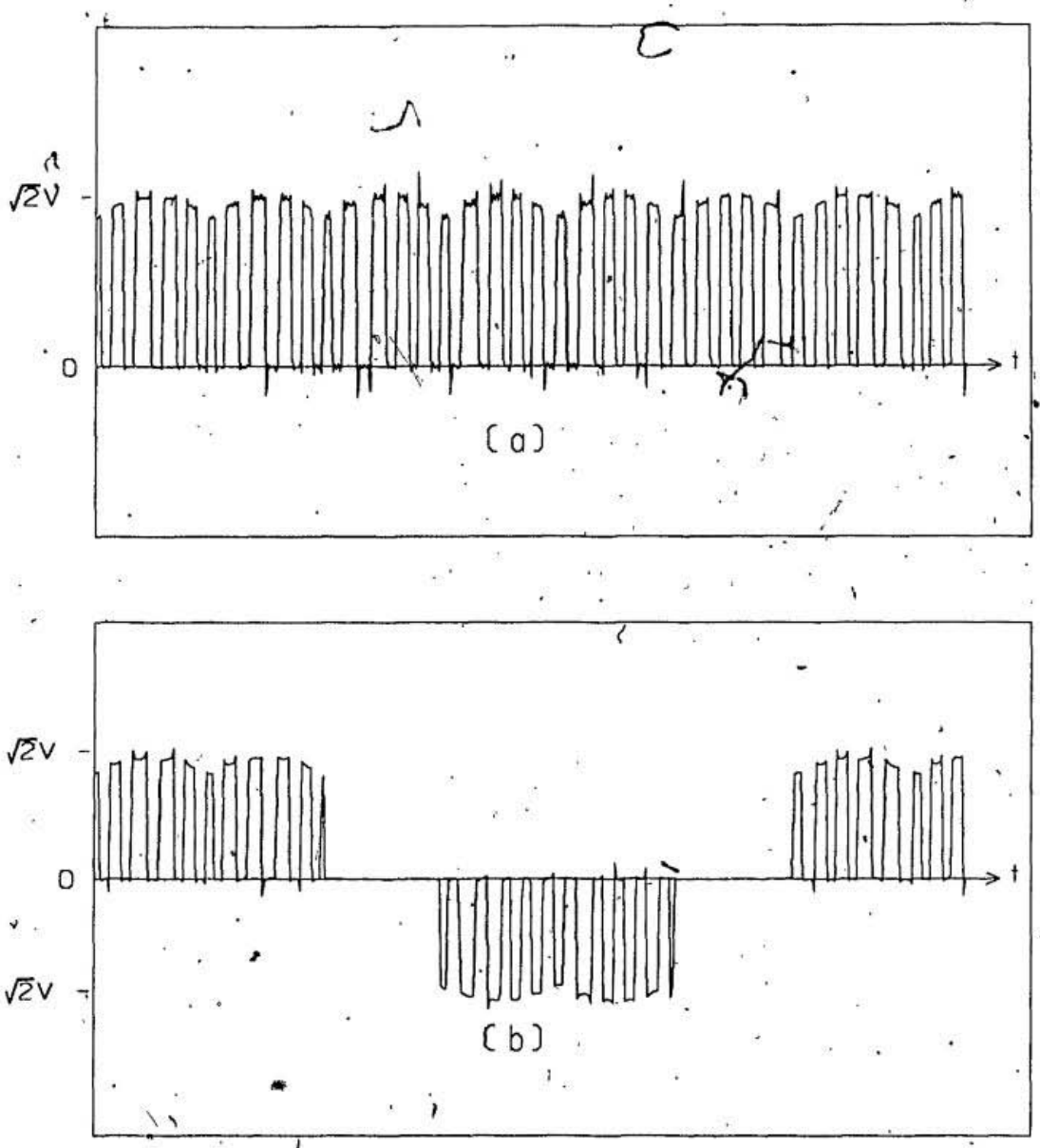


Figure 4.4: Simulated three phase DM converter waveforms for switching frequency = 1.8 kHz. V_o = 0.5 pu; (a) output voltage (b) input current

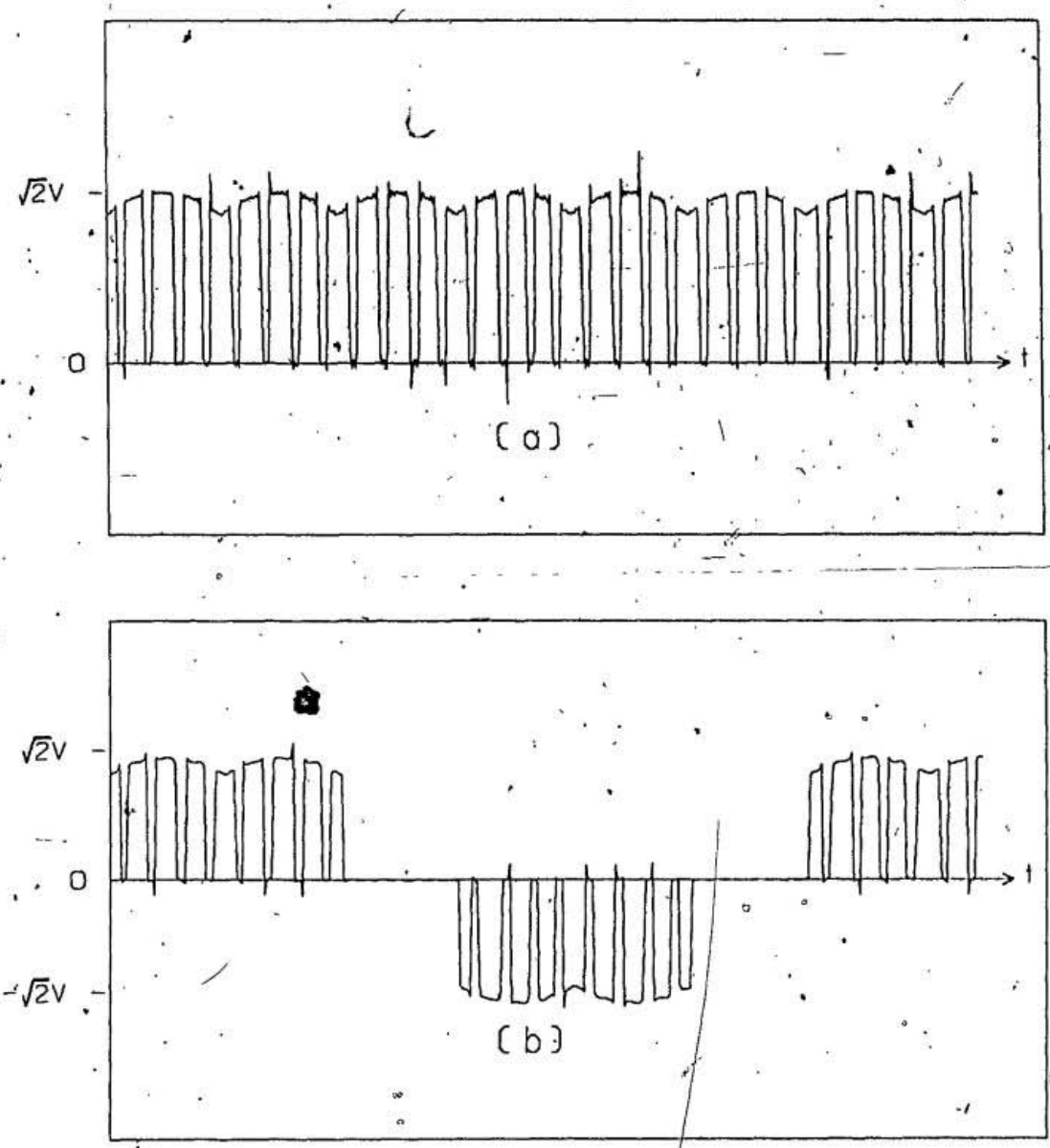


Figure 4.5: Simulated three phase DM converter waveforms for switching frequency = 1.8 kHz: $V_o = 0.7$ pu; (a) output voltage (b) input current

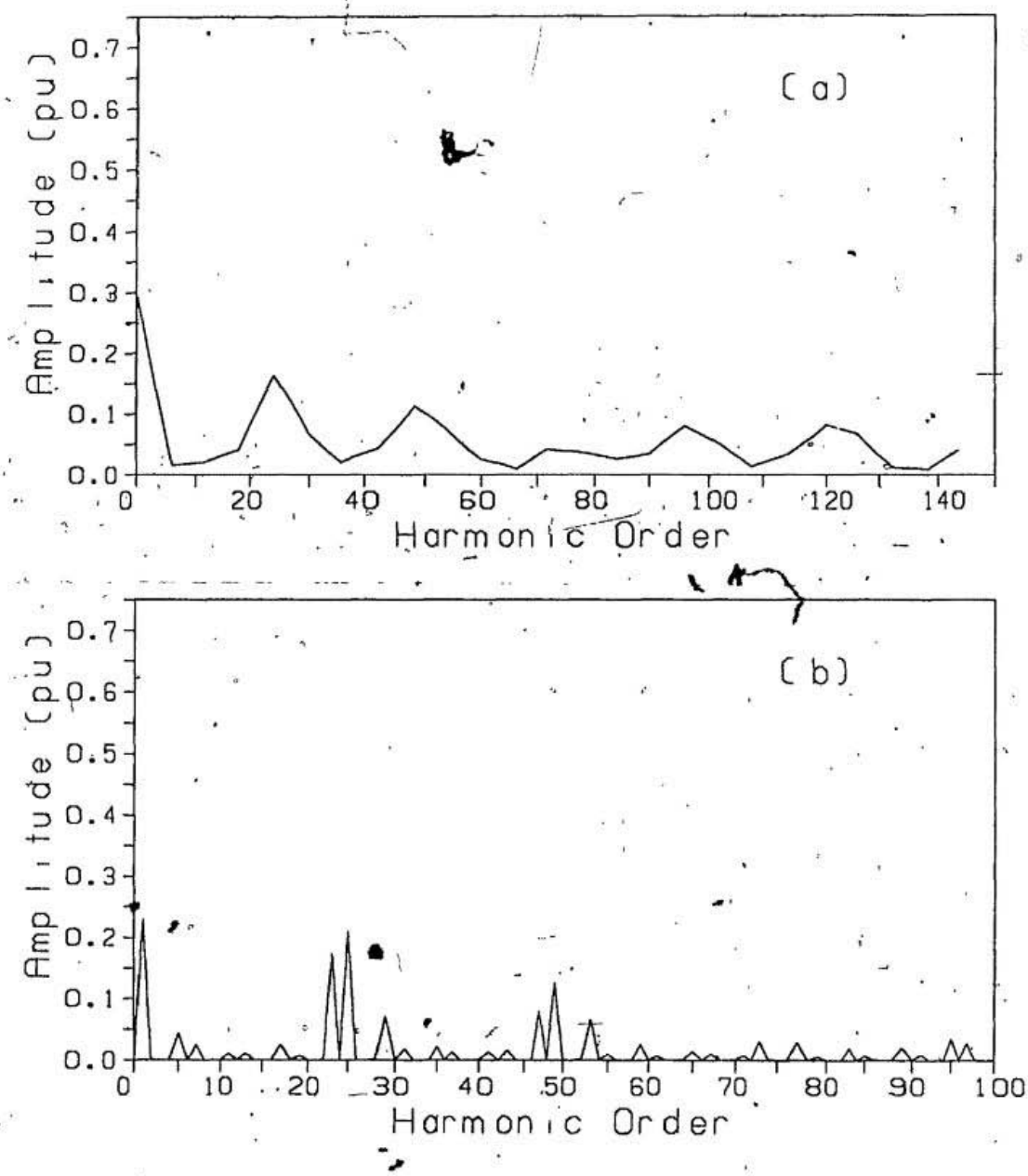


Figure 4.6: Theoretical harmonic spectra of three phase DM converter for switching frequency = 1.8 kHz: $V_o = 0.3$ pu; (a) output voltage (b) input current

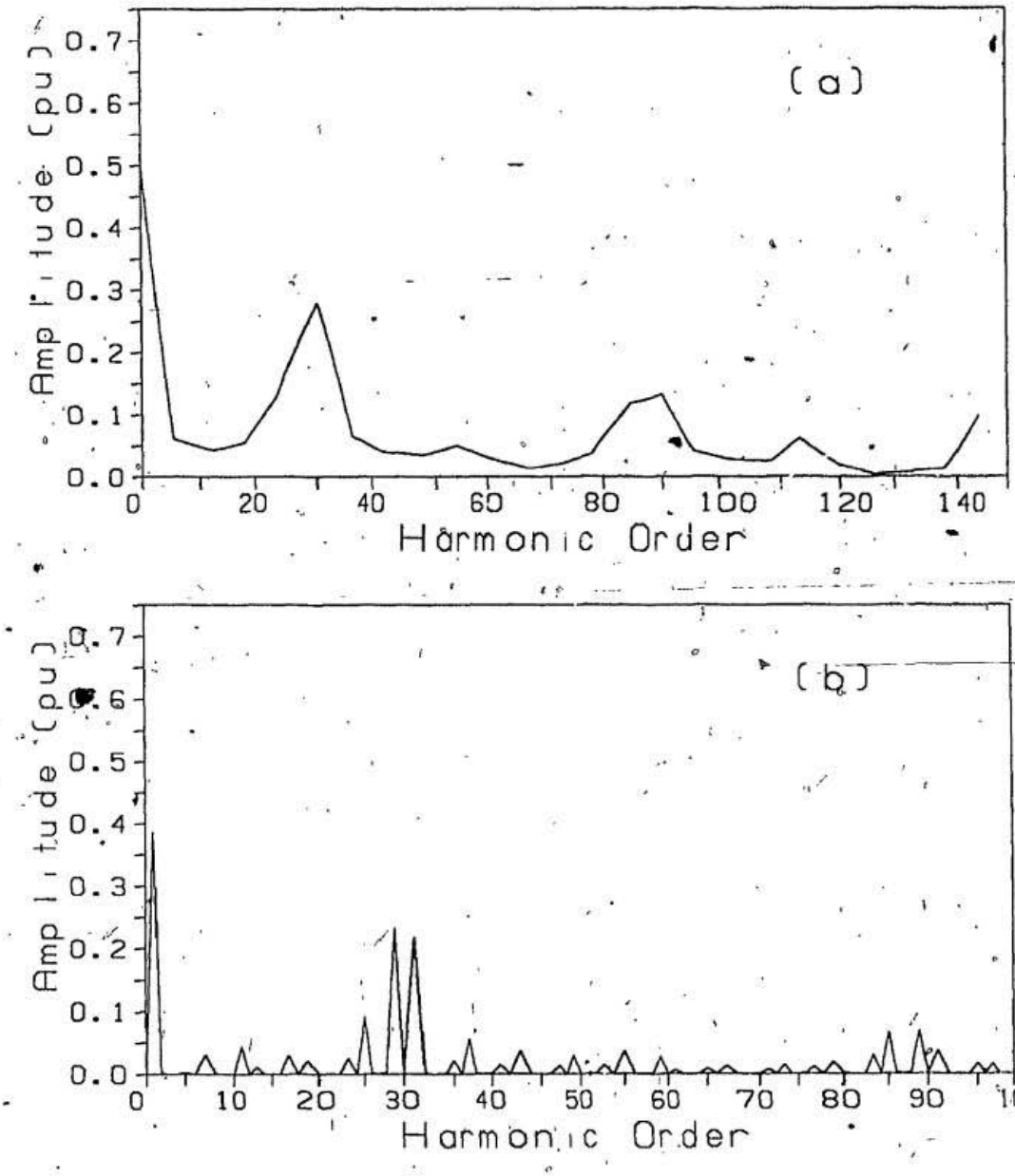


Figure 4.7: Theoretical harmonic spectra of three phase DM converter for switching frequency = 1.8 kHz: $V_o = 0.5$ pu; (a) output voltage (b) input current

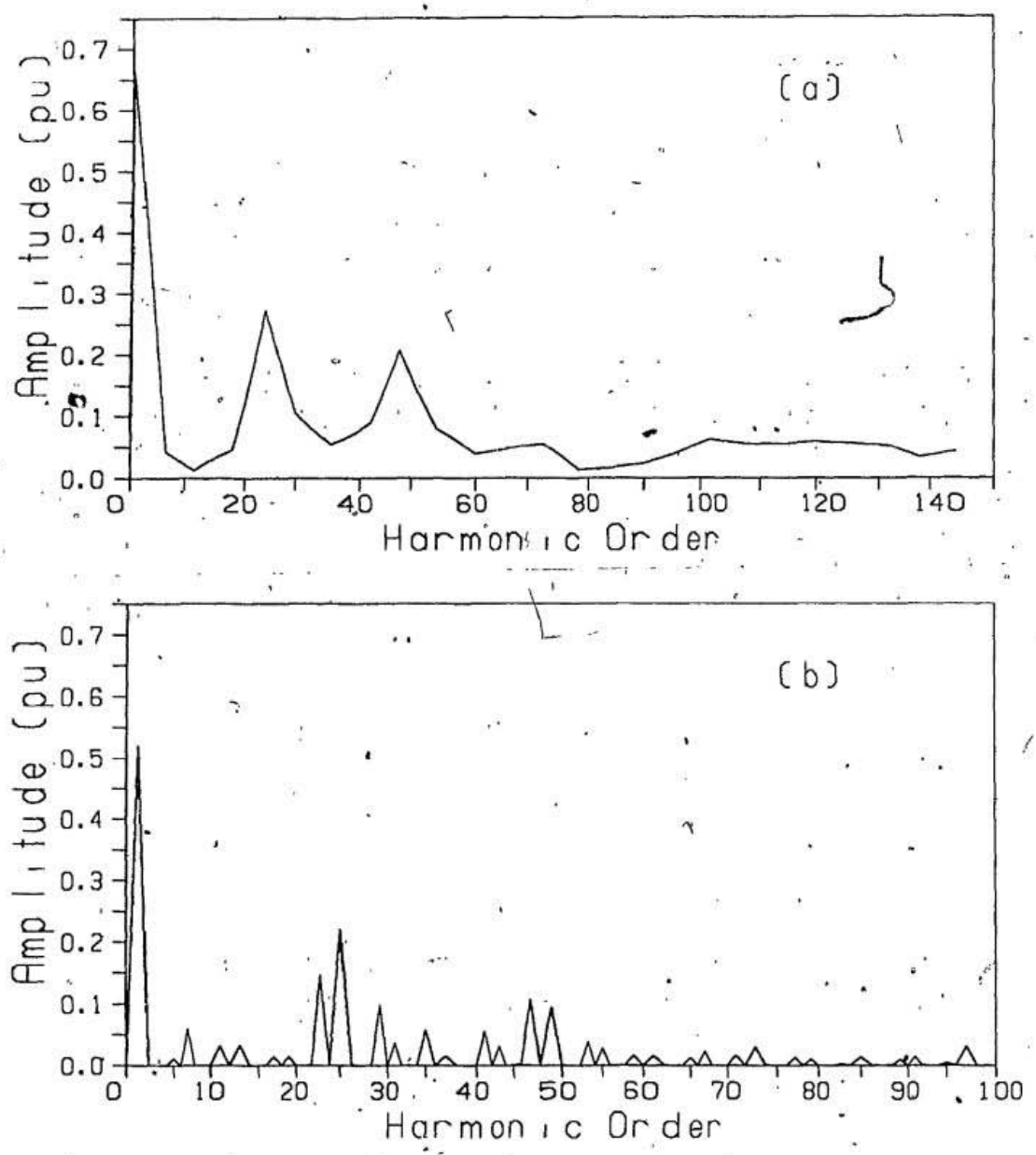


Figure 4.8: Theoretical harmonic spectra of three phase DM converter for switching frequency = 1.8 kHz: $V_o = 0.7$ pu; (a) output voltage (b) input current

spectra of the output voltage and input current waveforms for the same modulator parameters and output voltage levels of 0.3, 0.5 and 0.7 pu. Again, owing to the resistive load, the dominant harmonics in the input line current are centered about the ripple frequency and multiples of the ripple frequency. For the case of maximum converter switching frequency of 1.8 kHz and a delta setting of $\Delta_n = \Delta_p$, the dominant harmonic beyond the fundamental component in the output voltage waveform is given by $f_r/60$, which translates to the 30^{th} order harmonic. Correspondingly, the input current contains dominant harmonics of order 30 ± 1, which leads to the 29^{th} and 31^{st} being the dominant harmonics as seen in Fig. 4.7. As pointed out in the previous chapter, the intrinsic operation of the modulator results in a decrease in the converter switching frequency for output voltage levels above or below the 0.5 pu midpoint value. As a consequence, the dominant harmonic component in the output voltage waveform for output levels of $V_o = .3$ and .7 pu is of order 24. The corresponding dominant harmonic locations in the input current waveform are of order 23 and 25. These characteristic harmonic spectra are observed in the simulated results of Figs 4.6 and 4.8.

It is possible to shift dominant harmonics to the upper frequency range by appropriately increasing the switching frequency. However, it is well to note that the resulting improvement in performance is at the expense of increased switching losses.

4.2 Theoretical Performance of Three Phase DM Converter

Like other PWM controlled ac to dc converters, the three-phase DM converter introduces harmonics into the ac supply. Owing to the multiphase rectification process resulting from three-phase operation, the output voltage consists of six pulses. Consequently, the dc output quantities contain harmonic frequencies of order six times the input supply frequency in addition to subharmonic components arising from the PWM switching process. Harmonic currents injected into the ac supply line are of orders $6n \pm 1$ (n taking integral values 1,2,...), besides subharmonic components. One immediately sees the improvement in converter performance due to three-phase operation. Whereas in the single-phase converter, the 3^{rd} is the next dominant harmonic component after the fundamental, in this case the 5^{th} forms the lowest troublesome harmonic. The effect of lower order harmonics can be reduced by selecting the modulator parameters such that the dominant harmonics appear near the ripple frequency of the carrier wave. In this manner, the modulation circuit provides a direct control on the harmonic contents of the converter waveforms.

Theoretical performance characteristics of the three-phase DM converter with a resistive load and a maximum switching frequency of 1.8 kHz are illustrated in Figs. 4.9 to 4.11. Equations (3.16) - (3.18) were numerically solved to find the resistive load behavior of the converter with the delta modulation scheme. Power factor as a function of average output voltage is shown in Fig. 4.9. At low output voltage levels, harmonics near the ripple frequency have a relatively large magnitude compared to the fundamental component. As a result, the converter

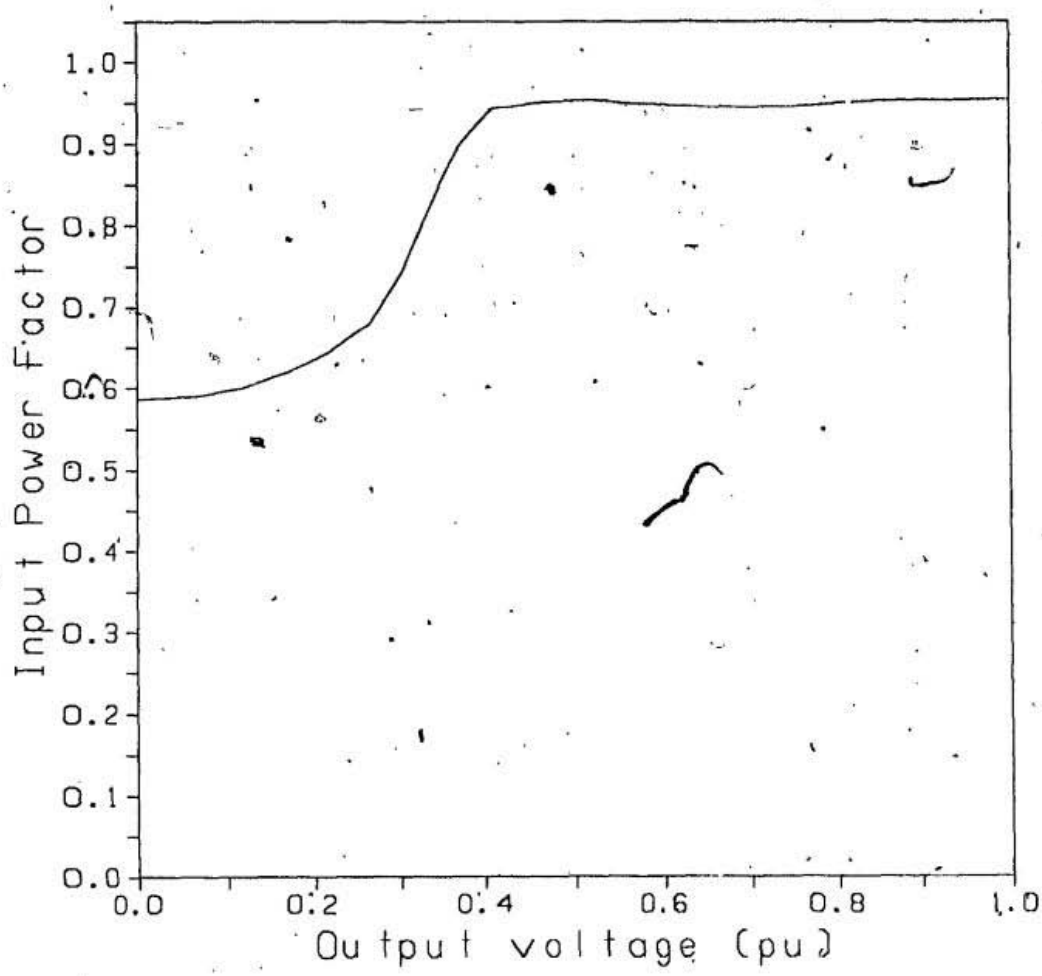


Figure 4.9: Input power factor as a function of average output voltage (three phase DM converter)

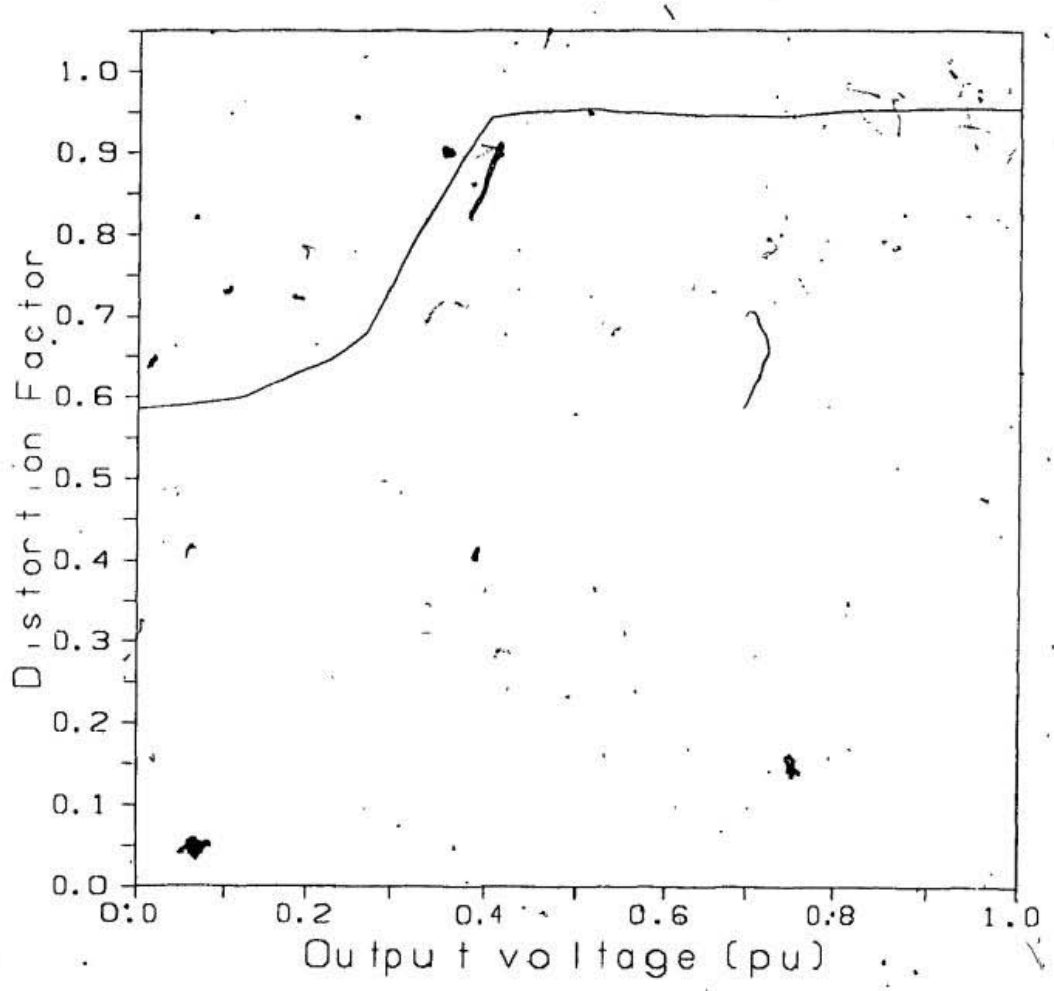


Figure 4.10: Distortion factor as a function of average output voltage (three phase DM converter)

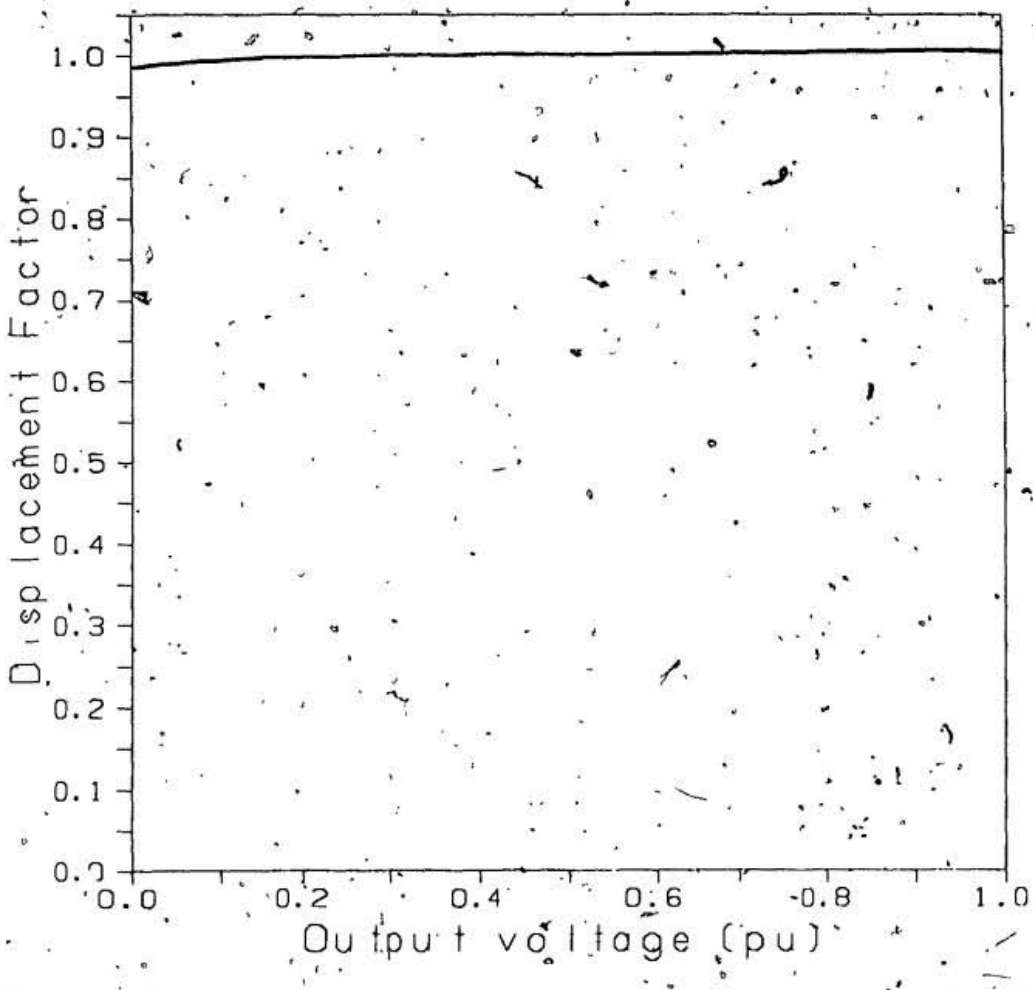


Figure 4.11: Displacement factor as a function of average output voltage (three phase DM converter)

requires more reactive power. This is reflected in the plot of distortion factor versus average output voltage in Fig. 4.10. It exhibits low values for low voltage levels but rapidly increases as the output voltage is increased. The displacement factor is close to unity over the control range as shown in Fig. 4.11.

The analytical results confirm the improvement in converter performance compared to the single-phase DM converter. For practical implementation, a filter is generally included in the input stage of the converter. Besides attenuating harmonic components above the cut-off frequency, the filter also reduces the magnitude of lower order harmonics by a factor depending on the order of the filter, thus improving the overall performance of the converter.

4.3 Implementation of Three Phase DM Converter

Implementation of the DM technique for a three-phase rectifier requires the use of three identical modulator circuits of Fig. 2.6. Each modulator is referenced to one individual phase of the three-phase supply, providing three modulated waveforms synchronized with the ac system. A detailed schematic diagram of one phase comprising the three-phase modulator is given in Appendix C.

4.3.1 Power Circuit Topology

Conversion of the fixed three-phase ac supply to a variable dc voltage is obtained by the bridge configuration of Fig. 4.12. The six pulse bridge switched in the DM scheme provides optimum performance. In fact, by the proper setting of the window widths in the aforementioned asymmetrical delta control (ADC) scheme,

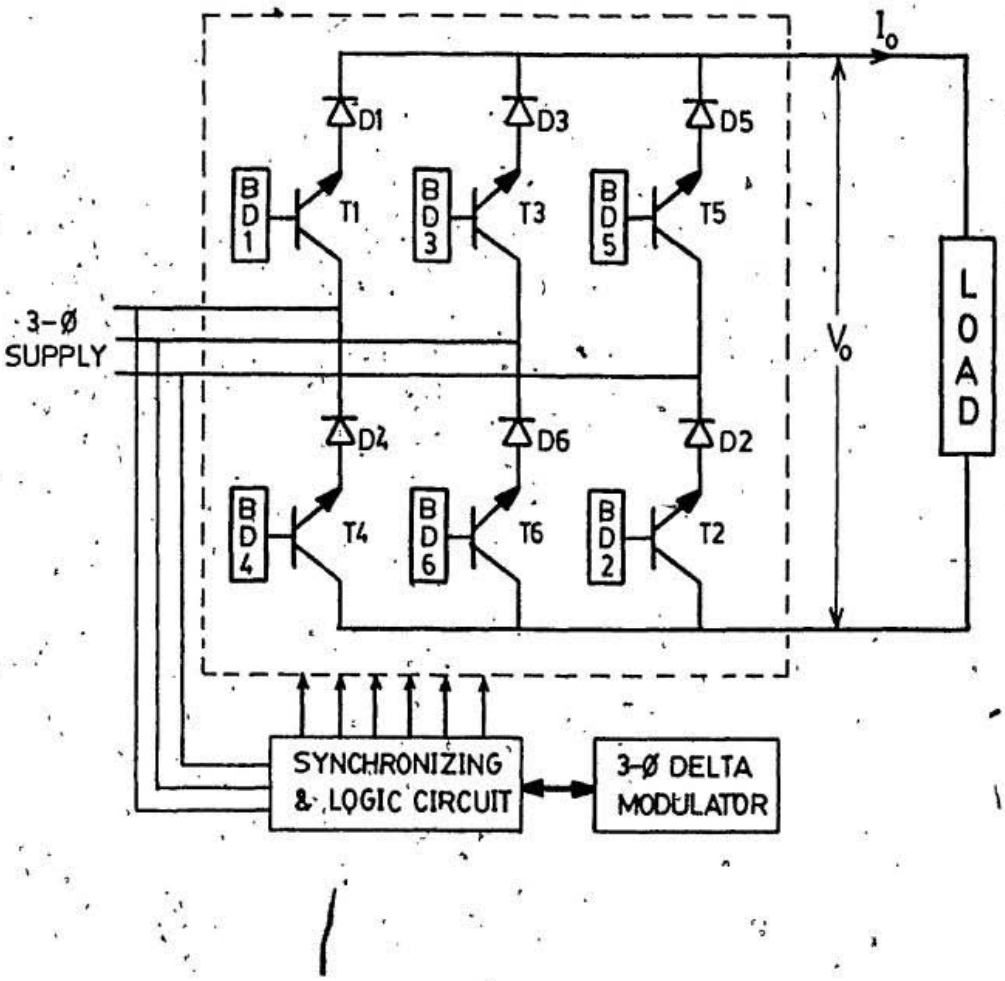


Figure 4.12: Three phase DM transistor bridge configuration

it allows distortion–free input currents and good regulation.

The circuit employs bipolar power transistors (Motorola 2N6251) as the power switching devices. As opposed to thyristors, power transistors are particularly suited to operate in PWM mode as circuit commutation is achieved by simply applying off–gate base pulses. With thyristors as the main switching devices, external circuits must be added for commutation purposes, and this usually results in a complicated control scheme. Another disadvantage of thyristor converters is that the converter undergoes many more topological modes of operation mainly due to the commutation circuitry.

To accommodate for the transistors switched in the PWM scheme, certain modifications to the bridge have been incorporated. The power diode in series with the emitter of each transistor serves two purposes. Firstly, it ensures the commutation of the conducting transistor after it has conducted during the specified interval, when a subsequent transistor on a different phase commences to conduct. Secondly, the diode provides isolation to the base drive circuit which must be referenced to the emitter.

Individual base drive circuits for each transistor were designed to meet the switching specifications of the converter controlled by the delta modulation process. The base drive circuits utilize a totempole arrangement of an npn–pnp complementary transistor pair. The push–pull arrangement provided by the complementary transistor pair allows fast turn–off of the main power transistors. The schematic diagram of the transistor base drive circuit is included in Appendix C.

4.3.2 Bridge Selection Logic

Selection of the transistor conduction is based on the criterion of maximum positive line to line voltages of the three-phase source applied to the bridge. The principle similar to the one adopted by phase angle controlled converters [3], enables the converter to yield maximum dc voltage corresponding to the peaks in the ac waveform. Assuming the three-phase supply to be symmetrical and perfectly balanced, the period of the source voltages is divided into six sectors as in Fig. 4.13. During the first 60 degree interval, phase voltage v_A is at its positive maximum while v_B is at a minimum. Hence, line to line voltage v_{ab} is maximum positive. Transistors T_1 and T_6 must, therefore, conduct to complete the current path. In the next interval, v_{ac} is at a positive maximum. The circuit is completed with transistors T_2 and T_1 conducting and T_6 commutated. Each transistor is allowed to conduct for two consecutive or a 120 degree interval. The correct transistor conduction sequence is illustrated in Fig. 4.13(c) with the transistors labelled as in Fig. 4.12.

Implementation of the logic circuit is facilitated by identifying the states of the source voltages in each of the six sectors. Three command signals X_A,X_B and X_C representing the states of v_{ab},v_{bc} and v_{ca} are generated by comparing the phase voltages v_A,v_B and v_C. The command variables take on a logic HI (1) value according to the following conditions:

$$\left.\begin{aligned} v_A > v_B \ ; \quad &\text{then } X_A = 1 \\ v_B > v_C \ ; \quad &\text{then } X_B = 1 \\ v_C > v_A \ ; \quad &\text{then } X_C = 1 \end{aligned}\right\} \tag{4.6}$$

In all other situations, they take a LO (0) logic value. The logic values of the com-

command signals in each interval are tabulated in Fig. 4.13(d). Since each transistor conducts for two intervals and the sequence of conduction is known a priori, the intermediate transistor gating signals $I_1, \ldots, I_6$ are determined by the combination of the logic signals according to the following Boolean expressions:

$$\left.\begin{aligned} I_1 &= X_A \cdot \bar{X}_B \cdot \bar{X}_C + X_A \cdot X_B \cdot \bar{X}_C \\ I_2 &= X_A \cdot X_B \cdot \bar{X}_C + \bar{X}_A \cdot X_B \cdot \bar{X}_C \\ I_3 &= \bar{X}_A \cdot X_B \cdot \bar{X}_C + \bar{X}_A \cdot X_B \cdot X_C \\ I_4 &= \bar{X}_A \cdot X_B \cdot X_C + \bar{X}_A \cdot \bar{X}_B \cdot X_C \\ I_5 &= \bar{X}_A \cdot \bar{X}_B \cdot X_C + X_A \cdot \bar{X}_B \cdot X_C \\ I_6 &= X_A \cdot \bar{X}_B \cdot X_C + X_A \cdot \bar{X}_B \cdot \bar{X}_C \end{aligned}\right\} \tag{4.7}$$

Equation (4.7) can be reduced by applying the laws of Boolean algebra as follows:

$$\left.\begin{aligned} I_1 &= X_A \cdot \bar{X}_C \\ I_2 &= X_B \cdot \bar{X}_C \\ I_3 &= \bar{X}_A \cdot X_B \\ I_4 &= \bar{X}_A \cdot X_C \\ I_5 &= \bar{X}_B \cdot X_C \\ I_6 &= X_A \cdot \bar{X}_B \end{aligned}\right\} \tag{4.8}$$

The set of equations indicate the simple logic required to obtain the intermediate transistor gating signals. The associated timing diagram of the six signals is shown in Fig. 4.14. The logic scheme provides the six transistor gating signals synchronized with the ac source. Individual gating signals have an on–time pulse covering two intervals with a repetitive frequency of the supply line. As a result, fluctuations in the ac line frequency will not adversely affect transistor switching. The other feature offered by the scheme is that only two transistors, on different

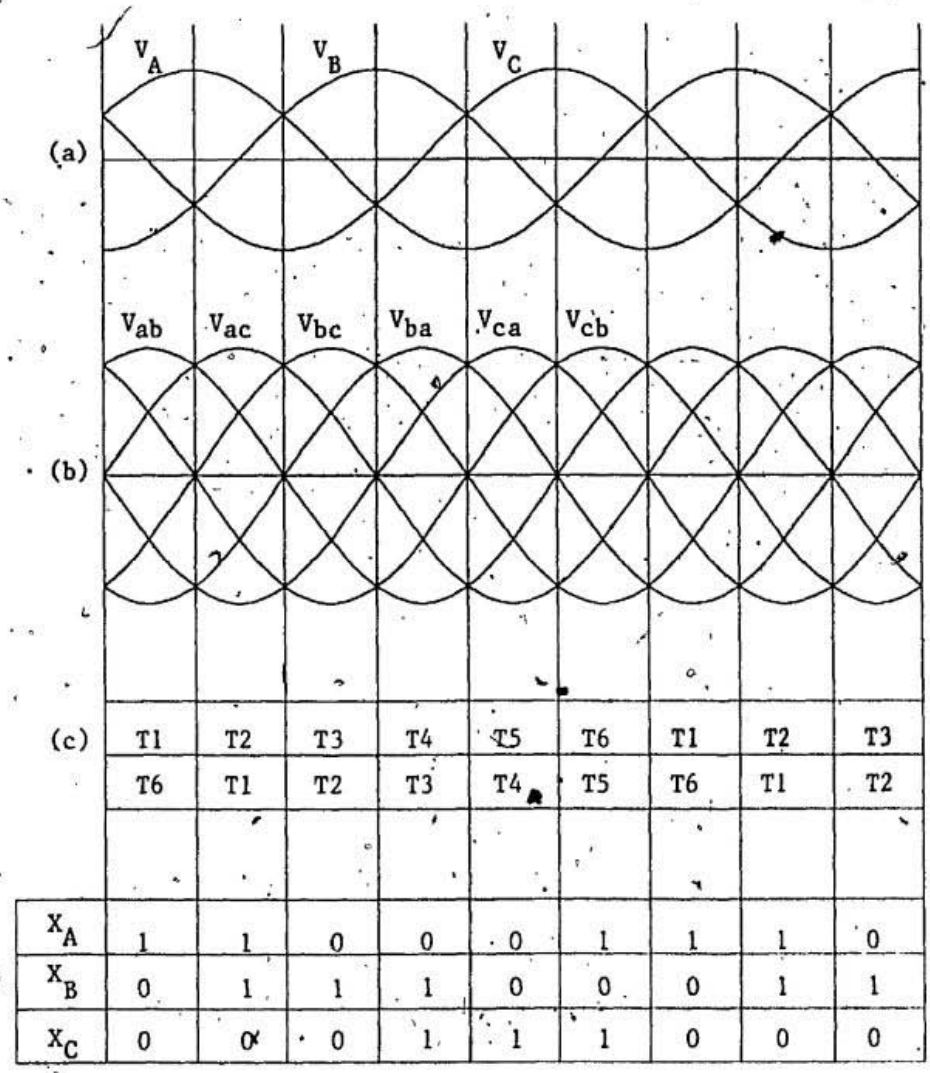


Figure 4.13: Selection of transistor conduction intervals: (a) Line to neutral reference voltages (b) line to line reference voltages (c) transistor switching sequence (d) states of the three phase source voltages

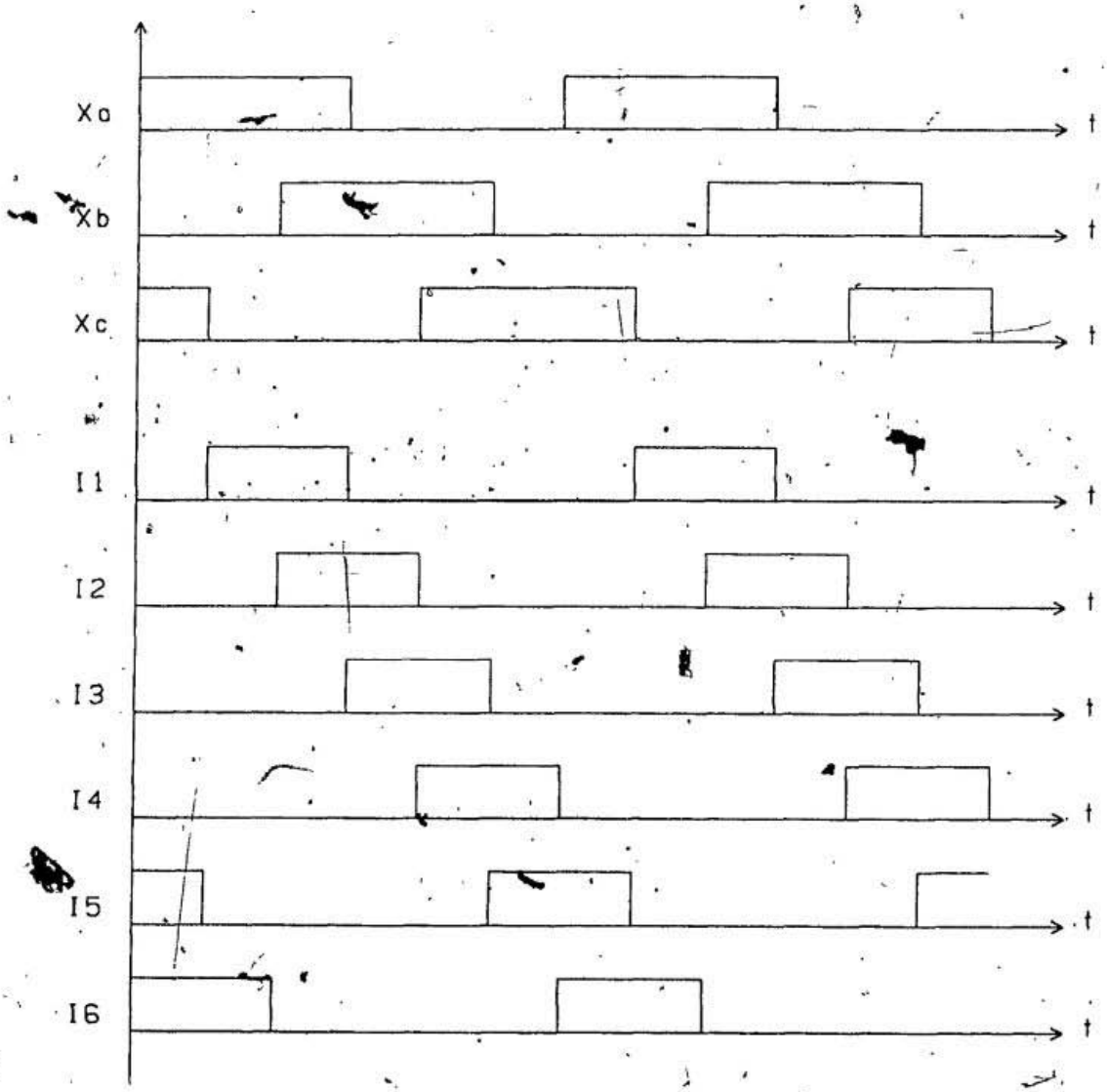


Figure 4.14: Timing diagram of the intermediate signals: (a) command signals (b) intermediate transistor signals

phases are simultaneously gated, eliminating the possibility of transistor misfiring and short circuit conditions.

4.3.3 Logic Circuit

In addition to the crucial task of selecting appropriate transistor conduction pairs, the logic circuit couples the intermediate pulses with the three delta modulator outputs to give the transistor base drive signals.

In the logic circuit of Fig. 4.15, the command signals are generated by three voltage comparators. Three low power transformers are used to step down the supply voltages to the level required for CMOS logic gates. The same low power signals also serve as the modulating signal inputs to each of the delta modulators comprising the three-phase modulation circuits. The command signals are processed by logic gates according to the logic scheme of Equation (4.8) to provide the intermediate 120 degree pulses $I_1, \ldots, I_6$. The intermediate pulses are ANDed with the respective modulated signals to give the transistor base drive signals. The output switching signals generated by the three-phase delta modulator circuits are designated M_A,M_B and M_C for phase A, phase B, and phase C, respectively.

Inspection of Fig. 4.12 reveals that transistors T_1 and T_4 are on phase A, with T_1 conducting on the positive portion of v_A and T_4 on the negative cycle of the waveform. Consequently the base drive signal for T_1 is obtained by ANDing I_1 with M_A and I_4 with $\bar{M}_A$. With this reasoning, the remaining base drive signals, and hence the ultimate delta PWM switching signals to the transistors

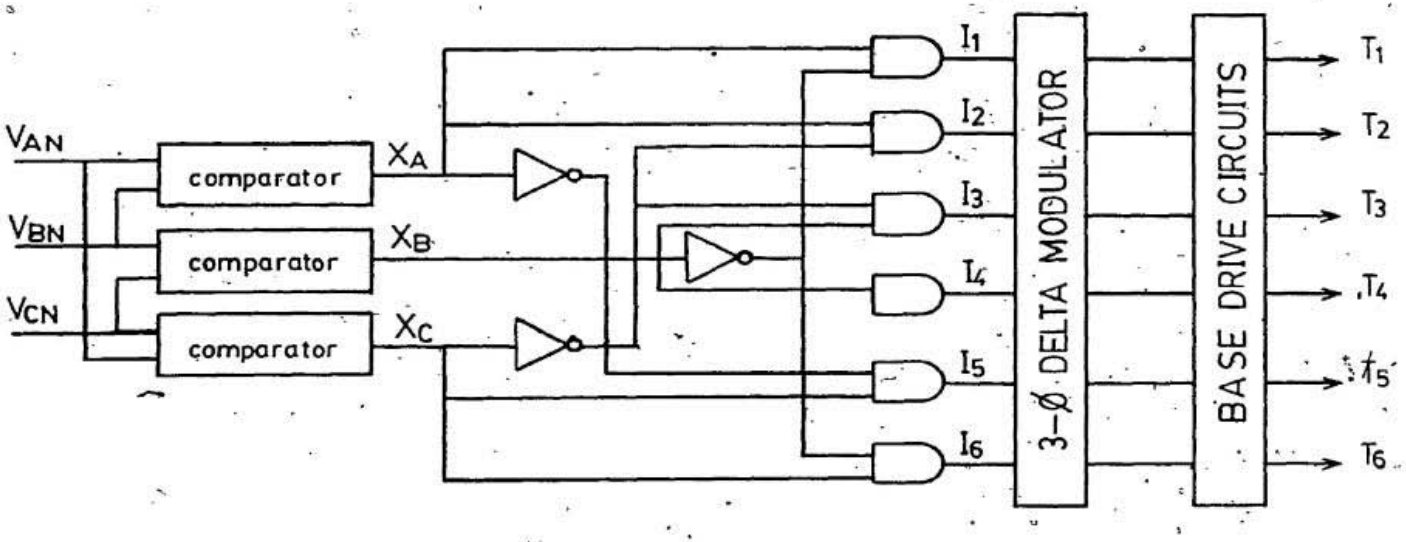


Figure 4.15: Block diagram of three phase logic circuit

are expressed as:

$$\left.\begin{aligned} T_1 &= I_1 \cdot M_A \\ T_2 &= I_2 \cdot \bar{M}_C \\ T_3 &= I_3 \cdot M_B \\ T_4 &= I_4 \cdot \bar{M}_A \\ T_5 &= I_5 \cdot M_C \\ T_6 &= I_6 \cdot \bar{M}_B \end{aligned}\right\} \tag{4.9}$$

where T_1 to T_6 are the six unique gating signals to the power transistors of Fig. 4.12.

4.4 Experimental Results

The three-phase DM converter prototype was built and subjected to a series of experimental tests to check the validity of theoretical results and the design method. The results presented here, pertain to a converter switching frequency of approximately 2 kHz. No input and output filters have been included in the experimental setup.

Figure 4.16(a) shows the three-phase PWM signals generated by the three-phase delta modulator superimposed on their respective reference source voltages. The three command signals X_A, X_B and X_C which determine the state of the three-phase source voltages are shown in Fig. 4.16(b). The intermediate signals which are used to determine the transistor switching sequence are shown in Fig. 4.16(c). The final base drive signals to the main power transistors are shown in Fig. 4.16(d).

Experimental output voltage and input current waveforms of the DM converter

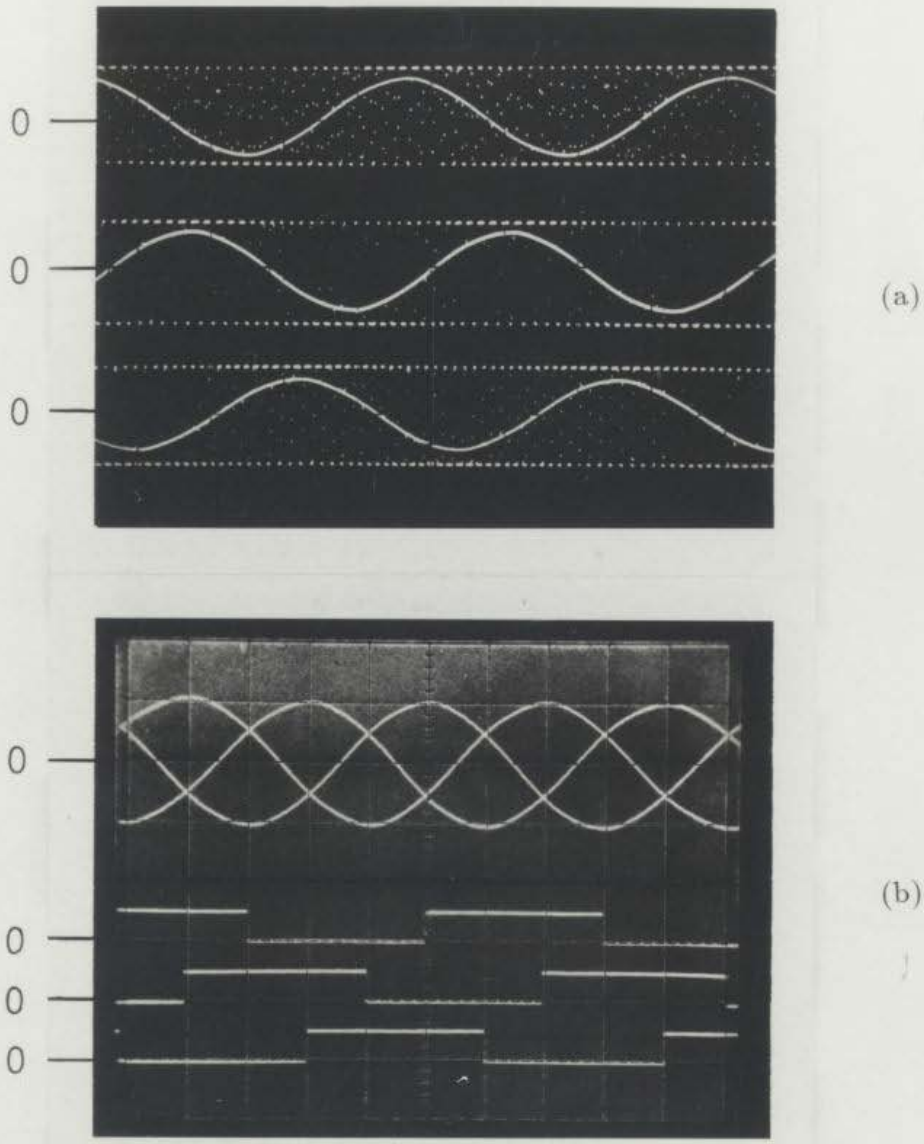


Figure 4.16: (a) Experimental three phase delta modulator switching waveforms (b) Command signals to identify states of the supply voltages

Vertical scale: 10 V/div

Horizontal scale : based on 60 Hz cycle

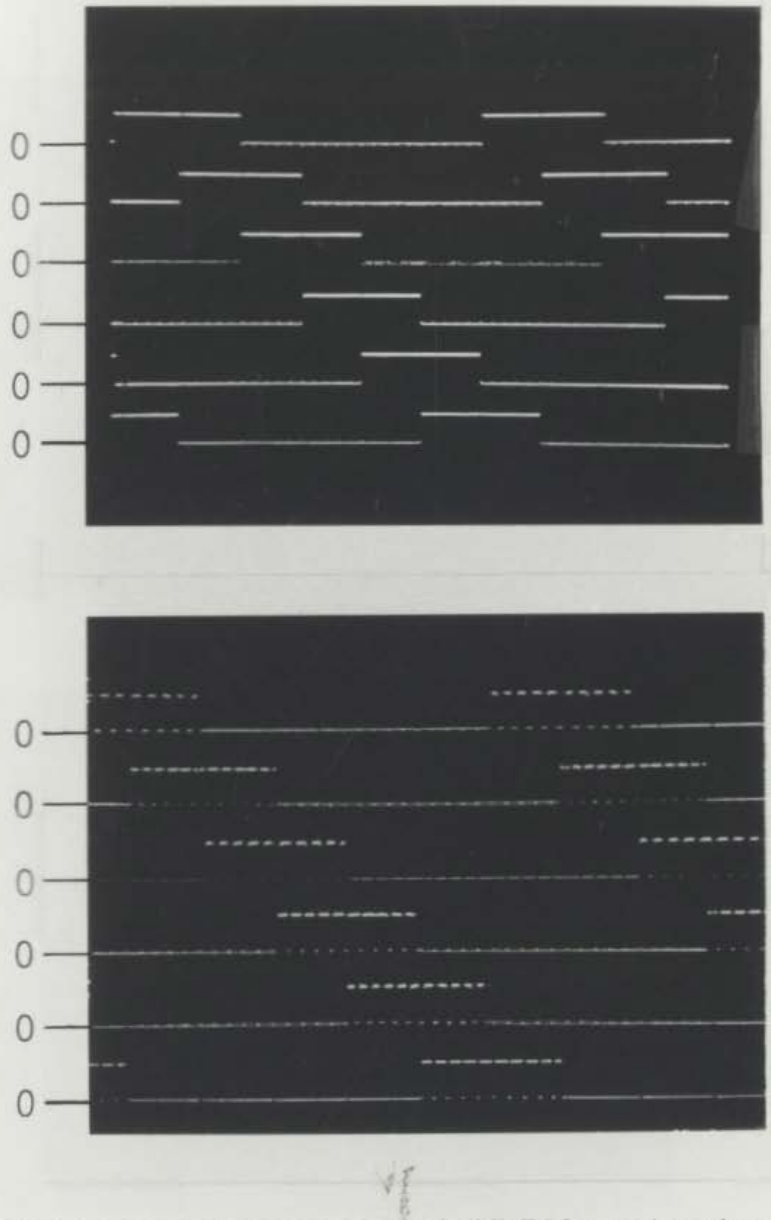


Figure 4.16: (c) Intermediate gating signals (d) DM transistor base drive signals
Vertical scale: all signals 10 V/div

Horizontal scale : based on 60 Hz cycle (2.78 ms/div)

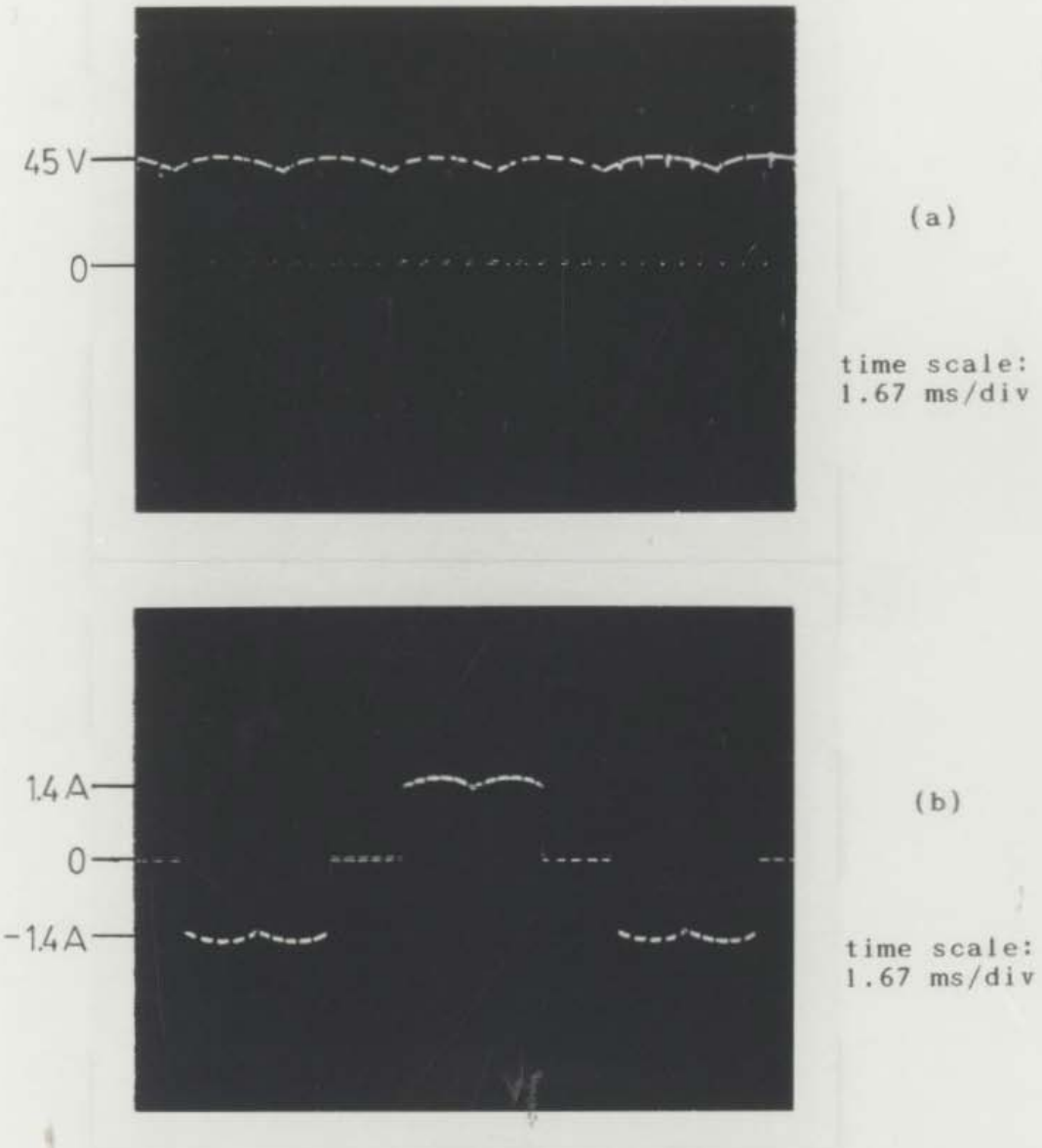


Figure 4.17: Experimental waveforms of three phase DM converter for $V_o = 0.3$ pu; (a) output voltage (b) input line current

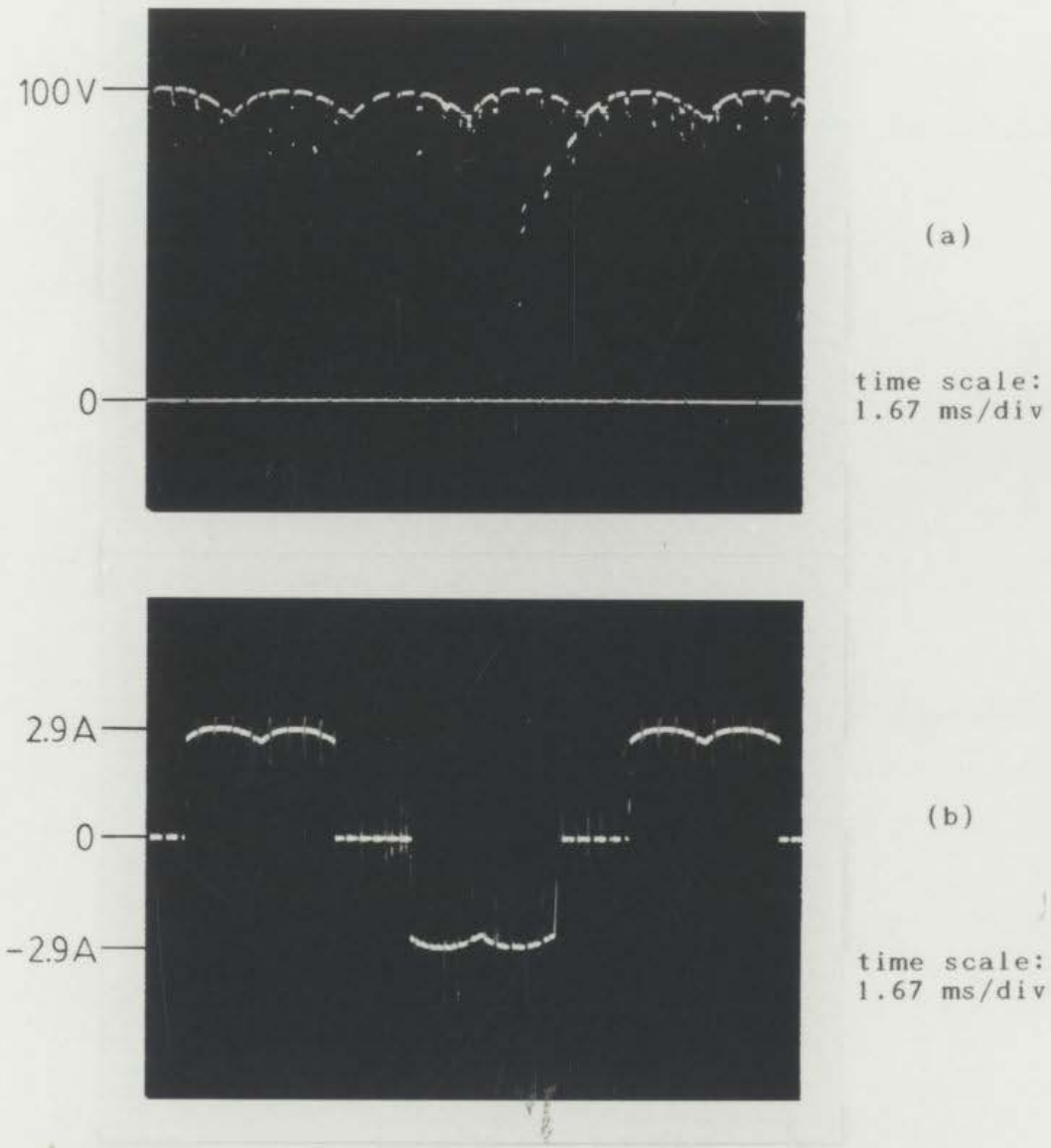
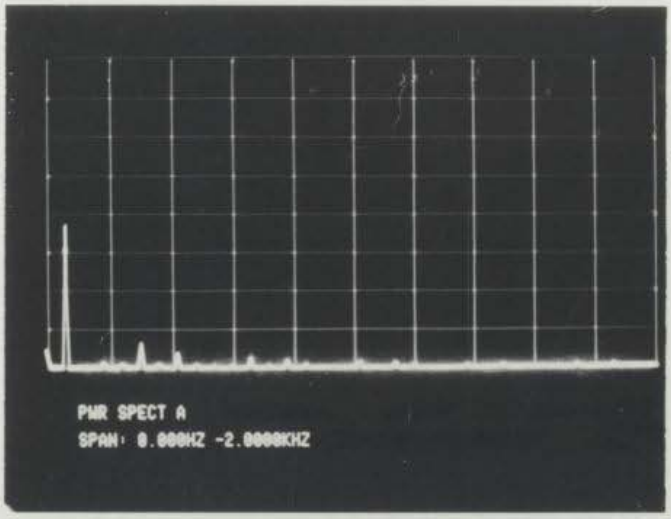
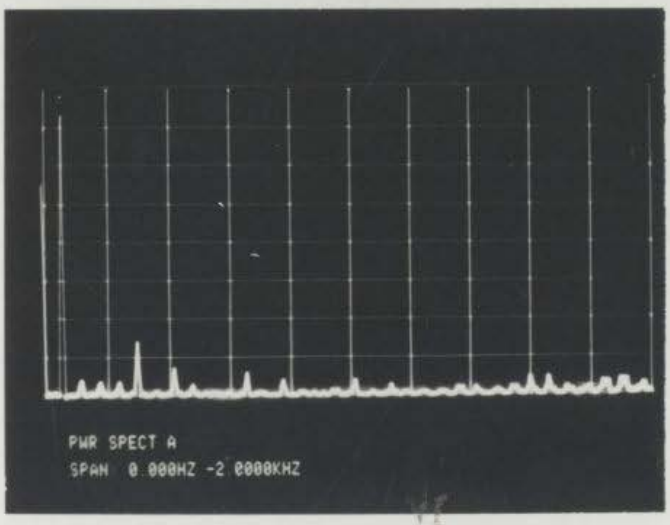


Figure 4.18: Experimental waveforms of three phase DM converter for $V_o = 0.7$ pu; (a) output voltage (b) input line current



For Io = 0.3 pu

$\frac{I_1}{I}$



For Io = 0.7 pu

$\frac{I_1}{I}$

Figure 4.19: Experimental input line current harmonic spectrum of three phase DM converter

with a resistive load are shown in Figs. 4.17 and 4.18 for two different output voltages of $V_o = 0.3$ pu and $V_o = 0.7$ pu. The input current line harmonic spectrum for the two cases are shown in Fig. 4.19. Although operation with a predominantly resistive load results in discontinuous load current, the experimental results clearly demonstrate the enhanced performance of the three-phase DM converter. This is confirmed by the spectrum analyser results of the input line current which show good attenuation of low order harmonics.

4.5 Concluding Remarks

Simulation results of the three-phase DM converter with a resistive load using the DFT approach indicated that the converter meets the desired criteria of high power factor and low harmonic distortion. Design of the three-phase delta modulator circuit and the logic circuit required for experimental implementation were described in detail. Experimental results of a prototype three-phase DM converter suggest a good agreement between the theoretical and actual results. The minor variations in the experimental results were due to switching transients, particularly di/dt transients due to transistor turn-off. These effects were not considered in predicting analytical results. The analysis presented in this chapter was based on the case of the converter with resistive loads. Performance of the converter with passive R-L and motor loads is presented in the following chapter.

Chapter 5

Experimental Performance of DM Converter with R-L and Motor Loads

So far operational aspects of the delta modulator have been considered and the design and implementation of both single-phase and three-phase DM converters have been presented. In each case, analysis of the DM converter was undertaken from the viewpoint of predicting the converter performance as a function of modulator parameters. The analysis were based on the converter subjected to resistive loads with theoretical results validated by experimental results on prototype DM converters. In the following sections, the performance of the three-phase DM converter under passive R-L and dynamic motor loads is analysed through experimental investigations.

5.1 DM Converter with R-L Load

Typical of PWM ac to dc converters [8 – 10,12], the DM converter injects harmonics into the supply. The harmonics together with the fundamental component

determine the performance of the converter under investigation. The study of the DM converter with R-L loads is an important aspect because most of the loads, by nature, contain a predominant inductive component. Further, the study provides an insight to the behavior of the converter with motor loads, which essentially comprises a complex R-L load.

Figure 5.1 shows the configuration of the converter under study. Freewheeling diode D_{FW} connected across the output terminals provides an alternate path for the load current to flow during the conducting transistor 'off - pulse' state. In multiple pulsewidth modulation schemes, the power transistors are turned on and off many time per 120 degree interval. The number of 'on - off' transistions are a function of the pulse numbers and as such are directly related to the converter switching frequency. Consequently, operation of the converter under multiple pulsewidth modulation can be analysed depending on the following three possible modes of operation [31]:

MODE 1:

Mode 1 is characterized by gating signals applied to the transistors and the source voltage appears across the load. In this case the load current rises.

MODE 2:

In Mode 2 freewheeling action takes place. This occurs when no gating signals are present at the transistor base i.e. when the transistors are in the 'off pulse' state. Under this condition, the output voltage is clamped at zero (neglecting the diode drop) and the load current freewheels through the diode.

MODE 3:

Mode 3 occurs when the transistors are in the 'off - pulse' state and the load

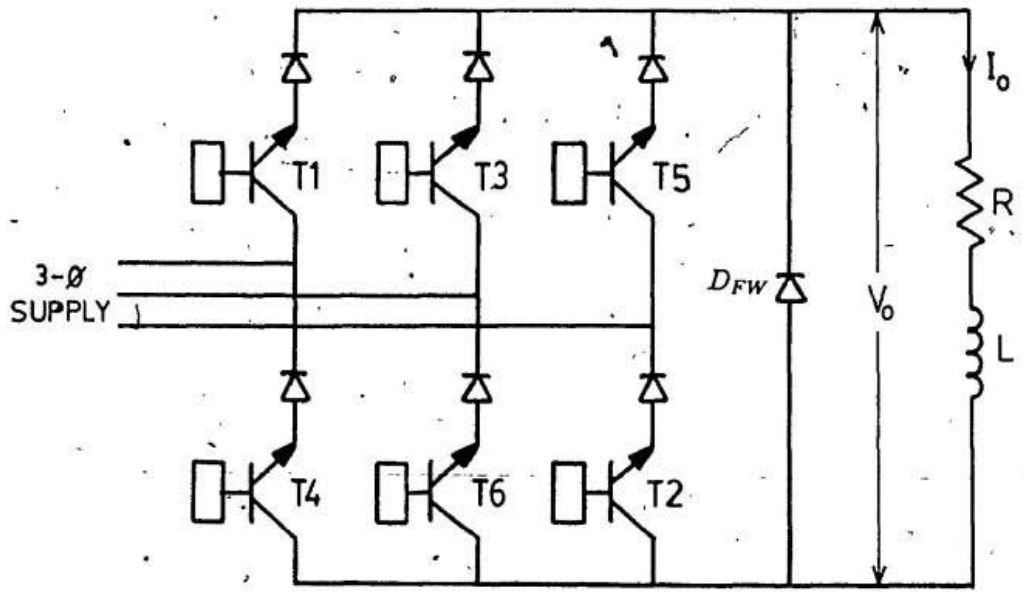


Figure 5.1: Three phase DM converter configuration with freewheeling diode

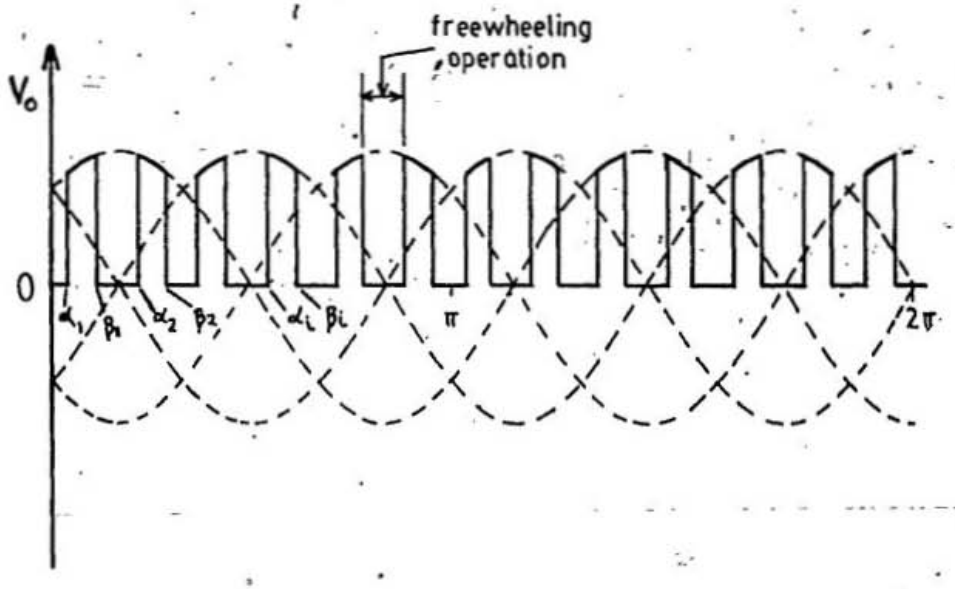


Figure 5.2: Typical output voltage waveform of three phase DM converter with R-L load

current decays to zero.

However, in multiple pulsewidth modulation control, Mode 3 is generally absent [9] due to the relative short duration of the 'off pulse'. In more realistic terms, for a given R-L load the range of discontinuous current mode of operation is substantially smaller compared to single pulsewidth modulation schemes. The expression for the average output voltage is given by

$$V_o = \frac{3\sqrt{2}\,V_L}{\pi} \sum_{i=1}^{N_p} \left[\frac{1}{2}(\cos\alpha_i - \cos\beta_i) + \frac{\sqrt{3}}{2}(\sin\beta_i - \sin\alpha_i) \right] \qquad (5.1)$$

where

N_p = number of pulses per 1/6 cycle

α_i = turn-on instant in radians

β_i = turn-off instant in radians

V_L = line to line supply voltage

Figure 5.2 shows the typical output voltage waveform of the DM converter over one 60 Hz cycle. The switching points (α's and β's) continuously change as the output voltage is varied by controlling the modulator window widths. The values of α and β for any converter switching frequency and output voltage levels are evaluated by solving Equations (2.15) to (2.17).

5.1.1 Performance of Converter with R-L Load

In the case of resistive load, as seen in the previous chapter, the converter operates in the discontinuous current mode over the entire control range. However under R-L loads, the load current is continuous due to freewheeling action. These characteristics are observed in the oscillograms of Figs. 5.3 and 5.4 which pertain

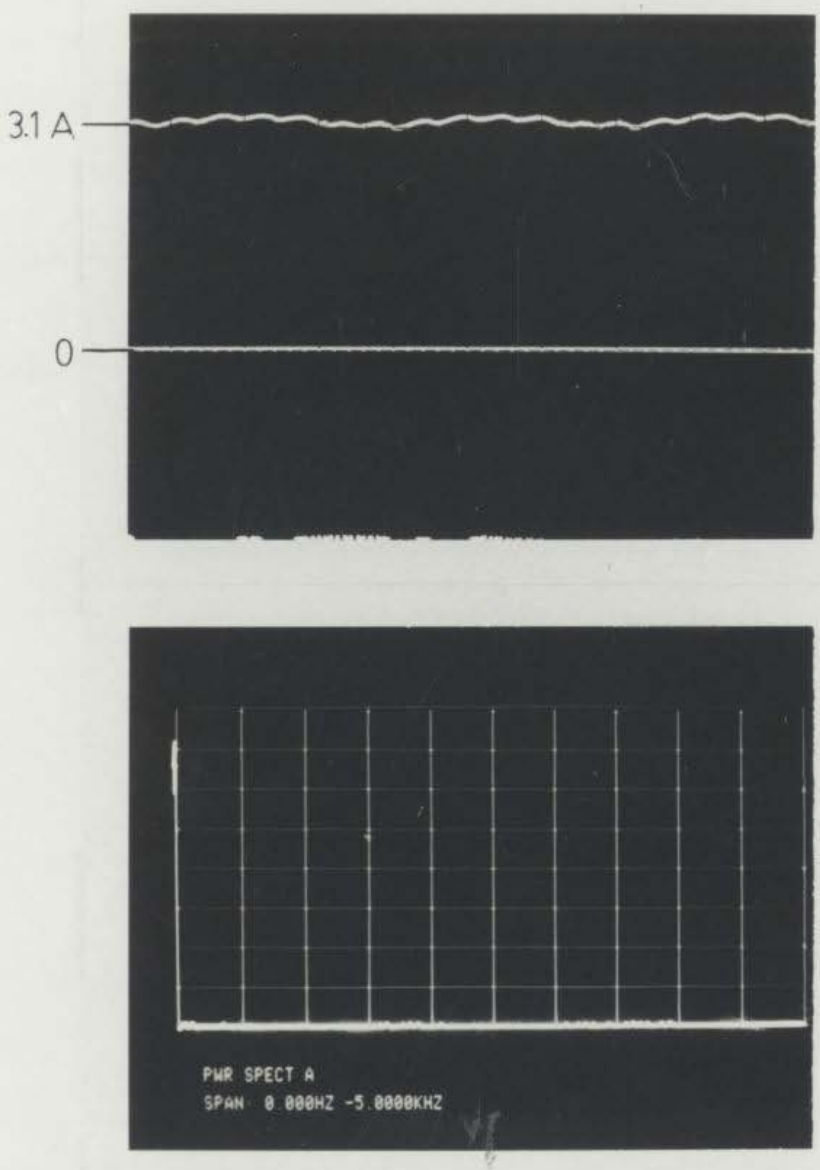


Figure 5.3: Experimental oscillograms of three phase DM converter with R-L load (a) output current waveform (b) corresponding harmonic spectrum

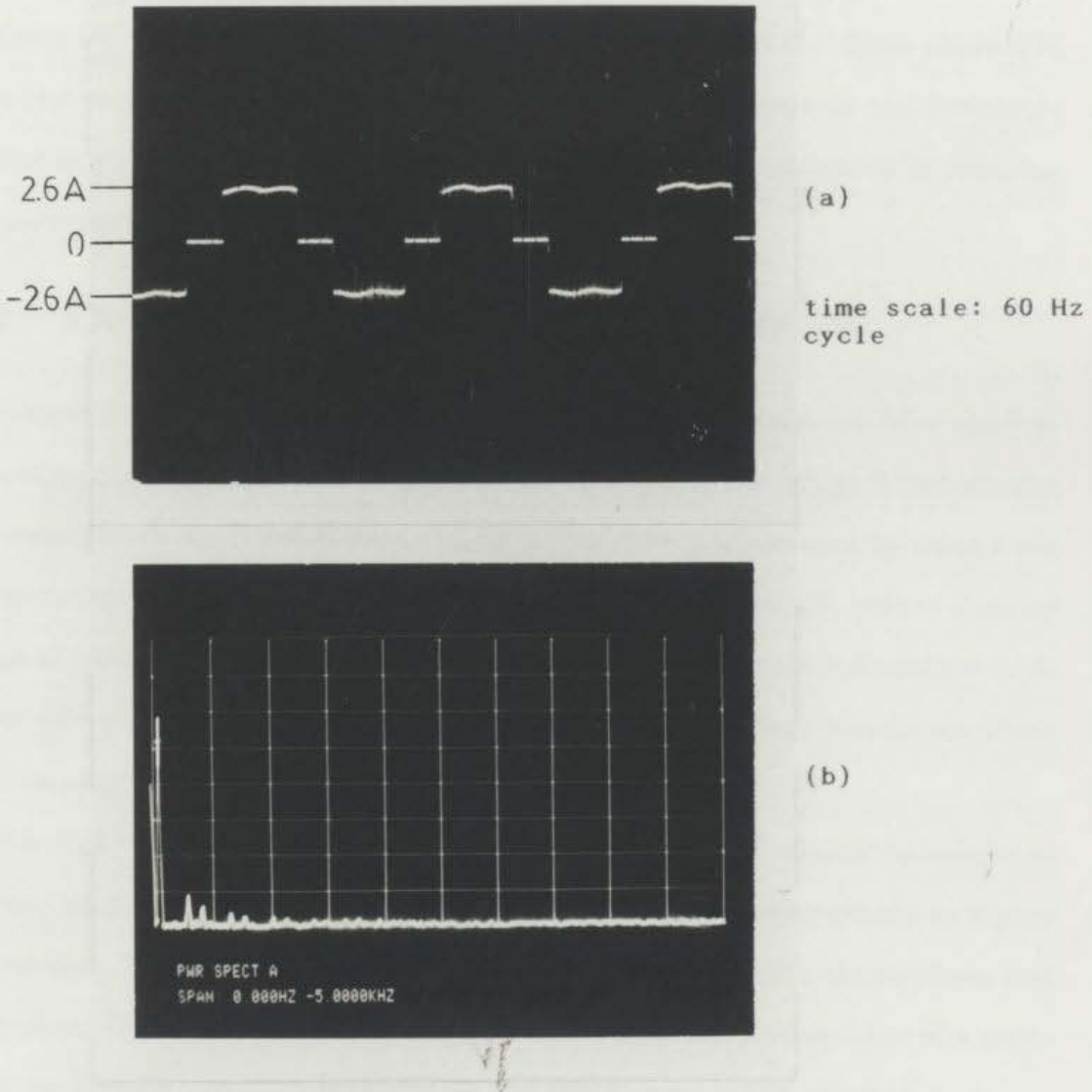


Figure 5.4: Experimental oscillograms of three phase DM converter with R-L load (a) input current waveform (b) corresponding line harmonic spectrum

to the three-phase DM converter under R-L load. Figure 5.3(a) shows the output current waveform of the DM converter and the corresponding harmonic spectrum is illustrated in Fig. 5.3(b). The input current waveform of one phase is shown in Fig. 5.4(a), while the harmonic spectrum is shown in Fig. 5.4(b).

From the experimental results, it can be concluded that the three-phase DM converter conforms to the requirements of continuous load current and low ripple content in the output. These characteristics are further investigated in studying the performance of the converter with motor loads.

5.2 Delta Modulated DC Motor Drive

The versatility of the dc motor has made it dominate in industrial drive applications of medium to large horse-power ratings. In recent years, a significant amount of research has been directed towards improving drive performance by using force commutation methods and PWM control techniques [5 - 10,12], rather than by means of passive reactive compensation schemes.[1,2]. The renewed interest in dc motor drives has been, by far, due to the introduction of power transistors which allow an easy implementation of PWM control strategies.

The DM technique has proved to be a successful PWM control technique as it draws near sinusoidal line currents and limits harmonic components to higher frequencies. These characteristics were demonstrated for both single-phase and three-phase DM converters. In the following sections the performance of a separately excited dc motor controlled with the DM scheme is investigated.

5.2.1 Separately Excited DC Motor

Speed control of separately excited dc motors can be achieved in two possible ways: (1) armature voltage control, and (2) field flux control. In the first method, speed of the motor is controlled by varying the armature voltage by means of a controlled rectifier and maintaining the field excitation at a constant value. Armature voltage control results in constant torque operation, allowing the speed to be controlled from almost zero to the rated speed. In the field control method, the armature terminal voltage is maintained at its rated value and the field voltage is controlled. With this control scheme, the speed of the motor can only be varied above the base speed and at the expense of falling torque. Field control results in the motor operating in the constant horsepower region.

Figure 5.5 shows the general set up of the converter - motor drive system. The armature terminals are supplied from the controlled three-phase DM rectifier and the field is excited from an independent dc source. Inclusion of the freewheeling diode, as mentioned earlier, has a number of advantages. Besides improving the power factor, freewheeling action also reduces the ripple content in the armature current, which otherwise leads to increased losses and a general derating of the motor. These advantages, however, are obtained at the expense of regenerative capability of the drive.

5.2.2 Basic Equations of the Motor

The armature circuit of the dc motor, is represented by the back emf E_b, the armature resistance R_a and armature inductance L_a, as shown in Fig. 5.5. The steady - state speed and torque equations of the motor are given as follows:

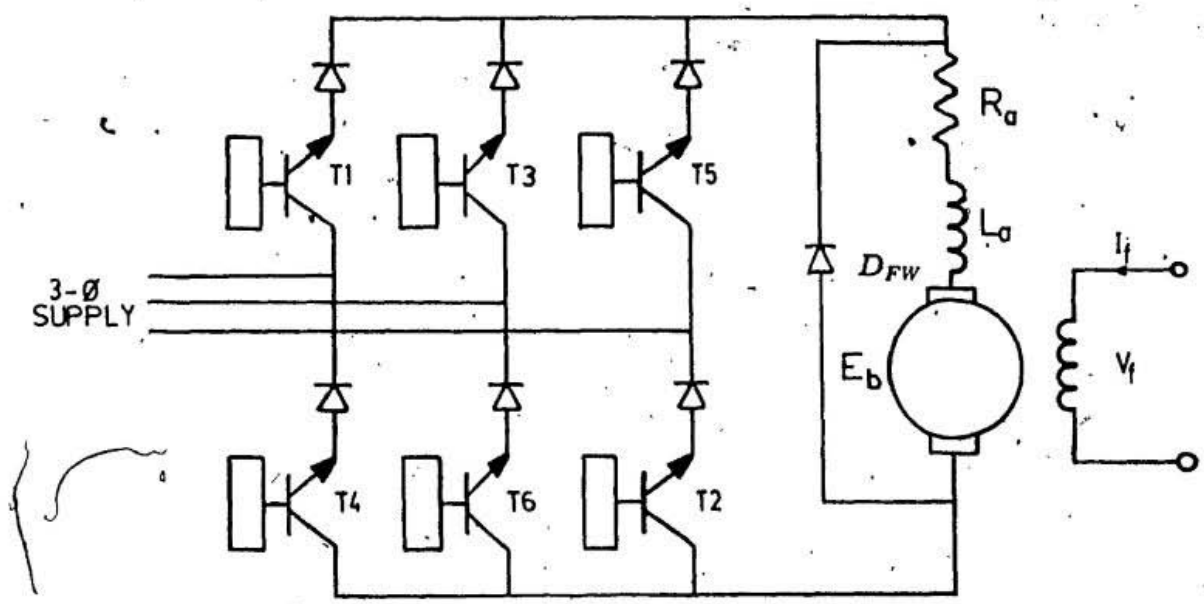


Figure 5.5: Three phase DM motor drive system

average back emf of the motor

$$E_b = K\,\phi\,N \tag{5.2}$$

average torque developed by the motor

$$T = K\,\phi\,I_a \tag{5.3}$$

where

I_a = average armature current [A]
N = steady-state speed [rad/sec]
$K\phi$ = motor constant [V-sec/rad]

The armature voltage equation in terms of average quantities is given by

$$E_a = R_a I_a + E_b \tag{5.4}$$

The steady-state speed of the motor is obtained by substituting Equation (5.2) in Equation (5.4) to give

$$N = \frac{E_a - I_a R_a}{K\phi} \tag{5.5}$$

Using the converter topology as shown in Fig. 5.5 and assuming continuous load current, the output voltage at the armature terminals is given by Equation (5.1) as

$$E_a = \frac{3\sqrt{2}V_L}{\pi} \sum_{i=1}^{N_p} \left[\frac{1}{2}(\cos\alpha_i - \cos\beta_i) + \frac{\sqrt{3}}{2}(\sin\beta_i - \sin\alpha_i)\right] \tag{5.6}$$

The steady-state motor speed can be expressed in terms of applied torque by substituting Equation (5.3) in Equation (5.5) to give

$$N = \frac{E_a}{K\phi} - \frac{R_a T}{(K\phi)^2} \tag{5.7}$$

The first term in Equation (5.7) represents the theoretical no-load speed while the second term represents the reduction in speed due to the applied torque. The theoretical no-load speed is a function of the converter switching signal and is controlled by varying the modulator parameters.

5.3 Performance Characteristics of DM Motor Drive

The three-phase DM converter with freewheeling diode was used to control the speed of a 1/4 hp, 120 V, 1800 rpm, dc motor. The motor rated parameters are given in Appendix D. Steady state performance of the motor was obtained for a maximum converter switching frequency of 2 kHz. Figure 5.6 shows the torque versus speed characteristics of the separately excited dc motor. The theoretical torque - speed characteristics were obtained by numerically solving Equation (5.7) for various load torque values and modulation parameters. Experimental points are also indicated in the same figure. For large Δ_p/Δ_n ratios, the armature current is constant resulting in good speed regulation. However, for low Δ_p/Δ_n ratios the experimental results show a slight variation from the predicted results due to load current tending to become discontinuous . The speed range also decreases as the ratio of Δ_p/Δ_n decreases.

Figure 5.7 shows typical results of power factor as a function average motor speed for constant torque operation. The supply power factor increases as the motor speed increases. Figure 5.8 shows that the distortion factor follows the pattern of power factor and also increases at the motor speed increases. The displacement factor is unity over the entire speed range as shown in Fig. 5.9.

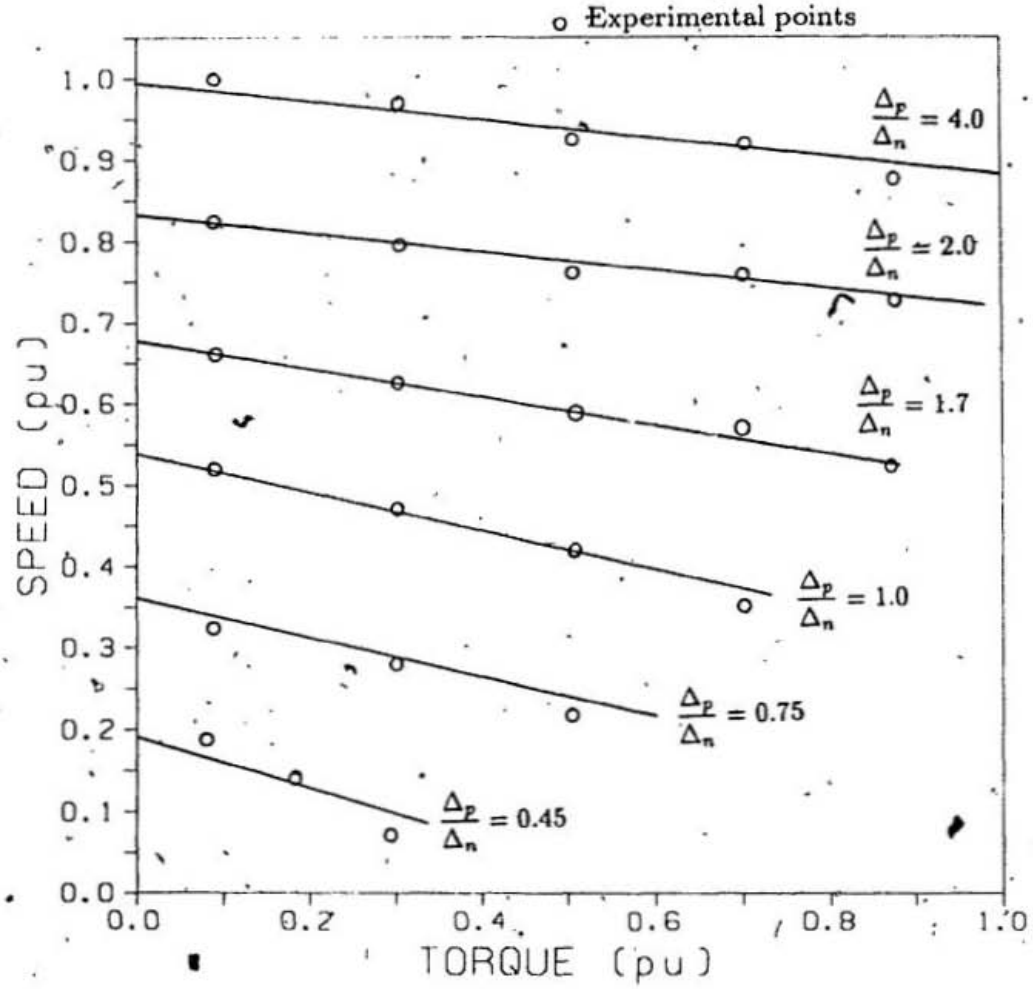


Figure 5.6: Torque speed characteristics of 1/4 Hp. dc motor controlled by three phase DM converter

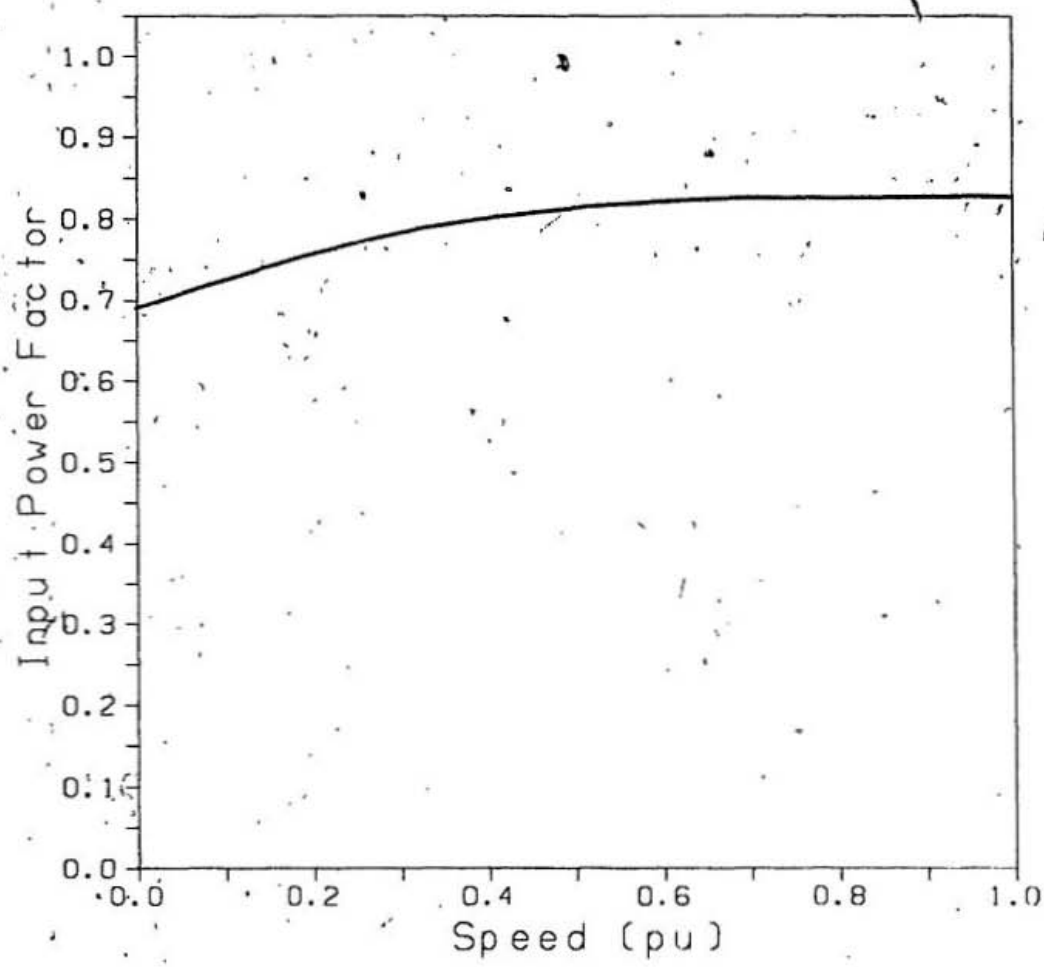


Figure 5.7: Power factor as a function of motor speed (experimental results)

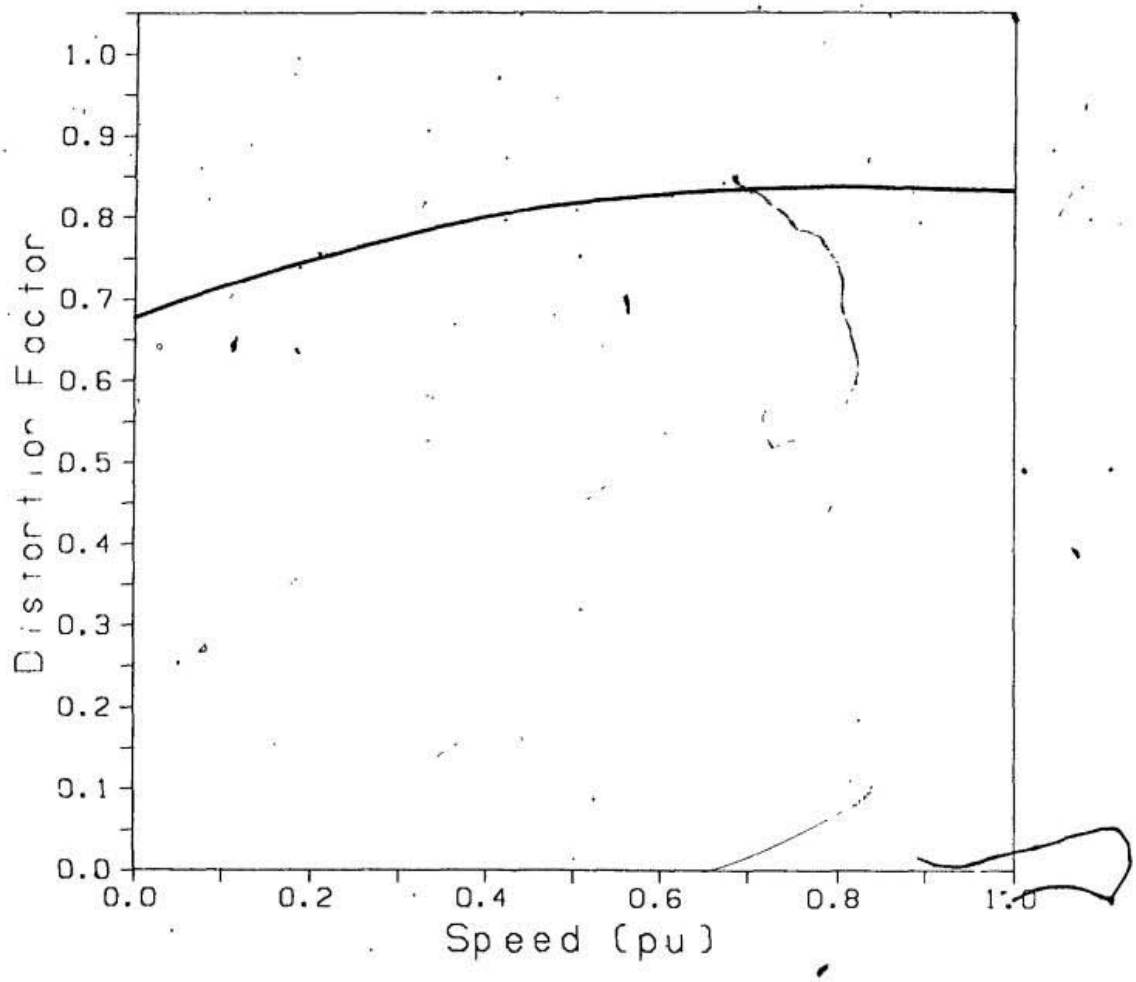


Figure 5.8: Distortion factor as a function of motor speed (experimental results)

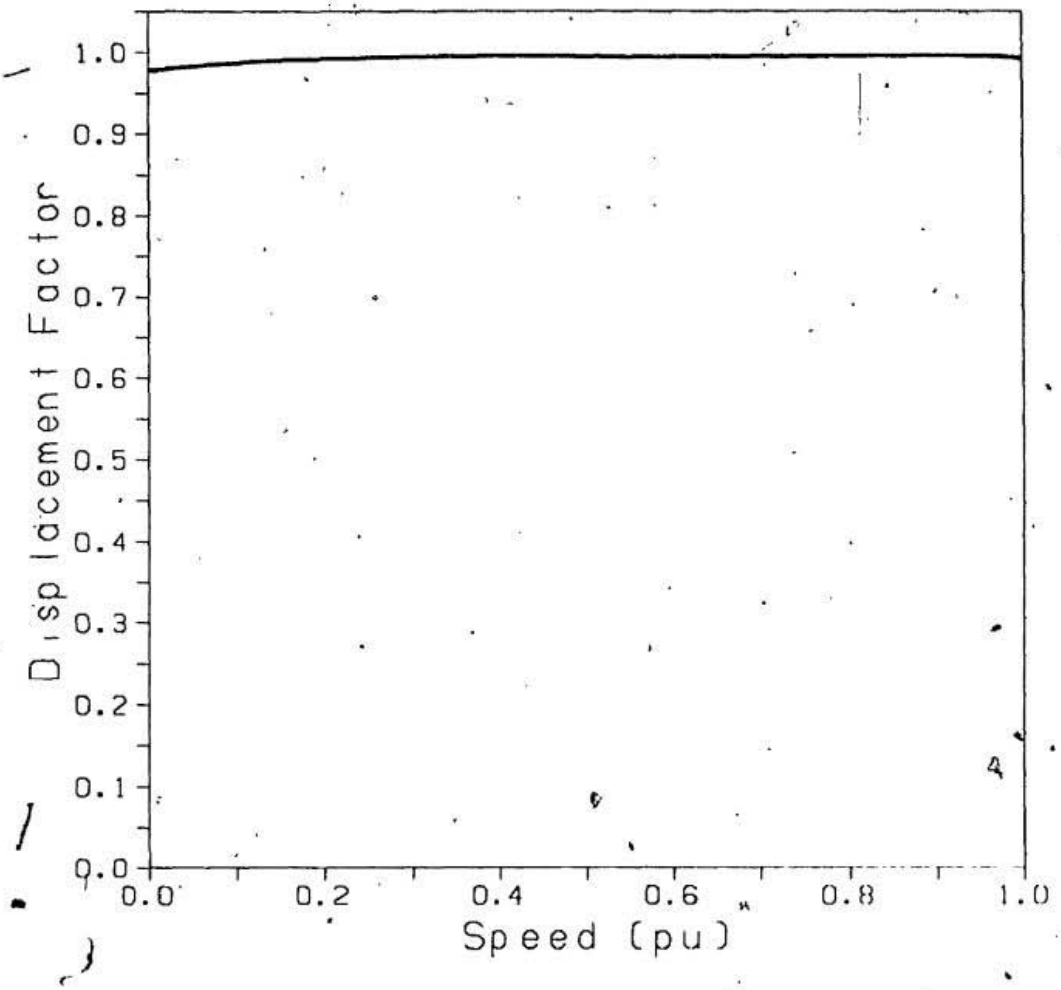


Figure 5.9: Displacement factor as a function of motor speed (experimental results)

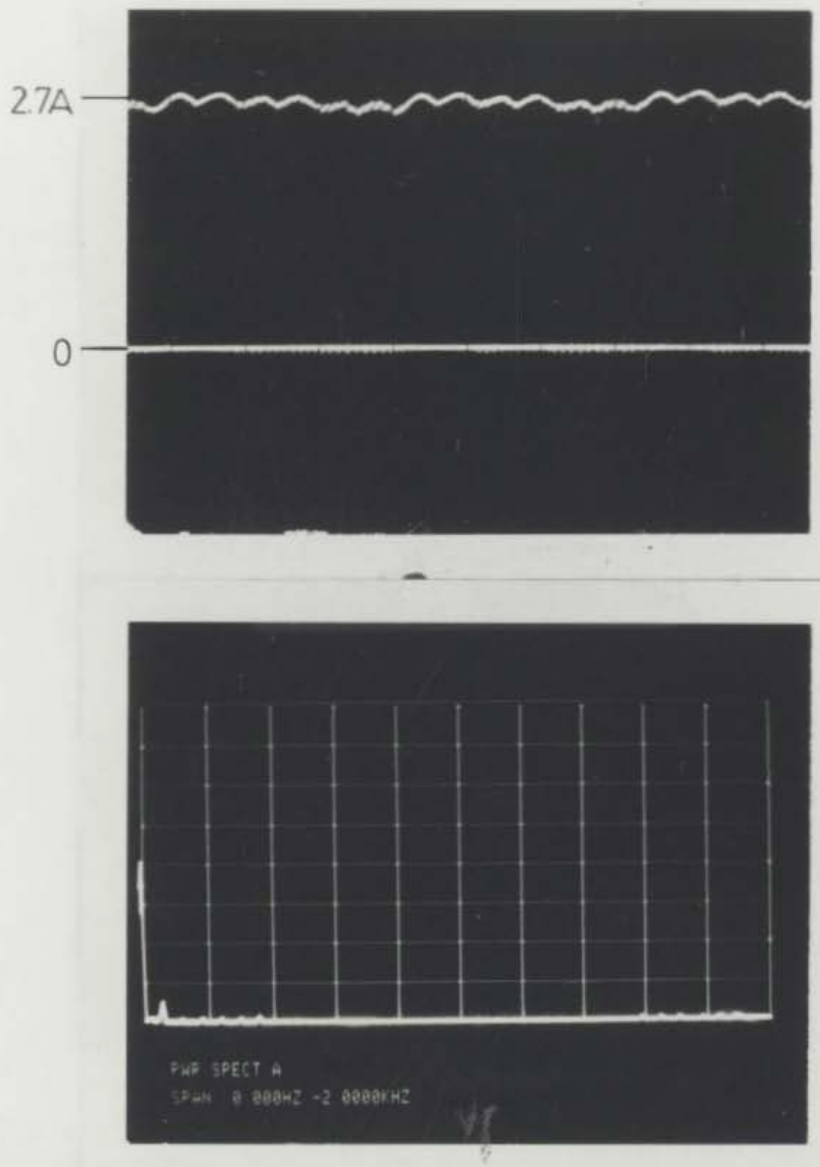
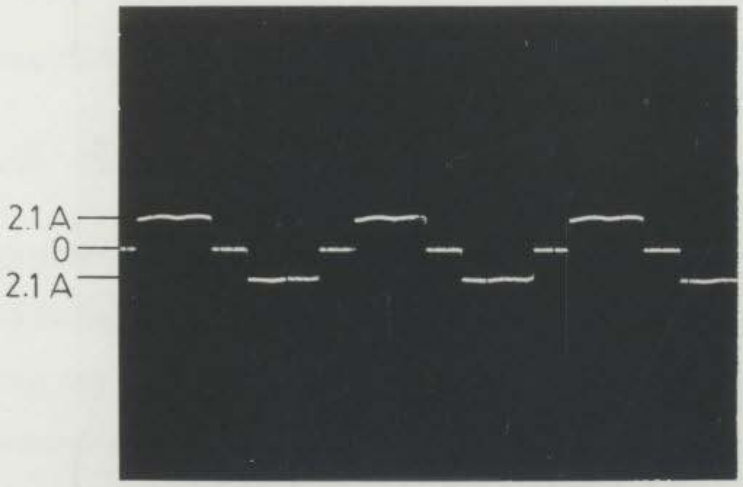
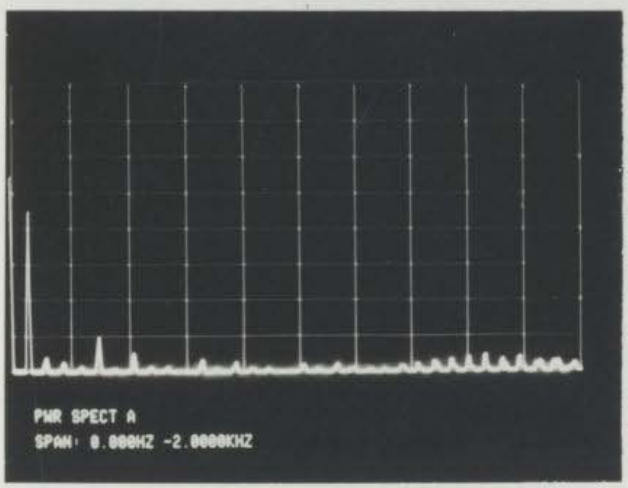


Figure 5.10: Experimental oscillograms of three phase DM converter with motor load: (a) armature current waveform (b) corresponding harmonic spectrum



(c)

time scale: based on
60 Hz cycle



(d)

Figure 5.10: continued: (c) input current of one phase (d) corresponding line harmonic spectrum

Typical experimental oscillograms of the DM motor drive are illustrated in Fig. 5.10. The armature current waveform shown in Fig. 5.10(a) indicates that the converter operates in the continuous current mode. The corresponding harmonic spectrum is shown in Fig. 5.10(b). Oscillograms of the input current waveform along with the harmonic spectrum are shown in Figs. 5.10(c) and (d).

5.4 Concluding Remarks

Experimental investigations of the performance of the three-phase DM converter with R-L and motor loads suggest that the DM converter provides enhanced power factor and low harmonic distortion. Inclusion of the freewheeling diode across the converter output terminals allows the load current to be continuous and ripple-free. This was demonstrated in the output current oscillograms which indicate negligible low order harmonic components. Of the predominant harmonics in the supply current, namely the 5^{th}, 7^{th}, 11^{th} and 13^{th} are of low amplitude and are almost constant over the entire operating range. These characteristics were observed for both cases of the converter suppling passive R-L and motor loads. In the case of the dc motor drive, a close agreement was found between theoretical torque-speed and experimental results.

Chapter 6

Conclusions

6.1 Summary

In this thesis, the analysis and implementation of the single-phase and three-phase delta modulated ac to dc converters have been presented. The predefined objectives of lower order harmonic attenuation, versatile control and improved operational power factor required for PWM controlled ac/dc converters were successfully realized using the delta modulation technique. The DM technique differs from the conventional carrier based PWM techniques, primarily due to its inherent self-carrier generating ability. This characteristic feature allows a simple circuit implementation of the modulator, without any additional complex circuit requirements for synchronization of modulating and carrier signals as is customary in most analog based PWM techniques currently in use. Of the family of delta modulators introduced in chapter 2, the rectangular wave delta modulator afforded a viable method to control converter output voltage. The control method was implemented by an asymmetrical control of the hysteresis quantizer window widths.

An analytical model was developed based on the intrinsic working principle of

of the rectangular wave delta modulator having asymmetrical hysteresis. The model provided a mathematical basis for accurately predicting convertor switching frequency. It also formulated a numerical approach for the determination of the PWM switching instances. Harmonic analysis of the single-phase and three-phase DM converter waveforms was carried out using the discrete Fourier transform approach. The converter output voltage and input current waveforms were defined in terms of generalized switching functions and the Fourier coefficients were evaluated using an efficient fast Fourier transform (FFT) algorithm.

Simulation results of the single-phase DM converter for different modulator parameters indicated a strong dependence of dominant harmonic distribution with modulator ripple frequency. This enabled the modulator to be designed to eliminate troublesome harmonic components up to a critical harmonic order, at the expense of increased commutation numbers. These results were verified both analytically and experimentally on a single-phase prototype DM converter. A comparative study of the performances of the conventional phase controlled converter and the DM converter revealed that the DM converter offers the advantages of higher power factor, lower harmonic distortion and reduced reactive power requirements.

The DM technique was extended to control the operation of three-phase ac to dc converters. Simulation results of the converter indicated that the three-phase DM converter exhibited switching characteristics similar to the single-phase DM converter. The converter switching frequency and dominant harmonic distribution pattern also followed those of the single-phase DM converter. Experimental investigations of the three-phase DM converter with R-L load suggested that the

DM converter meets the desired switching characteristics required for dc motor drives. Continuous mode of converter operation is feasible by inclusion of a free-wheeling diode across the output terminals. Due to multi pulsewidth modulation, the load current is mostly continuous resulting in an improvement in the ripple factor.

Finally, the performance of a separately excited dc motor fed from the three-phase DM converter was experimentally investigated. It was found that the torque-speed characteristics significantly improved due to continuous armature current. This was achieved without the use of any external inductance in the armature circuit. Since the displacement factor was held at unity over the entire control range, the power factor also improved.

6.2 Major Contributions

Major contributions of this thesis are:

- Demonstration of the possible use of delta modulation technique in single-phase and three-phase transistor ac to dc converters. It has been shown both analytically and experimentally that the delta modulation technique used for converter switching gives better performance than the conventional controlled rectifiers. The controllability of the delta modulation technique was found to be better than the sine PWM technique when implemented in analog circuit.

- Harmonic analysis of both the single-phase and three-phase DM converter waveforms were performed using the discrete Fourier transform method. To

use this approach, pertinent converter waveforms were defined in terms of generalized switching functions and harmonic components were numerically evaluated using an FFT algorithm. This method is simple and can readily be adopted in analysing any complex PWM waveform. Moreover, the DFT method is capable of calculating sub-harmonic components which are invariably present in PWM waveforms.

- Although the analytical model of the delta modulator presented pertains to ac to dc converters, it can be appropriately modified to suit inverter applications. Since in inverters, the switching waveform exhibits half wave symmetry, the hysteresis quantizer window widths are set equal (i.e. $\Delta_p = \Delta_n$). Variation in output voltage can easily be obtained by controlling the amplitude of the reference signal, keeping other modulator parameters constant. With the appropriate substitution $\Delta_p = \Delta_n$, equations (2.7) to (2.17) which provide modulator switching information are equally applicable for delta PWM inverters.

6.3 Recommendations for Future Work

Recommendations and avenues for future work include:

1. Analysis of the three-phase DM converter presented was based on the discontinuous current mode of operation encountered with resistive loads. Although performance of the converter with R-L and motor loads was investigated experimentally, detailed theoretical analyses were not within the scope of this thesis. It is suggested that the study be complemented by theoretical analysis of the converter performance due to continuous load

current operation with passive R-L and active motor loads. Secondly, it is recommended that a family of characteristic curves be developed to define discontinuous and continuous regions of DM converter operation for various modulator parameters and different load conditions.

2. Comparative evaluation of the performance of the DM converter with other PWM controlled converters should be undertaken.

3. Computer implementation of the DM technique is recommended. Since it is possible to predefine the delta PWM switching signal, the DM technique can be implemented using a dedicated microprocessor control system.

4. Design of the DM converter fed motor drive with regenerative braking capability should also be undertaken.

5. Investigate the performance of adaptive delta modulators, especially the tuned rectangular wave delta modulator and its applicability for both controlled rectifier and inverter systems.

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Appendix A

Derivation of DM Switching Instances

The differential encoding principle of the delta modulator results in the switching pulses to be quantized only in amplitude and not in time. The width of successive pulses are intrinsically determined by the hysteresis quantizer in the feedforward path (Fig. 2.5). Determination of the pulse widths is simplified by considering the hysteresis comparator as a bilevel quantizer with memory. Whenever the magnitude of the carrier wave exceeds the comparator threshold limit, it toggles state and each change of state results in a pulse transition i.e from $+V_s$ to $-V_s$ or vice - versa as may be the case. Hence as seen in Fig. A.1, the carrier wave appears to be bounded by the Δ_p and Δ_n threshold levels and oscillates between these preset limits. Each oscillation corresponds to a pulse width.

Since each pulse transition is a function of the previous quantizer state (sample value), it is necessary to determine a unique switching instant which will be the reference time instant for successive switching points. At system initiation, the carrier wave $v_C(t)$ begins to track the modulating sinusoidal signal $v_R(t)$ as shown in Fig. A.1. Therefore, the first switching instant, t_1 can be analytically determined by equating the instantaneous magnitudes of $v_C(t)$ and $v_R(t)$ as follows

$$\begin{aligned} M_p \cdot t_1 &= V_R \sin \omega_m t_1 + \Delta_p \\ t_1 &= \frac{V_R \sin \omega_m t_1 + \Delta_p}{M_p} \end{aligned}$$

The next subsequent switching point is obtained as

$$M_n\,(t_2 - t_1) = (V_R \sin \omega_m t_1 + \Delta_p) - (V_R \sin \omega_m t_2 - \Delta_n)$$

$$t_2 = t_1 + \frac{1}{M_n}\{(\Delta_p + \Delta_n) + V_R \sin \omega_m t_1 - V_R \sin \omega_m t_2\}$$

In general for each successive even switching instances $i = 2, 4, 6, \ldots$

$$t_i = \frac{1}{M_n}\{(\Delta_p + \Delta_n) + M_n t_{i-1} + V_R \sin \omega_m t_{i-1} - V_R \sin \omega_m t_i\}$$

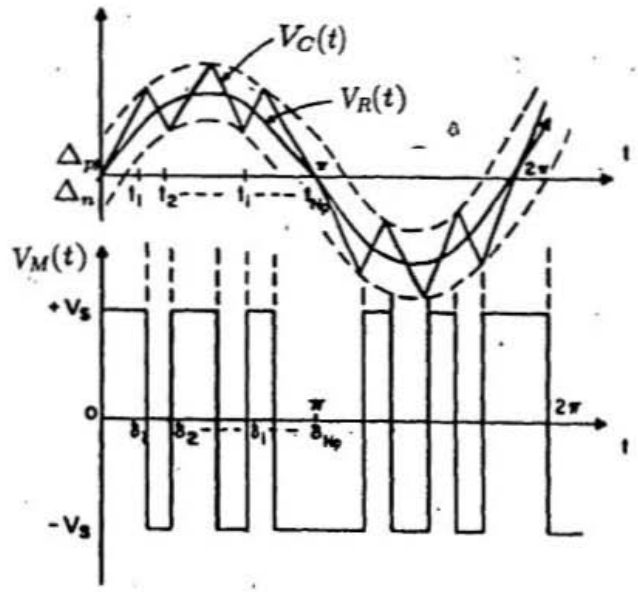

Figure A.1: Graphical encoding process of the delta modulator

Similarly for odd values, $i = 3, 5, 7, \ldots$

$$t_i = \frac{1}{M_p} \{(\Delta_p + \Delta_n) + M_p\, t_{i-1} - V_R \sin\omega_m t_{i-1} + V_R \sin\omega_m t_i\}$$

where

Δ_p	=	positive window width
Δ_n	=	negative window width
M_p	=	rising slope of carrier $v_C(t)$
M_n	=	falling slope of $v_C(t)$
ω_m	=	frequency of reference signal $v_R(t)$
V_R	=	amplitude of $v_R(t)$

The above equations are numerically computed to provide the switching instances. The Fortran computer program is listed in appendix B.

Appendix B

Computer Programs

B.1 Numerical Solution of Delta PWM Switching Instances

```
C*************************************************************
C       PROGRAM SOLVES THE CHARACTERISTIC DELTA MODULATION
C       EQUATIONS AND PROVIDES SWITCHING INSTANCES.  IMSL
C       ROUTINE ZREAL (V:10) IS USED TO SOLVE THE EQUATIONS.
C       DELTA.DAT=O/P DATAFILE WITH ALL SWITCHING INFO.
C       PWM.DAT=O/P DATAFILE CONTAINING SWITCHING POINTS
C*************************************************************
        COMMON PDELV,MDELV,VR,SLOPE,OMGA,FLAG,EQN
        REAL EPS,ERRABS,ERRREL,ETA,OMGA,PDELV,MDELV,MP,MN
        REAL SPTS(1000),LIMIT
        EXTERNAL F1,F,ZREAL
        EXTERNAL CARRIERWAVE,PWMWAVE
        OPEN(UNIT=9,FILE='DELTA.DAT',TYPE='NEW')
        OPEN(UNIT=7,FILE='PWM.DAT',TYPE='NEW')
C
        FR=60.
        PI=2.*ASIN(1.)
        OMGA=2.*PI*FR
        TMAX=1./FR
        TMAX2=TMAX/2.
        CRIT=TMAX2-(TMAX2*20.E-6)
C
C       SET MODULATOR PARAMETERS
C
        WRITE(6,*)'ENTER: VS+, VS-, VR, TAU=(1/RC)'
        READ(6,*)VSP,VSN,VR,TAU
        R1=10.E3
        R2=100.E3
        RATIO=R1/R2
        PDELV=VSP*RATIO
        MDELV=VSN*RATIO
        MP=VSP*TAU
        MN=VSN*TAU
        WRITE(9,2)VSP,VSN
  2     FORMAT(5X,'VS+ =',F10.4,3X,'VS- =',F10.4,/)
        WRITE(9,4)TAU,RATIO
  4     FORMAT(5X,'TAU =',F10.4,3X,'RATIO =',F10.4,/)
        WRITE(9,6)PDELV,MDELV
```

```
  6     FORMAT(5X,'PDELV =',F10.4,3X,'MDELV=',F10.4,/)
        WRITE(9,8)MP,MN
  8     FORMAT(5X,'MP =',F10.4,3X,'MN =',F10.4,//)
C
C       CHECK FOR SLOPE OVERLOAD
C
        IF((MP .LE. (OMGA*VR)) .OR. (MN .LE. (OMGA*VR))) THEN
                WRITE(6,1)
                WRITE(9,1)
  1             FORMAT(5X,'SLOPE OVERLOAD OCCURS'//)
                STOP
        ENDIF
C
        WRITE(6,10)
        WRITE(9,10)
  10    FORMAT(13X,'T',14X,'SEC',//)
        SPTS(1)=0.0
  20    FORMAT(11X,I3,6X,E15.6)
C
C       ASSIGN SUBROUTINE PARAMETERS
C
        EPS=1.E-8
        ERRABS=1.E-8
        ERRREL=1.E-8
        ETA=1.E-2
        ITMAX=500
        NROOT=1
        XGUESS=1.E-5
C
C       CALCULATE FIRST SWITCHING POINT
C
        N=1
        SLOPE=MP
        CALL ZREAL(F1,ERRABS,ERRREL,EPS,ETA,NROOT,
     * ITMAX,XGUESS,X,INFO)
        SPTS(N+1)=X
C
C       CALCULATE SUBSEQUENT SWITCHING POINTS
C
  50    N=N+1
        IF(JMOD(N,2) .NE. 0) THEN
                FLAG=-1.0
                SLOPE = MP
        ELSE
                FLAG=1.0
                SLOPE = MN .
        ENDIF
        EQN=(PDELV+MDELV)+SLOPE*X+FLAG*VR*SIN(OMGA*X)
```

```
      XGUESS=X*1.50
      CALL ZREAL(F,ERRABS,ERRREL,EPS,ETA,NROOT,
     * ITMAX,XGUESS,X,INFO)
      IF(X .GE. TMAX2)X=TMAX2
      SPTS(N+1)=X
      IF (X .EQ. TMAX2)GOTO 55
      IF (X .LE. CRIT)GOTO 50
55    WRITE(6,*)'N =',N
      NPTS=2*N+1
      WRITE(6,*)'NPTS=',NPTS
      DO 70 I=(N+1),NPTS
70    SPTS(I)=SPTS(I-N)+TMAX2
      WRITE(7,*)NPTS
      DO 80 I=1,NPTS
      II=I-1
      WRITE(7,*)SPTS(I)
80    WRITE(9,20)II,SPTS(I)
C
C     SUBROUTINE PWMWAVE CREATES A PLOTTING FILE OF
C     THE DELTA PWM SWITCHING WAVEFORM FROM THE
C     COMPUTED SWITCHING POINTS
C
      CALL PWMWAVE(SPTS,TMAX2,NPTS)
C
C     INCLUDE SUBROUTINE CARRIERWAVE TO OBTAIN PLOTTING
C     FILE OF THE CARRIER WAVEFORM
C
      CALL CARRIERWAVE(NPTS,PDELV,MDELV,OMGA,SPTS)
C
STOP
END
C*************************************************************
C FUNCTION DESCRIBING FIRST SWITCHING POINT EQUATION
C
REAL FUNCTION F1(X)
COMMON PDELV,MDELV,VR,SLOPE,OMGA,FLAG,EQN
REAL OMGA,PDELV,MDELV
F1=(PDELV+VR*SIN(OMGA*X))/SLOPE-X
RETURN
END
C*************************************************************
C GENERAL FUNCTION FOR ALL SEBSEQUENT SWITCHING POINTS
C
REAL FUNCTION F(X)
COMMON PDELV,MDELV,VR,SLOPE,OMGA,FLAG,EQN
REAL OMGA,PDELV,MDELV
F=(EQN-FLAG*VR*SIN(OMGA*X))/SLOPE-X
RETURN
```

```
END
C**********************************************************.
```

B.2 Single Phase DM Converter Analysis

B.2.1 Input Current Harmonic Analysis

```
C*************************************************************
C       INPUT CURRENT HARMONIC ANALYSIS OF 1-PHASE DM
C       CONVERTER USING FFT ALGORITHM. INPUT CURRENT
C       WAVEFORM IS DEFINED FROM THE DELTA PWM SWITCHING
C       POINTS. PERFORMANCE PARAMETERS OF THE 1-PHASE
C       CONVERTER ARE ALSO COMPUTED.
C       1PLC.DAT=O/P FILE CONTAINING HARMONIC SPECTRA
C*************************************************************
        REAL    SPTS(1000),PWM(4096),CN(2049),PHI(2049)
        REAL    OMGA,IRMS,I1,IH
        INTEGER CHECK,HN(2049)
        EXTERNAL FFT
C       EXTERNAL RECONSTRUCT
        OPEN(UNIT=5,FILE='PWM.DAT',TYPE='OLD')
        OPEN(UNIT=9,FILE='1PLC.DAT',TYPE='NEW')
        FR=60.
        PI=2.*ASIN(1.)
        OMGA=2.*PI*FR
        TMAX=1./FR
        READ(5,*)NPTS
        DO 10 I=1,NPTS
 10     READ(5,*)SPTS(I)
C
C       DEFINE LINE CURRENT WAVEFORM FROM PWM SWITCHING POINTS
C
        CHECK=(NPTS-1)/2+1
        IF(JMOD(CHECK,2) .EQ. 0) THEN
                NPTS=NPTS-1
                DO I=CHECK,(NPTS)
                SPTS(I)=SPTS(I+1)
                END DO
        ELSE
                NPTS=NPTS
        END IF
        TSAMPLE=TMAX/(2.**12.-1.)
        DELTS=0.
        NMAX=NPTS-1
        K=1
C
        DO 100 I=1,NMAX
        L=I+1
        IF(JMOD(I,2) .NE. 0) THEN
                FLAG=1.
```

```
      ELSE
     ,    FLAG=0.0
      ENDIF
 99   PWM(K)=FLAG*SQRT(2.)*SIN(OMGA*DELTS)
      DELTS=DELTS+TSAMPLE
      K=K+1
      IF(DELTS .LE. SPTS(L))GOTO 99
 100  CONTINUE
      NSAMPLE=K-1
      NCOEFF=NSAMPLE/2+1
C
C     COMPUTE FOURIER COEFFICIENTS
C
      CALL FFT(TSAMPLE,NSAMPLE,NCOEFF,PWM,HN,CN,PHI)
      WRITE(9,*)101
      DO 25 I=1,101
 25   WRITE(9,*)HN(I),CN(I)
C
C     CALCULATE CONVERTER PERFORMANCE PARAMETERS
C
      I1=CN(2)
      IRMS=0.0
      DO 17 I=1,100
 17   IRMS=IRMS + (CN(I)**2.)
      IRMS=SQRT(IRMS)
      WRITE(6,*)'I1=',I1
      WRITE(6,*)'I(rms) = ',IRMS
      DSF=COS(PHI(2))
      DTF=I1/IRMS
      PF=DTF*DSF
      WRITE(6,*)'Power Factor =',PF
      WRITE(6,*)'Displacement Factor =',DSF
      WRITE(6,*)'Distortion Factor =',DTF
C
C     INCLUDE SUBROUTINE RECONSTRUCT TO GENERATE PLOTTING
C     FILE OF CONVERTER SWITCHING WAVEFORM FROM COMPUTED
C     FFT COEFFICIENTS.
C     CALL RECONSTRUCT(NSAMPLE,CN,HN,PHI,OMGA)
C
      STOP
      END
C*************************************************************
```

B.2.2 Output Voltage Harmonic Analysis

```
C*************************************************************
C OUTPUT VOLTAGE HARMONIC ANALYSIS OF 1-PHASE DM
C CONVERTER USING FFT ALGORITHM. OUTPUT VOLTAGE
C IS DEFINED FROM PWM COMPUTED PWM SWITCHING POINTS.
C CONVERTER PERFORMANCE PARAMETERS ARE ALSO COMPUTED.
C 1PVO.DAT=O/P FILE CONTAINING HARMONIC SPECRTA
C*************************************************************
      REAL    SPTS(1000),PWM(4096),CN(2049),PHI(2049),OMGA
      INTEGER HN(2049)
      EXTERNAL FFT
C     EXTERNAL RECONSTRUCT
      OPEN(UNIT=5,FILE='PWM.DAT',TYPE='OLD')
      OPEN(UNIT=9,FILE='1PVO.DAT',TYPE='NEW')
      FR=60.
      PI=2.*ASIN(1.)
      OMGA=2.*PI*FR
      TMAX=1./FR
      TMAX2=TMAX/2.
      READ(5,*)NPTS
      DO 10 I=1,NPTS
 10   READ(5,*)SPTS(I)
      TSAMPLE=TMAX2/(2.**12.-1.)
      DELTS=0.
      K=1
C
C     DEFINE OUTPUT VOLTAGE WAVEFORM FROM PWM SWITCHING PTS
C
      I=1
 88   L=I+1
      IF(SPTS(I) .GE. TMAX2)GOTO 100
      IF(JMOD(I,2) .NE. 0) THEN
            FLAG=1.
      ELSE
            FLAG=0.0
      ENDIF
 99   PWM(K)=FLAG*SQRT(2.)*SIN(OMGA*DELTS)
      DELTS=DELTS+TSAMPLE
      K=K+1
      IF(DELTS .LE. SPTS(L))GOTO 99
      I=I+1
      GOTO 88
C
 100  NSAMPLE=K-1
      NCOEFF=NSAMPLE/2+1
C
C     COMPUTE FOURIER COEFFICIENTS
```

```
C
      CALL FFT(TSAMPLE,NSAMPLE,NCOEFF,PWM,HN,CN,PHI)
      WRITE(9,*)101
      DO 25 I=1,101
25    WRITE(9,*)HN(I),CN(I)
C
C     DETERMINE OUTPUT PERFORMANCE PARAMETERS
C
      VO=CN(1)/.9
      VRN=0.
      DO 17 I=2,100
17    VRN=VRN +((CN(I)**2.)/2.)
      VRMS=SQRT(VO*VO + VRN)
      WRITE(6,*)'Vo =',VO
      WRITE(6,*)'V(harmonics) =',VRN
      WRITE(6,*)'V(rms) =',VRMS
      RF=VRN/VO
      WRITE(6,*)'Ripple Factor=',RF
C
C     INCLUDE SUBROUTINE RECONSTRUCT TO GENERATE PLOTTING
C     FILE OF CONVERTER SWITCHING WAVEFORM FROM COMPUTED
C     FFT COEFFICIENTS.
C     CALL RECONSTRUCT(NSAMPLE,CN,HN,PHI,OMGA)
C
      STOP
      END
C*************************************************************
```

B.3 Three Phase DM Converter Analysis

B.3.1 Input Current Harmonic Analysis

```
C*************************************************************
C       INPUT CURRENT HARMONIC ANALYSIS OF 3-PHASE DM
C       CONVERTER USING FFT ALGORITHM. PROGRAM DEFINES
C       3-PHASE LINE CURRENT WAVEFORM ACCORDING TO COMPUTED
C       DELTA SWITCHING POINTS. PERFORMANCE PARAMETERS ARE
C       ALSO COMPUTED.
C       3PLC.DAT=O/P FILE OF HARMONIC SPECTRA.
C*************************************************************
        REAL SPTS(1000),PWM(4096),CN(2049),PHI(2049),OMGA
        REAL SW(1000),IRMS,I1
        INTEGER  HN(2049)
        EXTERNAL FFT
C       EXTERNAL RECONSTRUCT
        OPEN(UNIT=5,FILE='PWM.DAT',TYPE='OLD')
        OPEN(UNIT=9,FILE='3PLC.DAT',TYPE='NEW')
        FR=60.
        PI=2.*ASIN(1.)
        OMGA=2.*PI*FR
        T60=1./360.
        PI3=PI/3.
        READ(5,*)NPTS
        READ(5,*)(SPTS(I), I=1,NPTS)
        TSAMPLE=1./(FR*(2.**12.-1.))
C
C       DEFINE LINE CURRENT WAVEFORM FROM DELTA SWITCHING POINTS
C
        DELTS=0.
        K=1
        I=1
   10   L=I+1
        SW(I)=SPTS(I)
        IF((SPTS(I) .LT. T60) .AND. (SPTS(L) .GE. T60))GOTO 15
        I=I+1
        GOTO 10
   15   NMAX=4*I+1
        NMAX2=2*I+1
        I4=4*I
        I2=2*I
        IF(JMOD(I,2) .EQ. 0)GOTO 30
        DO 20 J=(I+1),(2*I-1)
        N=J+1-I
   20   SW(J)=SW(N)+T60
        SW(I2)=2.*T60
```

```
      DO 25 J=NMAX2,(4*I)
      N=J-2*I
25    SW(J)=SW(N)+3.*T60
      SW(NMAX)=6.*T60
      GOTO 50
30    DO 35 J=(I+1),(2*I)
      N=J-I
35    SW(J)=SW(N)+T60
      DO 40 J=(NMAX2),(NMAX)
      N=J-2*I
40    SW(J)=SW(N)+3.*T60
50    I=1
88    L=I+1
      IF(SW(I) .GE. 6.*T60)GOTO 100
      IF(JMOD(I,2) .NE. 0) THEN
            FLAG=1.
      ELSE
            FLAG=0.0
      ENDIF
99    IF(DELTS .LE. T60)X=DELTS+T60
      IF((DELTS .GT. T60).AND.(DELTS .LE. 2*T60))X=DELTS
      IF((DELTS .GT. 2.*T60).AND.(DELTS .LT. 3.*T60))X=0.
      IF((DELTS .GE. 3.*T60).AND.(DELTS .LE. 4.*T60))X=(2.*T60-DELTS)
      IF((DELTS .GT. 4.*T60).AND.(DELTS .LE. 5.*T60))X=(3.*T60-DELTS)
      IF(DELTS .GT. 5.*T60)X=0.
      PWM(K)=FLAG*SIN(OMGA*X)
      DELTS=DELTS+TS
      K=K+1
      IF(DELTS .LE. SW(L))GOTO 99
      I=I+1
      GOTO 88
100   NSAMPLE=K-1
      NCOEFF=NSAMPLE/2+1
C
C     COMPUTE FOURIER COEFFICIENTS
C
      CALL FFT(TSAMPLE,NSAMPLE,NCOEFF,PWM,HN,CN,PHI)
      WRITE(9,*)101
      DO 250 I=1,101
250   WRITE(9,*)HN(I),CN(I)
C
C     CALCULATE PERFORMANCE PARAMETERS
C
      I1=CN(2)
      WRITE(6,*)1,I1
      DO J=1,4
      J1=6*J
      J2=6*J+2
```

```
      WRITE(6,*)J1-1,CN(J1)
      WRITE(6,*)J2-1,CN(J2)
      END DO
      IRMS=0.0
      DO 17 I=1,100
   17 IRMS=IRMS + (CN(I)**2.)
      IRMS=SQRT(IRMS)
      WRITE(6,*)'I1=',I1
      WRITE(6,*)'I(rms) = ',IRMS
      TETA=PHI(2)-PI3
      DSF=COS(TETA)
      DTF=I1/IRMS
      PF=DTF*DSF
      WRITE(6,*)'Power Factor =',PF
      WRITE(6,*)'Displacement Factor =',DSF
      WRITE(6,*)'Distortion Factor =',DTF
C
C     INCLUDE SUBROUTINE RECONSTRUCT TO GENERATE PLOTTING
C     FILE OF CONVERTER SWITCHING WAVEFORM FROM COMPUTED
C     FFT COEFFICIENTS.
C     CALL RECONSTRUCT(NSAMPLE,CN,HN,PHI,OMGA)
C
      STOP
      END
C*************************************************************
```

B.3.2 Output Voltage Harmonic Analysis

```
C*************************************************************
C       OUTPUT VOLTAGE  HARMONIC ANALYSIS OF 3-PHASE DM
C     . CONVERTER USING FFT ALGORITHM. PROGRAM DEFINES
C       OUTPUT VOLTAGE WAVEFORM ACCORDING TO THE COMPUTED
C       DELTA SWITCHING POINTS. PERFORMANCE PARAMETERS ARE
C       ALSO COMPUTED.
C       3PVO.DAT=O/P FILE OF HARMONIC SPECTRA
C*************************************************************
        REAL    SPTS(1000),PWM(4096),CN(2049),PHI(2049),OMGA
        INTEGER HN(2049)
        EXTERNAL FFT
C       EXTERNAL RECONSTRUCT
        OPEN(UNIT=5,FILE='PWM.DAT',TYPE='OLD')
        OPEN(UNIT=9,FILE='3PVO.DAT',TYPE='NEW')
        FR=60.
        PI=2.*ASIN(1.)
        OMGA=2.*PI*FR
        T60=1./360.
        VOPU=3./PI
        READ(5,*)NPTS
        READ(5,*)(SPTS(I), I=1,NPTS)
        TS=T60/(2.**11.-1.)
        DELTS=0.0
        K=0
C
C       DEFINE OUTPUT VOLTAGE WAVEFORM FROM PWM SWITCHING POINTS
C
        I=1
  88    L=I+1
        IF(SPTS(I) .GE. T60)GOTO 100
        IF((SPTS(I) .LT. T60) .AND. (SPTS(L) .GT. T60))SPTS(L)=T60
        IF(SPTS(L) .GE. T60)SPTS(L)=T60
        IF(JMOD(I,2) .NE. 0) THEN
                FLAG=1.
        ELSE
                FLAG=0.0
        ENDIF
  99    K=K+1
        X=DELTS+T60
        PWM(K)=FLAG*SIN(OMGA*X)
        DELTS=DELTS+TS
        IF(DELTS .LE. SPTS(L))GOTO 99
        I=I+1
        GOTO 88
 100    NSAMPLE=K
        NCOEFF=NSAMPLE/2+1
C
```

```
C       COMPUTE FOURIER COEFFICIENTS
C
        CALL FFT(TSAMPLE,NSAMPLE,NCOEFF,PWM,HN,CN,PHI)
        WRITE(9,*)101
        DO 250 I=1,101
  250   WRITE(9,*)HN(I),CN(I)
C
C
C       DETERMINE PERFORMANCE PARAMETERS
C
        VO=CN(1)
        VRN=0.
        DO 17 I=2,4
   17   VRN=VRN +((CN(I)**2.)/2.)
        VRMS=SQRT(VO*VO + VRN)
        WRITE(6,*)'Vo (pu)= ',VO/VOPU
        WRITE(6,*)'V(harmonics) =',VRN
        WRITE(6,*)'V(rms) =',VRMS
        RF=VRN/VO
        WRITE(6,*)'Ripple Factor=',RF
C
C       INCLUDE SUBROUTINE RECONSTRUCT TO GENERATE PLOTTING
C       FILE OF CONVERTER SWITCHING WAVEFORM FROM COMPUTED
C       FFT COEFFICIENTS.
C       CALL RECONSTRUCT(NSAMPLE,CN,HN,PHI,OMGA)
C
        STOP
        END
C*************************************************************
```

B.4 Subroutines

B.4.1 Subroutine FFT

```
C*************************************************************
C       SUBROUTINE TO COMPUTE THE FOURIER COEFFICIENTS OF A
C       SAMPLED DATA ARRAY VIA IMSL ROUTINE FFTSC (VER: 9.2)
C*************************************************************
        SUBROUTINE FFT(TSAMPLE,NSAMPLE,NCOEFF,PWM,HN,CN,PHI)
        REAL  PWM(4096),ST(2049),CT(2049),PHI(2049),CN(2049)
        REAL  IWK(12),WK(12)
        INTEGER  HN(2049)
        COMPLEX  CWK(2049)
        EXTERNAL  FFTSC
C
C       DETERMINE FREQUENCY COMPONENTS
C
        DO J=1,NCOEFF
        H=(FLOATJ(J)-1.)/(NSAMPLE*TSAMPLE*60.)
        HN(J)=JNINT(H)
        END DO
C
C       COMPUTE COEFFICIENTS
C
        CALL FFTSC(PWM,NSAMPLE,ST,CT,IWK,WK,CWK)
        DO K=1,NCOEFF
        CT(K)=CT(K)/NSAMPLE
        ST(K)=ST(K)/NSAMPLE
        END DO
        CT(1)=CT(1)/2.0
        ST(1)=ST(1)/2.0
        CT(NCOEFF)=CT(NCOEFF)/2.0
        ST(NCOEFF)=ST(NCOEFF)/2.0
        DO I=1,NCOEFF
        CN(I)=SQRT(CT(I)**2.+ST(I)**2.)
        PHI(I)=ATAN2(ST(I),CT(I))
        END DO
        RETURN
        END
C*************************************************************
```

B.4.2 Subroutine PWMWAVE

```
C*************************************************************
C       SUBROUTINE TO GENERATE PWM SWITCHING WAVEFORM  FROM
C       COMPUTED SWITCHING POINTS
C       PWMWAVE.DAT=O/P FILE CONTAINING PLOTTING DATA
C*************************************************************
        SUBROUTINE PWMWAVE(SPTS,TMAX2,NPTS)
        REAL   SPTS(1000),M(1000),P(1000)
        OPEN(UNIT=11,FILE='PWMWAVE.DAT',TYPE='NEW')
        AMPP=1.0
        AMPN=-1.0
        M(1)=SPTS(1)
        P(1)=AMPP
        L=2
        FLAG=1.0
        DO 120 J=2,NPTS
        IF(J .NE. (NPTS)) THEN
        IF((SPTS(J) .EQ. TMAX2) .AND. (P(L-1) .EQ. AMPP)) FLAG=-1.0
           IF (FLAG .GT. 0.0) THEN
                IF(JMOD(J,2) .EQ. 0) THEN
                        M(L)=SPTS(J)
                        P(L)=AMPP
                        L=L+1
                        M(L)=SPTS(J)
                        P(L)=AMPN
                        L=L+1
                ELSE
                        M(L)=SPTS(J)
                        P(L)=AMPN
                        L=L+1
                        M(L)=SPTS(J)
                        P(L)=AMPP
                        L=L+1
               ENDIF
           ELSE
                IF(SPTS(J) .NE. TMAX2) THEN
                   IF(JMOD(J,2) .NE. 0) THEN
                        M(L)=SPTS(J)
                        P(L)=AMPP
                        L=L+1
                        M(L)=SPTS(J)
                        P(L)=AMPN
                        L=L+1
                   ELSE
                        M(L)=SPTS(J)
                        P(L)=AMPN
                        L=L+1
```

```
                        M(L)=SPTS(J)
                        P(L)=AMPP
                        L=L+1
                    ENDIF
                ENDIF
            ENDIF
        ELSE
                IF(P(L-1) .EQ. AMPN) THEN
                        M(L)=SPTS(J)
                        P(L)=AMPN
                ELSE
                        M(L)=SPTS(J)
                        P(L)=AMPP
                        L=L+1
                        M(L)=SPTS(J)
                        P(L)=AMPN
                ENDIF
        ENDIF
120     CONTINUE
        DO 130 I=1,L
130     WRITE(11,140)M(I),P(I)
140     FORMAT(F11.8,5X,F8.4)
        RETURN
        END
C*************************************************************
```

B.4.3 Subroutine CARRIERWAVE

```
C*************************************************************
C       SUBROUTINE TO GENERATE CARRIER WAVEFORM FROM
C       COMPUTED SWITCHING POINTS.
C       CARRIER.DAT=O/P FILE CONTAINING PLOTTING POINTS
C*************************************************************
        SUBROUTINE CARRIERWAVE(NPTS,PDELV,MDELV,OMGA,SPTS)
        REAL    . SPTS(1000),CARR(1000),LIMIT,PDELV,MDELV
        OPEN(UNIT=13,FILE='CARRIER.DAT',TYPE='NEW')
        CARR(1)=0.0
        DO 150 I=1,NPTS
        IF (I .NE. 1) THEN
                IF(JMOD(I,2) .EQ. 0) THEN
                        LIMIT=PDELV
                ELSE
                        LIMIT=-MDELV
        ENDIF
        CARR(I)=VR*SIN(OMGA*SPTS(I))+LIMIT
        ENDIF
  150   WRITE(13,140)SPTS(I),CARR(I)
        RETURN
        END
C*************************************************************
```

B.4.4 Subroutine RECONSTRUCT

```
C*************************************************************
C       SUBROUTINE TO RECONSTRUCT PWM WAVEFORM FROM
C       COMPUTED FOURIER COEFFICIENTS
C       RECONST.DAT=O/P FILE CONTAINING PLOTTING POINTS
C*************************************************************
        SUBROUTINE RECONSTRUCT(NSAMPLE,CN,HN,PHI,OMGA)
        REAL    RMW(500),CN(2049),PHI(2049),OMGA
        INTEGER HN(2049)
        OPEN(UNIT=10,FILE='RECONST.DAT',TYPE='NEW')
        INDX=1
        T=0.
        WRITE(6,*)'ENTER: PMAX (deg)'
        READ(6,*)PMAX
        DELT=(PMAX-0.)/500.
  650   RMW(INDX)=0.0
        SUMT=0.0
        DO 700 I=2,NSAMPLE
        RX=CN(I)*COS(FLOATJ(HN(I))*OMGA*T-PHI(I))
        SUMT=SUMT+RX
  700   CONTINUE
        RMW(INDX)=CN(1)+SUMT
        WRITE(10,*)T,RMW(INDX)
        T=T+DELT
        INDX=INDX+1
        IF( T .LE. PMAX)GOTO 650
        RETURN
        END
C*************************************************************
```

Appendix C

Schematic Diagrams

C.1: Single phase delta modulator

C.2: Base drive circuit

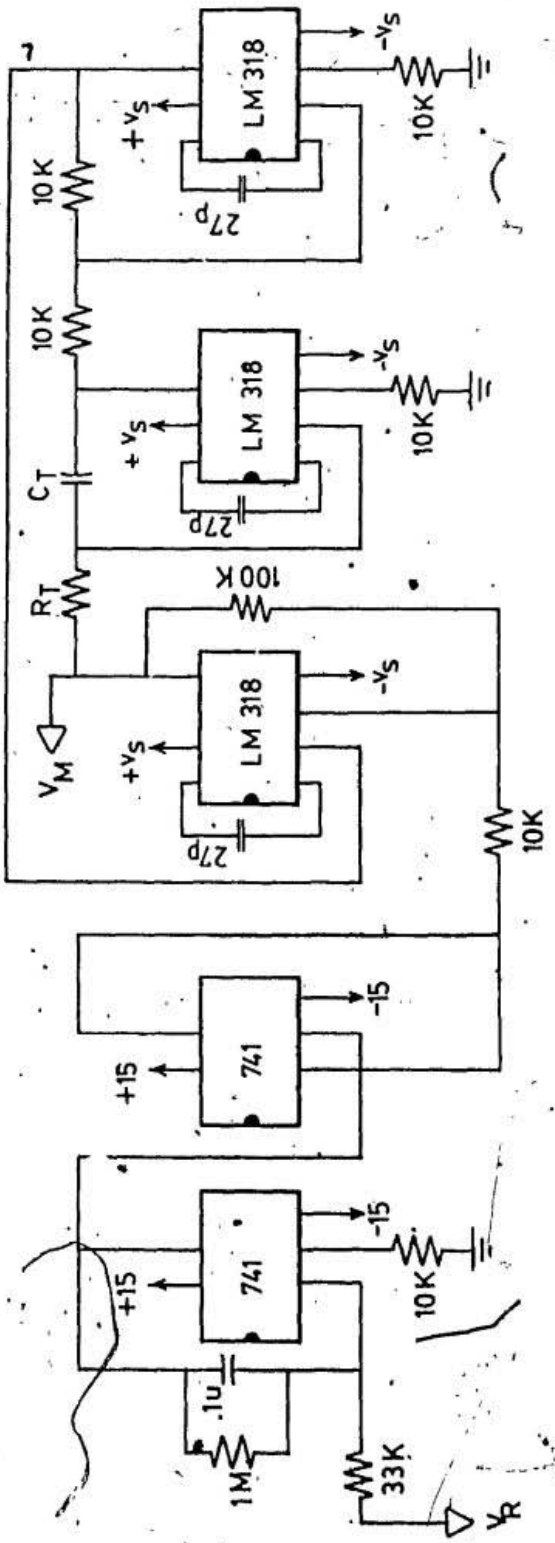

Figure C.1: Single phase delta modulator

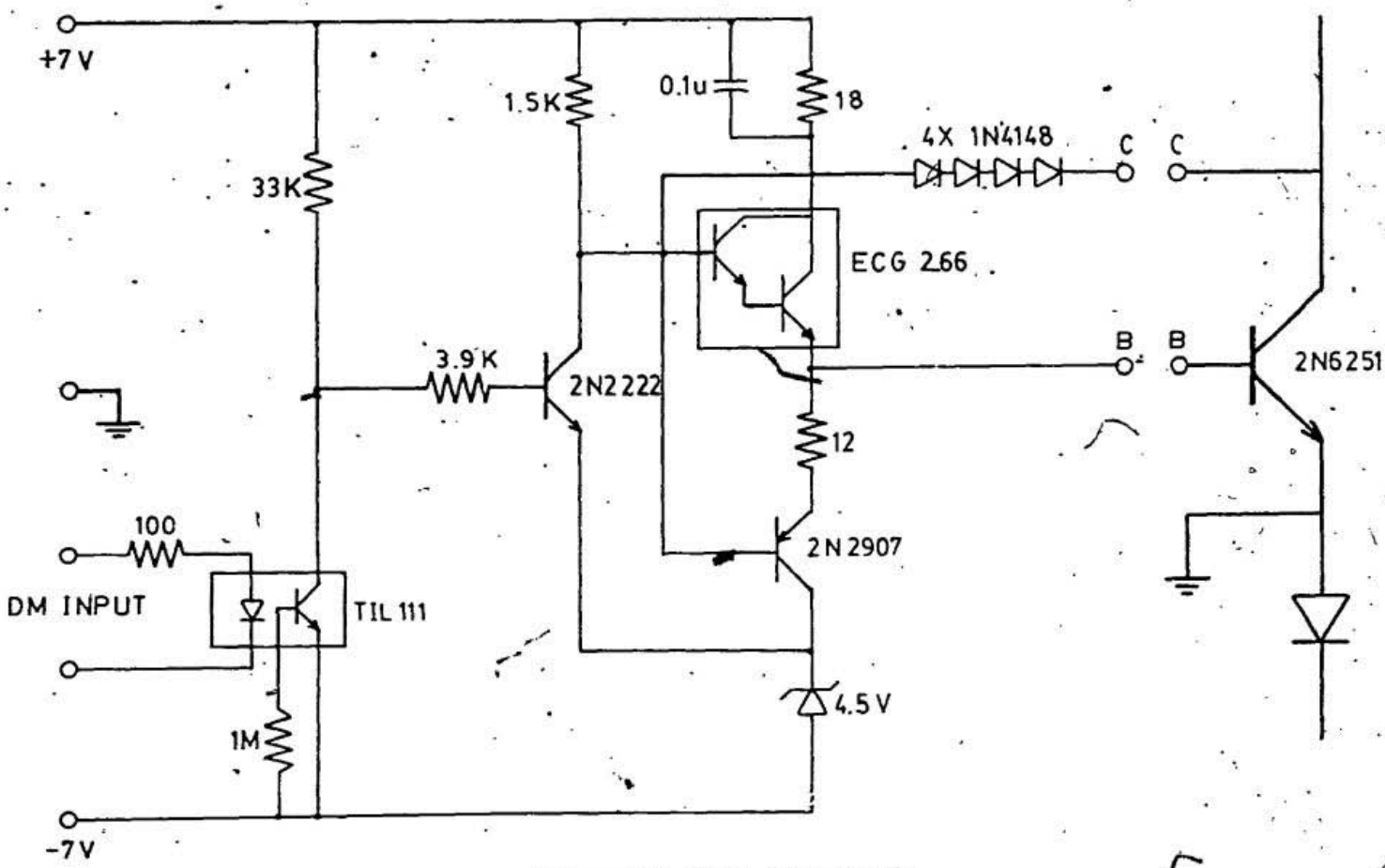

Figure C.2: Base drive circuit

Appendix D

Circuit Parameters

Motor rating and parameters:

Rated power	186.5 W (1/4 hp)
Rated voltage	120 V
Rated current	2.8 A
Rated speed	1800 rpm
Armature Resistance	8.0 Ω
Motor constant	0.63 V.s/rad

Power transistor parameters:

Type	Motorola 2N6251
V_{CE}	350 V
I_C continuous	15 A
I_C peak	30 A
P_D	175 W
Rise time t_r	2.0 μs
Fall time t_f	1.0 μs