PERFORMANCE OF CLASS-E INVERTERS UNDER NON-RESISTIVE LOADS

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ABSTRACT

Class-E inverters are popularly used in high frequency wireless power transmission because of their compact design and high efficiency. The inverter consists of resonant elements and a transistor, typically a wide band gap device that is toggled to provide an alternating current signal to the load. Although being a highly efficient and flexible converter, most analysis for this inverter assumes resistive loading. In the presence of non-resistive loading, the performance of the inverter can be negatively impacted.

This work investigates the performance of the load-independent Class-E and Class-E push-pull inverters under non-resistive loads. Several solutions are proposed to mitigate or prevent the associated performance degradations. Although the proposed solutions are flexible at working with any applications, the target application for this work is a capacitive coupled wireless power transfer system. It is shown that a suitable matching network or reactive power compensation can maintain highly efficient Class-E inverter performance even under non-ideal loading conditions.

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LIST OF ABBREVIATIONS AND SYMBOLS

f	The operating frequency of the inverter.
ω	The angular frequency where $\omega = 2\pi f$.
f_r	The resonance frequency of the filter, typically equal to f.
l, W, D	The length (l), Width (W) of a rectangular electrode and the distance (D) between each pair of electrodes.
L	The inductance of an inductor measured in Henries (H).
C	The capacitance of a capacitor measured in Farads (F).
V_{rms}	The rms voltage across a component. Also equal to V.
I_{rms}	The rms current through a component.
Z, Z^*	The impedance (Z) and the conjugate of the impedance (Z^*) of a network.
Q_n	The nth transistor on an inverter.
$s(t)$	The variable used to represent the transistor on/off behavior.
v_s	The voltage across the transistor of the Class-E inverter.
v_{sn}	The voltage across the nth transistor of the Class-E push-pull inverter.
V_{cc}	The input DC voltage of the Class-E inverter.
v_c	The voltage across the capacitor (C) of the Class-E inverter.
v_o	The output voltage of the Class-E inverter.
$V_{o,rms}$	The rms output voltage of the Class-E inverter.
V_n	The rms voltage of the nth harmonic.
i_s	The switch current of the Class-E inverter.

i_L	The load/output current of the Class-E inverter.
I_m	The amplitude of i_L.
i_{Ls}	The input current of the inverter leaving V_{cc}.
$V_{s1s}, V_{s2s}, V_{s1c}, V_{s2c}, V_{co}$	The Fourier series coefficients of v_s.
$V_{c1s}, V_{c2s}, V_{c1c}, V_{c2c}, V_{co}$	The Fourier series coefficients of v_c.
$I_{L1s}, I_{L2s}, I_{L1c}, I_{L2c}$	The Fourier series coefficients of i_L.
$L_s, L_x, L_r, L_L, L, L1, L2, L3,$	The inductors of the Class-E inverter, Class-E push-pull inverter and the matching network.
$C, C1, C2, C_{off1}, C_{off2}, C_s, C_L$	The capacitors of the Class-E inverter, Class-E push-pull inverter and the matching network.
X_1, X_2, X_3, X_L, X_c	The reactance of the Class-E inverter, Class-E push-pull inverter and the matching network.
B_1, B_2	The susceptance of the matching network.
R_L	The load resistance of the Class-E inverter.
p	The loading factor of the load-independent Class-E and Class-E push-pull inverter. This is a ratio of I_m and V_{cc}.
P	The total average power consumed by the load.
Q	The total reactive power generated or consumed by a component. OR The quality factor of a component or network.
S	The total complex power generated or consumed by a component where $S = P + jQ$.
P_{in}, P_{out}	The input and output power of the Class-E and Class-E push-pull inverter.

P_{switch}	The transistor/switch power loss in the Class-E inverter.
η	The efficiency of the inverter measured as a percentage. Typically calculated as P_{out}/P_{in}.
PF, $PF_{desired}$	The power factor and the desired power factor of a supply or load.
Q_{comp}	The reactive power to be supplied or absorbed by an external component to maintain a set PF.
θ_v, θ_i	The angle of the voltage and current phasors respectively.
Z_L	The equivalent load impedance seen by the matching network. Typically equal to the resonator impedance for wireless power applications.
Z_1	The equivalent impedance of the matching networks looking towards the load from $L2$.
Z_{in}	The input impedance of the matching network and the load impedance of the inverter when configured with a matching network.
VNA	Vector Network Analyzer
DC, AC	Direct Current and Alternating Current
WBG	Wide-bandgap
THD	Total Harmonic Distortion
WPT	Wireless Power Transfer
IPT	Inductive Power Transfer
RC^2	Resonant Capacitive Coupling
ZVS, ZCS	Zero Voltage Switching and Zero Current Switching
VIM	Variable Impedance Matching
MEMS	Micro-Electromechanical System

CHAPTER 1 - INTRODUCTION

High-frequency power transmission is a popular field of research that can benefit several applications. Wireless power transfer (WPT), an emerging area of power electronics and electromagnetics, is one of these applications that seeks to transmit electrical energy from a source to an electrical load without the use of cables. The critical component present in these applications are the power converters. To maintain a high system efficiency, the selected power converters must be able to handle the high frequency, power level and loading condition of the system.

A power inverter is a type of converter that takes in direct current (DC) and outputs alternating current (AC). The converter consists of one or more switching elements that are toggled at the desired frequency to achieve the signal conversion. Silicon MOSFETs are often used in these converters. However, increasing the frequency to the mega hertz (MHz) range can lead to very large switching losses, forcing researchers to look for alternatives. With the recent advances in wide-bandgap (WBG) devices such as Gallium Nitride (GaN), switching in the MHz range is becoming increasingly popular.

Among the multiple topologies available for power inverters, Class-E inverters are widely used since they consist of only one switching element and resonant elements. This leads to a simpler circuit design while achieving a high theoretical efficiency, which is desirable for a portable WPT system. Due to the performance and popularity of the Class-E inverter, there is a strong desire to develop models and analyses techniques to further identify the limitation of its current design and explore potential improvements. Several papers have investigated this topic and have modelled the inverter through different means [1] - [2]. For example, [1] has shown the modification of a Class-E design for load-independent operation. This enables the inverter to run in its nominal state under

a variable load. However, a purely resistive load is assumed, which is a very rare condition in a dynamically changing system such as WPT. There are no alternative topologies available at this moment that accommodate reactive loads while achieving efficiencies on par with the Class-E inverter.

1.1 Research Objective

The main purpose of this research is to provide a study of the Class-E inverter and identify its performance under a non-resistive load. The main challenges involved with designing Class-E inverters are maintaining the soft switching and reducing the distortion of the load voltage. It is important that the voltage and current on the switch be minimized under loading to reduce overvoltage and thermal stress. For WPT, any resonator displacement will affect the impedance of the load seen by the inverter. This can lead to hard switching and increase the losses in the system. In addition, while the Total Harmonic Distortion (THD) is low for Class-E inverters [3], the second harmonic component is high and distorted waveforms could still be observed during these loading conditions. Having a highly reliable inverter will increase the overall flexibility of the system.

To understand and mitigate this problem, the performance of the Class-E and Class-E push-pull inverter is investigated for inductive and capacitive loadings at multi-MHz frequencies (13.56 MHz and 27.12 MHz). These studies are also presented at several power levels. Different existing solutions such as power factor correction and matching networks are analyzed to correct the loading seen by the inverter. After applying these techniques, the expectation is that the inverter will operate with minimal switching loss while exhibiting high efficiency and low THD.

1.2 Thesis Organization

The upcoming chapters of the thesis are arranged as follows:

Chapter 2 provides the literature review for this work. Background information on wireless power transfer as well as the different inverter topologies used for high frequency applications are presented.

Chapter 3 shows the performance of the Class-E and Class-E push-pull inverter under a resistive load. The dominant harmonics of the inverter are investigated using a harmonic approximation technique. Comparisons between the standard and load-independent designs are also provided through a simulation study. The results from this chapter are used as a reference for later chapters.

Chapter 4 investigates the performance of the Class-E inverter under non-resistive loads. A simulation study is provided in which the loading seen by the inverter is replaced with a resistance and a series/parallel reactance. The power factor correction method is proposed to improve the non-ideal characteristics of the inverter observed during the simulation study.

Chapter 5 shows a study of the impedance matching technique to improve the non-ideal characteristics of the inverter presented in Chapter 4. The Class-E push-pull inverter with a variable impedance matching network is explored to support a variable non-resistive load. The studies are completed for a capacitively-coupled wireless power system when the resonators are displaced. The inverter is built on a test board and the simulation results are validated. The range of impedance that can be accommodated by each matching network is also discussed.

Chapter 6 concludes the thesis and discusses more ideas for future research topics.

CHAPTER 2 - LITERATURE REVIEW

Wireless power transfer (WPT) is an area of power electronics that seeks to transfer electrical energy without the use of cables. Power is transmitted over a relatively small to medium length distance separated by a medium such as air or glass. There is ongoing research to further increase this distance for more efficient and long-range wireless power transmission [4]. Within WPT, there are different techniques, each bringing its own advantages and disadvantages. Two of the more popular types are the resonant inductive power transfer (IPT) and resonant capacitive coupling (RC^2).

Resonant IPT gives the benefit of being less sensitive to the outer environment and resonator misalignment while operating at a lower frequency. Sources [5] - [6] show some examples and the designs for the IPT method. Despite being bulky, the flexibility to operate at different environments and the ease of working at lower frequencies make this the more popular choice of the two methods. However, since inductive systems operate using magnetic field coupling, any surrounding metal objects for example could lead to eddy current losses [7].

Capacitive coupling is based on the capacitive interaction between the transmitter and receiver electrodes. This is dependent on the dimensions of the resonator plates and the distance between the wireless link. Capacitive reactance is inversely proportional to the operating frequency, making it very difficult to transmit power at low frequencies [8] - [9]. Furthermore, due to the sensitivity of the system, lateral misalignment that can lead to impedance imbalance is a major concern.

While both methods have their pros and cons, the immediate benefits of a capacitive system are the much higher operating frequency in the multi-megahertz range, significantly lowering the size of the system, and the ability to accommodate nearby metals. Operating at a much higher frequency

will also introduce its own drawbacks, such as the increased cost of switching devices and the necessity to deal with parasitic impedance of the Printed Circuit Board (PCB). However, operating the system within an acceptable frequency to reduce this effect while also building a small portable WPT system is one of the key benefits of the capacitively-coupled system.

2.1 Typical Capacitive Wireless Power Transfer System

A typical capacitive WPT system is shown in Figure 2-1 [10]. The transmitter houses components and devices that generate the AC signal using an optional DC-DC converter and a DC-AC inverter. The AC waveform is then transferred through the wireless link (or resonators) and processed on the receiver end. The overall power level of the system is determined by the loading seen at the output, as well as the position of the two resonators which considerably changes the loading seen by the inverter. Since the efficiency of the wireless link is expected to change due to the sensitivity and displacements of the resonators, the transmitter efficiency is required to be high regardless of their position to maintain stability and reduce power loss.

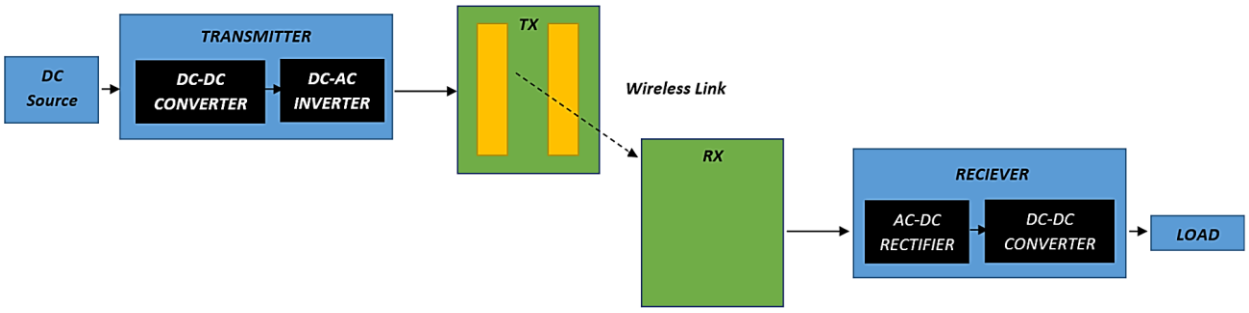


Figure 2-1: Block diagram for a typical capacitive wireless power transfer system

2.2 Resonator Topology

Resonators act as the wireless link for the system and come in different forms. A typical configuration of a resonator consists of two coplanar electrodes and passive tuning elements to resonate the system at the operating frequency. RC^2 for example contains a wide variety of electrode configurations. The most fundamental one is the rectangular design, where each electrode contains a self-capacitance and mutual capacitance to each of the electrodes. The dimensions of rectangular resonators consist of a length (l), width (W), and a gap (G) between the two electrodes and are aligned parallel to each other with a Distance (D) between each pair of electrodes. This is shown in Figure 2-2.

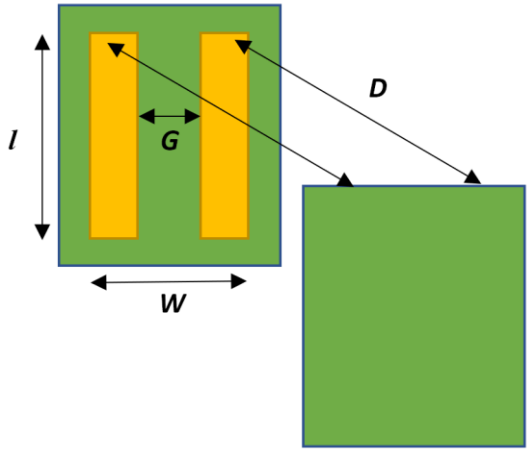


Figure 2-2: Rectangular resonators for RC^2 WPT

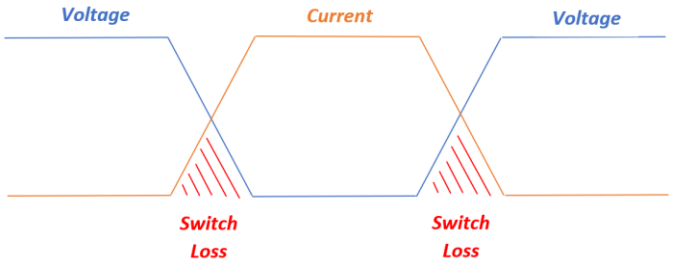
The tuning of the resonator is directly related to the value of the capacitance (C) seen at the input of the plates [9]. The required inductance (L) to tune the resonator at the operating frequency (f) is then found using (2.1).

$$L = \frac{1}{(2\pi f)^2 C} \tag{2.1}$$

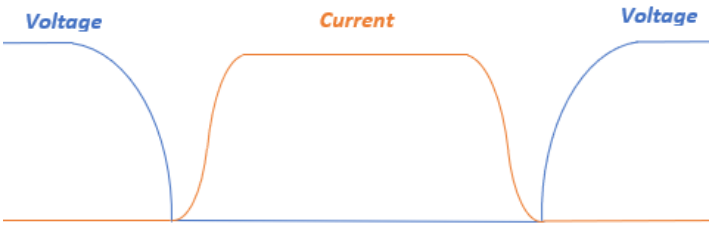
As mentioned, the presence of a foreign object will interfere with the tuning of the system. A metal shield is typically attached to reduce the environmental sensitivity and inductor requirements at the cost of coupling. Instruments such as a Vector Network Analyzer (VNA) are typically used to tune each resonator at the operating frequency.

2.3 Soft Switching versus Hard Switching

Two types of switching can be observed when operating a power converter: soft switching and hard switching. Hard switching is a case where the switch is on when desired and no control is applied to ensure smooth voltage and current transitions. As seen in Figure 2-3 (a), this often causes an overlap between the voltage and current curves, resulting in additional energy loss. Due to this, soft switching is preferred where this overlap is reduced using techniques such as Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) [11].



(a)



(b)

Figure 2-3: (a) Hard switching (b) Soft switching

ZVS is a switching method where the device is turned on after the voltage across it reaches zero. Similarly, ZCS is when the current flowing through the switch is brought to zero before turning it off.

Switching devices typically include parasitic capacitance that contribute to energy loss. For example, the energy stored in a capacitor is directly proportional to the voltage and is expressed as:

$$\text{Energy } = \frac{1}{2}\mathrm{C}v_s^2 \tag{2.2}$$

where C is the capacitance and v_s is the voltage across the switching device. Capacitors are incapable of discharging this energy instantly due to its nature and has a time delay. Due to this, ZVS is more widely used since it's more preferred to switch when the voltage is brought to zero.

2.4 Inverter

Transmitting power wirelessly through the resonators requires a high frequency sinusoidal signal. A DC-AC power converter or inverter is responsible for providing this signal with minimal distortion. For the RC^2 technology, a high operating frequency is preferred to reduce component costs and sizes. There are several types of power inverters with high operating frequencies such as classes A, B, AB, C, D, and E. Among these, the resonant Class D or E is preferred due to their high conversion efficiencies and soft switching performance [1] , [12] - [13]. As mentioned above, for WPT, the efficiency of the system varies with changes in spacing and misalignment of the resonators. This causes a load variation on the output of the inverter, which greatly impacts the overall converter efficiency. This is further explored in later chapters. A highly efficient transmitter employing a Class D or E inverter with load independence is preferred to maintain the stability of the system.

2.4.1 The Standard Class-D Inverter

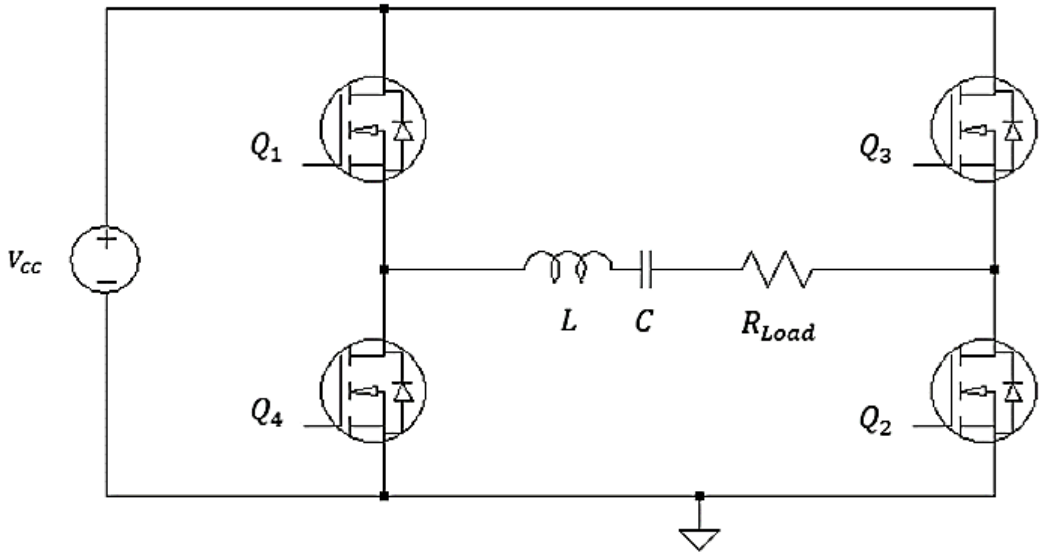


Figure 2-4: Full bridge Class-D inverter

A full-bridge Class-D inverter topology shown in Figure 2-4 consists of four switching devices connected to a load. Switch pairs $Q_1 - Q_2$ and $Q_3 - Q_4$ are toggled to output a square AC waveform. A series resonant LC network tuned to the fundamental frequency using (2.1) is inserted on the load side to eliminate the unwanted harmonics. Adding this modification significantly improves the overall efficiency of the inverter and outputs a sinusoidal waveform. The inverter also consists of a half bridge model that achieves similar results utilizing only two switches [14].

While being an extremely popular topology for high frequency power conversion, there are some noteworthy drawbacks. Driving the high side of the switch for example is challenging, making the control circuit of the inverter complex. Furthermore, the inverter is prone to high switch losses. A modified Class-D ZVS topology is required to control the switch loss of the inverter while maintaining the favourable features of the standard Class-D [12].

2.4.2 The Standard Class-E Inverter

The topology of the Class-E inverter is shown in Figure 2-5. Unlike the Class-D or its half bridge version, the Class-E inverter consists of only one switching device. The input DC voltage V_{cc} is converted to an AC signal v_0 across R_L by toggling this switch at a specified switching frequency. When the switch is on, current flows into the switch from the load, and when the switch is off, the shunt capacitor C_s drives the current to the load, developing a voltage across it. The inductor L_s controls the AC losses in the input while the residual inductance L_X controls the phase shift between the voltage and current in the switch node to minimize losses. To simplify, the summation of L and L_X is referred to as L_r. Like the Class-D topology, a resonant LC network tuned to the fundamental frequency is added to control the harmonics at the load.

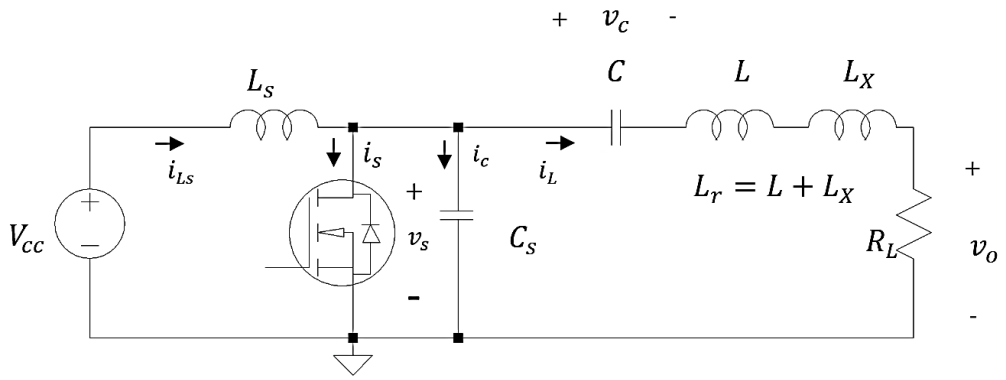


Figure 2-5: The Class-E inverter

The Class-D and Class-E inverter can utilize the parasitic capacitance of the switching device to achieve ZVS. However, ZVS is more easily achieved with the Class-E inverter if tuned adequately with the components that are already present in the circuit. Due to this, the Class-E inverter topology is heavily used for high frequency power transmission requiring very high efficiency and minimal component count. However, the main drawback is that the switch voltage is very large

and can reach up to 4 times the input voltage, as shown in Figure 2-6 [15]. Load-independence is also not built in with the Class-E topology and will require the designer to deviate from the original design principles.

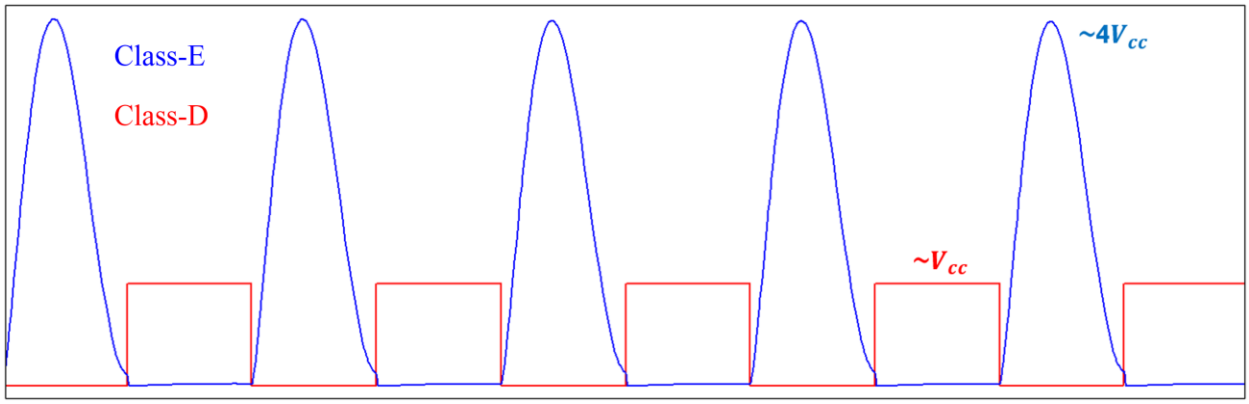


Figure 2-6: Class-E vs Class-D inverter switch voltage

The inverter must be designed to avoid the overvoltage and thermal stress of the switching device. For large power and voltage levels, the switching device must be selected such that it can withstand these effects. Alternatively, the design of the inverter can be modified to reduce these effects through external networks [16] or optimize the design through careful selection of components [17].

CHAPTER 3 - THE HARMONICS OF THE CLASS-E INVERTER

This chapter presents an analysis of the conventional or standard Class-E inverter under resistive loading and shows the dominant harmonics present in the switch node and output waveforms. The content of this Chapter is a modified version of the paper that was initially presented at the 2020 IEEE Newfoundland Electrical and Computer Engineering conference [3], and has been reproduced with permission from the authors.

3.1 Basic Concepts of the Standard Class-E Inverter

In this section, the standard Class-E inverter equations are derived and studied. Each equation is approximated to its harmonic content using Fourier analysis. The motivation for this approach is to demonstrate that the Class-E inverter is dependent on other harmonics in addition to the fundamental.

3.1.1 Design Equations for the Standard Class-E Inverter

The circuit for the single ended Class-E inverter shown in Figure 2-5 is repeated in Figure 3-1 for easy reference. As mentioned, the Class-E inverter consists of one switching device, an input inductor L_s, a DC source V_{cc}, a capacitor C_s in parallel with the switch, a series LC filter, a residual inductance L_X, and a load R_L. Assuming a 50% duty cycle, the following design equations can be used to calculate the components for a Class-E inverter [18].

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{3.1}$$

$$R_L = 0.5768\frac{V_{cc}^2}{P_{out}} \tag{3.2}$$

$$C_s = \frac{0.0292}{fR_L} \tag{3.3}$$

$$L_X = \frac{1.1525R_L}{2\pi f} \tag{3.4}$$

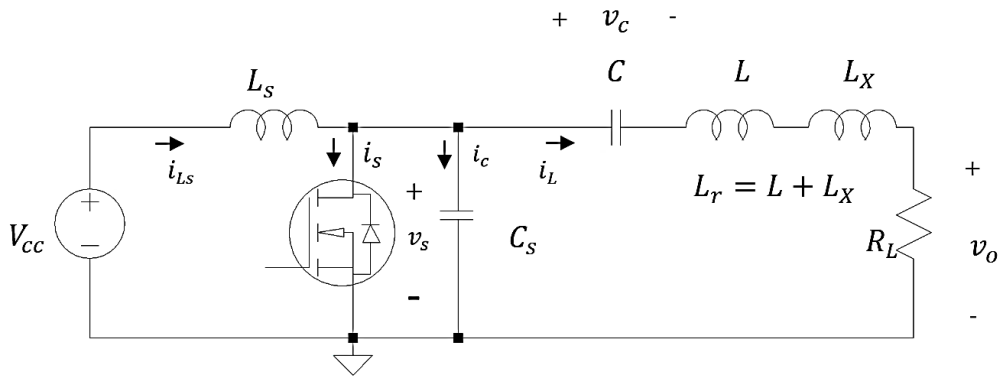


Figure 3-1: The Class-E inverter

3.1.2 Harmonic Approximation of the Class-E Inverter

To study the dominant harmonics of the Class-E inverter, Kirchhoff's voltage law (KVL) is first applied to the circuit above. This analysis gives (3.5)-(3.8).

$$\frac{L_s di_{Ls}}{dt} + v_s = V_{cc} \tag{3.5}$$

$$\frac{C_s dv_s}{d_t} = s(t)(i_{Ls} - i_L) = s(t)i_c \tag{3.6}$$

$$\frac{L_r di_L}{dt} + v_c + R_L i_L = v_s \tag{3.7}$$

$$\frac{C dv_c}{dt} = i_L \tag{3.8}$$

where $s(t)$ represents the switch on/off behavior defined as

$$s(t) = \begin{cases} 0, & nT < t \leq nT + T_{on} \text{ (switch on state)} \\ 1, & nT + T_{on} < t \leq (n+1)T \text{ (switch off state)} \end{cases} \quad (3.9)$$

where n is an integer, T is the switching period and T_{on} is the on-time of the switch. To show the influence of the harmonics on the switch and load voltage waveforms, (3.7)-(3.8) are approximated using harmonic components.

First, the load current i_L is approximately a sinusoid and is modelled using only its fundamental and second harmonic component. In addition, the operation of the inverter produces a dc shift in the voltage v_c across the resonant capacitor. So, the capacitor voltage is approximated by an offset voltage V_{co}, the fundamental and second harmonic components. The approximated expressions for v_c and i_L are given in (3.10) and (3.11).

$$v_c = V_{co} + V_{c1s}\sin(\omega t) + V_{c1c}\cos(\omega t) + V_{c2s}\sin(2\omega t) + V_{c2c}\cos(2\omega t) \quad (3.10)$$

$$i_L = I_{L1s}\sin(\omega t) + I_{L1c}\cos(\omega t) + I_{L2s}\sin(2\omega t) + I_{L2c}\cos(2\omega t) \quad (3.11)$$

where V_{c0}, V_{c1s}, V_{c1c}, V_{c2s}, V_{c2c}, I_{L1s}, $I_{L1c}, I_{L2s}, I_{L2c}$ are the corresponding Fourier series coefficients. Subscript "0" is used for the dc term, subscript "1s" is used for the fundamental sine term, subscript "1c" is used for the fundamental cosine term and so on. The derivatives of (3.10) are obtained as:

$$\frac{dv_c}{dt} = V_{c1s}\omega\cos(\omega t) - V_{c1c}\omega\sin(\omega t) + 2V_{c2s}\omega\cos(2\omega t) - 2V_{c2c}\omega\sin(2\omega t) \quad (3.12)$$

$$\frac{d^2v_c}{dt^2} = -V_{c1s}\omega^2\sin(\omega t) - V_{c1c}\omega^2\cos(\omega t) - 4V_{c2s}\omega^2\sin(2\omega t) - 4V_{c2c}\omega^2\cos(2\omega t) \quad (3.13)$$

Substituting (3.12) and (3.13) into (3.7) and (3.8), and equating the dc, sine and cosine terms yields the harmonic components of the switch voltage, v_s:

$$V_{s1s} = V_{c1s} - R_L C V_{c1c}\omega - L_r C V_{c1s}\omega^2 \tag{3.14}$$

$$V_{s1c} = V_{c1c} + R_L C V_{c1s}\omega - L_r C V_{c1c}\omega^2 \tag{3.15}$$

$$V_{s2s} = V_{c2s} - 2R_L C V_{c2c}\omega - 4L_r C V_{c2s}\omega^2 \tag{3.16}$$

$$V_{s2c} = V_{c2c} + 2R_L C V_{c2s}\omega - 4L_r C V_{c2c}\omega^2 \tag{3.17}$$

$$V_{s0} = V_{c0} \tag{3.18}$$

For the switch voltage, only the dc, fundamental and second harmonic components are considered since it is known to be the largest. If desired, the predicted error can be reduced by using more harmonic components. For a ZVS Class-E inverter with the switch operating at 50% duty cycle, the ratio of the switch voltage (v_s) to the DC input voltage (V_{cc}) is given by [19]:

$$\frac{v_s}{V_{cc}} = \begin{cases} 0, & 0 < \omega t \leq \pi \\ \pi(\omega t - \frac{3\pi}{2} - \frac{\pi}{2}\cos(\omega t) - \sin(\omega t)), & \pi < \omega t \leq 2\pi \end{cases} \tag{3.19}$$

Expanding (3.19) and calculating the Fourier series coefficients yields the following harmonic components for v_s in the interval $\pi < \omega t \leq 2\pi$:

$$v_s = V_{cc} - 0.4675V_{cc}\cos(\omega t) - 1.571V_{cc}\sin(\omega t) - 0.6667V_{cc}\cos(2\omega t) + 0.5236V_{cc}\sin(2\omega t) + \cdots \tag{3.20}$$

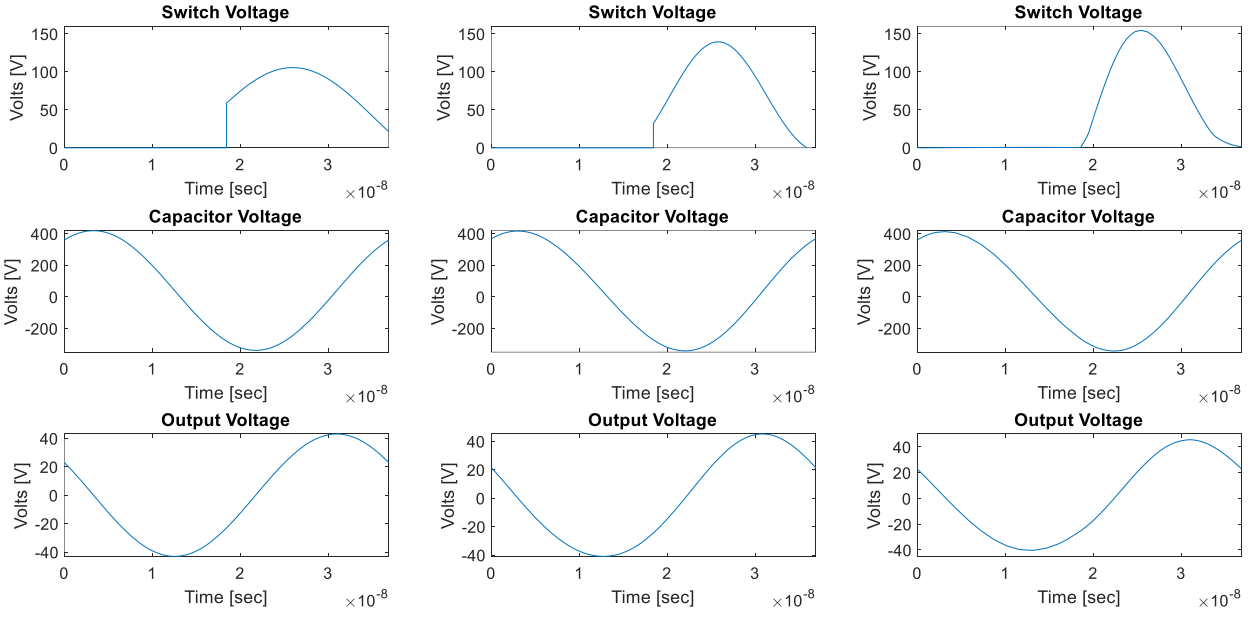
Now, $V_{s0}, V_{s1s}, V_{s1c}, V_{s2s}, V_{s2c}$ can directly be extrapolated from (3.20) using (3.14) to (3.18). The equations above were used to obtain the switch voltage v_s, capacitor voltage v_c, and the output voltage v_o, for the design components shown in Table 3-1. The parameters are chosen using (3.1) - (3.4) for a 100 W load Class-E inverter switching at 27.12 MHz.

Table 3-1: Circuit parameters for a 100 W, 27.12 MHz Class-E inverter with EPC2012 switch

Parameter	Value	Parameter	Value
R_L	9.23 Ω	C	72.2 pF

C_s	117 pF	L_s	1 uH
L_X	62.2 nH	V_{cc}	40 V
L	477 nH	f	27.12 MHz

The plots in Figure 3-2 were obtained in MATLAB using (3.14) - (3.18). The waveforms in Figure 3-2 (a) include the DC and fundamental terms, while those of Figure 3-2 (b) include the second harmonic component. Figure 3-2 (c) shows the actual waveform with all harmonics included. Due to the high quality-factor of the resonant filter, it is observed that the load current and hence the load voltage for the Class-E inverter is approximately a sinusoid. However, comparing Figure 3-2 (a) and (b), a small difference is noticed for the load voltage, and the second harmonic is not completely negligible.



(a) *(b)* *(c)*

Figure 3-2: Class-E switch, capacitor and output voltage using harmonic approximation: (a) DC + Fundamental; (b) DC + Fundamental + 2nd Harmonic (c) Actual waveforms

The importance of the second harmonic component in the Class-E design is clearly observed in the switch voltage. Approximately a 50 V difference is seen when comparing the switch voltage from Figure 3-2 (a) and (b). While the DC and fundamental components are expected to be present for typical systems, this analysis shows that for a Class-E inverter, the second harmonic component is also dominant. The hard switching seen on the switch voltage is the error introduced through the approximations and can be further reduced by adding more harmonic components, as shown in Figure 3-2 (c).

To further analyze and validate the results above, the waveforms are compared with LTSpice simulations. The circuit parameters given in Table 3-1 are used to simulate the inverter. Due to the low shunt capacitance C_s, the EPC2012 switch was selected. Ideal components are also considered in the simulations. The inductors contain a series resistance of $1\text{m}\Omega$ by default in LTSpice. Once simulated, the system provided an output power of 97.7W with an overall efficiency (η) of

$$\eta = \frac{P_{out}}{P_{in}} = \frac{97.7W}{102.35W} = 95.4\%$$

Figure 3-3 shows the obtained voltage waveforms for the switch v_s and the load v_o from LTSpice. It is observed that the output waveform closely matches the waveform obtained from the harmonic approximation procedure from Figure 3-2 (R_L = 9.23 Ω). The peak switch voltage from the simulations was slightly higher due to the strong third harmonic, which was neglected in the analytical model in Figure 3-2 (b). In addition, ZVS is maintained for this loading configuration. Furthermore, the overall THD of the output voltage was 7.37%, which is determined using (3.21)

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 \ldots}}{V_1} \tag{3.21}$$

where V_n is the rms voltage of the nth harmonic.

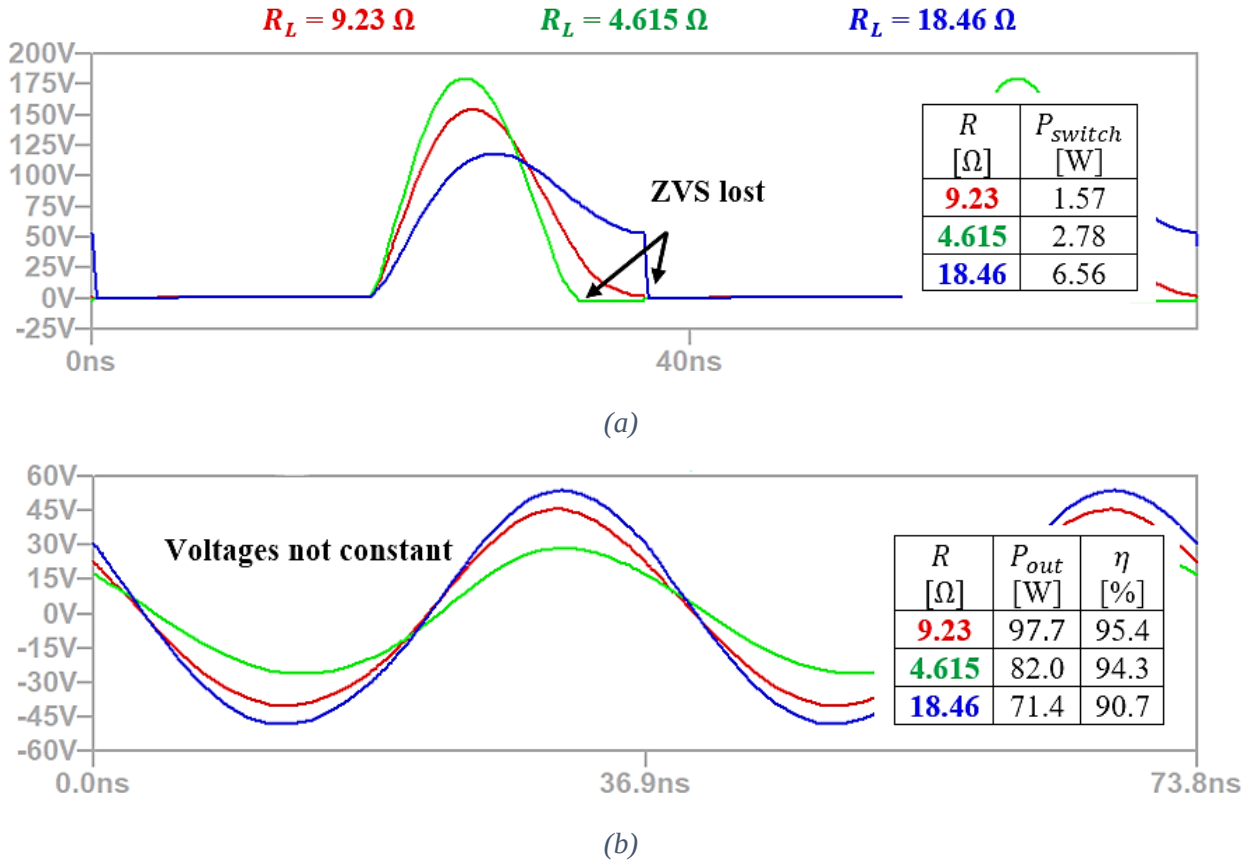


Figure 3-3: (a) Switch voltage (b) Output voltage for the standard Class-E when the load is varied

However, once the load is varied from its nominal value of 9.23 Ω, ZVS is lost, and the output voltage is no longer constant. Due to the hard switching, the converter switch loss and efficiency are also impacted. Having a constant regulated output voltage and ZVS in the switch node under load variation is beneficial and is explored in the next section.

3.2 The Load-Independent Class-E Inverter

Ensuring relatively constant output voltage and ZVS over a load variation requires a load-independent Class-E inverter. An example of this has been proposed by S. Aldhaher et. al. [1]. Furthermore, it is shown (see Figure 3-3) that switch loss and efficiency vary for the standard Class-E model when the load changes from its optimum value. The load-independent design procedure mitigates this issue for a *resistive* load.

The approach is based on defining a loading factor p which represents the ratio of the load current amplitude I_m to the input DC voltage V_{cc}. This factor increases as the load resistance decreases and vice versa. To obtain constant output voltage, the method proposed in [1] ensures the derivative of the ratio of the output voltage and the input voltage with respect to p is zero. Applying this condition results in a different set of design equations. Equations (3.22) - (3.26) are obtained for a 50% duty cycle and maximum loading. The circuit configuration of the load-independent Class-E is identical to Figure 3-1.

$$p = \frac{\omega L_s I_m}{V_{cc}} = 1.5 \tag{3.22}$$

$$I_m = \frac{2P_{out}}{1.5895V_{cc}} \tag{3.23}$$

$$q = \frac{1}{\omega\sqrt{L_s C_s}} = 1.2915 \tag{3.24}$$

$$R_L = \frac{(1.5895V_{cc})^2}{2P_{out}} \tag{3.25}$$

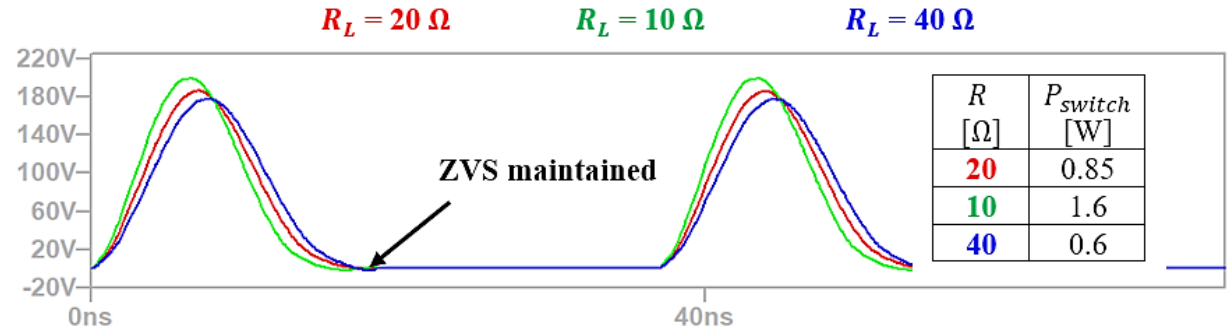
$$L_X = 0.2663L_s \tag{3.26}$$

Designing a 100 W load-independent Class-E inverter at 27.12 MHz using (3.22) - (3.26) gives the parameters in Table 3-2.

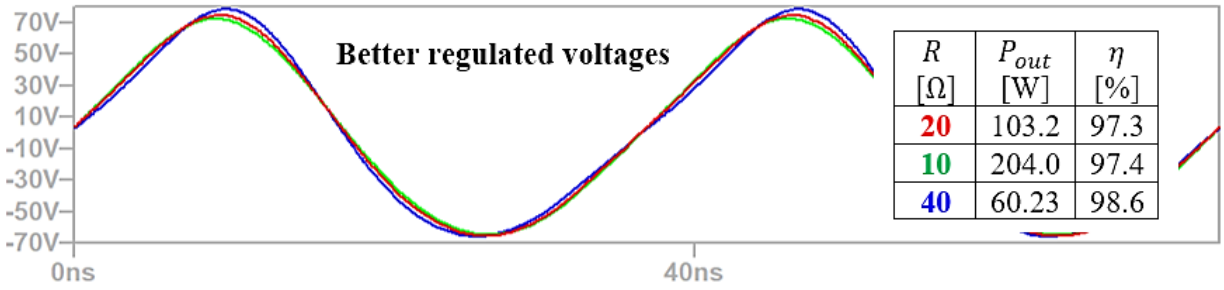
Table 3-2: Circuit parameters for the load-independent 100 W, 27.12 MHz Class-E inverter with EPC2019 switch

Parameters	**Value**	**Parameters**	**Value**
R_L	20 Ω	C	53.8 pF
C_s	184 pF	L_s	112 nH
L_X	30 nH	V_{cc}	40 V
L	640 nH	f	27.12 MHz

Comparing Table 3-1 and Table 3-2, the load-independent design requires a slightly larger shunt capacitor C_s and a significantly smaller input inductor L_s. As a result, the input current can no longer be assumed to be constant, due to the strong AC component. Thus, L_s now needs to be a high quality-factor RF inductor to reduce losses. To meet the 100 W requirement, the nominal load resistance is set to 20 Ω. The simulation was then conducted with the load resistance R_L varying from 0.5 to 2 times its nominal value. The obtained waveforms for the output and switch voltage for the load-independent circuit are shown in Figure 3-4.



(a)



(b)

Figure 3-4: (a) Switch voltage (b) Output voltage of the load-independent Class-E design

From Figure 3-4, it is observed that the load-independent design maintains ZVS within a loading range and the output voltage is better regulated. For the nominal resistance, the output power of 103.2W was obtained with an overall efficiency of 97.3%. However, like the standard Class-E inverter, this model also suffers from a large second harmonic component with a THD of 9% in

the output voltage for the nominal case. Furthermore, if a low quality-factor L_s is used, the load-independent design will also likely have reduced efficiency compared to the standard Class E, largely due to RF losses.

3.3 The Load-independent Class-E Push-Pull Inverter

The Class-E inverter family consists of alternate topologies, such as the Class-EF_2 and Class-E push-pull that improves upon its original design. The Class E push-pull inverter, shown in Figure 3-5, consists of two Class-E inverters with their transistors driven at opposite phases. The output circuit configuration contains both the resonant LC network and the load for each inverter connected in series. Alternatively, the load R_L can also be separated to obtain two single ended outputs but with large common-mode current at the second harmonic.

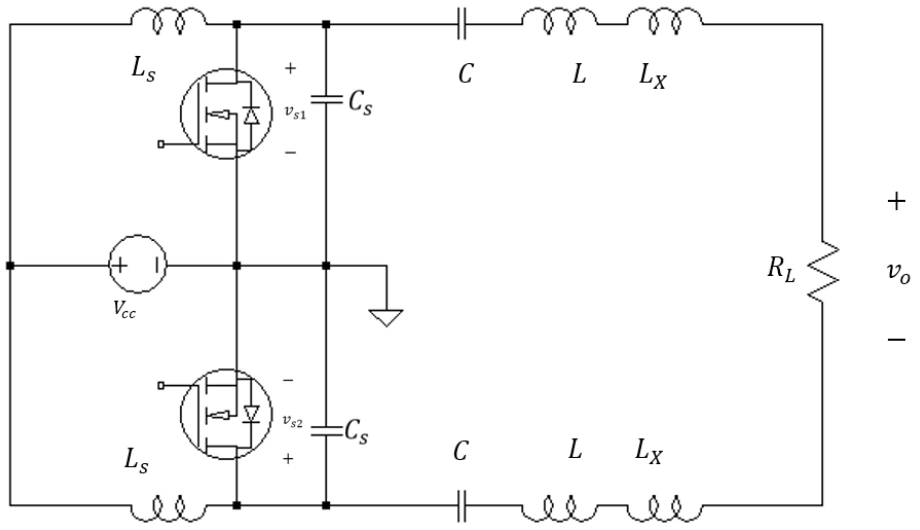
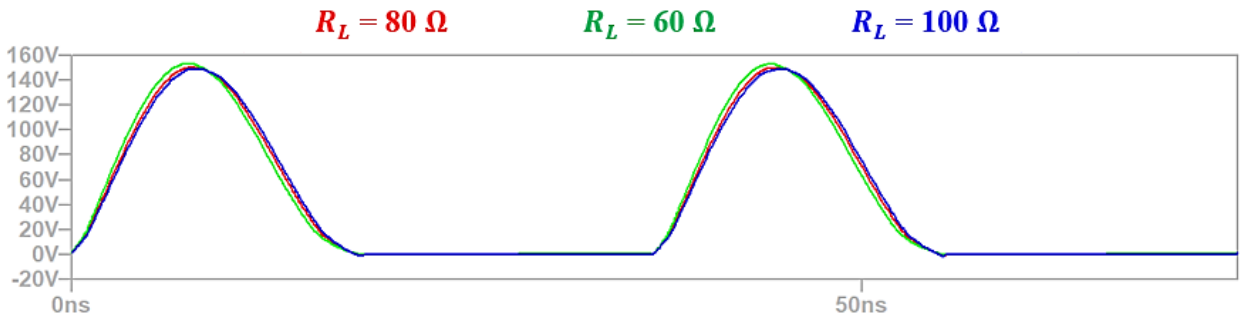


Figure 3-5: The Class-E push-pull inverter topology

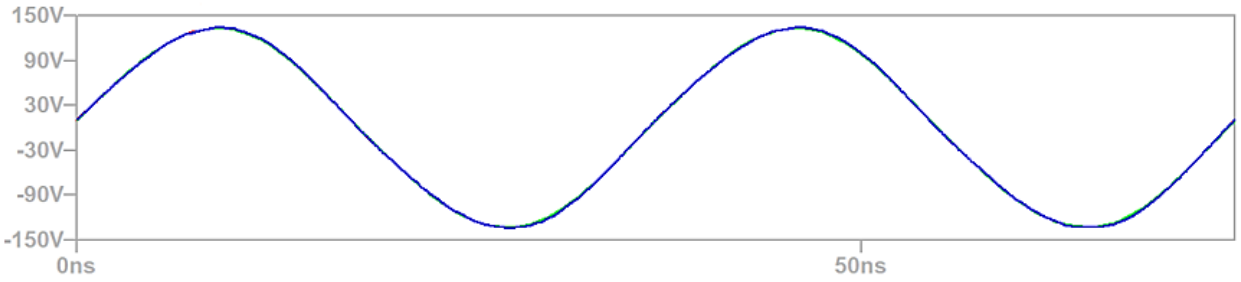
Due to the symmetrical design, a key benefit from the differential push-pull configuration is the ability to push double the power and the reduced THD of the output. Taking the previously simulated load-independent Class-E model from Table 3-2 and connecting it in the differential

push-pull configuration achieved a THD of approximatly 1.025%. From the earlier simulations, the load-independent Class-E inverter output had a THD of 9%. This is because the complementary push-pull operation significantly reduces the even harmonics present in the output signal.

After increasing the load resistance to 80 Ω to output approximately 100 W, the obtained output and switch voltage waveforms are shown in Figure 3-6. It is observed that the benefits of the load-independent design is still maintained in the form of constant output and ZVS in the switch voltage even after converting to the push-pull topology.



(a)



(b)

Figure 3-6: a) Switch voltage for the load-independent Class-E push-pull inverter b) Output voltage for the load-independent Class-E push-pull inverter

At the cost of increased component count, operating the inverter in the push-pull configuration will enable the user to have the benefit of outputting higher power levels with reduced distortion

in the waveforms. However, the large switch voltage in the Class-E inverter is still present and can only be reduced with techniques such as the Class-EF_2 design [1].

3.4 Summary

In this chapter, the Class-E inverter was modelled using harmonic approximation. Designs of a load-dependent and load-independent Class-E inverter was simulated for ideal resistive loads. It was observed that the load-independent model of the Class-E inverter provided a well-regulated output voltage and maintained ZVS under load variations. However, this inverter was seen to suffer from a large second harmonic component and high switch voltage. The Class-E push-pull configuration consisting of two load-independent Class-E inverters connected in differential mode was then introduced. The push-pull topology gave the ability to transmit more power and reduce the second harmonic component at the output due to its differential configuration. This inverter also maintained the benefits of the load-independent design. These are clear improvements when compared to the regular Class-E topology and make the push-pull inverter a great alternative.

CHAPTER 4 - PERFORMANCE OF THE CLASS-E INVERTER UNDER NON-RESISTIVE LOADS

In the previous chapter, the performance of the Class-E and Class-E push-pull inverter were explored for resistive loads. When the inverter sees a non-resistive load, the ideal operation of the inverter for both the Class-E and push-pull is expected to be disrupted. If a non-resistive component is part of the load, the nominal behaviours of the load-independent inverter such as ZVS and constant output with minimal THD will change. This chapter provides a study of the Class-E inverter under non-resistive loads and shows the effects of this change on the switch and output waveforms through simulation studies in the LTSpice platform.

4.1 Class-E Inverter under a Reactive Load

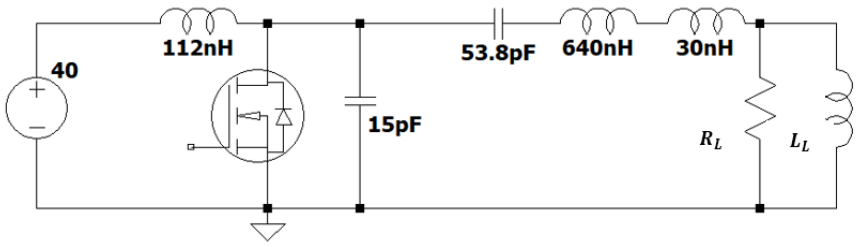
Typical load structures seen by the inverter for applications such as WPT contain an inductive or capacitive portion due to the tuning or misalignment of the resonators. The designed inverter needs to be able to handle this non-ideal loading to maintain system stability and high efficiency. In this section, the inverter performance is first analyzed when the load is directly replaced by a resistive and an inductive component in series and parallel configurations. Since the design equations from Chapter 3 are formulated around a purely resistive load R_L, some issues in performance are expected. One possible solution would be to design the inverter around the inductive component present in the load network using the design equations. However, it is an unrealistic expectation to change the inverter design when the load changes in real time in an operational environment. This is further explored in the next chapter. For now, it is important to study the inverter separately

without directly affecting its design and explore methods to counter the non-ideal effects when under non-resistive loads.

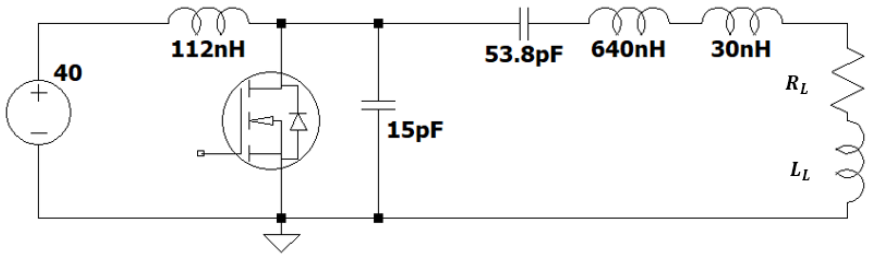
In the previous chapter, (3.14) - (3.18) showed the fundamental and second harmonic coefficients of the switch voltage waveform with respect to the load side components of the inverter. Adding a non-resistive element such as an inductance to the load side can be seen as increasing L_r. From those equations, it can be noted that all Fourier coefficients with the exception of the DC term will be affected when this change is made. Since the DC shift is constant while the frequency components change, the half sinusoidal waveform of the switch node will not reach *zero volts* when the transistor is switched on. The design example below shows this phenomenon in detail.

4.1.1 100 W Load-Independent Class-E Inverter with Inductive Load

For this analysis, the 100 W 27.12 MHz load-independent Class-E inverter from Chapter 3 is considered. A parallel and series load inductance L_L is now added and varied in the load network. The resulting circuit is shown in Figure 4-1.



(a)



(b)

Figure 4-1: 100 W 27.12 MHz Class-E inverters with (a) parallel (b) series load inductance

The 100 W system without the load inductance and with $R_L = 20\ \Omega$ from Chapter 3 gave the performance numbers shown in Table 4-1.

Table 4-1: 100 W 27.12 MHz load-independent Class-E inverter results when $R_L = 20\ \Omega$

Input Power [W]	Output Power [W]	Efficiency [%]	Switch Loss [W]
106.02	103.20	97.34	0.85

The information in this table will be used as a reference in the upcoming studies. First, the parallel load inductance case from Figure 4-1 (a) is considered. After varying this inductance, the following results in Table 4-2 are obtained.

Table 4-2: 100 W 27.12 MHz load-independent Class-E inverter with parallel L_L load when $R_L = 20\ \Omega$

Inductance L_L [nH]	RMS Output Current i_L [A]	RMS Output Voltage [V]	Input Power [W]	Output Power [W]	Efficiency [%]	Output THD [%]
1	11.8	2.02	30.31	0.178	0.6	7.18
10	7.13	47.92	48.40	6.44	1.33	9.25
100	2.88	39.6	72.05	68.29	94.8	12.24
500	2.11	46.87	97.67	95.50	97.7	10.78
1000	2.09	47.72	101.05	99.03	98.0	10.29

As the inductance is increased, the inverter performs at its nominal operation. This is because the parallel impedance of the inductor is very large, and it behaves as an open circuit at the switching frequency of 27.12 MHz. Furthermore, significant power loss is noticed for the 1 nH and 10 nH case. The switching component will not survive with this loading.

Similarly, applying the inductance in series to the load resistance, as shown in Figure 4-1 (b), gives the results in Table 4-3. The behavior is opposite to that of Figure 4-1 (a) as expected. The lower reactance of the inductor has very little effect on the inverter while larger reactance approaches an open circuit on the load side.

Table 4-3: 100 W 27.12 MHz load-independent Class-E inverter with series L_L when $R_L = 20\ \Omega$

Inductance L_L [nH]	**RMS Output Current i_L [A]**	**RMS Output Voltage [V]**	**Input Power [W]**	**Output Power [W]**	**Efficiency [%]**	**Output THD [%]**
1	2.06	48.18	103.18	100.9	97.8	9.58
10	2.07	47.92	101.59	99.22	97.6	9.95
100	1.59	46.03	60.58	58.39	96.4	17.95
500	0.544	50.59	7.84	6.82	86.9	39.18
1000	0.29	52.84	2.59	1.872	72.3	47.75

Similar to the previous case, the input power is greatly affected for certain cases when an inductance L_L is connected to the load. This is because the load-independent design will try to regulate the voltage at a constant RMS ($V_{o,rms}$) value, but the impedance of the load network (Z) will contribute to a change in power level (P). This is shown by the complex power (S) equation in (4.1).

$$Re\{S\} = \mathrm{Re}\left\{\frac{\left|V_{o,rms}\right|^2}{Z^*}\right\} = P \tag{4.1}$$

This effect is seen in Table 4-3 for cases including and above 100 nH, where the impedance becomes significantly large and severely reduces the power level of the system.

Due to the change in the filter response on the load side, the output voltage waveform of the inverter for the series case is also seen to be distorted. To show this, first the transfer function of the load network is derived in (4.2).

$$\frac{v_o}{v_s} = \frac{\sqrt{R_L^2 + \omega^2 L_L^2}}{\sqrt{R_L^2 + \left(\omega L_L - \frac{1}{\omega C} + \omega L_r\right)^2}} \tag{4.2}$$

Figure 4-2 shows the resulting frequency response for this network when the load inductance is varied. It can be observed that the peak of the response is shifted from the fundamental frequency as the inductance is increased, resulting in less attenuation at larger harmonics. This results in more harmonics and increased THD at the output, as shown in Table 4-3.

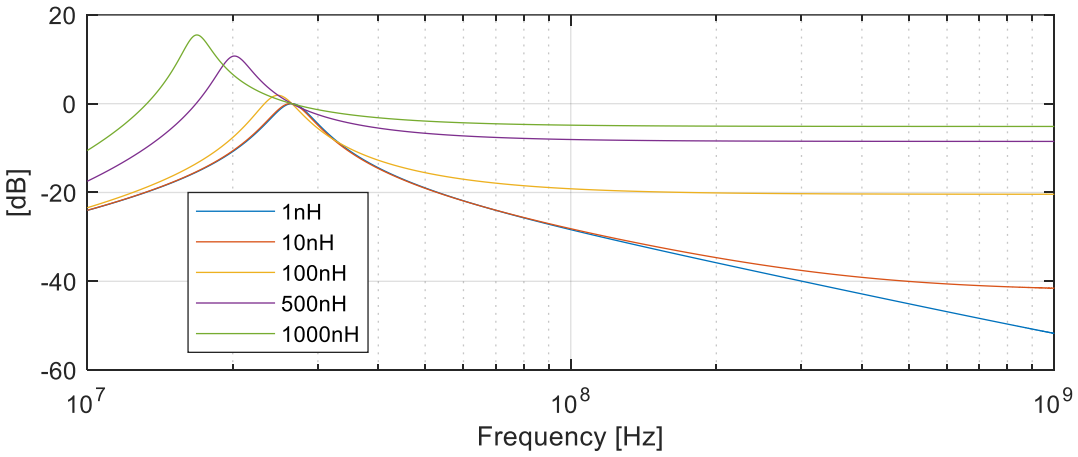


Figure 4-2: Frequency response of the load network at each inductance

Figure 4-3 shows the highly distorted output voltage waveform for the 500 nH case, which is far from its ideal sinusoidal shape. This waveform has a THD of 39%, significantly larger than the 9% obtained for the resistive case. Modifying the load series LC filter to accommodate the

additional inductance will improve this waveform, but it's not a practical solution when the load changes in real-time.

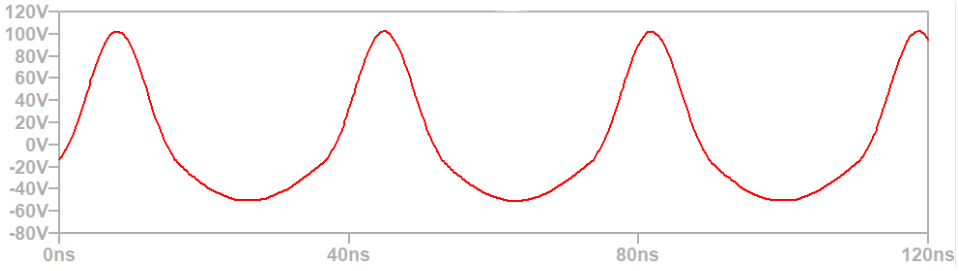


Figure 4-3: Distorted output voltage waveform for the 100 W Class-E inverter with 500 nH series load inductance

In addition, increasing the series load inductance L_L introduces switch losses identified as diode conduction. The switch voltage briefly appears negative before the on state, as shown in Figure 4-4. The increase in inductance also contributes to a higher peak voltage and more losses on the switch, applying additional stress to the device.

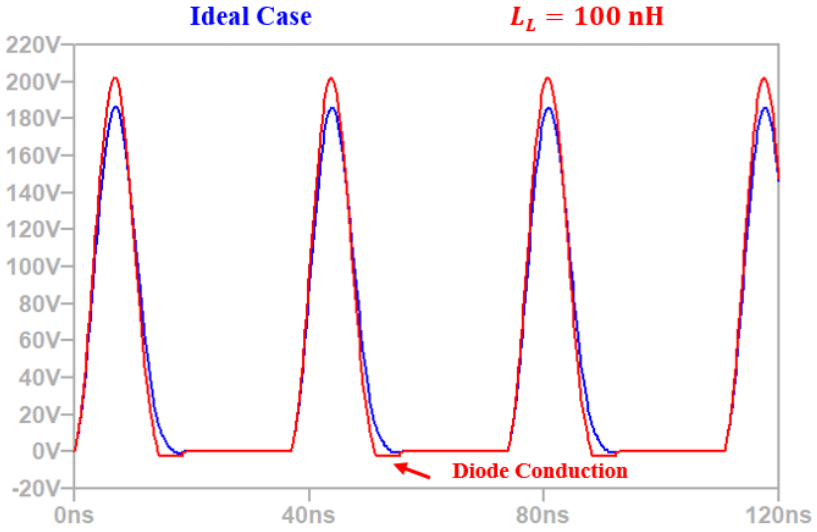


Figure 4-4: Diode conduction in the switch voltage for inductive loads

4.1.2 100 W Load-Independent Class-E Inverter with Capacitive Load

If the inductance L_L in Figure 4-1 (b) is replaced with a series 1nF capacitor, the switch voltage in Figure 4-5 is obtained. It is observed that the peak switch voltage decreases, and the capacitive load introduces hard switching.

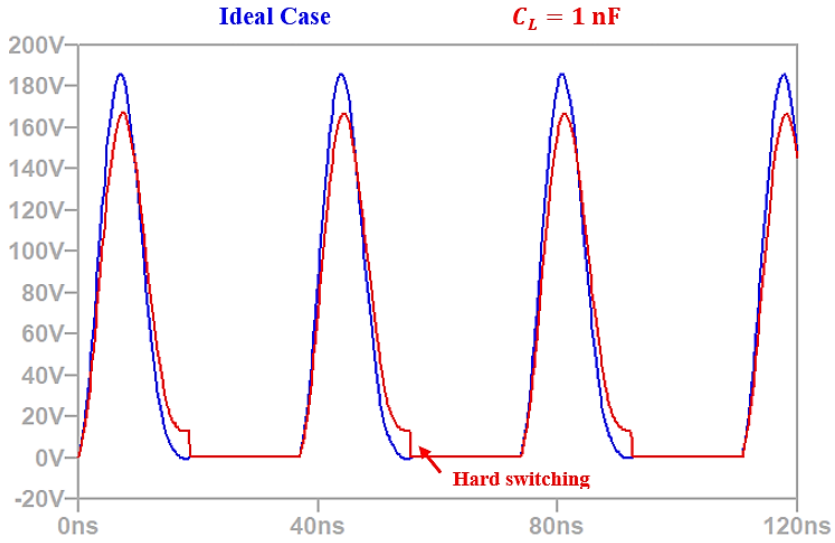


Figure 4-5: Hard switching in the switch voltage for capacitive loads

The frequency response also drastically changes when the capacitor value is lowered. This is shown in Figure 4-6. Unlike the previous case, the frequency response severely attenuates the fundamental component, altering the amplitude of the output waveform. Hence, depending on the type of loading, a non-resistive load can severely alter the THD of the output due to the change in the frequency response and introduce switching losses in the inverter. These types of loading are worst-case scenarios that need to be addressed to prevent switch failure.

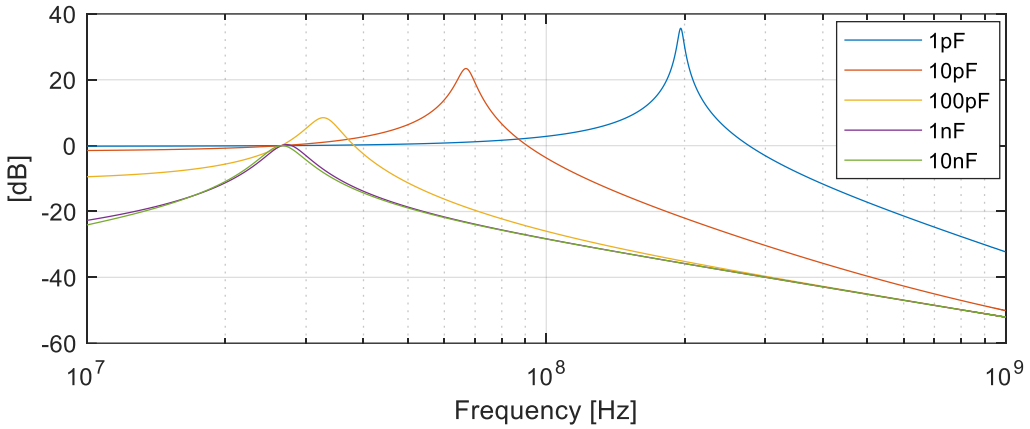


Figure 4-6: Frequency response of the load network at each capacitance

4.2 Shunt Resonant Filter

In the previous section, it was shown how the non-resistive load leads to distorted output waveforms, switch losses and significant decrease in power level for a Class-E inverter. It is important to present a purely resistive load to the inverter to mitigate these effects and maintain an efficient operation. The possible solutions to counter some of these effects, based on the shunt resonant RLC circuit, are presented in this section.

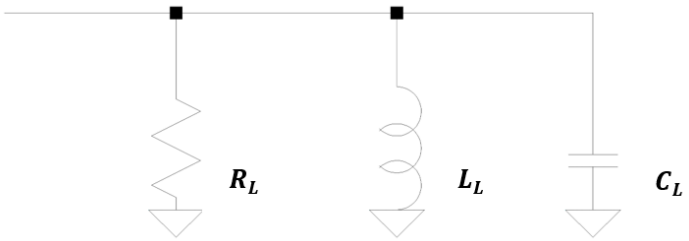


Figure 4-7: The shunt resonant RLC circuit

The topology for the shunt resonant *RLC* circuit is shown in Figure 4-7. Tuning this network for resonance at f_r using (4.3) will pass the fundamental component of the output signal to the load. For this case, the inductance L_L and capacitance C_L will act as an open circuit. With a high quality-

factor, the benefit of this network is that the fundamental component of the signal on the load side is not affected, while higher order harmonics are significantly reduced.

$$f_r = \frac{1}{2\pi\sqrt{L_L C_L}} \tag{4.3}$$

The quality-factor (Q) and bandwidth (BW) of a *RLC* parallel resonant filter are determined using (4.4) and (4.5):

$$Q = 2\pi f_r C_L R_L \tag{4.4}$$

$$BW = \frac{f_r}{Q} \tag{4.5}$$

The impedance response of this network is shown in Figure 4-8. From (4.4) and (4.5), a significant decrease in load resistance will show an increase in the bandwidth of the filter. Increasing the quality factor reduces this bandwidth, attenuating the higher and lower order harmonics. It is recommended to keep C_L as high as possible to avoid losing the quality of this filter under a variable load.

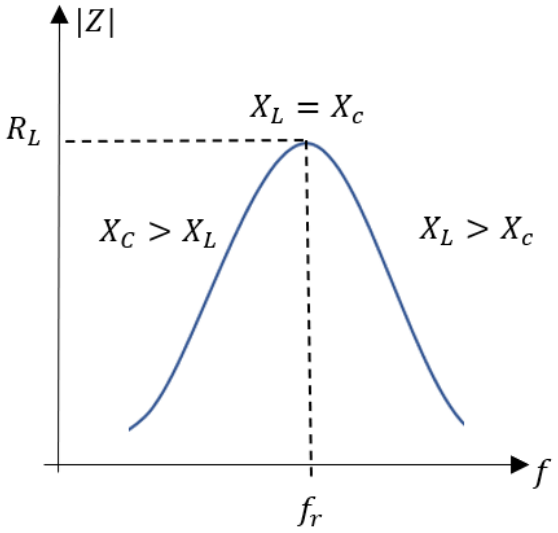


Figure 4-8: Impedance response for RLC resonant filter

4.2.1 Resonant RLC Circuit for the Parallel Case

For the load with parallel inductance, the effect of this component can be easily reduced by attaching a resonant parallel capacitor using (4.3), where L_L is the inductance present on the load side, f_r in this case is the switching frequency and C_L is the required capacitance. The resulting circuit is presented in Figure 4-9.

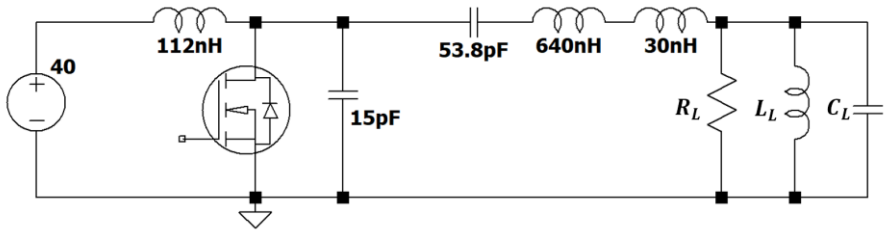


Figure 4-9: Class-E inverter with parallel L_L and RLC circuit

Table 4-4 shows the performance of the inverter for two loading conditions with the parallel inductor L_L and the required capacitance C_L inserted on the load side. The effect due to the tolerance of the capacitor is also shown. It is observed that the tolerance of the required capacitor can have significant effect on the performance of the inverter, especially for low load inductance values.

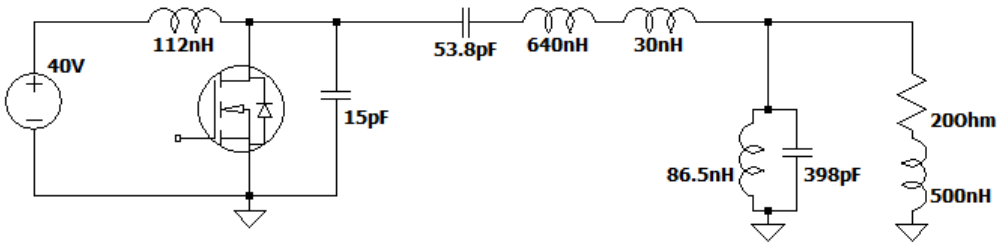
Table 4-4: 100 W 27.12 MHz load-independent Class-E inverter with C_L applied at 10% tolerance

Inductance L_L [nH]	**Req. Cap C_L [pF]**	**Output Power [W]**	**Efficiency at Req. Cap [%]**	**Req. Cap at ±10% variance [pF]**	**Output Power [W]**	**Efficiency [%]**
10	3440	100.96	97.15	3780	124.79	76.5
				3090	67.15	93.5
100	344	101.22	98.07	378	101.86	97.8
				309	98.47	97.8

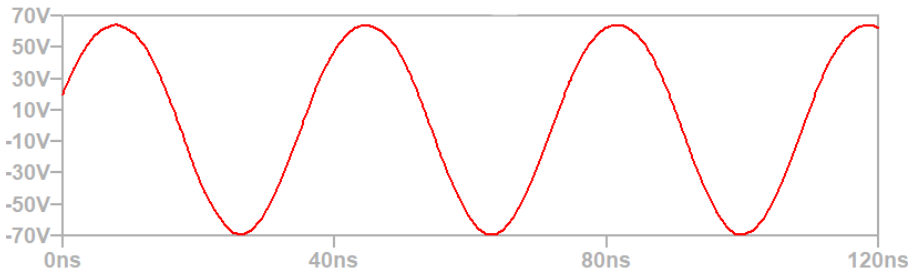
The inverter has been corrected to operate at its nominal state under all loadings. The $\pm$10% variance in capacitance reduces the performance compared to the nominal case but is still a considerable improvement compared to Table 4-2. However, since this setup requires changing the capacitance C_L for each loading, it may not be a practical solution for a dynamic system.

4.2.2 Resonant RLC Circuit for the Series Case

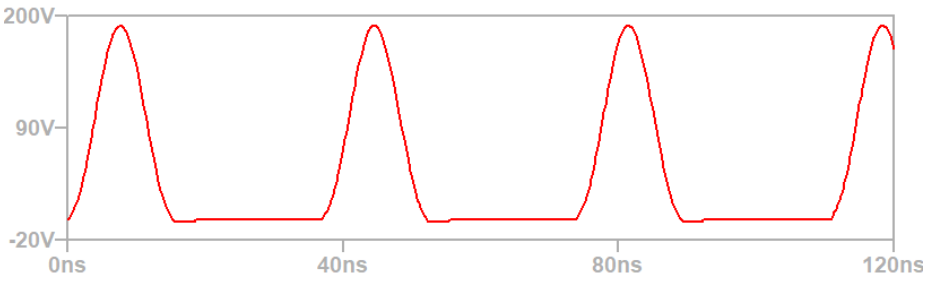
The shunt resonant *RLC* circuit is used for the series case from Figure 4-1 (b) to improve the THD of the output waveforms. Using (4.3) - (4.5) and selecting a bandwidth of 20 MHz, f_r = 27.12 MHz and $R_L = 20\ \Omega$ yield the circuit and filter shown in Figure 4-10 (a). Figure 4-3 showed the heavily distorted waveform in the output of the inverter for the 500 nH case. This effect is significantly reduced in Figure 4-10 (b), resulting in a THD of 4.1%. However, since the loading is reactive, diode conduction is still present in the switch voltage waveform.



(a)



(b)



(c)

Figure 4-10: (a) 100 W 27.12 MHz load-independent Class-E inverter with RLC resonant filter (b) Improved output voltage waveform with RLC resonant filter (c) Diode conduction in switch voltage

Table 4-5 also shows the improved THD with this network, which was fixed for each loading under the series case. Power level and efficiency are also identical to those of Table 4-3.

Table 4-5: Output power and improved THD for the series case using the resonant RLC filter

Inductance L_L [nH]	**Output Power with *RLC* [W]**	**Efficiency with *RLC* [%]**	**Output THD with *RLC* [%]**
1	101.4	98.4	3.51
10	99.8	98.3	3.87
100	58.9	96.7	5.71
500	6.73	85.7	4.28
1000	1.83	68.5	3.90

4.3 Power Factor Correction

Power factor correction (PFC) is a popular technique used in large power systems to reduce the phase difference between the voltage and current waveforms, such that real power is maximized, and reactive power is minimized [20]. This technique presents a purely resistive load to the AC source. The load-independent Class-E inverter in Figure 4-10 for example, acts as a constant AC source within a loading range. Although the distorted output voltage waveforms were fixed by using a resonant *RLC* filter, the inductance or capacitance in the load network contributes to large

load current and diode conduction/hard switching in the switch node. Power factor correction can be applied to minimize the reactive portion of the load and reduce these non-ideal effects without affecting the power level.

The power factor (PF) of a supply is given by

$$\mathrm{PF} = \cos(\theta_v - \theta_i) \tag{4.6}$$

where θ_v and θ_i are the voltage and current angles respectively. For a resistive load, the voltage and current waveforms are in phase resulting in a power factor of unity. However, a power factor of 0.95 and above is adequate since the reactive power portion of the load will be sufficiently low. To correct the power factor to a desired value, reactive power must either be supplied or absorbed using an external supply or by installing reactive components. This can either be done by connecting a capacitor for reactive power supply, or inductance for reactive power absorption across the load network. Figure 4-11 shows the network configuration for supplying reactive power.

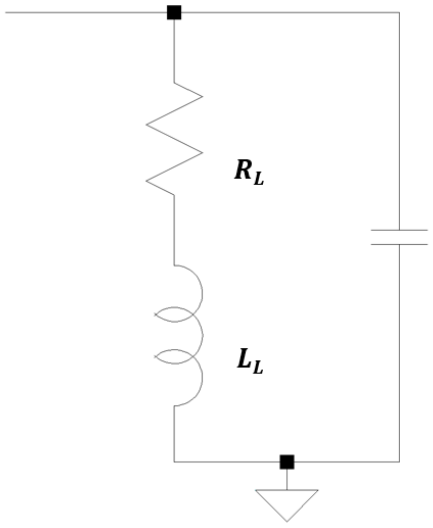


Figure 4-11: Power factor correction on load network for reactive power supply

The total reactive power of the new load network (Q) is found by using the desired power factor ($PF_{desired}$) and the voltage of the load (v_o).

$$Q = \tan(\cos^{-1}(PF_{desired}))\text{real}\left\{\frac{|v_o|^2}{(R_L + jX_L)^*}\right\} \tag{4.7}$$

The required reactive power to be supplied or absorbed (Q_{comp}) is then found using (4.8).

$$Q_{comp} = Q - \text{imag}\left\{\frac{|v_o|^2}{(R_L + jX_L)^*}\right\} \tag{4.8}$$

Now PFC is applied by taking the 500 nH case from Table 4-5 to improve the diode conduction shown in Figure 4-10 (c). The resonant *RLC* filter is still applied to improve the output waveforms. Figure 4-12 shows the circuit with a desired power factor of 0.95 applied with a capacitance of 60 pF.

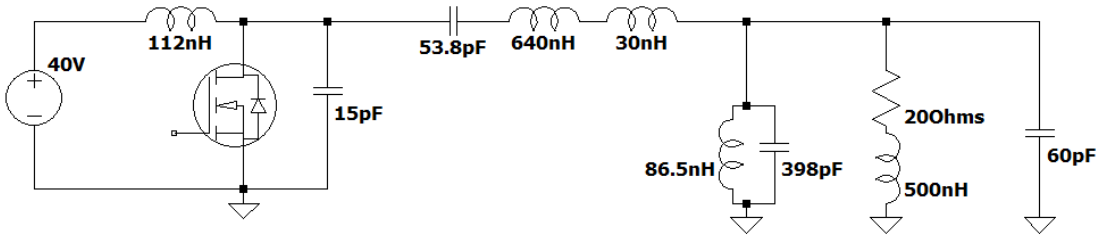


Figure 4-12: Load-independent Class-E inverter with RLC shunt and power factor correction (PF = 0.95)

Table 4-6 shows the performance comparison between the circuit from Table 4-5 and the modified inverter with the shunt resonant *RLC* filter and PFC applied. It can be observed that efficiency has improved with minimal change in the output voltage. The RMS output current is also slightly reduced, but the power level of the inverter is almost unchanged. To control the power level of the inverter under a non-resistive load, another approach is required.

Table 4-6: Performance comparison of the Class-E inverter with power factor correction and RLC circuit

	RMS Output Current i_L [A]	**Output Voltage [V]**	**Load Real Power [W]**	**Load Reactive Power [VAR]**	**Efficiency [%]**	**Output THD [%]**
Without PFC (RLC included)	0.583	47.7	6.73	24.9	85.7	4.28
With PFC (PFC = 0.95)	0.239	48.6	6.93	2.21	93.1	2.86

The benefit of this method however is shown in Figure 4-13, which is the reduced diode conduction. This is because the reactive power component of the load is reduced, and the inverter sees a significant real power draw. This can be further improved by increasing the power factor closer to unity. The simulations show that having a combination of the parallel resonant filter and the power factor correction method mitigates the distorted output voltage and the diode conduction in the switch.

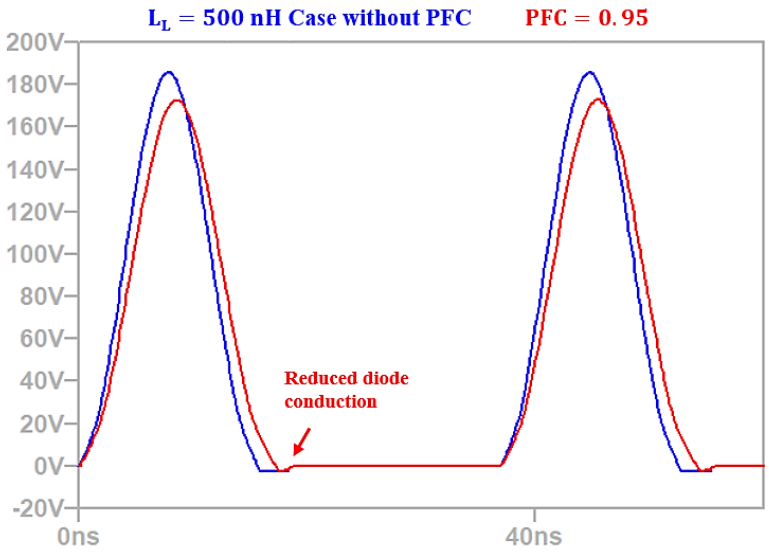


Figure 4-13: Improved diode conduction in the switch voltage with PFC at the 500 nH load series inductance

The simulations presented in this section for PFC were carried out for a fixed load. Alternative solutions exist, such as reconfiguring the LC filter on the load side when the load is fixed. With controlled switching however, PFC can be utilized throughout a variable load commonly seen in WPT. A variable capacitor/inductor bank can be built to toggle the individual components required for each loading, similar to the designs done in larger power systems [20]. The next chapter presents the switching techniques for variable impedance matching that can also be applied for PFC.

4.4 Summary

In this chapter, the performance of the load-independent Class-E inverter was studied when the load is replaced with a series and parallel inductive network and a series capacitive network. Large inductive loads were shown to cause distorted output waveforms and diode conduction in the switch. Similarly, small capacitance on the load was shown to cause hard switching. A simple resonant *RLC* filter was constructed to improve the output of the inverter. However, to avoid the diode conduction or hard switching, a resistive load must be presented to the inverter.

Power factor correction was shown to be the proof of this assumption and is a great solution to reduce the reactive power component of the load network, which reduces hard switching and diode conduction. The combination of the resonant filter and power factor correction is a good solution if non-distorted output waveforms and ZVS in the switch node are desired. However, the main drawback is that the power level is determined by the load impedance and is not controllable. The inverters investigated so far were all designed for a 100 W 27.12 MHz operation, which was not seen in Table 4-5 and Table 4-6 when the load reactance was increased. Although the resistive

portion of the load network was kept constant, the inductance transforms the magnitude of the overall impedance of the load, which significantly alters the power level.

If the power level is to be maintained constant under a varying load, another solution is required which is discussed in the next chapter. But if it is needed to have the load dictate the power drawn from the system, the PFC method is a great alternative, since it gives a true load independent transmitter. Using the switching methods described in the next chapter, a single shunt compensator circuit can be inserted on the load side that switches in the required capacitance and/or inductance to reduce the reactive power draw.

CHAPTER 5 - VARIABLE IMPEDANCE MATCHING FOR DYNAMIC LOADS

The response of a load-independent Class-E inverter to non-resistive loads was shown in the previous chapter. A significant drop in efficiency and power level was observed in addition to switch losses and distorted output waveforms. A shunt resonant *RLC* filter and a power factor correction method was shown to compensate this effect and operate the inverter in its nominal condition. In this chapter, an impedance matching solution is studied that achieves a similar result while keeping power levels consistent. This is useful for applications with dynamic loading such as WPT, where having the ability to control the output power is required during resonator misalignments while preventing hard switching or diode conduction in the switch voltage.

5.1 Basic Concept of Impedance Matching

Impedance matching is a design process that is typically used to transform one impedance to another to control the power transmission. For a load-independent Class-E inverter, since the output voltage is constant, the load can be transformed to a desired resistance R_L based on (3.22) - (3.26) across a variable load. In this chapter, the load will be transformed to a fixed value from a variable load, which is referred to as variable impedance matching. The same concept can be utilized for the standard Class-E inverter design from Chapter 3, where the load is transformed to the designed inverter load resistance. First, the analysis is presented for a fixed load, referred to as constant impedance matching.

Constant impedance matching is implemented using matching networks. These matching networks can also act as filters and be used to reduce the harmonic content of the output. There are multiple

matching network topologies available in the literature [21]. In this chapter, the two main types of matching networks studied are the following:

- Double-L network
- Double-T network

Cascaded designs are pursued instead of the single network to control the input impedance due to the variable load. The additional network allows the load to be transformed to a desired resistive portion while minimizing the imaginary part. A single network is unable to support larger variations in the load impedance and will become apparent in the studies below.

5.1.1 The Double-L-Network

The double-L-network is a simple "L" shaped *LC* filter that is cascaded as shown in Figure 5-1. This network can be configured to provide a low pass or high pass response. In this section, the double-L network is configured to provide a low pass response to pass electromagnetic compatibility (EMC) standards and give access to the shunt capacitors for dynamic impedance matching in the upcoming sections.

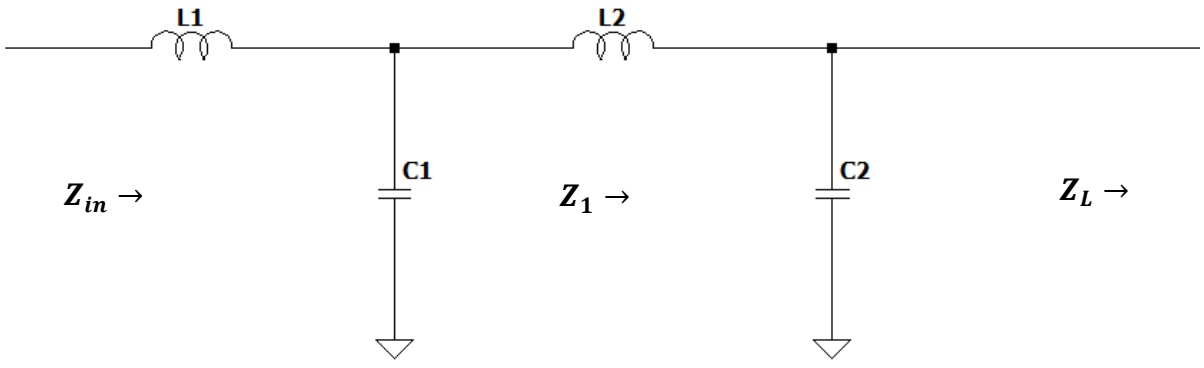


Figure 5-1: The double-L network

In Figure 5-1, Z_L is the actual load impedance and Z_{in} is the load impedance seen by the Class-E inverter. Since it was already shown how the Class-E inverter performs under resistive loads, this and upcoming sections will only focus on non-resistive loads. However, these matching networks can be utilized to transform one purely resistive load to another to achieve a desired power level.

Analyzing the matching network from Figure 5-1 gives the following equations for the input impedance. Combining C_2 and Z_L on the load side gives:

$$Z_L || \frac{1}{jB_2} \tag{5.1}$$

where B_2 is the susceptance of C_2. Combining this parallel combination with X_2, the reactance of L_2, gives:

$$Z_1 = jX_2 + \frac{Z_L}{1 + jB_2 Z_L} \tag{5.2}$$

Similarly, using parallel combination again with B_1 gives the input impedance Z_{in}.

$$Z_{in} = jX_1 + \frac{Z_1}{1 + jB_1 Z_1} = jX_1 + \frac{jX_2 + \frac{Z_L}{1 + jB_2 Z_L}}{1 + jB_1 \left[jX_2 + \frac{Z_L}{1 + jB_2 Z_L} \right]} \tag{5.3}$$

The equation above contains four variables (X_1, X_2, B_1, B_2) that can be optimized to transform Z_L to a purely resistive impedance Z_{in}. Reactance X_1 and X_2 are typically fixed, and the two capacitors will allow for better control of the input impedance.

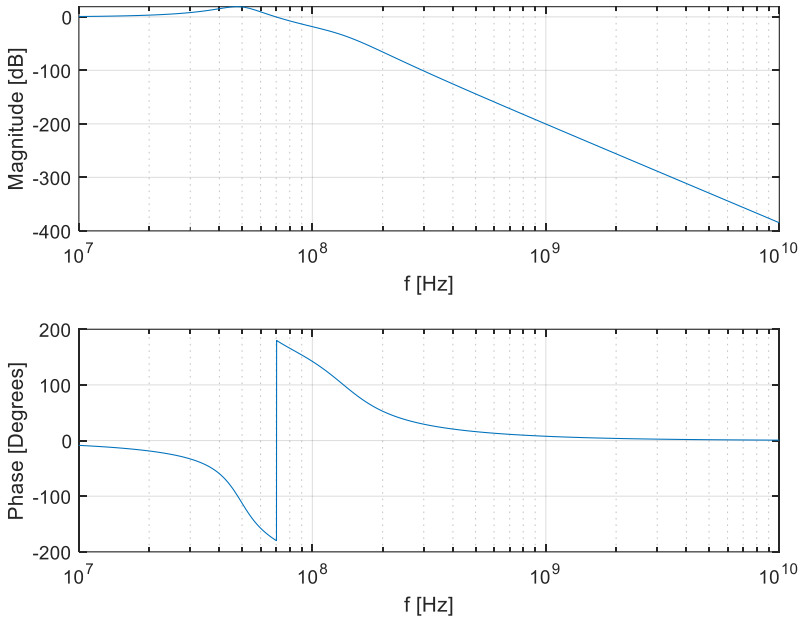


Figure 5-2: Magnitude and phase response for double-L impedance matching network

[Zin = 40 Ω, Z_L= 60+1.1 Ω, L_1=70 nH, L_2=70 nH C_1=150 pF, C_2=20 pF]

As mentioned above, the double-L impedance matching network can also act as a filter for the circuit. With proper tuning, a low pass filter response can be obtained to eliminiate the high harmonic content presented from the Class-E inverter switch voltage shown in Chapter 3. However, since the filter response is heavily dependent on the components used for matching, the filter properties may prove to be difficult to control. Figure 5-2 shows an example of the ideal magnitude and phase response obtained from the double-L matching network when the desired input impedance is set to 40 Ω.

5.1.2 The Double-T-Network

A double-T-network includes an additional inductance when compared to the double-L network. The network configuration is shown in Figure 5-3. The middle inductance L_2 is the combined inductance after the two single-ended T networks are cascaded.

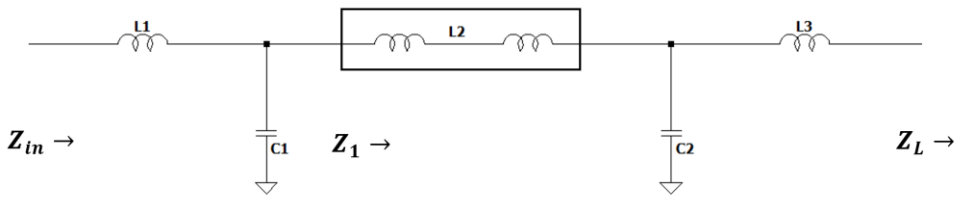


Figure 5-3: The double-T impedance matching network

Using the simplified circuit of Figure 5-3 and following the same procedure established in (5.1) - (5.3), the resulting equations for the input impedance are shown in (5.4) - (5.5).

$$Z_1 = jX_2 + \frac{jX_3 + Z_L}{(jX_3 + Z_L)jB_2 + 1} \tag{5.4}$$

$$Z_{in} = jX_1 + \frac{Z_1}{Z_1 jB_1 + 1} \tag{5.5}$$

5.2 Variable Impedance Matching Network (VIM)

In applications such as WPT, the load seen by the inverter can vary due to the displacement of the resonators, contact with foreign objects and environmental conditions. Using a fixed matching network under a varying load will make the inverter perform at its ideal state only at its designed load. The matching network itself will need to change for each loading configuration.

Reconstructing the matching network would yield the best performance for each loading, but it is impractical to do this manually. Automating this process through controlled switching is preferred. It is also much easier to switch in shunt capacitors because they add in parallel with one end referenced to ground. Popular methods for achieving this includes using PIN diodes [22], MEMS switches [23], Varactors [24], and Relay switches [25]. Each capacitor bank contains a pre-installed number of capacitors that are toggled using one of the methods above.

Using this information, the automated matching algorithm determines the correct capacitances for a given load impedance Z_L. A detector circuit is typically present on the load side that measures the magnitude and phase of the load impedance. The control circuit containing a microcontroller then runs an optimization algorithm that selects the best set of capacitors to provide the desired input impedance. The design of this detector circuit and control scheme of the microcontroller is not the focus of this thesis work. The selected capacitors are then turned on using any of the switching methods described above. The paper shown in [24] utilizes a π network with varactor capacitors that are configured to match automatically. Similarly, [26] shows an *LC* network for a magnetic system.

5.2.1 The Variable Double-L Network

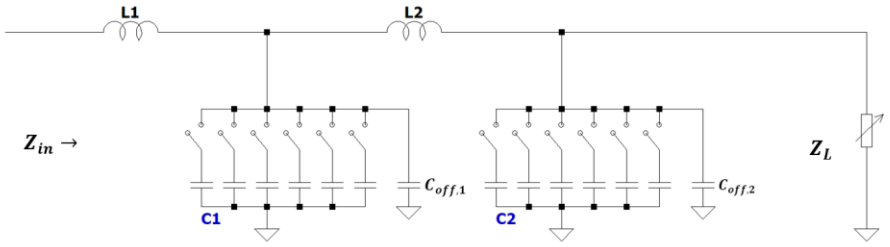


Figure 5-4: The variable double-L network using the MM3100 MEMS device

A variable double-L network with a set of switching device is shown in Figure 5-4. The design for each loading is identical to (5.3). However, due to the presence of the switching device, the voltage and current on the shunt capacitors may need to be limited. For example, the MM3100 is a Micro-Electromechanical System (MEMS) device with an array of 6 switches that contains a maximum voltage rating of 141 V_{rms} and current rating of 1 A_{rms} for each branch [27]. The voltage rating is considered for the switch off state while the current rating is important for its on state. Taking this limitation into consideration, the maximum allowable capacitance per branch can be found using (5.6).

$$C = \frac{I_{rms}}{\omega V_{rms}} \tag{5.6}$$

This gives a maximum capacitance of 82 pF when the operating frequency is 13.56 MHz, 41 pF for 27.12 MHz and 27 pF for 40.68 MHz. Furthermore, due to the voltage rating of the switch, the maximum load resistance is also limited. For an output power of 100 W, the maximum load resistance (R_L) is limited to 198 Ω. Scaling the power level to 500 W severely brings this value down to approximately 40 Ω. Systems that require a larger matching range across variable loads will need to verify if the switching device is adequate for the design. PIN diodes such as MA4P7104F-1072T for example contain a large peak reverse bias voltage rating (400 V) and can accommodate larger capacitance [28]. These diodes act as a switch for RF by toggling between the forward bias (on state) and reverse bias (off state) conditions.

5.2.2 The Variable Double-T Network

Figure 5-5 shows the resulting variable double-T network with two variable shunt capacitor banks. As before, L2 is the combined inductances of the single-ended T networks after cascading to form the double-T network. Unlike the double-L network, the additional inductance L3 needs to be considered when determining the maximum load resistance (R_L) for the design.

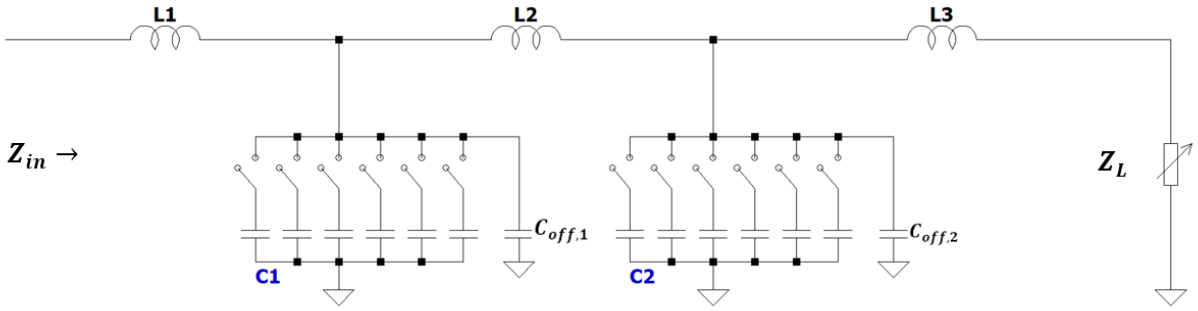


Figure 5-5: The variable double-T network using the MM3100 MEMS device

5.3 Experimental Study of the Double-L VIM Network

A Class-E push-pull inverter at 13.56 MHz with a double-L VIM network was simulated and tested on a RC^2 WPT system [29]. Figure 5-6 and Figure 5-7 show the setup for the constant power test and the transmitter PCB. The network consists of the following 6 predetermined capacitors per each branch: 20 pF, 40 pF, 80 pF, 150 pF, 150 pF, 150 pF. These capacitors are also toggled using the MA4P7104F-1072T PIN diodes for each loading. The capacitors can be simultaneously connected in giving a total capacitance of 590pF per each branch. The test setup consists of a transmitter board housing the Class-E push-pull inverter and the double-L matching network. The inverter utilizes eGaN EPC2019 FETs for the switching. The output of the matching network is connected to the transmit resonator, and the output of the receive resonator is terminated by two 50Ω RF loads.

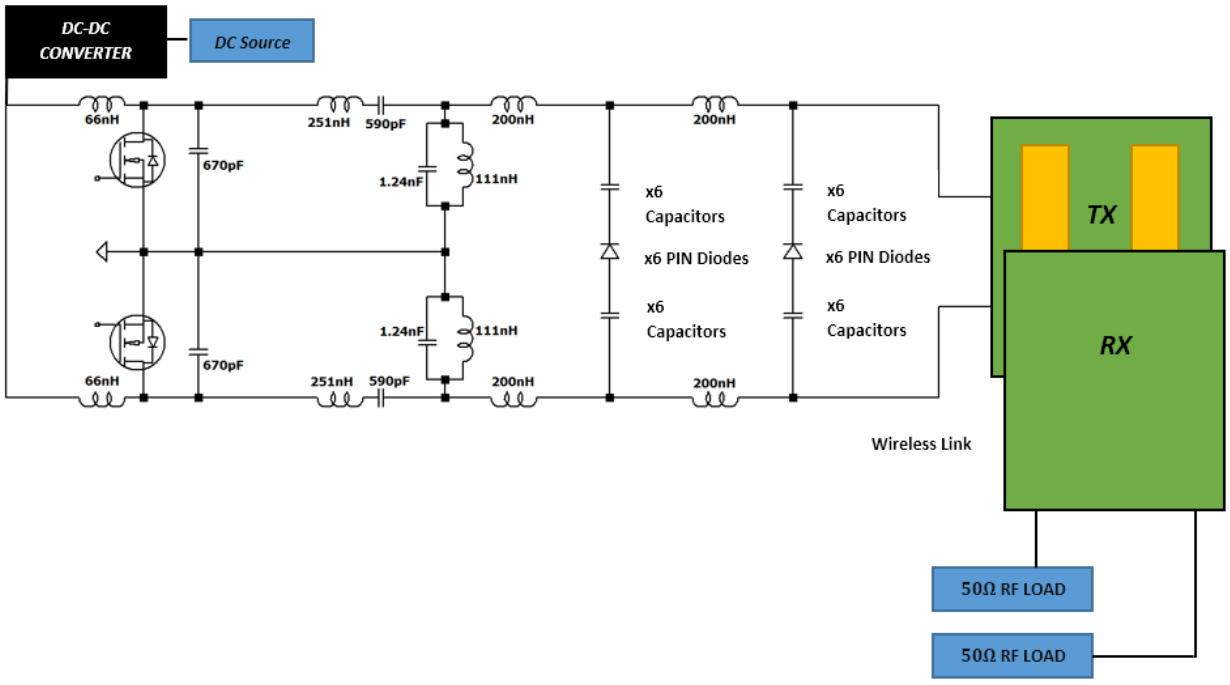


Figure 5-6: 13.56 MHz load-independent Class-E inverter with VIM network setup for the constant power test

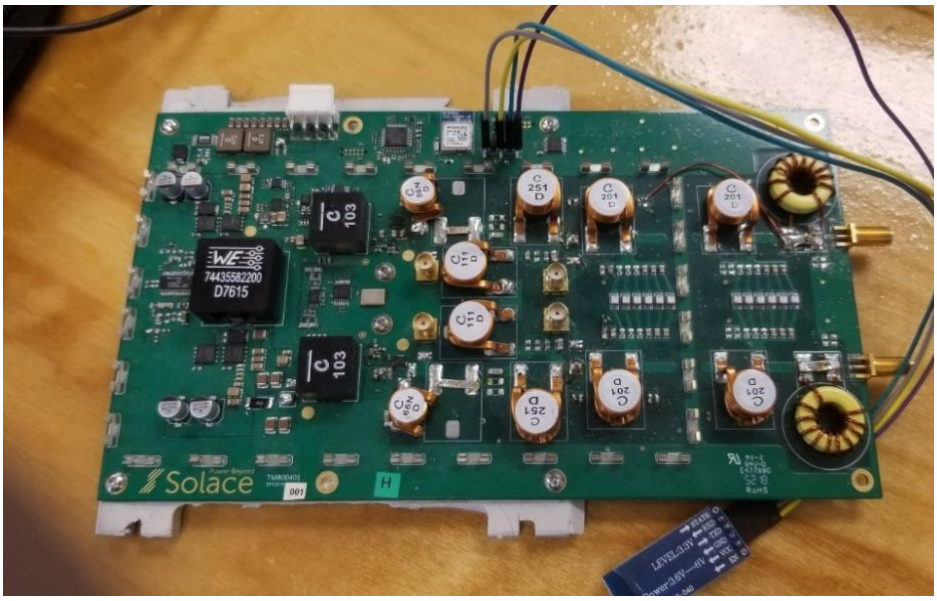


Figure 5-7: Transmitter board used for testing the inverter and VIM network [29]

Table 5-1 shows the single ended load impedance range considered in the simulation. These are the input impedance of the resonator (or wireless link) tuned at approximatly 55mm displacement between the two. These are also the equivalent single-ended impedances seen by each phase of the differential push-pull inverter without a matching network (Z_L). Displacing these resonators from this position is shown to drastically affect the measured impedance.

Table 5-1: Resonator impedance values

Resonator Displacement (Plate-Plate) [mm]	$\boldsymbol{Z_L}$ **[Ω]**
80	10 - 4i
75	12.7 - 3.3i
70	15 - 2.6i
65	18 - 1.8i
60	26 - 0.3i
55	31 - 0.2i
50	38 - 0.6i
45	50 - 2.2i
40	61 - 6i
35	73 - 13i
30	91 - 31i
25	102-54i

Using (5.3) and the 6 shunt capacitors, the inductors L1 and L2 for the matching network are determined such that the largest matching range is obtained for the impedances shown in Table 5-1. The values of L1 and L2 were optimized using a MATLAB script based on the following criteria: search for an input impedance (Z_{in}) that prioritizes obtaining the desired *real* component, while minimizing the *imaginary* component. The desired input impedance is set to 15 Ω with an allowed error of ± 1 Ω and $\pm j2$ Ω. This script is attached in Appendix A.

Figure 5-8 shows the largest matching range possible across the resonator impedance for some inductor combinations. This range is once again limited due to the 6 preinstalled capacitors listed above. With this setup, the double-L network is unable to transform the resonator impedance to 15 Ω for the entire loading range.

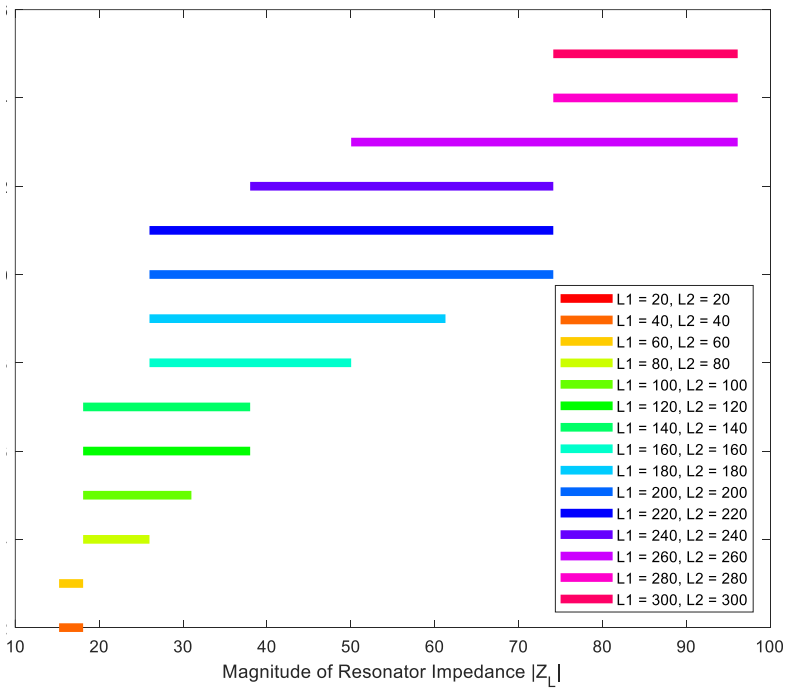


Figure 5-8: Double L impedance matching range across variable load for different inductor [nH] combinations (Zin = 15 Ω, C1 & C2 =20 pF, 40 pF, 80 pF, 150 pF, 150 pF, 150 pF)

Using an inductance of 200 nH for L1 and L2, Figure 5-9 shows the matchable impedance range of the double L network on the Smith chart. The blue points display all the possible loadings that can be matched to 15 Ω while the red points are the resonator impedance from Table 5-1. These values are all normalized by 50 Ω. It is observed that the network is able to provide a balanced support over the inductive and capacitive regions while slightly favouring the former. However, as concluded above, it is unable to handle load impedances with larger resistive and reactive components.

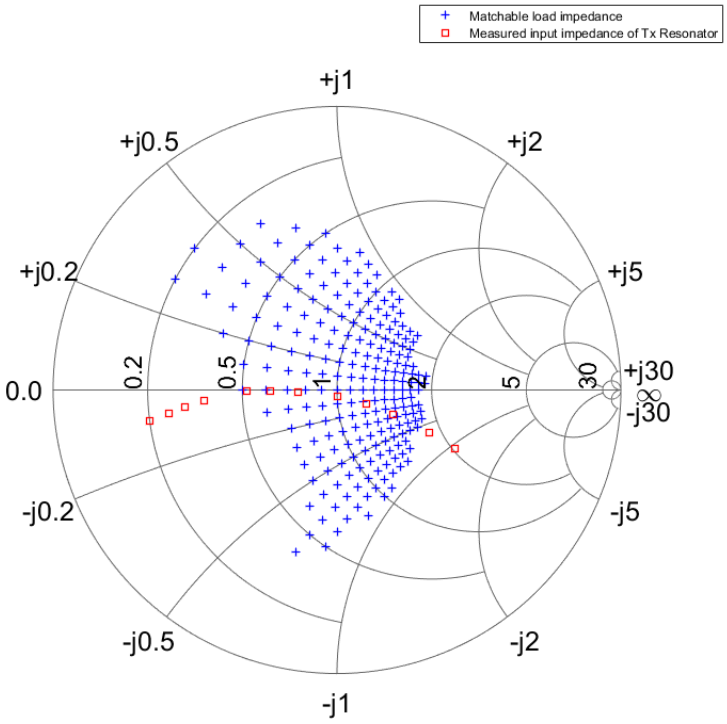


Figure 5-9: Range of load impedance that can be matched using the double-L network normalized by 50 Ω [Zin = 15 Ω, L1=L2=200 nH, C1 & C2 =20 pF, 40 pF, 80 pF, 150 pF, 150 pF, 150 pF]

Before proceeding to measure the input impedance using the chosen L1 and L2 values, the quality factor for each inductance is determined to validate the simulations during the experiments. Unlike

the previous LTSpice simulations, the components and PCB have parasitic elements that significantly alter the impedances and the efficiency of the inverter. Table 5-2 shows the measured quality factor and series resistance of all the Coilcraft inductors installed on the board [30]. The circuit configuration is provided in Figure 5-6.

Table 5-2: Coilcraft air core inductor quality factor

Inductance [nH]	Quality Factor [Q]	Rs [Ω]
66	90	0.063
111	80	0.118
201	100	0.171
251	110	0.194

Other parasitic elements on the board are also determined to reduce the simulation error. To determine the PIN diode capacitance and the PCB parasitics, the input impedance of the matching network is measured at different loadings when all diodes are off using a VNA . The inductances L1 and L2 are set to 200 nH. In an ideal single-ended system, the resulting impedance will equal the summation of the load and the impedance of the series inductors L1 and L2 shown in Figure 5-4. In a differential connection like in Figure 5-6, the single-ended value is be doubled. But, as seen in Table 5-3, the offset in the shunt capacitance due to parasitics significantly alters the expected result.

Table 5-3: Differential input impedance at 13.56 MHz of the double-L VIM when all 6 PIN diodes are off

Z_L [Ω] →	100	80	60	40	20
Measured Z_{in} [Ω]	93.2+7.2i	85.6+24.9i	73+43i	54.2+60i	29.7+71.3i
Expected Z_{in} [Ω]	100.7+68i	80.7+68i	61.7+68i	41.7+68i	21.7+68i

The least squares method (LSM) was used to accurately estimate the shunt offset capacitances due to parasitics ($C_{off,1}$ and $C_{off,2}$ in Figure 5-4) based on the data in Table 5-3 and (5.3). This yielded

$C_{off,1}$ = 49 pF and $C_{off,2}$ = 26 pF. The MATLAB script for determining the offset capacitance is given in Appendix B.

Using the results above, simulations are conducted in LTSpice to attain constant power over a variable load. Table 5-4 shows the simulation results for a 25 W 13.56 MHz load-independent Class-E push-pull inverter with the double-L VIM network. The parasitic offset capacitors identified above were taken into consideration when determining the C1 and C2 values with L1=L2=200 nH such that the desired input impedance of 15 Ω with an allowed error of ± 1 Ω and $\pm j2$ Ω is achieved. The resulting Z_{in} is also provided which is found using (5.3) with the corresponding L1, L2, C1, C2, $C_{off,1}$ and $C_{off,2}$values.

Table 5-4: The performance of the simulated 25 W load-independent Class-E push-pull inverter with VIM

Displacement [mm]	**Z_L [Ω]**	**L1 [nH]**	**L2 [nH]**	**C1 [pF]**	**C2 [pF]**	**Calculated Z_{in} [Ω]**	**LTSpice Peak Switch Voltage [V]**	**LTSpice Output Power [W]**	**LTSpice Inverter Efficiency [%]**
60	26 - 0.3i	200	200	560	40	14.58+1.99i	54.65	23.46	74.40
55	31 - 0.2i	200	200	480	40	14.59+1.16i	54.65	23.21	76.40
50	38 - 0.6i	200	200	400	80	14.43-0.05i	54.65	24.92	75.75
45	50 - 2.2i	200	200	280	120	15.41+1.05i	54.65	24.40	76.42
40	61 - 6i	200	200	120	200	15.24-0.55i	54.65	23.13	75.44
35	73 - 13i	200	200	80	160	14.02+0.81i	54.65	25.10	77.75

Within the limited range, constant power is achieved using the double-L network in simulations. The slight deviation in power level occurs because of the ± 1 Ω error allowed in the input impedance. Ideally this and the imaginary component error should be set to zero, but is not practical and the range shown in Figure 5-8 and Figure 5-9 will be significantly reduced.

The simulations results are now verified with an experimental test. Table 5-5 shows the resonator impedance that can be transformed to 15 Ω, the calculated input impedances Z_{in} shown before, as well as the actual measured input impedance Z_{in} from the transmitter board after building this circuit. The measured impedances are very close to the desired value since the offset parasitics were included in the simulations.

Table 5-5: Input impedance measurement considering the parasitic offset capacitance

Displacement [mm]	**Z_L [Ω]**	**L1 [nH]**	**L2 [nH]**	**C1 [pF]**	**C2 [pF]**	**Calculated input impedance with parasitics Z_{in} [Ω]**	**Measured input impedance from VNA Z_{in} [Ω]**
60	26 - 0.3i	200	200	560	40	14.58+1.99i	14.81+1.82i
55	31 - 0.2i	200	200	480	40	14.59+1.16i	14.80+0.31i
50	38 - 0.6i	200	200	400	80	14.43-0.05i	14.32+0.40i
45	50 - 2.2i	200	200	280	120	15.41+1.05i	14.76+0.32i
40	61 - 6i	200	200	120	200	15.24-0.55i	14.89+1.71i
35	73 – 13i	200	200	80	160	14.02+0.81i	14.51 + 1.8i

The 25 W 13.56 MHz Class-E push-pull inverter was then tested over the impedance range that can be transformed to approximately 15Ω. Since this is a load-independent inverter in combination with VIM network, the switch voltage is expected to be the same across the load range above.

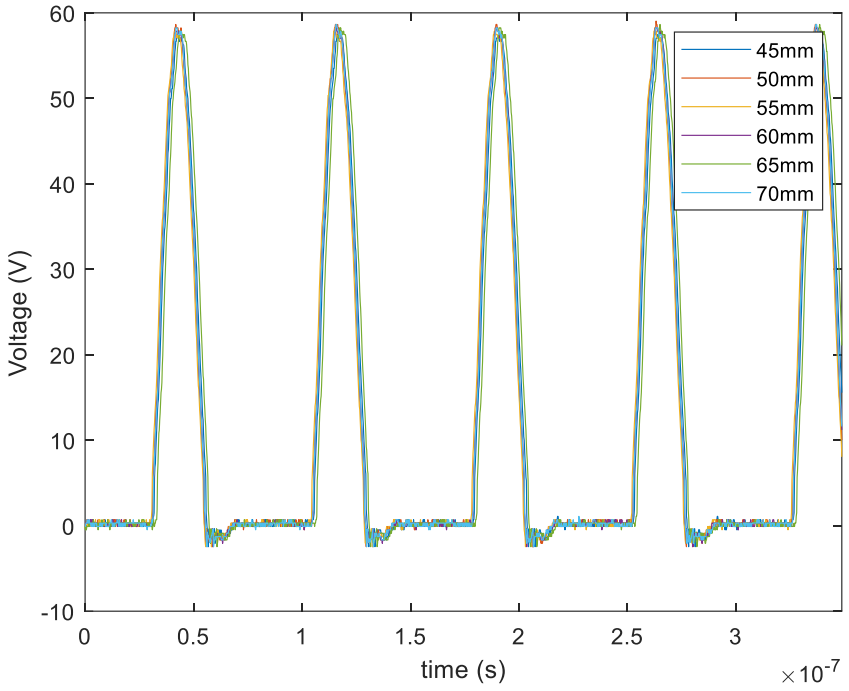
Table 5-6 shows the results obtained during the constant power test. V_{cc} is set to 11V for all cases and the measured output power is the total received power at the two 50 Ω RF loads. The efficiency of the inverter was estimated by making the following assumptions: efficiency of the DC-DC converter and the wireless link is 90% respectively under the load variation. The table also shows that constant power of approximately 23-25 W is achievable with the Class-E push-pull inverter and the VIM network, albeit with slight deviations. Note that the RC^2 resonators are extremely sensitive to physical movements and a slight deviation in displacement could result in a larger change in impedance. Since the resonators were physically moved by hand to change the

impedance, this could act as a source of error for some of the lower power cases (22.1W) in Table 5-6, where the actual impedance is slightly different from the expected resonator impedance Z_L.

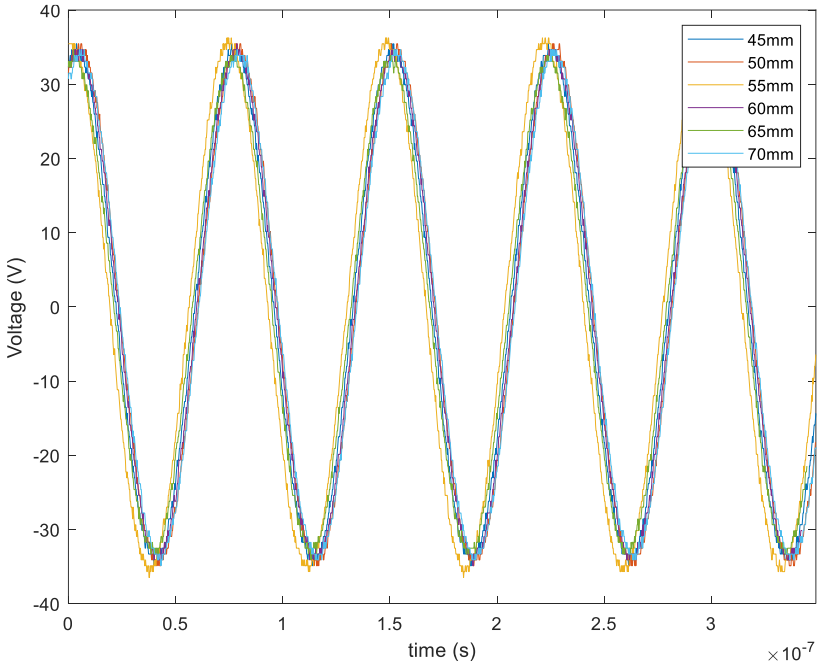
Table 5-6: Performance results for the Class-E push-pull inverter with VIM network

Displacement [mm]	**Z_L [Ω]**	**Measured Peak Switch Voltage [V]**	**Measured RMS Output Voltage [V]**	**Input Power to Transmitter [W]**	**Measured Output Power [W]**	**Estimated Inverter Efficiency [%]**
60	26 - 0.3i	58.733	21.264	36.450	23.232	78.69
55	31 - 0.2i	58.733	22.647	34.500	22.090	74.89
50	38 - 0.6i	58.733	21.978	35.200	23.232	77.19
45	50 - 2.2i	58.733	22.932	36.700	24.800	79.04
40	61 - 6i	58.733	23.299	35.700	23.814	78.02
35	73 - 13i	58.733	22.364	34.350	23.232	79.10

From the waveforms shown in Figure 5-10, all switch voltages are similar, but slight diode conduction is observed. This is due to the $j2\ \Omega$ deviation allowed for Z_{in}, as well as the limitations of the components and the parasitic impedances altering the desired results. The constant switch node waveform however translates to constant output voltage with small deviations as shown in Figure 5-10 (b).



(a)



(b)

Figure 5-10: 25 W 13.56 MHz Class-E push-pull with double-L VIM (a) switch voltage waveform (b) output voltage waveforms

5.4 Experimental Study of the Double-T VIM Network

In this section, the performance of the double-T VIM network is presented through an experimental study. As in section 5.3, the experimental study was conducted with a Class-E push-pull inverter and a double-T VIM network. Once again, the following 6 predetermined capacitors are considered for each branch: 20 pF, 40 pF, 80 pF, 150 pF, 150 pF, 150 pF. Table 5-3 showed the severe influence of the parasitics during the experimental study. For the variable double-T network, the parasitic offsets $C_{off,1} = 49$ pF and $C_{off,2} = 26$ pF are considered in the model when determining the required C1 and C2 capacitance for each loading. Similar to the earlier study, Figure 5-11 shows the largest matching range possible for each inductor combination with the six pre-selected capacitors. The resonator impedances (Z_L) are identical to Table 5-1. The desired resistance is also once again set to 15Ω with an allowed error of ± 1 Ω and $\pm j2$ Ω in the real and imaginary parts.

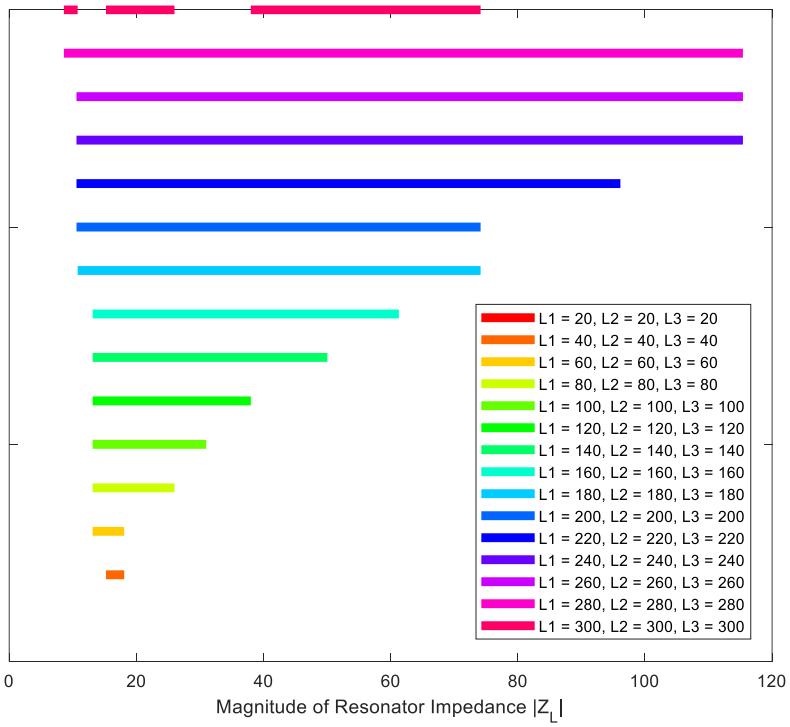


Figure 5-11: Double T impedance matching range across variable load for different inductor [nH] combinations (Zin = 15 Ω, C1 & C2 =20 pF, 40 pF, 80 pF, 150 pF, 150 pF, 150 pF)

Unlike the variable double-L network, a significant increase in the matching range is observed. The previous section showed that the variable double-L can support up to 25mm displacement with the resonator. With the variable double T, the entire range can be covered. For the test below, the inductances are set to L1=L2=L3=200 nH.

Figure 5-12 shows the range of impedance that can be matched to 15 Ω with the double-T network when L1=L2=L3=200 nH on a Smith chart. Each red point indicates the resonator impedance normalized to 50 Ω. Due to the additional inductance L3, the data points in the Smith Chart are now shifted towards the capacitive region when compared to Figure 5-9. Hence the double-T network is more appropriate for applications that contain large capacitive loads. Since the resonator impedances (Z_L) from Table 5-1 are largely capacitive, an immediate improvement in the matching range is noticed compared to the double-L design.

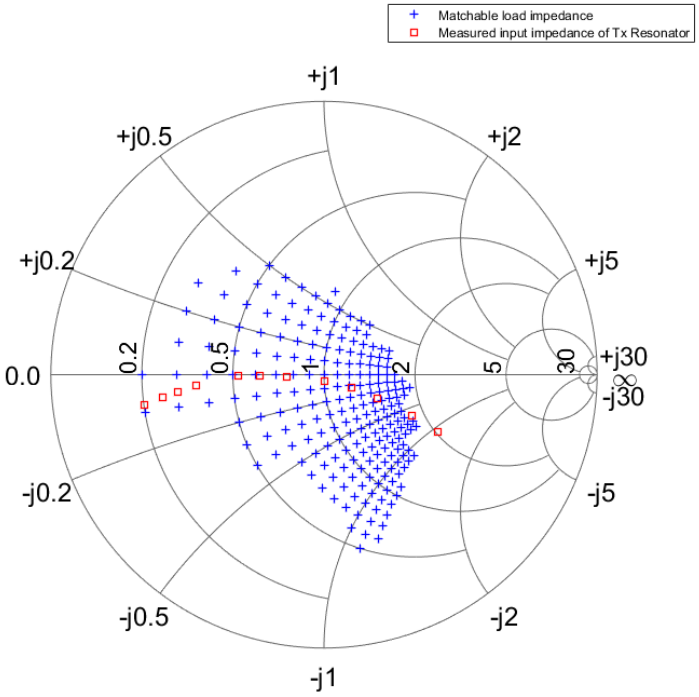


Figure 5-12: Range of load impedance that can be matched using the double-T network normalized by 50 Ω [Zin = 15 Ω, L1=L2=200 nH, C1 & C2 =20 pF, 40 pF, 80 pF, 150 pF, 150 pF, 150 pF]

Table 5-7 shows the load range that can be matched to 15 Ω (Z_L), and the calculated and measured input impedances for each loading. The required capacitance C1 and C2 for each case is also presented. Including the effects of the board parasitic impedance in the simulations made the measured input impedance agree with the calculated results with less discrepancies.

Table 5-7: Input impedance measurement with the double-T network

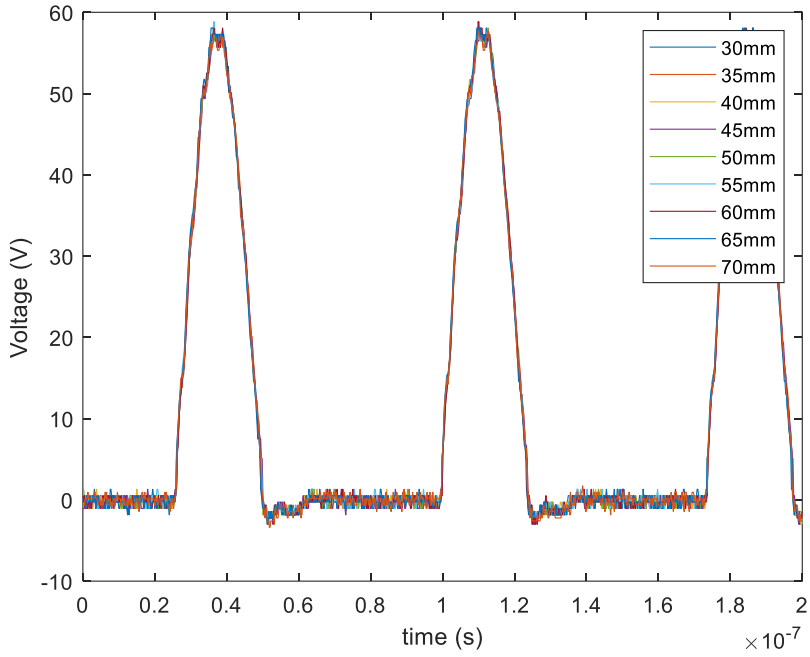
Displacement [mm]	**Z_L [Ω]**	**L1 [nH]**	**L2 [nH]**	**L3 [nH]**	**C1 [pF]**	**C2 [pF]**	**Calculated input impedance with parasitics Z_{in}[Ω]**	**Measured input impedance from VNA Z_{in}[Ω]**
80	10 - 4i	200	200	200	560	560	14.39-0.73i	15.4 + 0.7i
75	12.7 - 3.3i	200	200	200	520	520	15.21+1.05i	15.5 + 2i
70	15 - 2.6i	200	200	200	520	400	14.95-0.61i	14.9 + 1i
65	18 - 1.8i	200	200	200	480	320	15.10-1.22i	15.2 + 0.3i
60	26 - 0.3i	200	200	200	440	240	14.77-1.32i	15.1 - 1i
55	31 - 0.2i	200	200	200	360	280	14.76+1.03i	14.6 + 1.5i
50	38 - 0.6i	200	200	200	320	200	14.92-1.12i	14.7 - 0.8i
45	50 - 2.2i	200	200	200	200	240	14.77+1.23i	15.2 + 1.2i
40	61 - 6i	200	200	200	120	240	14.87+1.37i	15.1 + 1.1i
35	73 - 13i	200	200	200	80	200	15.05-1.18i	14.9 - 1.6i

The constant power test for the 25 W 13.56 MHz load-independent Class-E push-pull inverter was repeated with the variable double-T network. Table 5-8 shows that constant power is achievable for a wider displacement using this network. However, once again, the allowed error of ± 1 Ω for the input impedance, as well as the discrepancy error during resonator displacement caused the power level to be reduced for some cases. This translates to slightly lower efficiency.

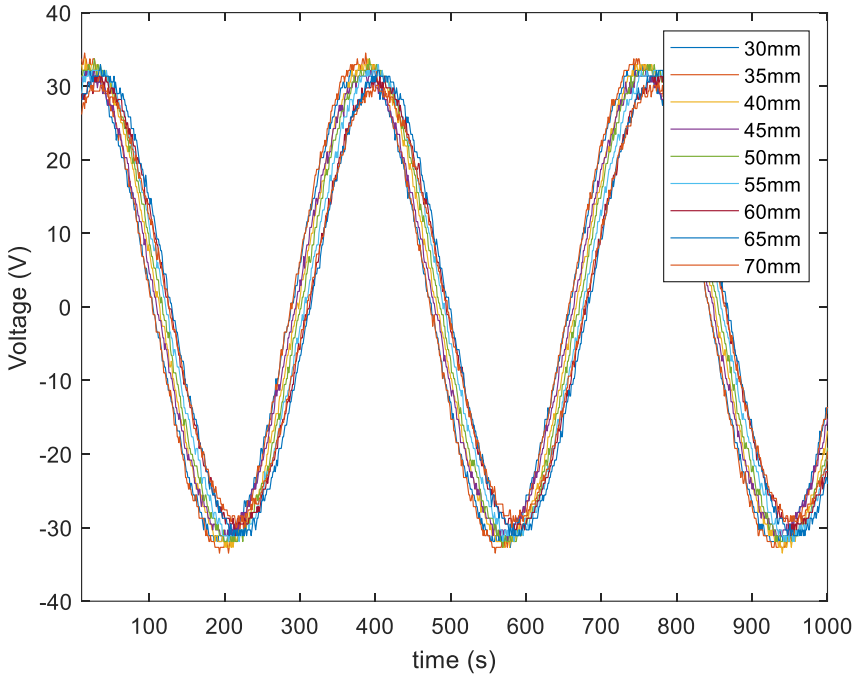
Table 5-8: Class-E push-pull inverter voltage and power measurements with the double-T network

Displacement [mm]	**Z_L [Ω]**	**Measured Peak Switch Voltage [V]**	**Measured RMS Output Voltage [V]**	**Input Power to Transmitter [W]**	**Measured Output Power [W]**	**Estimated Inverter Efficiency [%]**
80	10 – 4.0i	58.1	22.647	35.4	20.6116	71.88
75	12.7 - 3.3i	58.1	21.978	34.5	19.5364	69.91
70	15 - 2.6i	58.1	22.932	35.1	20.7936	73.14
65	18 - 1.8i	58.1	23.299	34.7	21.7156	77.26
60	26 - 0.3i	58.3	22.364	32.5	20.0704	76.24
55	31 - 0.2i	58.1	23.535	34.4	22.09	79.28
50	38 - 0.6i	58.1	23.665	33.7	22.2784	81.61
45	50 - 2.2i	58.1	22.977	32.1	20.9764	80.68
40	61 - 6i	58.1	23.788	33.8	22.6576	74.95
35	73 - 13i	58.1	23.298	32.6	21.7156	71.88

Similar to the double-L network, the Class-E push-pull inverter inherits its load-independent trait throughout the variable loading due to constant impedance matching. This is seen through the measured constant output and switch voltage waveforms shown in Figure 5-13. However, some diode conduction is still present due to the $j2\ \Omega$ deviation allowed for Z_{in}, and the parasitics of the board altering the design. The matching network, however, is shown to resolve the issues presented in Chapter 4 for the Class-E inverter under reactive loads by maintaining consistent power levels, efficiencies and showing less distorted waveforms in the output.



(a)



(b)

Figure 5-13: 25 W 13.56 MHz Class-E push-pull with double-T VIM (a) switch voltage waveform (b) output voltage waveforms

5.5 Summary

In this chapter, the performance of the Class-E push-pull inverter with the variable impedance matching network is investigated under a variable non-resistive load. Two matching networks were studied that gave similar performance values. As shown in the Smith Charts, to maintain matching for low inductive and capacitive loads, the double-L network is recommended, whereas the double-T favors more of the capacitive region. Results obtained through simulation and experimental study showed that the impedance range of the double-T that can be matched is superior due to the input impedance of the transmitter resonator falling in the capacitive region in the Smith Chart. These networks can be further optimized to provide extended support across the load range. The double L network for example can be improved by making sure the load impedance falls in the middle region of the Smith Chart, which can be purposely done by detuning the transmit resonator. Depending on loading, the matching networks can also be modified by adding series and shunt components, such that the impedance points in the Smith Chart are shifted to support the desired load impedances.

The analysis presented in this chapter is for the case where the user can obtain a desired load by controlling the output power of the system. The drawback of this solution is that the resulting system is bulky as it requires two or more large inductances for each channel.

CHAPTER 6 - CONCLUSION AND FUTURE WORK

6.1 Thesis Summary

This thesis studied the performance of Class-E inverter design under non-resistive loading which can be observed in WPT systems, where the resonators present a non-resistive impedance to the inverter when displaced or if a foreign object is introduced. Since the efficiency of the wireless link varies due to these factors, it is important to make sure the inverter is operating in a stable and efficient manner. First, the dominant harmonics of the Class-E inverter was studied, and the load-independent design was presented. The performance was then studied under a non-resistive load. Several methods were studied to deal with fixed and variable non-resistive loads, which includes the power factor correction method, constant impedance matching, and variable impedance matching. Simulations were performed in LTSpice and MATLAB to demonstrate the functionality of these methods. In addition, a test board was used to experimentally validate the variable impedance matching results obtained through simulation.

The results of the work through simulation and the experimental investigation revealed that under a heavy inductive load, the switch node of a Class-E inverter shows diode conduction. Similarly, a highly capacitive load shows hard switching. Furthermore, since the frequency response of the load network is affected by the introduction of these non-resistive components, the load waveforms are also heavily distorted. Power factor correction with a resonant *RLC* filter was shown to improve both the switch node and output voltage waveforms. Implementing this solution requires a varying capacitor bank on the load side that is toggled at each loading. An alternative solution is to use a matching network to convert the actual load and present it as a resistance to the inverter. Being simpler to construct, power factor correction is the suggested method to maintain the high

efficiency and waveform quality of the Class-E inverter. This method allows the load to dictate the power drawn from the system. However, if it is desired to control the power output of the inverter, then a variable impedance matching network is recommended.

The results of a Class-E inverter operating under a varying non-resistive load with a variable impedance matching network was also investigated. The load "seen" by the inverter is the input impedance seen at the transmitter resonator of an RC^2 WPT system when the wireless link is displaced from its original tuned position. Using variable double-L and double-T networks, constant power was achieved across the load range. During the constant power test, the measured impedances of the transmitter resonator were capacitive, and the double-T network proved to be the superior design. Based on the test results, it is expected that the range of impedance that can be transformed using the two matching networks can be further improved by adding series and shunt components. Keeping the load impedance within the range of the Smith Chart will significantly improve the matching range of the system.

6.2 Contributions of the Thesis

This work presents an overview of the solutions available to overcome the challenges of designing a highly efficient and stable Class-E inverter at multi-MHz frequencies. A harmonic analysis of the inverter was provided that shows the dominant frequencies that lead to non-ideal waveforms in the switch and output. Although Class-E inverters are widely used for many applications, typical work presented in literature is not provided for reactive loads. From Chapter 4 onwards, this work shows the effect of reactive loads on the inverter's switch voltage, output power, THD and efficiency, which are crucial for WPT.

The first important contribution of the work is the simulation study of the PFC method in Chapter 4. Although widely popular in power systems, the PFC method is applied and presented for the first time for Class-E inverters under variable non-resistive loads at multi-MHz frequencies. A thorough search of the relevant literature yielded no related articles. The topics discussed under PFC in this work will be expanded to build a load independent transmitter that accommodates reactive loads for RC^2 and IPT systems. This will be developed into a publication in the future.

The second contribution is the study of various impedance matching solutions, which adds to the body of knowledge in the area of Class-E inverters under variable non-resistive loading. While matching networks are widely used for load transformation, for the first time, the networks used in this investigation incorporates component parasitics that were determined through estimation techniques, providing a highly accurate simulation model for RC^2 WPT.

This work also led to the publication of two articles, [3] and [17]. Article [3] provides the harmonic approximation technique from Chapter 3, in addition to an overview of the different Class-E inverter topologies. To optimize the load-independent Class-E inverter, article [17] was developed, which shows an optimization method using Design of Experiments to obtain the components that give the lowest possible peak switch voltage and current for a specified power level. Designing the inverter for resistive loads using this method and applying the techniques from Chapter 4 or Chapter 5 gives a highly flexible inverter that can accommodate reactive loads while keeping the waveforms favorable.

6.3 Future Work

Throughout this work, power factor correction and variable impedance matching were used to address issues caused by non-resistive loading of a Class-E inverter. However, upon further

inspection, there may be potential to further improve the analysis done in the previous chapters. For example, simulating the PFC method showed an improvement in the switch node and efficiency of the inverter. However, in building a VAR compensator on a test board, pre-determined capacitors and inductors will need to be selected to support the load range, similar to the variable impedance matching network in Chapter 5. It will be interesting to test the performance of the PFC method with pre-selected components similar to the VIM tests done in Chapter 5. Due to time constraints, this test was not completed in the M. Eng. program. However, as mentioned before, the results from this test will be used to build a load independent transmitter that accommodates reactive loads.

For variable impedance matching, this work only examined the two networks: the variable double-L and the variable double-T. There would be great value in reducing the size of these networks to obtain a compact design. Using series components that can be varied to compensate for variable loading can be investigated. However, issues such as switching transients and overvoltage stresses will need to be addressed. This will open the possibility to use a single L or T network by dynamically adjusting both series and shunt components at each loading.

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APPENDIX A: MATCHING RANGE SCRIPT

A MATLAB script was written to determine the largest matching range possible for different inductor combinations. This is used to obtain the plots in Figure 5-8 and Figure 5-11. The script below is written for the variable double-T network and is built using (5.4) and (5.5). In each iteration, the input impedance is calculated based on the constraints applied. The values that pass this condition are stored and updated. The resistive part of the input impedance that provides the lowest error to the desired value is prioritized.

```
close all
clear all

%Set the operating frequency here. Set to 13.56MHz
w = 2*pi*13.56e6;

%% Initialize Capacitor and Inductor values.
%Cap_values contain all possible capacitance obtainable from the shunt, starts and increments by 40pF for
%numc times
%The Ind_values is an array that contains all possible inductor combinations, starts and increments by 20nH for
%numl times
Cap_values (1) = 40;
Ind_values(1) = 20;
numc = 15;
numl = 15;
Caps = [160 160 160 80 40 20];
index = 0;

for c = 2:numc
Cap_values(c) = Cap_values(c-1) + 40;
end

%Applies the parasitic capacitance from Appendix B for each Cap_values based on the # of PIN diodes that are
%off
for c1 = 1:numc
current_cap(c1) = Cap_values(c1);
for c2 = 1:6
if (current_cap(c1) - Caps(c2) >= 0)
                    current_cap(c1) = current_cap(c1) - Caps(c2);
    index = index + 1;
end
end
Cap_values_actual1(c1) = Cap_values(c1) + 2*49/6*(6-index);
Cap_values_actual2(c1) = Cap_values(c1) + 2*26/6*(6-index);
index = 0;
end
```

```
for l = 2:numl
Ind_values(l) = Ind_values(l-1) + 20;
end

Ind_values_comb = [[transpose(Ind_values) transpose(Ind_values)
transpose(Ind_values)];nchoosek(Ind_values,3)];

%Real error is how far real(zin) deviates from R
%The solution will also be within +/-Imag error that is set below
R = 15;
R_error = 1;
Imag_error = 2i;
Zin_good = 0;
Zin_good_actual = 0;
good_k1 = [ ];
good_k2 = [ ];
good_i1 = [ ];
good_i2 = [ ];

%% Set load impedances here
Zload =  [10-4i 12.7-3.3i 15-2.6i 18-1.8i 26-0.3i 31-0.2i 38-0.6i 50-2.2i 61-6i 73-13i 91-31i 102-54i];

%% Calculates best possible match with given inductance and cap values
for i=1:length(Ind_values_comb)
for z=1:length(Zload)
for k1=1:length(Cap_values)
for k2=1:length(Cap_values)
ZL = Zload(z);
L1 = Ind_values_comb(i,1)*1e-9;
L2 = Ind_values_comb(i,2)*1e-9;
L3 = Ind_values_comb(i,3)*1e-9;
C1 = Cap_values(k1)*1e-12 ;
C2 = Cap_values(k2)*1e-12 ;

Z1 = 1/(1i*w*C1);
Z2 = 1/(1i*w*C2);
Y1 = 1/Z1;
Y2 = 1/Z2;
X1 = 1i*w*L1 + 0.17;
X2 = 1i*w*L2 + 0.17;
X3 = 1i*w*L3 + 0.17;

Z2 = (X3 + ZL)/((X3 + ZL)*Y2 + 1) + X2;
Zin = Z2/(Z2*Y1 + 1) + X1;

Y1_actual = 1i*w*Cap_values_actual1(k1)*1e-12;
Y2_actual = 1i*w*Cap_values_actual2(k2)*1e-12;
Z2_actual = (X3 + ZL)/(((X3 + ZL)*Y2_actual) + 1) + X2;
Zin_actual = Z2_actual/(Z2_actual*Y1_actual + 1) + X1;

if (abs(real(Zin) - R) < R_error && abs(imag(Zin)) < abs(imag(Imag_error)))
   if (abs(real(Zin) - R) < abs(real(Zin_good) - R))
   good_k1 = k1;
   good_k2 = k2;
   good_i = i;
   Zin_good = Zin;
```

```
    Zin_good_actual = Zin_actual;
    end
end
end
end

Zin_optimized(i,z) = Zin_good;
Zin_optimized_actual(i,z) = Zin_good_actual;

C_optimized{i,z} = [{Cap_values(good_k1)},{Cap_values(good_k2)};
{Cap_values_actual1(good_k1)},{Cap_values_actual2(good_k2)}];
if(Zin_optimized(i,z) == 0)
    C_optimized{i,z} = '0';
end
Zin_good = 0;
Zin_good_actual = 0;
end
end
%% Impedance and Cap solutions
Zin_All = [[[] Zload]; Zin_optimized];
Zin_All = [ [[" "] [" "] [" "];Ind_values_comb] Zin_All];

Zin_All_actual = [[[] Zload]; Zin_optimized_actual];
Zin_All_actual = [ [[" "] [" "] [" "];Ind_values_comb] Zin_All_actual];

Zload_C = arrayfun(@num2str,Zload,'UniformOutput',false);
Ind_values_comb_C = arrayfun(@num2str,[[" "] [" "] [" "];Ind_values_comb],'UniformOutput',false);
C_All = cat(1, Zload_C, C_optimized);
C_All = cat(2, Ind_values_comb_C, C_All);
```

APPENDIX B: LSM SCRIPT FOR PARASITICS

A MATLAB script was written to determine the parasitic offset capacitance in the transmitter board.

```
%% Insert data here. For Double T:
ZL = [100 80 60 40 20];
ydata = [123+16i 120+41i 106+70i 83+99i 48+122i];

C = sym('C',[1,2]);
Z = sym('Z',[1,1]);
f = 13.56e6;
w = 2*pi*f;
L1 = 200e-9;
L2 = 200e-9;
L3 = 200e-9;

X1 = 0.17 + 1i*w*L1;
X2 = 0.17 + 1i*w*L2;
X3 = 0.17 + 1i*w*L3;
YC1 = 1i*w*(C(1)*1e-12);
YC2 = 1i*w*(C(2)*1e-12);

Z2 = (2.*X3 + ZL)./((2.*X3 + ZL).*YC2 + 1) + 2.*X2;
Zin = Z2./(Z2*YC1 + 1) + 2.*X1;

g = matlabFunction(Zin,'Vars',{C,Z})

x0 = [1,1];
size(ydata)
size(g([1,1],ZL))

%Fits data to Zin:

c = abs(lsqcurvefit(g,x0,ZL,ydata))
```