DEVELOPMENT OF A MULTI-MEGAHERTZ FREQUENCY CONVERTER FOR WIRELESS POWER APPLICATIONS

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A Thesis submitted to the School of Graduate Studies

in partial fulfillment of the requirements for the degree of

Master of Engineering

Faculty of Engineering and Applied Science

Memorial University of Newfoundland

December 2020

St. John’s, Newfoundland and Labrador

Abstract

A novel wave-shifting, frequency-reducing converter topology is developed, with the target application of capacitive wireless power transmission. The new topology combines a Class-E synchronous rectifier and Class-D inverter. Zero-voltage switching is achieved, and the converter is load-independent.

The developed converter is an AC-AC converter, which can divide the input frequency by any even whole number. The power throughput of the rectifier is less than that of the total converter, especially when the ratio of input to output frequency is small. Therefore, the wave-shifting converter has a potential advantage in efficiency over AC-DC-AC frequency reducers. The feasibility of the converter is demonstrated by simulation and experimental results. The intended application of the developed converter is to drive an isolation transformer in a capacitive wireless power rectifier. High-frequency transformers have been investigated, and it is shown that a suitable transformer is compatible with the developed converter.

Acknowledgements

Many thanks go to my supervisor Dr. John E. Quaicoe for his excellent support and technical guidance. His interest and approachability have been pivotal to my success in this Master's program.

I would like to offer sincere thanks to the staff of Solace Power for sharing their knowledge and equipment in the pursuit of this research. At Solace I have found not only a rich collection of technical expertise, but a cohesive team dedicated to advancing their scientific field.

I wish to thank the MUN School of Graduate Studies (SGS) and the Natural Sciences and Engineering Research Council (NSERC) for their generous funding, which has enabled me to give full focus to this research work.

Finally, I offer immense gratitude to my wife (and fellow graduate) Hla U May Marma for her endless patience and support. *Kee ju tang re, kremashe.*

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List of Abbreviations and Symbols

f_0	The input frequency to the wave-shifting converter.
f_L	The output frequency of the wave-shifting converter.
T_0	The input period of the wave-shifting converter.
T_L	The output period of the wave-shifting converter.
n	The frequency division factor, a positive even number.
$v_{IN}(t)$	The voltage across the input port of the wave-shifting converter.
$v_{INp}(t)$, $v_{INn}(t)$	The voltage with respect to ground at the positive and negative input terminals of the wave-shifting converter.
$v_S(t)$	The voltage across the input to the rectifier impedance-matching network, where $v_S = v_H - V_{DC}$. A high-frequency sine wave.
v_{TRIG}	The output from the trigger circuit, a logic-level square wave.
V_{pk}	The amplitude of v_S.
V_{DC}	The rectifier output voltage, nominally equal to V_{pk}.
I_{DC}	The DC component of the inverter input current.
V_M	The magnitude of the fundamental component of v_{Br}.
I_M	The magnitude of the low-frequency output current from the inverter.
$G(n)$	The inverter voltage gain. Defined as the ratio of V_M to V_{pk}.
$v_H(t)$	The voltage across the input to the inverter, a sine wave with a DC offset.
$i_H(t)$	The current at the input to the inverter.
$v_{Br}(t)$	The voltage across the output of the inverter.
$v_L(t)$	The voltage across the converter load, a low-frequency sine wave.
$i_L(t)$	The current through the converter load, a low-frequency sine wave.
$p_H(t)$	The instantaneous power flowing into the inverter.
P_H	The average real power that flows into the inverter.
$p_L(t)$	The instantaneous power delivered to the load.

P_L	The average real power delivered to the load.
P_R	The average real power that flows through the rectifier.
P_D	The average real power that flows directly from the source to the load, not through the rectifier. Assuming no losses, $P_L = P_R + P_D$.
c_p	Power capability of the complete wave-shifting converter.
c_{pR}	Power capability of the rectifier within the wave-shifting converter.
c_{pH}	Power capability of the inverter within the wave-shifting converter.
$L_2, L_3, L_4,$ C_2, C_3, C_4	The inductors and capacitors of the rectifier impedance-matching network.
L_5, C_5	The DC pass inductor and its resonant capacitor.
$L_6, L_7, L_8,$ C_7, C_8	The inductors and capacitors of the source impedance-matching network.
$L_9, L_{10},$ C_9, C_{10}	The inductors and capacitors of the output filter.
R_L	The converter load resistance.
R_{eq}	The equivalent DC resistive load seen at the rectifier output.
R_R	The resistance seen looking into the rectifier from v_S.
R_H	The resistance seen looking into the inverter from v_H, at frequency f_0.
R_D	The resistance seen looking into the inverter from v_S.
R_S	The total resistance of the converter looking from the source impedance matching network into v_S. Equal to the parallel combination of R_R and R_H.

1 Introduction

1.1 Background

Wireless power transmission (WPT) has been gaining attention for medium- and high-power applications in recent years due to demand from the electric vehicle market and advancements in high-speed semiconductors. This is a fast-growing field with new use cases appearing regularly as the technology is improved.

Wireless power has been widely researched and used in low power applications with short transmission distances, such as smartphone charging and implantable medical devices. It is particularly suitable wherever frequent plugging and unplugging occurs, or where reliability is an issue for flexible wiring harnesses. Wireless power stands to improve the convenience and reliability of many industrial and consumer applications.

Two major types of coupling are used in wireless power transmission: magnetic coupling (inductive wireless power or IPT) and electric coupling (capacitive wireless power or CPT). Thus far, inductive wireless power is more widely used, but it has several drawbacks. Among these are its effect of heating nearby metal objects, which is a problem for safety and efficiency. Another problem with IPT is the large weight of higher-powered systems resulting from the use of heavy ferrite materials. Furthermore, IPT is highly sensitive to misalignment between the transmitting and receiving coils. Both the weight and sensitivity to misalignment are particularly problematic; however, IPT is widely used in electric vehicle charging.

Capacitive wireless power is growing in popularity since it avoids the problems of IPT. A CPT coupler can be constructed from lightweight conductive foil, and is less sensitive to misalignment. Furthermore, the electric fields used by CPT do not heat metal objects. However, CPT has its own flaws such as the inherent hazards of high voltage.

A critical component of a wireless power system is the high-frequency rectifier that receives power from the wireless coupler. In an inductive system, the rectifier is galvanically isolated from the transmitter by the magnetic coupler itself. In a capacitive system, there is no such

isolation – despite the air gap, the receiver remains electrically coupled to the transmitter. What is proposed in this work is a novel high-frequency AC-AC converter that forms part of an isolated rectifier for capacitive wireless power systems.

1.2 Motivation

The motivation for this work is the need for an isolated wireless power rectifier, in which the load is galvanically isolated from the capacitive coupler. The utility of an isolated rectifier is the elimination of ground loops, and the containment of hazardous electric fields within the coupler.

1.2.1 Need for Isolation

The question arises why isolation is needed at all in a wireless power system. In an inductively coupled system, isolation is not needed since power is transferred by a magnetic field, so an applied voltage between the transmitter and receiver has no effect. The coupler itself may be thought of as an air-core isolation transformer.

In a capacitively coupled system, as targeted in this research, isolation is relevant because the energy transfer occurs electrically. The transmitter and receiver are electrically coupled, so despite the air gap there is no galvanic isolation. A voltage applied between the transmitter and receiver changes the operation of the system in several ways.

If a voltage is applied between the respective ground electrodes of the transmitter and receiver in a capacitive system, the operating voltage will be superimposed on that voltage. In that case, the peak electric field strength within the coupler will be greater than it otherwise would be. Greater electric field strength means an increased risk of arcing (dielectric breakdown between the transmitter and receiver electrodes). It also means potentially greater dielectric losses in the transmission medium.

To achieve electromagnetic compatibility and to ensure the safety of nearby persons, the fields must be contained within the coupler. In a capacitive system, this typically means that the live electrodes are shielded by ground electrodes. Power is transmitted through high electric fields between the live electrodes, while the ground electrodes form a “bubble” of low voltage that minimizes the radiated energy and the region of hazardous electric fields.

Considering the safe limits of human exposure to electric fields, a voltage applied between the transmitter and receiver in a high-power system would change the size and shape of the hazardous fields around the coupler. At 27.12 MHz, the safe limits for controlled and uncontrolled exposure to electric fields are 67.9 V/m and 30.4 V/m respectively; and at 30-300 MHz the safe limits for controlled and uncontrolled exposure are 61.4 V/m and 27.5 V/m respectively [1]. Therefore, the safety of personnel cannot be guaranteed in the vicinity of a wireless power system that operates near these limits if the rectifier is not isolated.

1.2.2 Need for Multi-Megahertz Frequency Converter

The power throughput in a loosely coupled capacitive wireless power system is proportional to the operating frequency [2]. To achieve high efficiency and power density, wireless power technology pushes for higher frequency in the tens of megahertz, which is limited mainly by the capability of existing power electronics. Meanwhile, current power transformer technology is limited to lower frequency on the order of one megahertz or less, to minimize losses and parasitic effects. The main challenge in implementing an isolation transformer in a wireless power system is this disparity in operating frequencies. This leads to the notion of a frequency changer to get the best performance from both components – a high-frequency transmitter/receiver, and a low-frequency isolation transformer. The expectation is that combining these will produce a system with high power throughput and high efficiency.

1.3 Objective of the Research

The objective of this research is to investigate a novel design for a wireless power isolated rectifier. Whereas a solution may be realized using existing technology in a rectifier/isolated DC-DC topology, there is interest to discover whether an AC-AC/transformer/rectifier topology is technically feasible or advantageous.

The research is targeted at capacitively-coupled wireless power systems in the 10-100 W range. Inductively-coupled systems are inherently isolated, and therefore do not require isolation in the receiver. Furthermore, lower-powered systems have less need for isolation due to their typically lower operating voltages and harmless field strength.

1.4 Thesis Organization

The remaining chapters of this thesis are arranged as follows:

Chapter 2 contains the literature review. The technologies that contribute to the proposed converter are examined, including resonant rectifiers, frequency converters, and high-frequency transformers. The limitations of these at higher frequencies are established.

Chapter 3 presents the wave-shifting converter topology in general terms. It describes the function of each part and explains the design procedure followed to implement the converter.

Chapter 4 shows the development of a wave-shifting converter for 27.12 MHz input and 1.695 MHz output. The design procedure, simulation results and experimental results are presented and analyzed.

The proposed wave-shifting converter is analyzed in Chapter 5, to illuminate the expected performance of the circuit. The power capability, input impedance and other parameters are determined as functions of the converter load and frequency division factor. Modifications and improvements to the converter are also proposed in this chapter – the modified converter is not part of the analysis proper, but is derived from the 27.12 MHz converter in the previous chapter.

In Chapter 5.8, it is shown that the wave-shifting converter is adaptable to higher frequencies. A 40.68 MHz simulation model is developed using models of real GaNFET switches. The performance of the 40.68 MHz model is compared to the expected values based on the analysis in Chapter 5.

Finally, Chapter 5.9 discusses the high-frequency transformer that is part of the isolated WPT rectifier. The parasitic phenomena affecting the operation of a transformer at megahertz frequencies are discussed. An experimental power transformer is constructed and analyzed in the context of the wave-shifting converter.

Chapter 7 concludes the thesis, summarizing the contributions. Future work that could be undertaken to further develop the wave-shifting converter is discussed.

2 Literature Review

The converter developed in this work relies on components that have been investigated previously. These components include the wireless power resonator, the synchronous resonant rectifier, the inverter, and the high-frequency power transformer. Existing work in the field is covered in this chapter, including converter topologies that perform the same task at lower frequency.

2.1 Resonant Rectifiers

Many topologies of resonant rectifiers exist, which achieve various performance characteristics and compatibility with other circuits. These are distinguished from non-resonant rectifiers by the fact that energy is stored in a resonant capacitor-inductor pair, which oscillates at (or near) the operating frequency of the circuit.

2.1.1 Class-E Rectifier Topologies

The Class-E resonant rectifier is favoured for its efficient switching and low electromagnetic emissions [3], and low component count. Many variations on the Class-E topology exist, some of which are better-suited to certain applications than others. An important distinction between the different types is whether they are voltage-driven or current-driven. Examples of both are shown in Figure 2.1 [3]. For a capacitively-coupled wireless power system, voltage-drive rectifiers are preferred because the capacitive coupler is characterised by its operating voltage. Moreover, the voltage on the coupler determines the strength of the field that it produces.

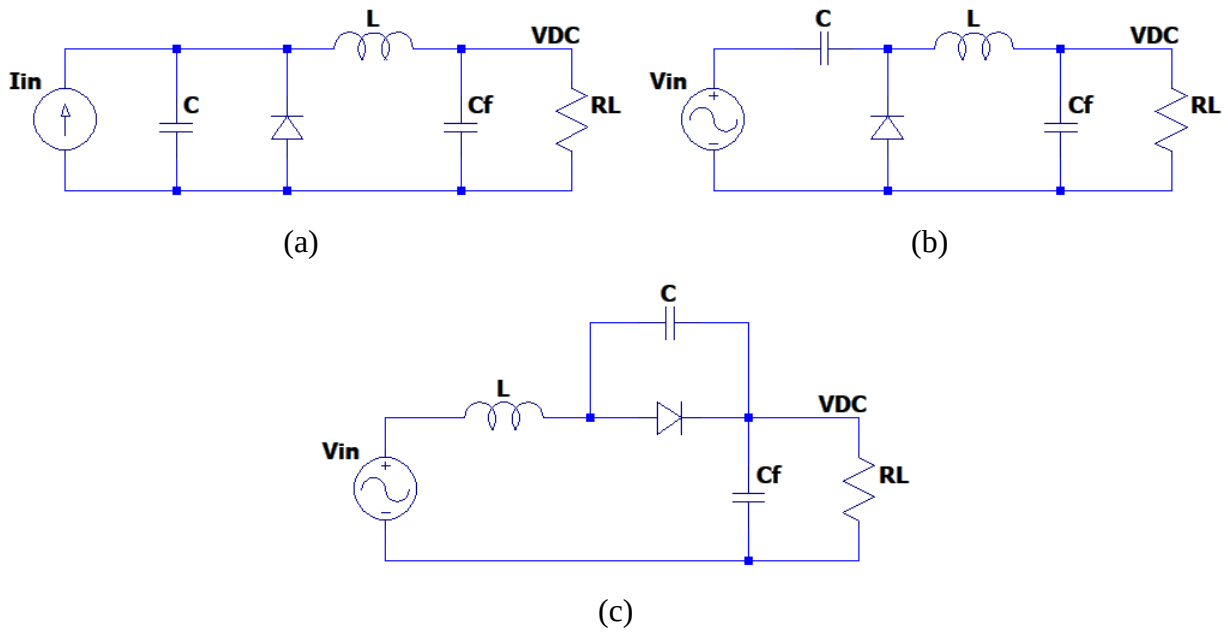


Figure 2.1: Class-E rectifier topologies. a) Current-driven rectifier; b) Voltage-driven rectifier with series capacitor; c) Voltage-driven rectifier with series inductor.

A further distinction between Class-E rectifier topologies is whether the DC load current flows through the supply. It is clear that no DC current flows at the input of the voltage-driven rectifier of Figure 2.1 (b), since it has a series capacitor. However, the rectified load current does flow through the supply of the rectifier in Figure 2.1 (c). The circuit of Figure 2.1 (b) is more suitable for CPT systems, since a capacitive coupler cannot pass DC current.

2.1.2 Class-EF Rectifier

The Class-EF resonant rectifier adds an extra resonant LC pair to the Class-E topology to improve its switching characteristics (see Figure 2.2). Compared to the Class-E rectifier, the Class-EF achieves lower peak switch voltage and current, and therefore has a higher power capability [4]. The extra LC pair has a resonant frequency that is higher than the operating frequency, which adds a frequency component to the switch voltage waveform that cancels the peak present in the Class-E rectifier. The Class-EF rectifier retains the zero-voltage and zero-voltage-derivative switching characteristic of the class-E rectifier, and can be designed to be load independent as proven in [4].

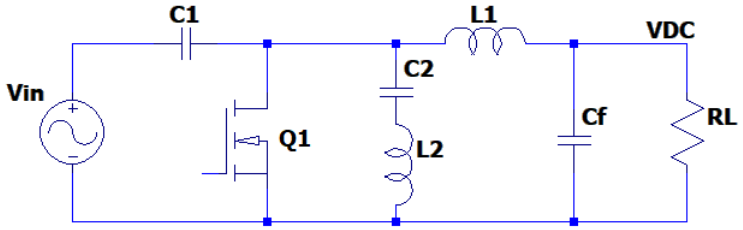


Figure 2.2: Class-EF rectifier topology.

2.1.3 Zero-Voltage Switching

As a semiconductor switch transitions between the on and off states, it spends a finite amount of time in the linear region during which it dissipates power resistively. At high switching frequencies in the tens of megahertz, these switching power losses are a significant concern for system efficiency and thermal management [5].

A solution to minimize switching losses is to implement zero-voltage switching (or soft switching). In a resonant circuit, reactive components are used to shape the switch voltage or current waveform such that the product of voltage and current in the switch is minimized at the switching instant.

It is shown in [4] that without specific design consideration, the conventional Class-E and Class-EF rectifiers achieve ZVS only at nominal load. It is shown in [4] that a more robust and useful implementation is possible by reducing the output inductor to shape the switch node voltage.

An alternative approach to reduce switching stresses is the use of a dissipative RC snubber circuit to absorb the voltage and current spikes that occur during hard switching. However, the RC snubber only moves the power loss from the switch to the resistor, so it does not improve efficiency, and does little to alleviate thermal concerns [5].

2.1.4 Synchronous Rectifiers

In the traditional passive (diode) rectifier, there is a lower limit on the conduction loss that can be achieved due to the forward voltage drop that is inherent in all diodes. A voltage drop between 0.6 and 1.0 V is typical for standard diodes, and as low as 0.3 V for Schottky diodes. The forward voltage drop dissipates power whenever the diode is conducting, and the forward

voltage is relatively unaffected by current – therefore the power loss is proportional to the diode current [5].

In a synchronous rectifier, the diode is replaced by an active switch. Instead of a fixed forward voltage, active switches such as GaNFETs exhibit a fixed on-resistance, which is typically in the range of 10 to 100 mΩ. At moderate switch currents (approximately 5 A or greater), active switches outperform diodes in conduction losses. Synchronous rectifiers offer improvements in efficiency and thus maximum power due to the reduced need for thermal management [5].

The main drawback of the synchronous rectifier is increased complexity. Whereas a diode is a passive device that conducts automatically in response to the applied voltage, the active switch requires a gate driver and a triggering circuit to turn it on at the correct moment. At the system level, the triggering logic and gate drive losses reduce the total efficiency.

The function of the triggering circuit in a synchronous rectifier is to derive a digital gate drive signal for the synchronous switch, such that it conducts at the correct time during each cycle. With an operating frequency in the tens of megahertz, propagation delay through the signal processing components is a significant obstacle which makes it infeasible to simply trigger the switch according to the voltage across it (as is inherently done by a passive diode). Instead, the trigger signal may be sampled from other nodes in the circuit preceding the rectifier. This approach proves challenging in practice, since the phase, amplitude and zero-crossings of the voltage waveforms may be inconsistent as the rectifier load and supply voltage are varied.

An alternate approach relies on a phase-locked loop (PLL) to generate the gate drive signal. The digital output signal from the PLL is a square wave with the desired duty cycle. Closed-loop control is used to maintain synchronization between a variable oscillator and the rectifier switch voltage. A phase-locked loop is used to drive a synchronous rectifier in a 190 kHz inductive wireless power system in [6]. Another PLL is used in a synchronous rectifier operating at 1 MHz in [7].

The known difficulties of using a PLL are the locking time and the RMS jitter [7]. Compared to a voltage-comparator trigger circuit, the PLL takes longer to settle into phase with the rectifier, since it takes multiple cycles to lock onto the rectifier phase (as compared to a voltage

comparator, which starts instantly). The locking time of the PLL in [7] is reported as 8 μs, or 8 cycles at 1 MHz. Jitter refers to the cycle-to-cycle phase variation, or "phase noise" of the signal. The synchronous rectifier of [7] reports a PLL with an RMS jitter of 8 ns at 1 MHz, which performs adequately in a ZVS synchronous rectifier so as not to degrade performance. Thus, although it requires precise tuning to achieve good performance, the phase-locked loop is a robust triggering solution.

2.1.5 Load-Independent Class-E Rectifier

Whereas typical synchronous rectifiers lose ZVS as the load is varied, in [7] a load-independent synchronous rectifier is proposed. On its own, the load-independent rectifier is a significant improvement on the Class-E topology. It is also an important component of the wave-shifting converter developed in this work.

As shown later in the analysis of the converter, the equivalent load on the rectifier differs from the load at the converter output. Also, the insertion of an isolation transformer at the output produces a different image impedance that is not easily controllable. As such, the load-independent rectifier is needed to accommodate the variations in equivalent rectifier load from other parts of the system.

2.2 Frequency Converters

Multiple methods exist for changing the frequency of AC power, to adapt between systems with different operating frequencies. Most of these target line-frequency applications such as traction motors or centrifuges.

2.2.1 Matrix Converter

The single-phase matrix converter proposed by Zuckerberger, et al. [8] doubles the 15 Hz input frequency in a traction application, thereby reducing transformer size. The input voltage passes directly into an active full bridge, where it is selectively inverted using PWM. This scheme requires a switching frequency much higher than the input fundamental to minimize the size of the filter components. Due to the low operating frequency, a high switching frequency is no obstacle.

A similar scheme is used by Ahmed et al. [9] to lower the frequency by a factor of 2, by changing the polarity of the input in each cycle (see Figure 2.3). This arrangement only requires a switching frequency on the order of the input frequency, which makes it appealing for operation at RF. However, the switching occurs when the voltage slew rate is at its maximum, requiring extremely fast toggling as the frequency increases. This approach is related to the converter developed in this work, but here measures are taken to eliminate the voltage derivative.

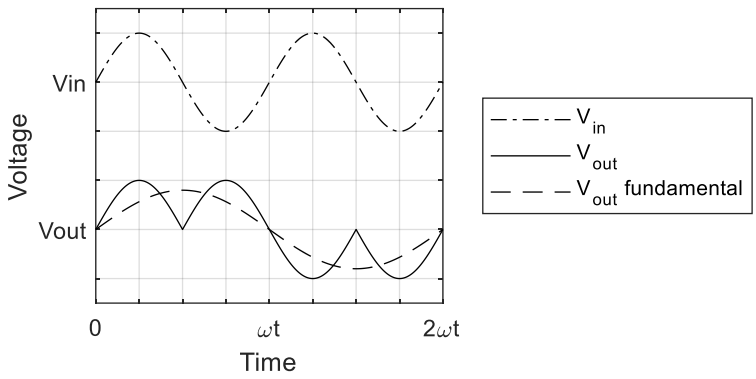


Figure 2.3: Frequency reduction by changing polarity during each cycle.

A three-phase system is used in [10] to boost the frequency of a generator up to 360 Hz for transmission, with a switching frequency of 960 Hz. Three-phase has the advantage of being able to construct the output from multiple different input voltages; however, for now three-phase systems in wireless power transfer are not the norm. Moreover, this system is not compatible with zero-voltage switching.

2.2.2 Limitations of Existing Frequency Converters for RF Applications

Existing frequency converters which operate at line frequency are fundamentally unsuitable for operation at radio frequency. One reason for this is that all existing designs have either hard switching at non-zero voltage, or switching at non-zero voltage derivative. Another reason is that existing designs often rely upon a switching frequency that is higher than the operating frequency. The operating frequency is defined as the frequency that carries the power, whereas the switching frequency is the rate at which the switching occurs.

To maintain adequate efficiency and low operating temperatures, RF switching converters must make use of zero-voltage switching. They must also have a switching frequency that is not significantly higher than the operating frequency.

The converter of [9] switches at the zero-crossings of the input sine wave. While this does satisfy the need for zero-voltage switching, the switching occurs at the maximum voltage derivative. The voltage slew rate at the zero crossings of a waveform of amplitude V_{pk} and frequency f is given by Equation (2.1).

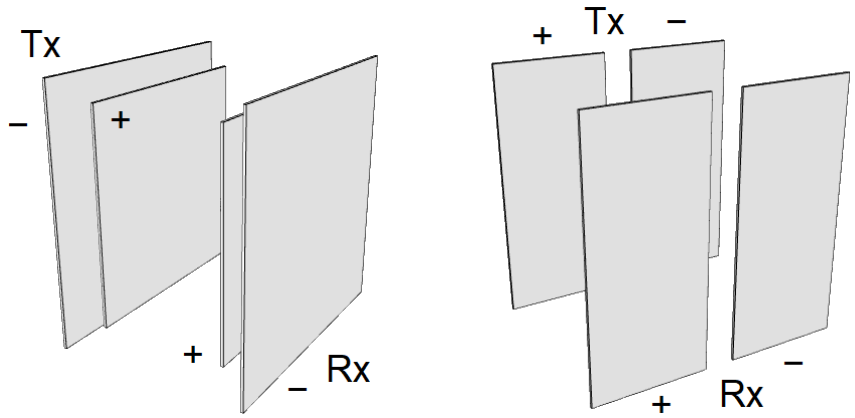
$$\left.\frac{dv}{dt}\right|_{v=0} = V_{pk} 2\pi f \tag{2.1}$$

For example, in a system with input frequency f = 27.12 MHz and V_{pk} = 50 V, the slew rate is 8520 V/µs. Considering a gate driver that can toggle within 3 ns (such as Texas Instruments LMG1210), the voltage will change by 25.6 V during the switching. Therefore, zero-voltage switching at the zero-crossings of a sinusoidal RF voltage waveform is unfeasible.

2.3 Capacitive Wireless Power Resonators

The set of transmitter and receiver electrodes, together with their resonant inductors in a capacitive wireless power system is referred to as the resonator. A basic resonator has four electrodes or plates. Six capacitances can be measured in the four-plate coupler, between each unique pair of plates. The greatest of these capacitances will be between facing pairs of transmitter and receiver electrodes, and it is through these capacitances that power flows [2].

There are two common configurations of four plates: a vertical stack of two outer plates and two inner plates (column arrangement), or an array of two equal pairs each lying in a plane (row arrangement) [11]. These are shown in Figure 2.4, with “Tx” and “Rx” indicating the transmitting and receiving electrode pairs, respectively. The column-arrangement coupler has the advantage of low emissions since it is bounded by two ground plates [12]. However, in practice it is more difficult to tune since it is electrically asymmetrical, i.e. the capacitance seen between inner plates is different from the capacitance seen between outer plates. The row-arrangement coupler has the opposite characteristics: electrically it is symmetrical, but it suffers from high electric field emissions due to the exposed outer surfaces of the electrodes [2].



(a) (b)

Figure 2.4: Four-plate capacitive coupler structures. a) Column arrangement; b) Row arrangement.

Practical resonators for higher power need shielding to limit harmful electric fields in the vicinity. A more practical coupler has six plates, and combines the best features of both four-plate designs mentioned above (see Figure 2.5). Whereas the four-plate couplers are defined by six capacitances, the six-plate coupler has fifteen. The six-plate coupler described in [2] has four smaller live electrodes enclosed by two larger ground electrodes. The live electrodes form a balanced structure, which also has benefits for the power electronics that drive the circuit, since the power can be shared between two phases.

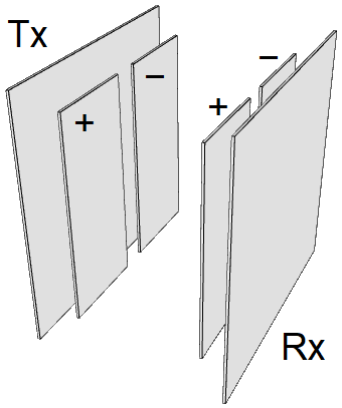


Figure 2.5: Six-plate capacitive coupler structure.

2.4 High-Frequency Transformers

The operation of an isolation transformer at high frequency is not significantly different from low frequency, however the design is largely driven by the need to mitigate parasitic effects.

2.4.1 Geometry

In [13], the design forces on traditional E-core transformers and modern planar transformers are considered as the frequency is increased, and the ratio of AC resistance to DC resistance F_R is measured. It is noted that the transformer is the limiting component for operating frequency in many power supplies, and indeed so is the case for the isolated rectifier proposed in this work.

It is determined by Evans and Heffernan in [13] that an E-core transformer is inadequate for operation at Megahertz frequencies due to core material and shape. As the frequency increases, it is necessary to minimize the winding layers and lengthen the core. The result is a long spindle-like transformer having a relatively large-volume core, and windings constructed from thin sheets of foil on the order of 0.1 mm.

It has also been shown that planar transformers, in spite of their convenient construction, are problematic due to the large leakage flux in the axial direction which is incident on the face of thin foil windings. The result is large eddy current losses in the conductors [13].

Minimizing the leakage flux between primary and secondary windings is essential to minimize eddy current losses. A manufacturing technique for a toroidal-core transformer with interleaved windings that eliminates leakage flux and the proximity effect between adjacent conductors is proposed in [13]. The manufacturing technique can be used to implement transformers of arbitrary winding ratios, but for a one-to-one isolation transformer the lessons can be applied in a simple wire-wound construction.

The ratio F_R for an interleaved toroidal transformer is about 1.5 at 1 MHz, but increases exponentially to 4 at 10 MHz and beyond [13]. Due to the increased losses, power transformers are only suitable for operation at an order of magnitude or more below the operating frequency of modern wireless power systems. This is the basis of the need for frequency reduction in an isolated rectifier.

2.4.2 Parasitic Effects

Practical power transformers suffer from parasitic effects which reduce their performance. Some parasitic effects are present at any frequency, including winding resistance, core losses and leakage flux. Others become relevant only at Megahertz frequencies, such as inter-winding capacitance and the proximity effect. Parasitic effects relevant to transformers operating at Megahertz frequencies are discussed in this section.

2.4.2.1 Winding Resistance

The basic property of wire resistance is responsible for losses in the transformer, which is proportional to the square of the winding current. At low frequencies, this loss is independent of the operating frequency, but at Megahertz frequencies it is exacerbated by the skin effect and proximity effect, which reduce the effective cross-sectional area of the wire.

2.4.2.2 Skin Effect

The skin effect causes the current in a conductor to become concentrated near the surface in response to a magnetic field within the conductor, caused by the current itself.

As an example, the skin depth of copper at 1 MHz is 65 µm, so the effective cross-sectional area of a 20 AWG copper wire at 1 MHz is only 30% of the DC area.

2.4.2.3 Proximity Effect

The proximity effect, like the skin effect, causes the current in a conductor to become concentrated in response to other conductors carrying the same current. Like the skin effect, it is the result of local electromagnetic fields in the vicinity of a conductor [14].

For conductors carrying current in the same direction, as in the turns of a transformer winding, the current becomes concentrated at the outer edges of the conductors (where they are farthest from each other). For conductors carrying current in opposite directions, the current becomes concentrated at the inner edges (where the surfaces of the two conductors are closest) [15].

Litz wire can eliminate skin effect losses by using many individually-insulated strands to make up a single conductor. However, the proximity effect causes the majority of the current to be

carried at the surface of the overall bundle. In extreme cases, reverse current may flow at the center of the bundle as demonstrated in [16].

2.4.2.4 Leakage Inductance

Leakage inductance is the portion of the magnetic field generated by each winding that does not couple to the other winding. The leakage flux contributes to eddy current losses and core losses, but does not transfer power through the transformer.

2.4.2.5 Inter-Winding Capacitance

Capacitance between the primary and secondary windings is especially relevant for the isolation transformer in this work.

2.4.3 Construction Techniques

The parasitic effects discussed in the previous section can be combatted by strategic construction of the transformer. In addition to material selection, the core shape, winding arrangement and proportions of the transformer all contribute to its high-frequency performance.

2.4.3.1 Coaxial Transformer

In the high-frequency coaxial transformer (HFCT) structure, the primary winding forms a concentric layer that encloses the secondary winding. The windings may have one or more turns, and in the case of a unity turns ratio both windings may be constructed from a generic coaxial cable [17]. The use of coaxial windings is effective in eliminating leakage flux in an HFCT [18].

The core of a HFCT is often constructed from two adjacent stacks of ferrite toroidal cores. The windings form rectangular loops passing through the centers of the toroids [15]. For transformers with complex winding arrangements, the windings are constructed from straight wire segments that are terminated at printed circuit boards at either end of the core [18].

The HFCT is a desirable structure for operation between 0.3 and 1.0 MHz as demonstrated in [16] and [18]. Since it is practical to construct from common materials, it supports the inclusion of Faraday shielding, and it has low leakage flux.

2.4.3.2 Interleaved Windings

To prevent the effect of leakage inductance from accumulating between adjacent turns of a winding, the primary and secondary windings can be interleaved. By alternating turns of the primary and secondary on the same winding layer, the magnetic flux paths that encircle one winding and not the other are minimized [13]. Compared with the non-interleaved transformer, a larger proportion of the magnetic flux will flow around both primary and secondary, thus achieving high magnetic coupling.

2.4.3.3 Faraday Shielding

Inter-winding capacitance can couple high-frequency energy through the transformer, resulting in common-mode problems [15]. One method of reducing this parasitic coupling is the insertion of a grounded conductive shield between the two windings [18]. The shield eliminates capacitive coupling between the primary and secondary windings, thus improving the transformer's electromagnetic compatibility.

In the coaxial transformer, Faraday shielding contributes only a small amount to eddy current losses since the shield conductor lies parallel to the magnetic flux lines [18]. However, depending on the form of the windings, a Faraday shield may be impractical to implement.

2.5 Summary

In this chapter, it has been established that to implement galvanic isolation in a WPT rectifier, a suitable high-frequency transformer is needed. Existing power transformers are limited to an operating frequency of about 1 MHz, which is an order of magnitude below the operating frequencies of modern WPT systems. A multi-megahertz frequency converter is needed to interface one to the other.

Existing frequency converters have been reviewed, which reveals that most designs target line-frequency applications. These are fundamentally unsuitable for multi-megahertz operation due to relatively high switching frequencies or high voltage slew rates at the switching instants.

Synchronous resonant rectifier topologies have been investigated because a load-independent resonant rectifier is a component of the converter proposed in this work. The concerns affecting the rectifier apply equally to the proposed converter.

The concerns of power transformer operation at megahertz frequencies have been discussed. The parasitic effects that lead to power loss have been identified, along with construction techniques that can minimize those effects. High-frequency building techniques are needed to achieve the best performance and small transformer size for a given power level.

3 Development of the Wave-Shifting Converter Topology

The wave-shifting converter proposed in this thesis is a novel topology for reducing the frequency of a multi-megahertz AC voltage. It was originally conceived as an adaptation to RF of the line-frequency matrix converter. The output frequency equals the input frequency divided by an even number (n = 2, 4, 6…). The converter consists of a synchronous rectifier and a full-bridge inverter. Both the rectifier and inverter achieve zero-voltage switching, furthermore the inverter achieves zero-voltage-derivative switching. A simplified block diagram of the converter is shown in Figure 3.1, where RF indicates the high-frequency input and LF indicates the low-frequency output.

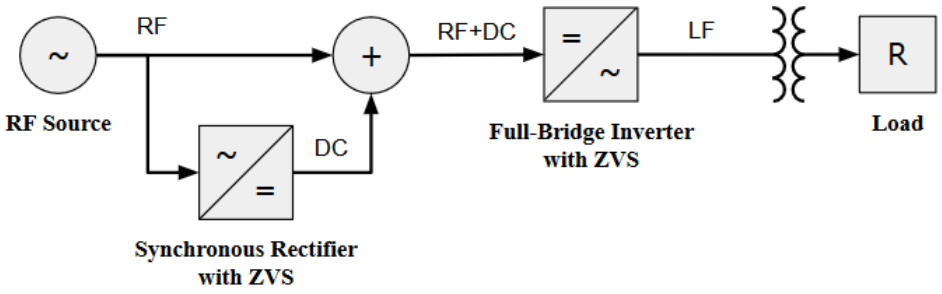


Figure 3.1: Simplified block diagram of the proposed converter.

The wave-shifting converter is a component of a complete isolated RF rectifier. The traditional implementation of an isolated RF rectifier is to rectify the input RF waveform to DC using either a passive or synchronous rectifier, then to cascade with an isolated DC-DC converter. The isolated DC-DC converter typically consists of a lower-frequency inverter (between 100 kHz and 1 MHz), a transformer, and a rectifier. The wave-shifting converter integrates the RF rectifier and inverter into a single stage, which is loaded with a transformer and lower-frequency rectifier, which connects to the load. In this work, the lower-frequency rectifier is not considered, because low-frequency rectification is a solved problem.

3.1 Principle of Operation

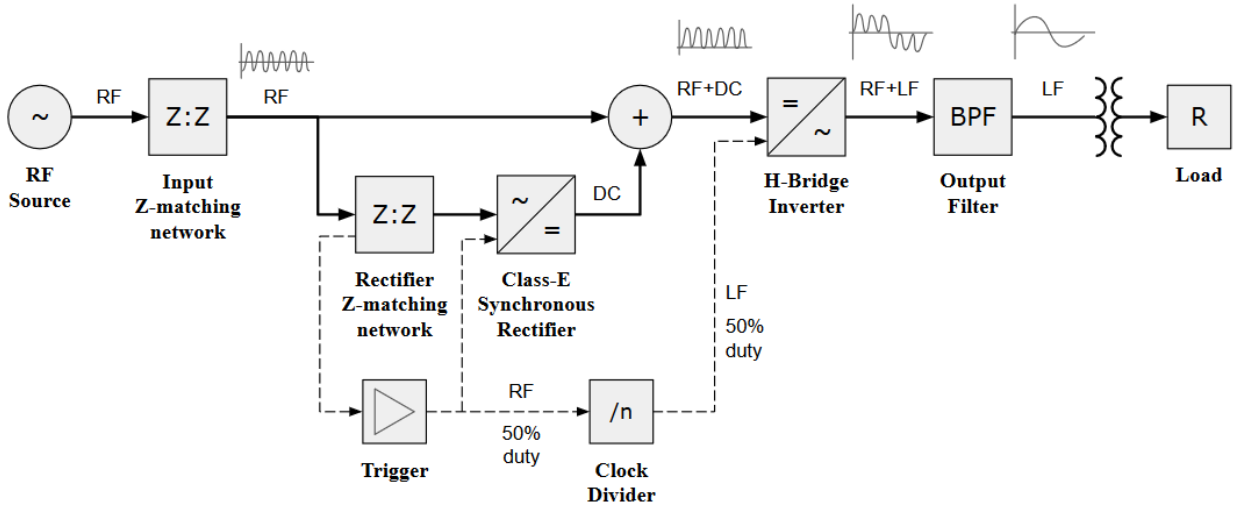


Figure 3.2: Block diagram of the proposed wave-shifting converter.

The complete block diagram of the proposed wave-shifting converter is shown in Figure 3.2, along with some sample voltage waveforms shown for clarity. The power path is shown by solid arrows, and signals are shown by dashed arrows. The circuit schematic of the power path is shown in Figure 3.3 on page 21. Starting from the left side of Figure 3.2, a high-frequency voltage source is coupled to the converter by a passive impedance-matching network. The RF source is presumed to be a capacitive wireless power receiver. From there, the power is split into two branches. The lower branch passes through another impedance-matching network and is then rectified to DC. The upper branch voltage (a high-frequency sine wave) and the DC voltage are added together in series to create the "shifted wave", represented by the sum operation at the center of the diagram. It is important that the DC voltage is equal to the peak voltage of the sine wave, because this produces a wave with its valleys at 0 V. The purpose of the shifted wave is to create instants of zero voltage and zero voltage derivative, that are suitable for soft switching in the inverter. The shifted wave enters the full-bridge inverter, which toggles at the output frequency. The inverted waveform is filtered to produce a clean low-frequency sine wave. The low-frequency power passes through an isolation transformer and finally arrives at the load.

Both the rectifier and inverter have synchronous switches, which are driven by a trigger signal derived from the rectifier impedance matching network. The trigger signal has a frequency equal

to the input, whereas the inverter requires a low-frequency trigger signal. This is achieved by a digital clock divider inserted between the trigger circuit and the inverter gate drivers.

Practically, the summation of voltages is implemented by connecting the negative input terminal of the RF source v_{INn} to the DC rectifier output V_{DC}. The connection is shown in the schematic of Figure 3.3 (b). This results in a difference in ground potential between the high-frequency input and the low-frequency output. This difference in ground references within the circuit is acceptable because the converter is intended for use with an isolation transformer, which makes the ground potential difference irrelevant. The upshot is that the required shifted wave is created, and the rectifier, trigger circuit and inverter all share a common ground.

In order for the converter to achieve ZVS as intended, the rectifier DC output must equal the peak AC voltage that is input to the sum operator. This is achieved passively by the rectifier impedance-matching network. This network is composed of two back-to-back LCL impedance inverters and has the effect of multiplying the impedance seen at the input to the rectifier by a constant factor. Whereas the rectifier is load independent, the DC voltage is proportional to the amplitude of the rectifier input voltage. Thus, the DC voltage varies proportionately to the peak voltage at the input to the sum operation. The rectifier impedance matching network is designed so that these voltages are equal, even as the load resistance and supply voltage are varied.

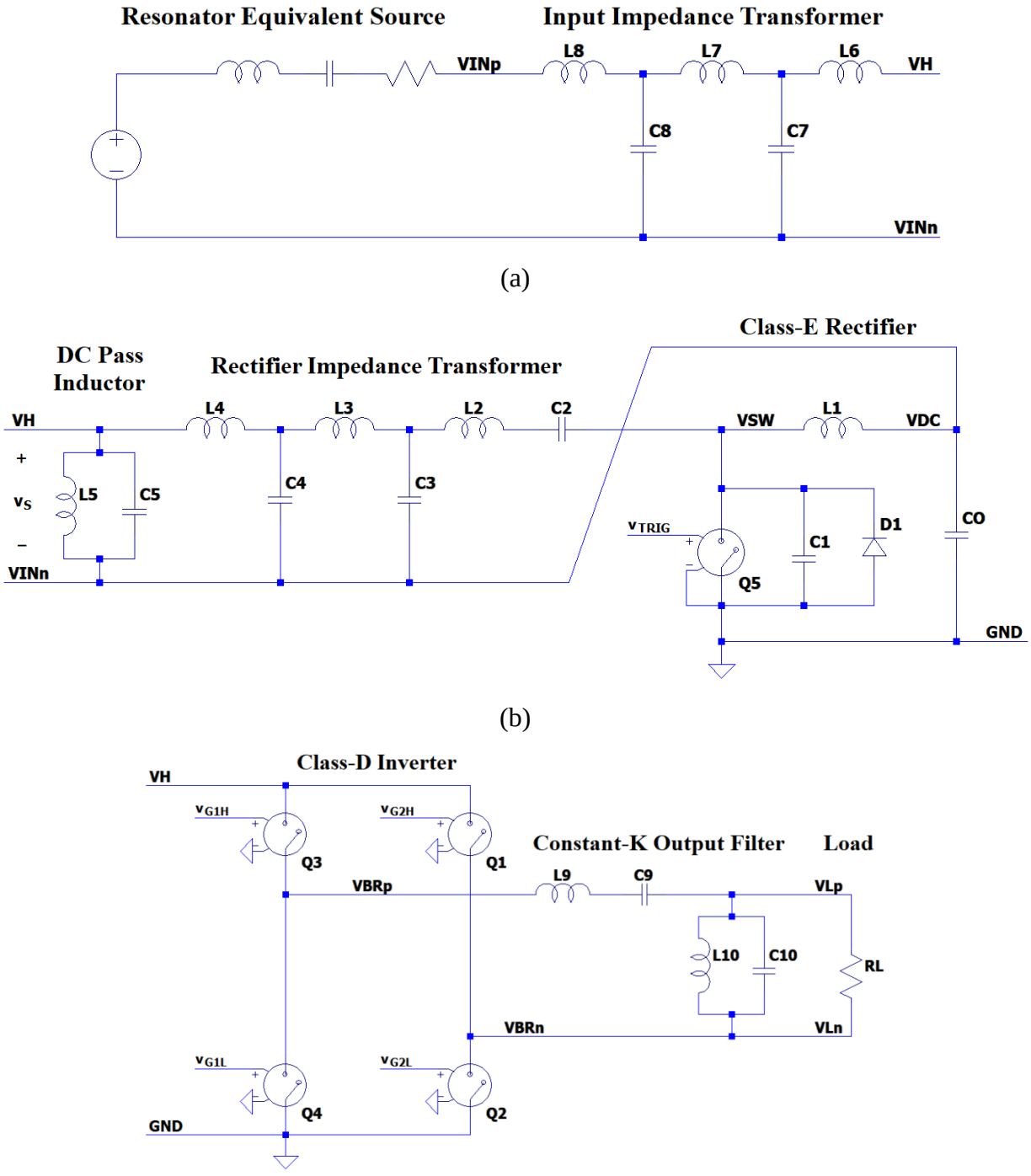


Figure 3.3: Schematic diagram of the wave-shifting converter. a) Source and input impedance transformer; b) Rectifier and rectifier impedance transformer; c) Inverter and output filter.

3.2 Trigger Circuit

The trigger circuit used in the proposed wave-shifting converter is a simple voltage comparator design shown in Figure 3.4 (a). The voltage at the circuit node between L_2 and L_3 (v_{L23}) is sampled and compared to a reference voltage (V_{REF}) by an analog comparator. V_{REF} is selected such that the duty cycle of the comparator output is 50%. A digital logic buffer converts the comparator output to a clean square wave of 0-5 V. The square wave is passed through an adjustable RC delay for tuning, and from there it is distributed to the rectifier gate driver and inverter clock divider in Figure 3.4 (b).

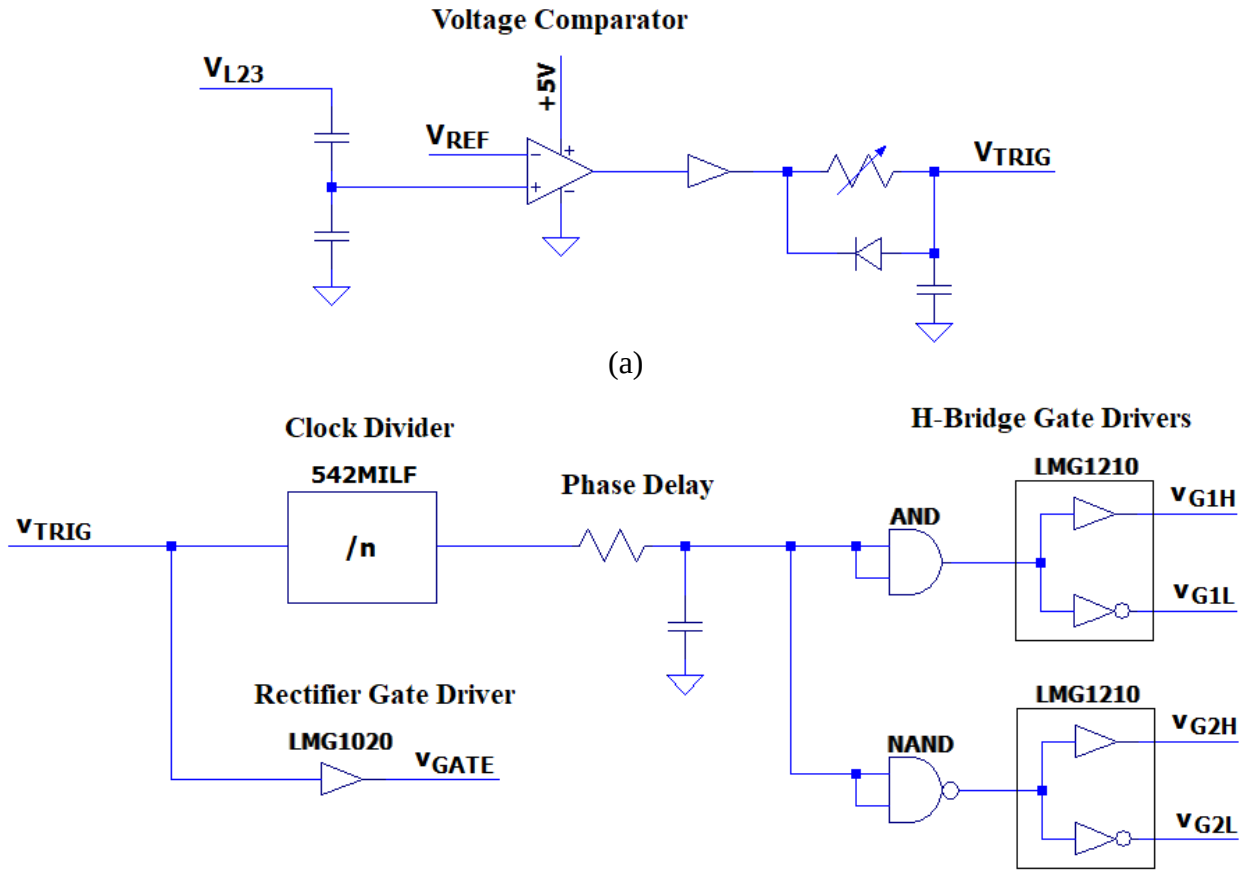


Figure 3.4: Simplified synchronous rectifier trigger circuit. a) Voltage comparator trigger; b) Clock divider and gate drivers.

The wave-shifting converter features a Class-E load-independent synchronous rectifier and a Class-D full-bridge inverter. Both the rectifier and inverter are driven by a single trigger circuit –

the rectifier clock is taken directly from the trigger output v_{TRIG}, while the lower-frequency inverter clock is derived by a digital clock divider (see Figure 3.4 (b)). In the experimental converter, a clock division factor of n = 16 was chosen for ease of implementation; however, any even integer can be used. The relationship between the output frequency (f_L) and the input RF (f_o) is expressed in terms of n in Equation (3.1).

$$f_L = {}^{f_0}/_{n} \tag{3.1}$$

The switching of the inverter occurs in phase with the valleys of the input voltage waveform. Propagation delay between the inverter clock and gate driver output is compensated by an RC delay network. Complimentary clock signals for the positive and negative half-bridge drivers are derived by passing the clock signal through logical AND and NAND gates having equal propagation delays.

The inverter switches are driven by two LMG1210 half-bridge gate drivers. The shoot-through condition is prevented by a built-in programmable dead time between one switch turning off and the other turning on. The gate signals v_{G1H}, v_{G1L}, v_{G2H}, and v_{G2L} for the inverter switches are created by the LMG1210 drivers.

A timing diagram of the important waveforms is shown in Figure 3.5. The phase of the rectifier gate signal v_{GATE} is such that the rising edges coincide with the positive zero-crossings of the input voltage v_S. However, the inverter switching occurs in the valleys of v_H. Therefore, assuming ideal logic elements with no propagation delay, the low frequency clock requires a phase delay of three quarters of the input period T_0.

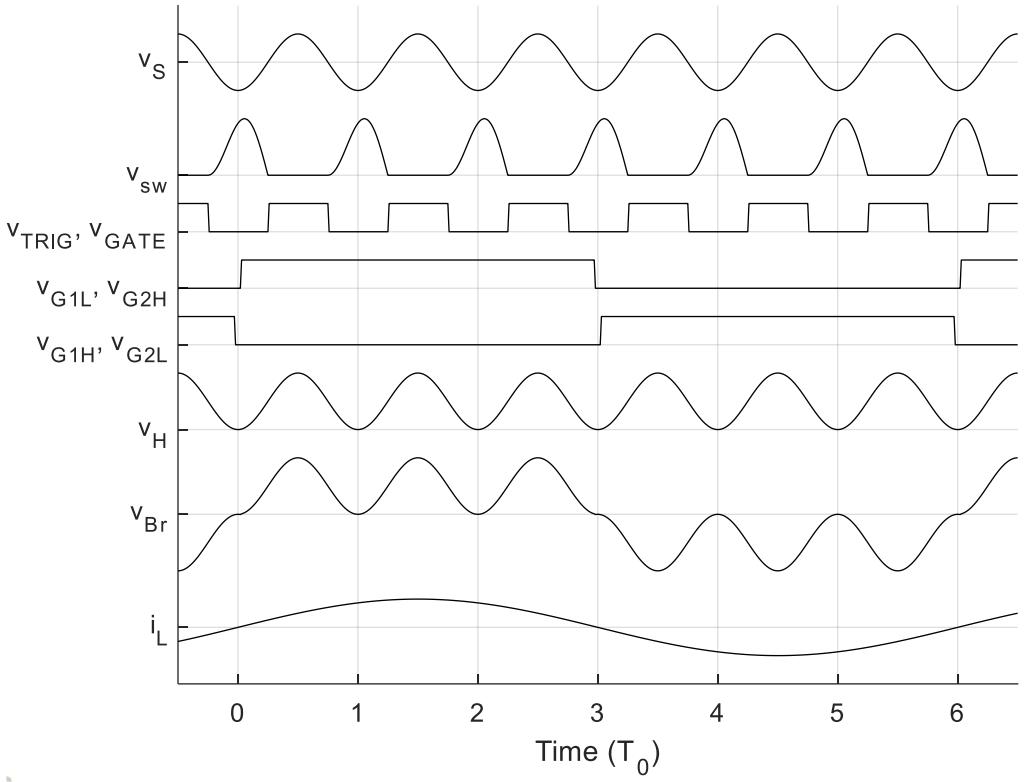


Figure 3.5: Timing diagram of main waveforms for n = 6 (vertical axis not to scale).

3.3 Design of the Wave-Shifting Converter

This section describes the design process for the general wave-shifting (WS) converter.

3.3.1 Load-Independent Class-E Rectifier

The first step in the development of the wave-shifting converter is the design of a load-independent Class-E resonant rectifier. The design equations for the rectifier are taken from [19] and augmented by the load-independent criteria established in [4].

The rectifier design requires a real switch to be selected. In practice, GaNFET transistors are used because they support multi-megahertz switching frequencies. The rectifier is designed with a constant capacitance C_1 (which absorbs the output capacitance of the switch and the diode parasitic capacitance). However, the output capacitance (C_{OSS}) of a real switch is voltage dependent. Moreover, C_{OSS} tends to be higher for switches with higher voltage and current ratings. It is convenient to simulate the rectifier using an ideal switch initially, then change to a

real device model once a suitable GaNFET has been selected. When selecting a GaNFET, one with an output capacitance somewhat less than the nominal C_1 should be chosen to ensure consistent behaviour across the entire operating voltage range. The difference between the design value of C_1 and the average value of C_{OSS} for the chosen GaNFET is made up by fixed capacitors.

The rectifier alone is simulated with nominal component values, as shown in Figure 3.6. (Resistor R_2 is included only to allow current measurement through the switch.) While accurate simulation models are needed for the switches, ideal models are adequate for the passive components [20]. At this stage, the standard voltage-driven topology is used in which the input and output share a ground reference. The circuit will be rearranged later to be integrated with the WS converter.

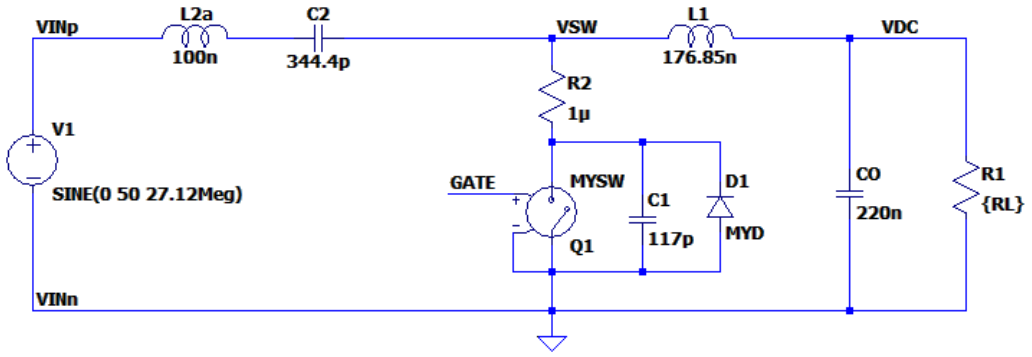


Figure 3.6: Class-E rectifier simulation model with ideal switch.

Note the LC resonant pair between the input and switch node (L_{2a} and C_2). This is a generic band-pass filter which decouples the sinusoidal input voltage from the switch node waveform. It also allows a DC voltage difference between the switch node voltage, which has an average value equal to the output voltage, and the input voltage which has an average value of zero. This filter does not affect the input impedance of the rectifier at the operating frequency f_0. The impedance seen by the supply is capacitive as per the design equations in [19].

3.3.2 Differing Ground References

The Class-E low dv/dt rectifier topology is modified to achieve a difference in ground potential between the RF input and DC output.

The standard Class-E low dv/dt rectifier topology is excited across the switch by an RF source with DC-blocking. In the wave-shifting converter, the source is instead connected across the filter inductor as shown in Figure 3.7. In this arrangement the source is coupled through the large output capacitor and thus excites the circuit across the switch as before. The circuit operates as normal, but the negative input terminal is equal to the rectified DC voltage instead of the common ground. Importantly, no RF voltage (except the ripple voltage) is applied between the negative input terminal and the DC ground, therefore avoiding any EMI emission.

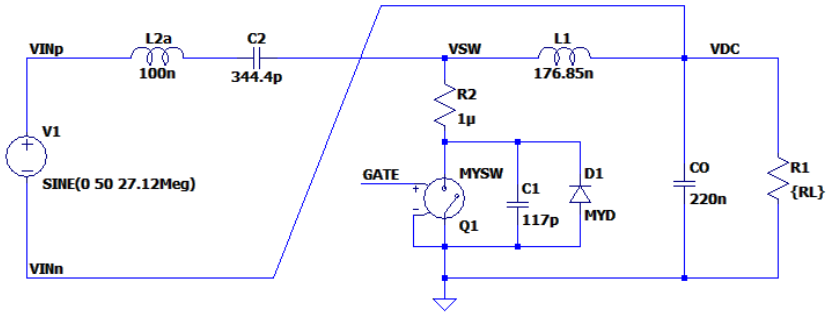


Figure 3.7: Class-E rectifier with different input and output ground references.

Now the voltage between nodes V_{INp} and ground is the series combination of the RF input voltage and the DC rectifier output voltage.

3.3.3 Rectifier Impedance Transformer

After confirming the operation of the rectifier in simulation, the rectifier impedance transformer is designed to achieve a voltage V_{DC} equal to the peak voltage V_{pk} at the input to the network. The impedance transformer is a double impedance inverter, comprising two cascaded LCL T-networks.

The single impedance inverter is a two-port network as shown in Figure 3.8. At resonant frequency, it has the property that the impedance Z_{in} seen looking into one port is inversely proportional to the impedance Z_L connected across the other port. The single impedance inverter is fully defined by its resonant frequency and its characteristic impedance.

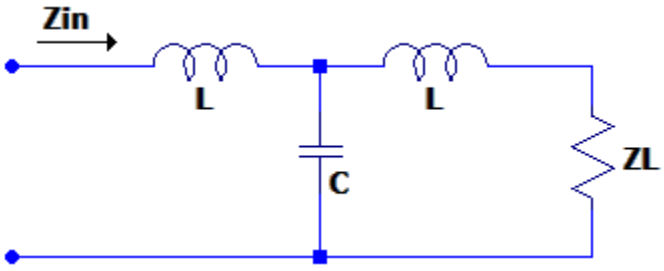


Figure 3.8: Single impedance inverter network.

At resonant frequency, reactances ωL and $1/\omega C$ have equal magnitude X, which is also equal to the magnitude of the characteristic impedance.

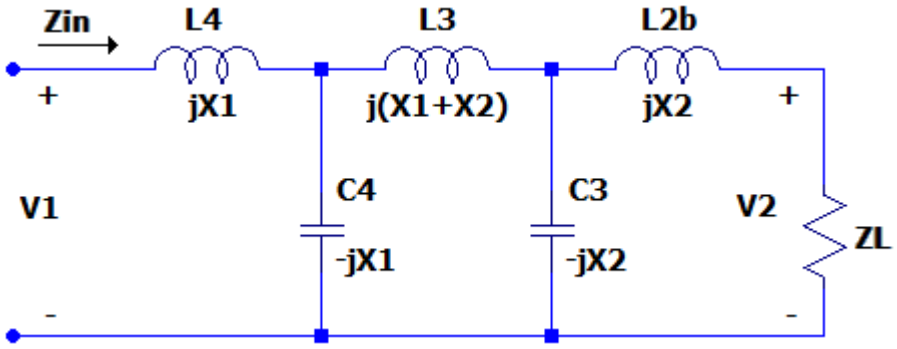


Figure 3.9: Impedance transformer composed of two impedance inverters.

Two cascaded impedance inverters behave as an impedance transformer, having a fixed ratio of input voltage to output voltage (and likewise input current to output current) at the resonant frequency. The transformer ratio can be chosen by proper selection of the two characteristic impedances. In the wave-shifting converter, the rectifier impedance transformer is fully defined by the operating frequency, the required voltage gain A, and one selected inductor value. The voltage gain is defined in Equation (3.2).

$$\mathrm{A} = \frac{V_2}{V_1} \tag{3.2}$$

Given the equation for a single impedance inverter in Equation (3.3), the relationship between input and output impedance for two cascaded impedance inverters with characteristic impedances X_1 and X_2 is expressed in Equation (3.4).

$$\mathrm{Z}_{in} = \frac{\mathrm{X}^2}{Z_L} \tag{3.3}$$

$$\mathrm{Z}_{in} = \frac{{\mathrm{X}_1}^2}{({\mathrm{X}_2}^2/Z_L)} = \left(\frac{\mathrm{X}_1}{\mathrm{X}_2}\right)^2 Z_L \tag{3.4}$$

Assuming that the network is lossless, the impedance transformation is expressed in terms of the input and output voltages by Equation (3.5). The voltage gain A in terms of the characteristic impedances X_1 and X_2 is given in Equation (3.6).

$$\frac{\mathrm{Z}_L}{\mathrm{Z}_{in}} = \left(\frac{\mathrm{V}_2}{\mathrm{V}_1}\right)^2 \tag{3.5}$$

$$\frac{\mathrm{V}_2}{\mathrm{V}_1} = \frac{\mathrm{X}_2}{\mathrm{X}_1} = A \tag{3.6}$$

The middle inductor in the impedance transformer is the largest of the three. It may be chosen by the designer based on available components; however the chosen value has some consequence for the performance of the converter.

The impedance seen at the middle of the impedance transformer places a practical constraint on the choice of middle inductor. Considering Equation (3.3) for the single impedance inverter, if the chosen inductor is too small, then the image impedance will be too low, resulting in high currents and therefore greater losses. Likewise, if the chosen inductor is too large, the image impedance will be too high resulting in excessively high voltages on the capacitors. Moreover, the chosen inductor value determines the capacitor values, and these must be large enough to overcome parasitic capacitance in the design. In general, the image impedance at the middle of the impedance transformer should be between Z_{in} and Z_L, although this is not a rigid constraint. To achieve this, the constraint of Equation (3.7) should be applied. Equation (3.7) assumes that $A > 1$. If $A < 1$, the signs must be reversed.

$$\frac{Z_L(A+1)}{A^2\omega_0} \leq L_3 \leq \frac{Z_L(A+1)}{A\omega_0} \tag{3.7}$$

Although the impedance transformer is assumed to be lossless, in practice high-quality inductors and capacitors should be chosen to maximize the efficiency of the converter.

Given a value of the middle inductor L_3, the component values L_4 and L_{2b} and their resonant capacitors C_4 and C_3 can be determined.

$$L_3 = L_4 + L_{2b} \tag{3.8}$$

$$X_1 = \omega_0 L_4 \tag{3.9}$$

$$X_2 = \omega_0 L_{2b} \tag{3.10}$$

$$L_4 = \frac{L_3}{A+1} \tag{3.11}$$

$$C_4 = \frac{1}{{\omega_0}^2 L_4} \tag{3.12}$$

$$C_3 = \frac{1}{{\omega_0}^2 L_{2b}} \tag{3.13}$$

The series inductor L_{2a} in the existing series-LC pair is absorbed into the impedance transformer, such that $L_2 = L_{2a} + L_{2b}$. In practice, an off-the-shelf inductor should be selected with a value close to L_2. Then L_{2a} is recalculated, holding L_{2b} constant and using the selected value of L_2. The resonant capacitor C_2 is changed to resonate with the new value of L_{2a} at the operating frequency f_0. The resonant capacitor may be adjusted later to nullify the rectifier input reactance.

The designed impedance transformer is inserted between the RF supply and the rectifier. The result is that the peak value of the input voltage is equal to the rectifier output voltage, so the voltage between the positive input terminal and ground is a sine wave with a DC offset, with its valleys occurring at zero volts.

It should be pointed out that the stability of the rectifier is dependent upon the filtering effect of the impedance matching network. An improper choice of filter response results in the rectifier becoming unstable, which is manifested by subharmonic oscillation at the switch node. In general, if the rectifier is unstable the inductor values should be reduced and the capacitors increased.

3.3.4 Inverter and Low-Frequency Clock

The next stage in the design is the connection of the inverter. Supposing that a half-bridge inverter were to be used, the rectifier would be unloaded for multiple cycles at a time, therefore the half-bridge inverter is likely to cause instability. For this reason, a full bridge Class-D

inverter is chosen to maintain a continuous load on the rectifier. In theory, the load-independent Class-E rectifier can tolerate an open load condition [4]. However, it does not perform well when the load is varied intermittently as in this application. Furthermore, the full-bridge inverter doubles the output voltage, thus achieving higher power.

The inverter is driven by a synchronous clock signal at a lower frequency than the RF input. As described in Section 3.2, the inverter clock is produced by a digital frequency divider. In the ideal case, only two complementary gate drive signals are required; one for positive load polarity and one for negative. In practice, there are four unique gate drive signals derived from two half-bridge gate drivers. The four gate signals have duty cycles of approximately 50%, with a minimal dead-time during which both switches in each half-bridge are turned off to prevent shoot-through.

3.3.5 DC Pass Inductor

Since the target application for the designed converter is a capacitive wireless power transfer system, no DC current is permitted to flow through the RF input. However, DC current equal to the average rectified load current does flow through the input to the inverter. Hence, a parallel-resonant LC pair (L_5 and C_5) is fitted between the v_H and v_{INn} nodes of the circuit as shown in Figure 3.3 (b). This pair allows the DC current component to circulate through the inductor without disrupting the high-frequency operation. Inductor L_5 is chosen from off-the-shelf parts, and capacitor C_5 is chosen to resonate with L_5 at the input frequency f_0. The function of the DC pass inductor is illustrated in Section 5.3.2.

3.3.6 Output Filter

It is assumed that any energy at a higher frequency than f_L will be lost in the transformer. Therefore, the output filter is essential to maintain the efficiency of the converter. The inverter output contains odd harmonics of the output frequency. The lowest of these is $3f_L$, so the output filter must pass energy at f_L and stop energy at $3f_L$. The harmonic content of the inverter output is discussed in Section 5.2.1.

A constant-K bandpass filter topology is chosen for its steep cut-off of -40 dB/decade, and its simple construction. The filter consists of a series LC pair and a parallel shunt LC pair. This

filter is specified by the upper and lower cut-off frequencies, and the characteristic impedance of the load [21]. The schematic is shown in Figure 3.10.

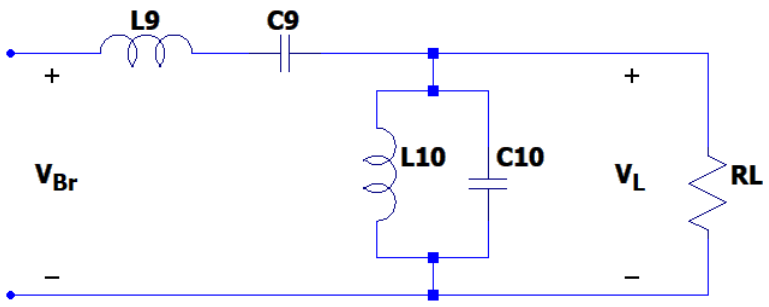


Figure 3.10: Constant-K bandpass filter.

The component values for the constant-K filter may be selected in terms of the lower cut-off frequency ω_1, the upper cut-off frequency ω_2, and the characteristic impedance Z_0 using Equations (3.14) to (3.17).

$$L_9 = \frac{2Z_0}{(\omega_2 - \omega_1)} \tag{3.14}$$

$$C_9 = \frac{(\omega_2 - \omega_1)}{2Z_0\omega_2\omega_1} \tag{3.15}$$

$$L_{10} = \frac{Z_0(\omega_2 - \omega_1)}{2\omega_2\omega_1} \tag{3.16}$$

$$C_{10} = \frac{2}{Z_0(\omega_2 - \omega_1)} \tag{3.17}$$

The center frequency of the filter at which its phase response is zero occurs at $\omega_c = \sqrt{\omega_2\omega_1}$. Thus, ω_c should be set equal to ω_L to achieve a resistive image impedance at nominal load, and ω_2 should be chosen as low as possible to yield practical component values. Clearly, both LC pairs are resonant at ω_c, so the filter appears as a straight wire at the center frequency.

3.3.7 Input Impedance Transformer

The design of the impedance matching network is the same as in Section 3.3.3. Inductors L_6 and L_8, and capacitors C_7 and C_8 are chosen by selecting L_7. The resulting input impedance is given in Equation (3.18), where R_S is the impedance seen looking into the converter from v_S (see Figure 3.3 (b)).

$$Z_{in} = \left(\frac{X_1}{X_2}\right)^2 R_S \tag{3.18}$$

3.4 Summary

This chapter has defined the operation of the wave-shifting converter and laid out its essential components. The rationale for the "shifted wave" is to achieve zero voltage and zero voltage-derivative at the inverter switching instants. The relationship between the rectifier and inverter switch timings has been defined. The switch timings are synchronized by a single trigger circuit and clock divider.

The design process has been defined to enable the construction of wave-shifting converters using any chosen input frequency and frequency division factor. The converter is versatile and can divide the input frequency by any even number chosen at design time. In the next chapter, the wave-shifting converter is implemented and tested experimentally at 27.12 MHz input, with a frequency division factor of n = 16.

4 Design of the Wave-Shifting Converter at 27.12 MHz

Following the procedure in Chapter 3, a wave-shifting converter was designed having an input frequency of 27.12 MHz, a frequency division factor of n = 16, and an output frequency of 1.695 MHz which is compatible with a suitable high-frequency transformer. This 27.12 MHz converter was simulated in LTspice, and an experimental prototype was constructed. In the simulation model, the clock divider is implemented by four cascaded D flip-flops and a delay line. In the experimental unit, the MILF542 clock divider chip is used.

4.1 Component Values of the 27.12 MHz to 1.695 MHz Wave-Shifting Converter

The values of the resonant components and switches are given in Table 4.1. The design choices resulting in these values are elaborated below.

Table 4.1: Component values of the 27.12 MHz wave-shifting converter.

Component	**Value**	**Component**	**Value**
L_1	176.9 nH	C_1	116.8 pF
L_2	250 nH	C_2	550 pF
L_3	250 nH	C_3	246 pF
L_4	110 nH	C_4	313 pF
L_5	110 nH	C_5	313 pF
L_6	60 nH	C_O (DC capacitor)	220 nF
L_7	200 nH	C_7	578 pF
L_8	140 nH	C_8	245 pF
L_9	4507 nH	C_9	1956 pF
L_{10}	782 nH	C_{10}	11268 pF
Rectifier diode D_1	C3D1P7060Q	Rectifier GaNFET Q_5	EPC2012C
		Inverter GaNFETs Q_1-Q_4	EPC2019

The load-independent synchronous rectifier designed for this application requires a total switch capacitance C_1 of 116.8 pF. The selected rectifier GaNFET Q_5 (EPC2012C) has an output capacitance of 64 pF at 100 V (half the rated voltage). Thus, ceramic capacitors totalling 52.8 pF are needed.

The rectifier impedance transformer was designed by simulating the rectifier alone to determine the required voltage gain. Figure 4.1 shows the rectifier input voltage and DC output voltage before the impedance-matching network is inserted in the 27.12 MHz converter. The magnitude of the supply voltage is 50 V and V_{DC} is 28 V. Therefore, a voltage gain of A = 1.79 is required. The supply voltage V_{pk} was set to 50 V because the rated voltage of Q_5 is 200 V, and the Class-E rectifier has a peak switch voltage greater than 3 times V_{DC}. Thus the rectifier switch will operate close to maximum power and with some safety margin.

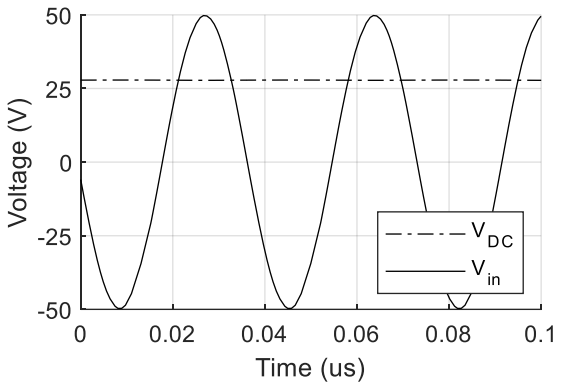


Figure 4.1: Voltage waveforms in the simulated rectifier.

Solving Equations (3.8) to (3.13) using the given values in Table 4.2 yields the component values for L_4, L_{2b}, C_4, and C_3. The middle inductor is chosen to be 250 nH since this is the largest air-core inductor available off-the-shelf. The inductor L_2 is chosen to be equal to L_3, which determines the value of the DC-blocking capacitor C_2.

Table 4.2: Specification for the rectifier impedance-matching network.

Variable	**Symbol**	**Value**
Frequency	f_0	27.12 MHz
Middle inductor	L_3	250 nH
Input peak voltage	V_{pk}	50 V
DC output voltage	V_{DC}	28 V

Simulation shows that the designed network has the correct transformation ratio, which yields a DC voltage equal to the input peak voltage as shown in Figure 4.2.

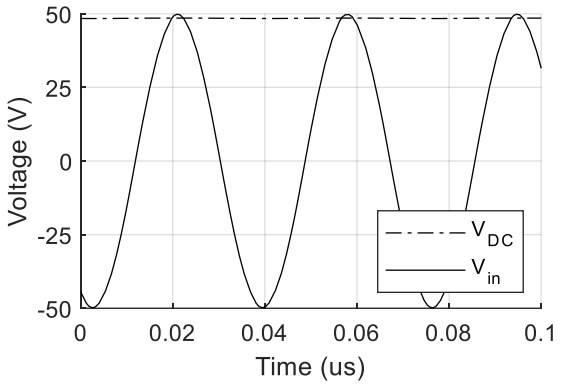


Figure 4.2: Correctly matched V_{pk} and V_{DC} in the simulated rectifier.

The output filter was designed using Equations (3.14) to (3.17). For the experimental prototype, the cutoff frequency ω_2 was chosen to be $1.5\omega_L$. The filter characteristic impedance Z_0 was set to the nominal load resistance of 20 Ω, yielding the component values for L_9, C_9, L_{10}, and C_{10}.

4.2 Experimental Prototype of the Wave-Shifting Converter

Two experimental prototypes of the wave-shifting converter were constructed on standard two-layer FR4 printed circuit boards. Both units are functionally identical. The prototypes are based on the 27.12 MHz input, 1.695 MHz output converter designed above. A photograph of the converter is shown in Figure 4.3. The SMA connectors on the left side are the high-frequency input (bottom) and the low-frequency output (top). The rectifier is located at the bottom right of

the board, and the inverter is at the top center. The smaller board on the right side contains the trigger circuit.

Figure 4.3: Prototype of the wave-shifting converter. The main board measures 15 cm long.

A list of the integrated circuits and power inductors used in the prototypes is given in Table 4.3. Generic components and hand-wound inductors are not listed.

Table 4.3: Integrated circuits used in the experimental prototype.

Component	**Manufacturer**	**Part Number**
Rectifier gate driver	Texas Instruments	LMG1020
Inverter gate drivers	Texas Instruments	LMG1210
Trigger comparator	Linear Technology	LT1719
Clock divider	Renesas	542MILF
Inverter clock AND gate	Diodes Incorporated	74LVC1G08
Inverter clock NAND gate	Diodes Incorporated	74LVC1G00
Rectifier GaNFET	Efficient Power Conversion	EPC2012C
Inverter GaNFETs	Efficient Power Conversion	EPC2019
Air-core inductors	Coilcraft	1010VS-141ME, 2014VS-111ME, 2014VS-201ME, 2014VS-251ME

4.2.1 Test Equipment and Calibration

The following equipment was used for all experiments:

- Marconi Instruments 2026 signal generator.
- Electronic Navigation Industries 3200L RF power amplifier.
- Rigol DP832 triple DC power supply.
- Rohde and Schwarz RTE 1104 oscilloscope.
- Flir E4 thermal camera.
- TEH100 non-inductive power resistors.
- 24 V, 60 mm cooling fan.

The two oscilloscope current probes used to measure the converter performance introduce a delay compared to voltage probes. To counteract this, the oscilloscope's de-skew function was used. The test setup for de-skewing consists of an RF power amplifier connected by 50 Ω coaxial cable to a non-reactive resistive load. Both current probes and a voltage probe were connected to the cable, and the current probe skew was adjusted until the measured currents and voltage were in phase. The current probes were then swapped, and the measurement was repeated to confirm that the probe position did not affect the readings. This calibration procedure was repeated before each test where voltage and current probes were used together.

4.2.2 Rectifier Test and Results

Before operating the complete system, the rectifier was tested with a DC resistive load, and with the inverter disconnected. This is facilitated by opening a jumper on the circuit board. The purpose of this testing is to tune the synchronous rectifier trigger circuit, and to confirm that the rectifier achieves zero-voltage switching.

To ensure that the triggering circuit timing is the same as the timing of the diode if the switch were not in the circuit, the rectifier is initially operated in passive mode. During this test, the active rectifier switch remains off while a parallel diode conducts. The purpose of this is to have the active switch assist the diode without forcing the switch timing. The trigger circuit is adjusted such that the rising edges of its output lead the turn-on of the diode (when the switch node

voltage falls to zero) by about 4 ns. The leading trigger output counteracts the propagation delay through the gate driver.

When the trigger timing is close to the correct value, the rectifier gate driver is enabled by closing a jumper on the circuit board. A final adjustment is performed to eliminate diode conduction. Diode conduction is observable in the switch node voltage waveform as a negative voltage spike preceding turn-off, often accompanied by ringing as shown in Figure 4.4. The spike where the voltage falls below 0 V is observable. After tuning the trigger circuit, the rectifier is operated with a resistive DC load and its efficiency is measured.

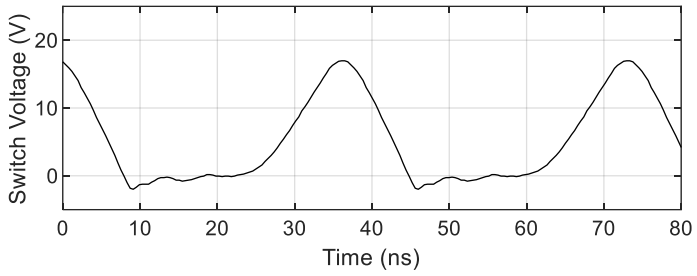
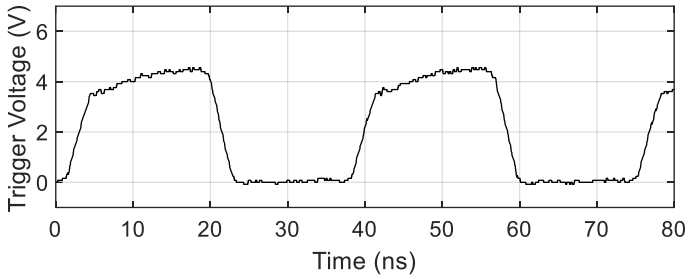


Figure 4.4: Passive rectifier switch node voltage.

The rectifier switch node waveform and the trigger circuit output are shown in Figure 4.5, when the rectifier is operating in synchronous mode. Note that the switch node voltage lags the trigger signal by about 4 ns. This accounts for the propagation delay through the rectifier gate driver. It is clear that the trigger is correctly tuned, since there is minimal overshoot and no ringing when the switch turns on.



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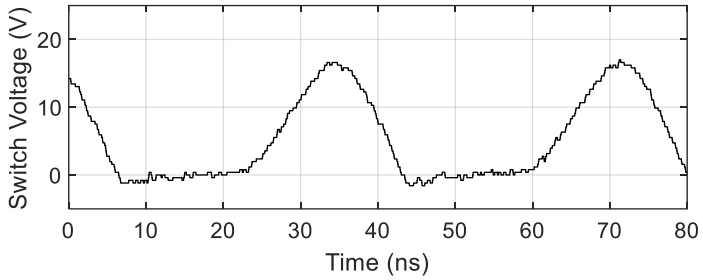


(b)

Figure 4.5: a) Trigger voltage; b) Rectifier switch node voltage.

The rectifier performance for DC loads of 16, 20 and 50 **Ω** is compared in Table 4.4. In each case, the power was limited by the rectifier switch temperature.

Table 4.4: Rectifier DC test performance.

Value	**R_L = 16 Ω**	**R_L = 20 Ω**	**R_L = 50 Ω**
DC Voltage (V)	19.2	22.9	23.7
Peak Switch Voltage (V)	94.9	115.4	124.2
Ratio of Peak Switch Voltage to DC Voltage (V)	4.94	5.04	5.24
Input Power (W)	31.2	34.7	12.9
Output Power (W)	22.9	26.0	11.2
Efficiency	73.5%	74.8%	87.0%

At each load level, the rectifier switch duty cycle is 65%, as compared to the design value of 50%. This results in a higher ratio of peak switch voltage to DC voltage, and therefore the

rectifier power capability is less than nominal. From [19], the power capability of the rectifier is 0.0981 at 50% duty cycle, but only 0.0845 at 65% duty cycle, representing a 14% reduction. Furthermore, from [19] the expected ratio of peak switch voltage to DC voltage at 65% duty cycle is 5.1, which agrees with the experimental measurements. This is compared to the nominal ratio of 3.6 at 50% duty cycle – the additional voltage stress on the switch accounts for the reduction in power capability. Referring to the Class-E rectifier design equations in [19], the 65% duty cycle suggests that the parallel switch capacitance is lower than nominal, despite being correctly tuned for ZVS.

4.2.3 Inverter Test and Results

The inverter switch timing must also be adjusted separately from the rectifier. The purpose of this test is to adjust the phase of the low-frequency clock that drives the inverter.

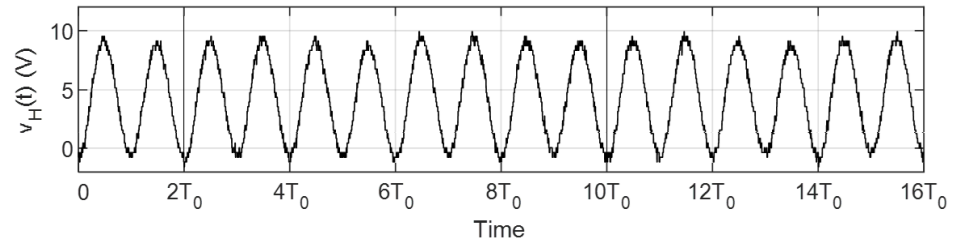
For this test, the rectifier operates with a resistive DC load so that the trigger circuit is operating normally. The output of the trigger circuit is the high-frequency clock, and this is passed through a digital clock divider to produce the low-frequency clock.

To ensure that the inverter does not interfere with the operation of the rectifier, it is disconnected from the rectifier. The inverter is supplied by a low DC voltage of 6 V and loaded with a 20 Ω resistor. Thus, the output voltage of the H-bridge can be measured and compared directly with $v_H(t)$, the shifted RF voltage waveform that would normally be the input to the inverter. This eliminates the need to estimate the propagation delay through the half bridge drivers.

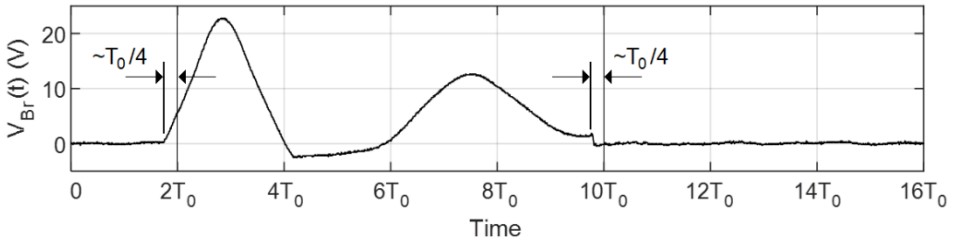
When the inverter is supplied by DC, its output voltage waveform is a square wave with ringing. The quality of the output is not important for this test; only the position of the rising and falling edges is relevant.

Figure 4.6 shows the voltage at one half-bridge output of the inverter with respect to ground, and $v_S(t)$. The ringing in the output voltage is the result of the large parasitic inductance of the load resistor. It is not a problem because the switching instants are clearly discernable. The correct phase of the H-bridge requires these switching instants to occur in the valleys of $v_H(t)$ (or

$v_S(t)$). As shown here, the switching is leading by about $T_0/4$. The adjustment was implemented by an RC delay with R = 100 Ω and C = 100 pF, at the input to the inverter gate drivers.



(a)



(b)

Figure 4.6: a) Input voltage to the inverter; b) Output voltage of the inverter.

4.3 System Performance Test and Results

With the rectifier and inverter timing properly tuned, the experimental wave-shifting converter was operated under varying supply voltage and load conditions. The supply was varied in increments of 1.0 dB, and the load was set to 15, 20, 25, and 50 Ω using fixed non-inductive resistors.

In the test setup, simultaneous measurements of supply and load power by voltage and current could not be performed, because the oscilloscope used has only four channels. To measure the load power would require two voltage probes and one current probe. Since the load is known to be resistive, the load power was measured by current only. Accurate values for the average load power were calculated using spreadsheet software to integrate the recorded data from the oscilloscope.

Unlike the load power, the supply power was measured using one voltage probe and one current probe. Spreadsheet software was used to integrate the recorded data from the oscilloscope to obtain the average supply power.

4.3.1 Supply and Load Variation

As the magnitude of the input voltage to the wave-shifting converter varies, it is expected that the output voltage should vary proportionately and that the rectifier and inverter should maintain ZVS. Likewise, as the load is varied ZVS should be maintained.

The experimental and simulated normalized output voltage for variations in the supply voltage and varying load resistance are shown in Figure 4.7. It is observed that for a given load resistance, the magnitude of the output voltage is proportional to V_{pk} (the magnitude of the voltage at the input to the rectifier impedance-matching network), and the ratio does not vary significantly with respect to V_{pk}. The simulated results likewise show that the output voltage is proportional to V_{pk}; however, the grouping is much closer to the nominal value of 1.27 (the normalized fundamental magnitude of a square wave) [22].

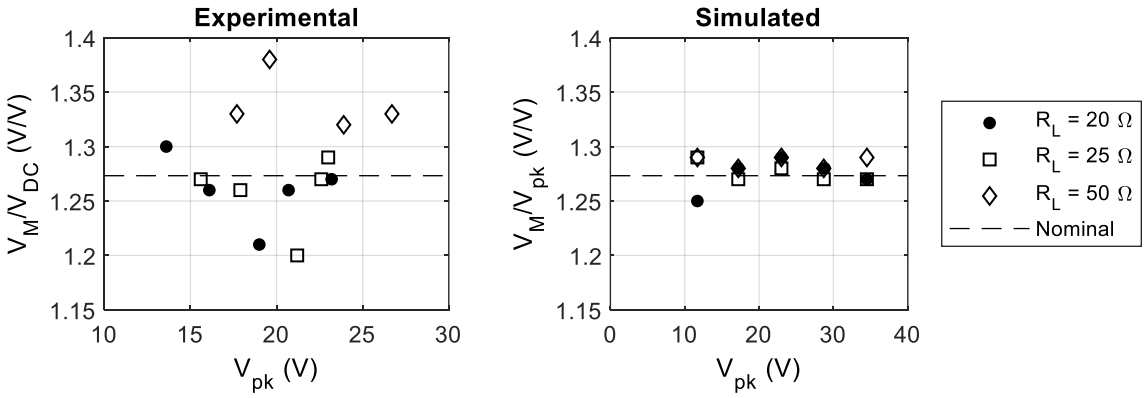


Figure 4.7: Normalized load voltage over supply variation.

Although it was assumed in the analysis that V_{DC} is always equal to V_{pk}, simulation results show that the ratio V_{DC}/V_{pk} decreases as the supply voltage increases (see Figure 4.8). Here, V_{pk} is taken as the magnitude of a sinusoidal voltage with the same RMS value as the simulated $v_S(t)$. The decline in V_{DC} is explained by deviation in the trigger circuit timing, since the trigger circuit is slightly load-dependent.

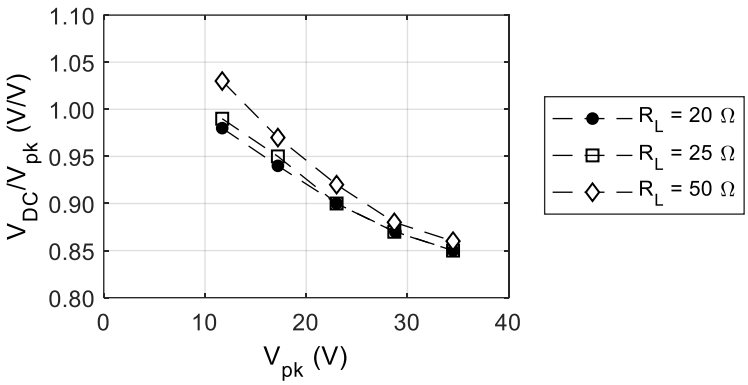
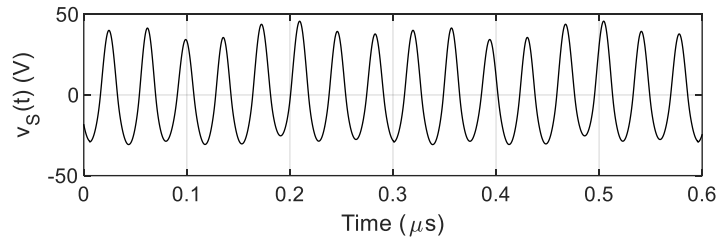


Figure 4.8: Simulated variation in V_{DC} with respect to V_{pk}.

Although the DC voltage is lower at higher supply voltages, ZVS in the inverter is nevertheless maintained since the harmonic content of $v_S(t)$ changes the height of its peaks. Ideally $v_S(t)$ is sinusoidal, but experimentally and in simulation it has harmonic distortion due to the inverter switching. The plot of $v_S(t)$ in Figure 4.9 shows the distortion during one cycle of the output. Notice that the peaks are higher and sharper than the valleys due to the second harmonic. The plot of $v_{Br}(t)$ shows that ZVS is maintained, and the voltage is continuous where the inverter output changes from positive to negative.



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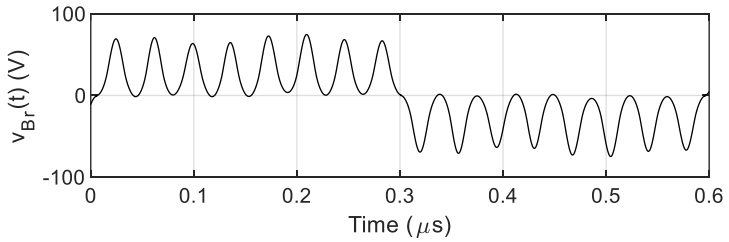


(b)

Figure 4.9: Harmonic distortion in a) input voltage (v_S); b) inverter output voltage (v_{Br}).

The Fourier transform of $v_S(t)$ in Figure 4.10 shows that in addition to the nominal frequency f_0 (27.12 MHz), it also contains even harmonics of f_L (1.695 MHz). The even harmonics are due to the rectified load current that flows at the input to the inverter. The load current is sinusoidal and has a frequency of f_L, so the current at the inverter input contains even harmonics of f_L with the dominant harmonic of $2f_L$, appearing in $v_S(t)$.

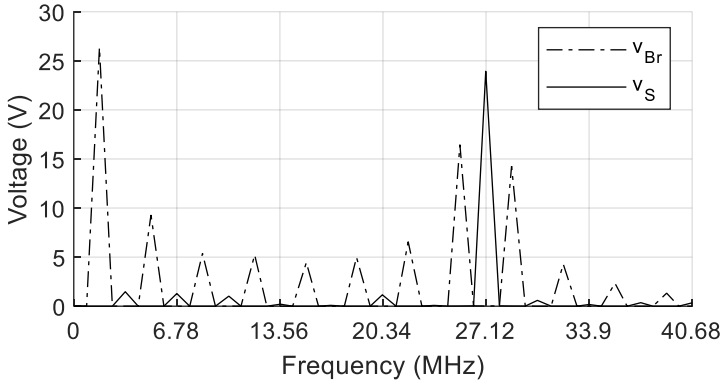


Figure 4.10: Fourier transform of simulated inverter input and output voltages.

4.3.2 Efficiency and Load Power

The efficiency of the experimental wave-shifting converter is plotted for various resistive loads in Figure 4.11. The efficiency is highest at the nominal load of 20 **Ω**, and is consistent as the supply voltage is varied.

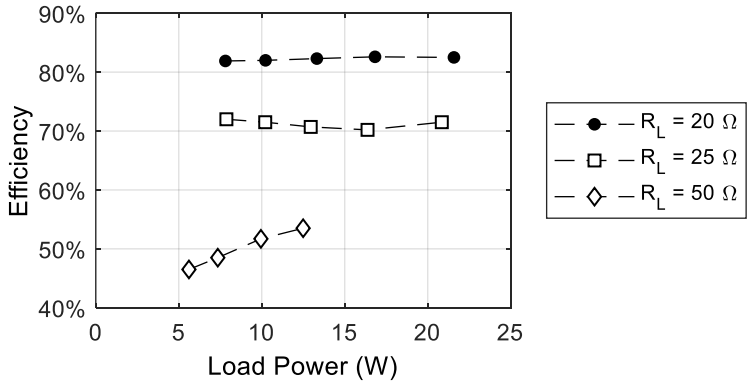


Figure 4.11: Experimental converter efficiency over output power.

The efficiencies plotted here do not consider the power consumed by the digital logic elements of the circuit (the trigger circuit and clock divider) which consume about 0.5 W. For the

experimental prototype, the logic was supplied by an external 5 V DC power supply. In practice, a DC-DC converter powered by the rectifier output would provide the logic power.

The power delivered to the load closely matches the simulated values for a given DC voltage, as shown in Figure 4.12. The load power calculated using Equation (5.7) is virtually identical to the simulated values. The experimental and simulated results of the load power are virtually identical.

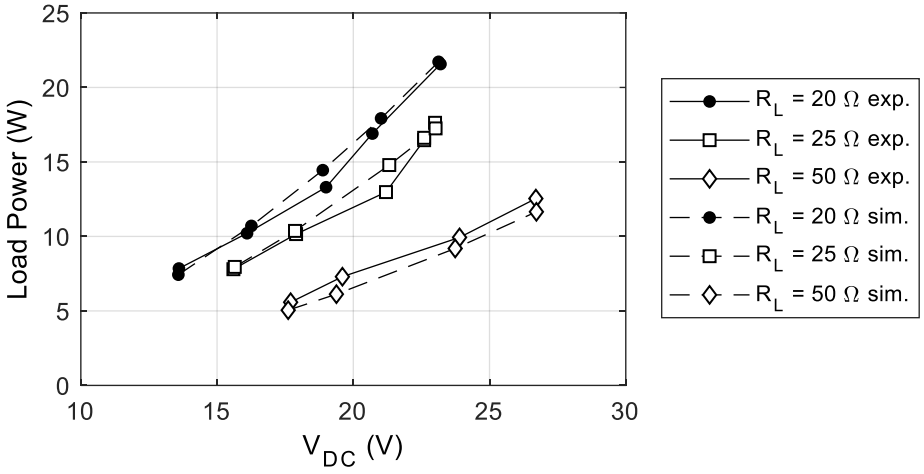


Figure 4.12: Experimental and simulated load power as a function of DC voltage.

4.3.3 Stability

During testing, the power of the experimental prototype converter was limited by instability in the rectifier. In all loading conditions, subharmonic oscillation was observed at the rectifier switch node as the supply voltage was increased. The subharmonic oscillation causes a loss of ZVS in the rectifier, and thus the switch temperature rises rapidly and exceeds the safe operating limit of 100°C. An example of the distorted switch waveform is shown in Figure 4.13, for a load resistance of 25 Ω and a load power of 9.4 W. The switch temperature during the experimental runs is plotted in Figure 4.14. The white points across the top of the graph define the sudden jump in temperature at the point where the subharmonic oscillation appears. Comparing the trend lines on the graph, it is clear that subharmonic distortion causes the temperature to jump by about 20°C.

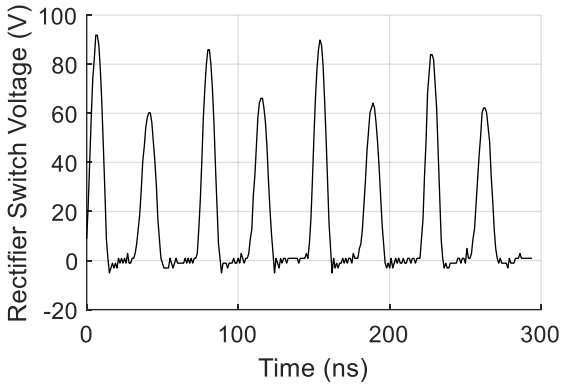


Figure 4.13: Subharmonic distortion of rectifier switch voltage.

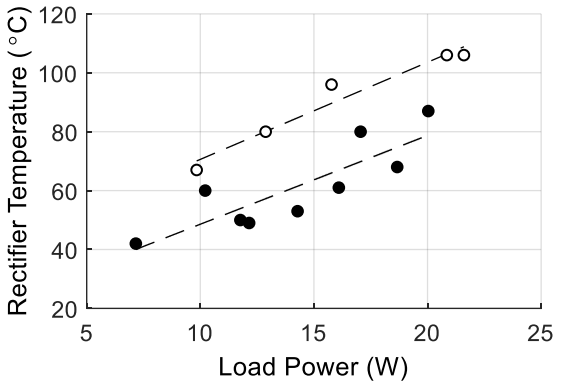


Figure 4.14: Temperature of rectifier switch as a function of load power.

Simulations conducted after the experimental runs suggest that a rectifier impedance-matching network constructed from smaller inductors and larger capacitors, which retains the same impedance transformation ratio, can improve the stability. It is hypothesized that the reason for the improvement is that the modified network can pass lower frequencies, thus removing energy at subharmonic frequencies from the rectifier.

Since the input signal to the triggering circuit is taken at the circuit node between inductors L_2 and L_3, the triggering circuit is suspected to contribute to the problem. One potential remedy to the rectifier stability problem is a more robust trigger circuit such as a phase-locked loop (PLL) that can absorb cycle-to-cycle timing errors. Another remedy would be to use different component values for the rectifier impedance transformer. Recall that one inductor value is chosen arbitrarily in the impedance transformer design. Changing this inductor would provide different filtering characteristics, and thus reduce the harmonic distortion.

4.3.4 Sources of Loss

Only the total efficiency of the system was measured experimentally. In this section, the contributions to power loss from various parts of the wave-shifting converter circuit are estimated using simulation.

A significant source of loss in the wave-shifting converter is the large number of series-connected power inductors. In total there are ten inductors through which the power flows. Most of the inductors used in the prototype belong to the Coilcraft 2014VS series. The quality factor of these inductors at 27.12 MHz is about 160. Computing the AC resistance based on the inductance and Q factor results in values between 110 and 260 mΩ. The hand-wound air-core inductors are assumed to have similar Q factors.

The wave-shifting converter was simulated with a 20 Ω load and 50 V peak supply, using inductor resistance as calculated above. The supply power was 26.9 W and the load power was 22.7 W, therefore the simulated efficiency was 85% which agrees with the experimental performance. The contributions of each component to the total power loss are given in Table 4.5. Notably, inductor resistance is a major contributor to the overall power loss in the circuit.

Table 4.5: Simulated contributions to power loss.

Source	**Simulated Power Loss (mW)**	**Contribution**
HF inductor resistance	3131	75%
LF inductor resistance	555	13%
Rectifier switch (EPC2012C)	290	7%
Inverter switches (EPC2019)	215	5%

In the experimental units, the inductors were seen to heat up by only a few degrees, while the rectifier switch reached the highest temperature of any component. It is reasoned that the inductor power loss is spread over a much larger volume of material, hence the small temperature rise. Also, the rectifier switch losses are likely higher than the simulated values, due to imperfect ZVS as discussed previously.

4.4 Summary

In this chapter, the operation of the wave-shifting converter has been confirmed experimentally. Two physical prototypes of the converter have been assembled and tested.

Before each prototype is operated for the first time, the trigger circuit must be tuned to agree with the natural commutation of the rectifier in passive mode. The phase delay between the rectifier and inverter switching is adjusted to ensure that the inverter achieves zero-voltage and zero-voltage-derivative switching.

The maximum efficiency for the complete system was 82.5% at a low-frequency load power of 21.6 W. The root cause of the low load power is subharmonic distortion in the rectifier switch node voltage. The distortion causes a loss of ZVS and a rapid temperature increase of the rectifier switch. For a given load power, the appearance of subharmonic distortion causes the temperature to rise by 20°C. Nevertheless, the experimental performance agrees with the simulated converter.

Sources of power loss in the circuit have been compared by simulation. Accurate values of inductor AC resistance were calculated using the Q factor from the inductor datasheets. It was determined that the many high-frequency inductors in the circuit contribute 75% to the losses, while the rectifier and inverter switches contribute 7% and 5% respectively.

In the next chapter, the expected performance of the converter is analyzed mathematically, providing insight into the experimental observations.

5 Analysis of the Wave-Shifting Converter

In this chapter, the operation of the proposed converter is analyzed. The expected behaviour of the circuit derived here provides the basis upon which to evaluate the accuracy of the simulation models, and to evaluate the performance of the experimental prototypes.

Some improvements to the circuit are proposed at the end of the chapter, which promise to reduce the size and number of components. Also, a balanced configuration of the converter is suggested that would be compatible with a balanced capacitive coupler.

5.1 Assumptions

The following assumptions are made about the wave-shifting converter for the purpose of analysis:

- All switches and diodes are ideal, that is they have zero on-resistance and voltage drop, and zero capacitance.
- The converter is driven by an ideal sinusoidal voltage source which does not allow DC current to pass.
- The load is purely resistive.
- The output filter is of high quality; therefore, the inverter output current is sinusoidal and in-phase with the inverter output voltage.
- The rectifier input impedance is purely resistive, i.e. the rectifier input reactance is cancelled out by the resonant pair L_2 and C_2.
- Parasitic resistances in the circuit are negligible, therefore the supply power is equal to the load power.

5.2 Harmonics

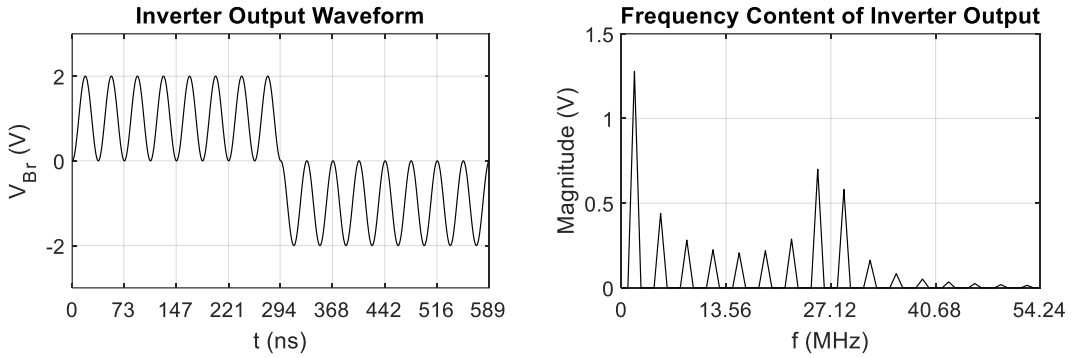
5.2.1 Harmonic Content of the Inverter Output

Because the wave-shifting converter has a high-frequency waveform passing through an inverter, the inverter output contains harmonics at odd multiples of the inverter switching frequency f_L.

The input to the inverter is composed of a sinusoidal voltage superimposed on a DC voltage, hence the inverter output resembles a square wave modulated by the input frequency f_0.

The frequency content at the output of the inverter can be understood by considering the modulation effect on the components of the input. The Fourier transform of the input voltage contains just two components of equal magnitude, one at DC and the other at the input frequency.

The Fourier transform of a square wave contains odd harmonics of the fundamental (the output frequency) which decay in inverse proportion to the frequency. Therefore, the resulting frequency domain representation of the inverter output resembles that of the low-frequency square wave, plus a double-sided copy with a frequency shift as shown in Figure 5.1.



(a) (b)

Figure 5.1: Inverter output for n = 16: a) Ideal waveform; b) Fourier transform.

The harmonic content has implications for the output filter design. Specifically, the next-highest frequency that must be eliminated is equal to $3f_L$, where f_L is the output frequency.

In Figure 5.1 (b), only the component at f_L (the lowest frequency) delivers power to the load. The magnitude of this component, normalized to V_{pk}, is defined as the inverter voltage gain $G(n)$ as shown in Equation (5.1).

$$G(n) = {V_M}/{V_{pk}} \tag{5.1}$$

5.2.2 Stability of the Rectifier

A key difficulty of the wave-shifting converter topology is the effect of the inverter harmonics on the operation of the rectifier. The harmonics cause a switching waveform that varies cycle-to-cycle, which results in a loss of ZVS. This problem is observed in simulation and in the experimental converter (see Section 4.3.3).

The rectified load current flows at the input to the inverter. The load current is sinusoidal and has a frequency of f_L, so the current at the inverter input has a fundamental frequency of $2f_L$. This produces even harmonics of f_L that distort the voltage $v_S(t)$. The distortion is manageable as long as the load is non-reactive.

For a non-reactive load, the load current is in-phase with the fundamental of the inverter output voltage $v_{Br}(t)$ (see Figure 3.5) and the zero-crossings of the current coincide with the inverter switching. However, if the load is reactive, the inverter switchings occur at non-zero current. This results in greater harmonic content being propagated back to $v_S(t)$ which in turn interferes with the rectifier ZVS. Therefore, the wave-shifting converter cannot tolerate a reactive load.

5.3 Power Calculation

In this section, analytical expressions are developed for calculating the nominal power delivered to a resistive load for a given supply voltage.

5.3.1 Power Delivered to Load

The instantaneous power delivered to the load is defined as the product of voltage and current in the load resistance R_L. Assuming that the output filter is lossless and of high quality (i.e. it rejects all frequencies except f_L), the load voltage $v_L(t)$ will be sinusoidal with magnitude V_M defined by the inverter voltage gain.

$$v_L(t) = V_M \sin(\omega_L t) \tag{5.2}$$

$$V_M = V_{pk} G(n) \tag{5.3}$$

Likewise, the output current will be sinusoidal with magnitude I_M.

$$i_L(t) = I_M \sin(\omega_L t) \tag{5.4}$$

Where $$I_M = \frac{V_M}{R_L} \tag{5.5}$$

The instantaneous load power is then defined as the product of voltage and current at the inverter output.

$$p_L(t) = v_L(t) i_L(t) \tag{5.6}$$

The average load power P_L is obtained as:

$$P_L = \frac{{V_M}^2}{2R_L} = \frac{{V_{pk}}^2 G^2(n)}{2R_L} \tag{5.7}$$

The power flowing through the inverter is similarly defined as the product of the inverter input voltage $v_H(t)$ and input current $i_H(t)$. The input voltage is a high-frequency sinusoidal waveform with a DC offset that gives the wave-shifting converter its name. The AC part of $v_H(t)$ is $v_S(t)$, which is measured across the output port of the source impedance-matching network. The DC part is V_{DC}, the output voltage of the rectifier. It is assumed that $V_{DC} = V_{pk}$.

$$v_H(t) = V_{DC} + v_S(t) = V_{pk}(1 - \cos(\omega_0 t)) \tag{5.8}$$

Where $$v_S(t) = -V_{pk} \cos(\omega_0 t) \tag{5.9}$$

Retaining the assumption of a lossless and high quality output filter, the current at the inverter output equals the load current $i_L(t)$. Considering the inverter as a rectifier in reverse, the rectified load current flows at the input of the inverter. The inverter input current is denoted $i_H(t)$ in Equation (5.10).

$$i_H(t) = |I_M \sin(\omega_L t)| \tag{5.10}$$

The DC component of $i_H(t)$ is denoted I_{DC} in Equation (5.11).

$$I_{DC} = \frac{2I_M}{\pi} \tag{5.11}$$

Thus, the instantaneous power flowing into the inverter is expressed by $p_H(t)$ in Equation (5.12).

$$p_H(t) = v_H(t) i_H(t) = V_{pk}(1 - \cos(\omega_0 t))|I_M \sin(\omega_L t)| \tag{5.12}$$

The average power P_H is computed over half of the output period, which is expressed by the definite integral in Equation (5.13).

$$P_H = \frac{2}{T_L}\int_0^{T_L/2} p_H(t)dt = \frac{2V_{pk}I_M}{T_L}\int_0^{T_L/2}(1-\cos(\omega_0 t))\sin(\omega_L t)\,dt \tag{5.13}$$

The solution to Equation (5.13) is given in Equation (5.14). The average power is proportional to ${V_{pk}}^2$ and inversely proportional to R_L, which implies that the converter behaves as a voltage multiplier. It is clear from the result that the average inverter power depends only upon the input voltage and the frequency division factor, and is not dependent on the operating frequency.

$$P_H = \frac{{V_{pk}}^2 G^2(n)}{2R_L} \tag{5.14}$$

Since the circuit is assumed to be lossless, the inverter input power and load power are equal. Equating Equations (5.7) and (5.14) results in the following expression for the inverter voltage gain $G(n)$:

$$G(n) = \frac{4n^2}{\pi(n^2-1)} \tag{5.15}$$

The voltage gain is plotted in Figure 5.2, which shows that $G(n)$ approaches $4/\pi$ as n increases. This is to be expected, since the Fourier transform of a pure square wave has a fundamental magnitude of $4/\pi$ [22]. The fundamental low-frequency voltage is larger in magnitude for small frequency division factors, due to the greater agreement between the inverter output voltage and the low-frequency sine wave. This can be interpreted in terms of Figure 5.1 as the two peaks in the Fourier transform coming together and overlapping.

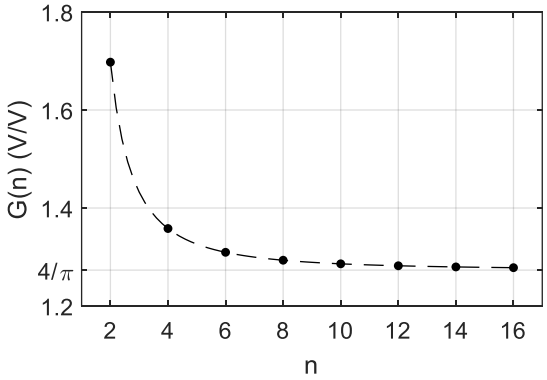


Figure 5.2: Inverter voltage gain over frequency division factor.

5.3.2 Power Through the Rectifier

Since the wave-shifting converter is not an AC-DC-AC converter, the power flow through the rectifier is not identically equal to the power through the inverter. The AC component of the inverter input current $i_H(t)$ is coupled through the rectifier output capacitor and flows through the pass inductor L_5. The DC component I_{DC} flows through the rectifier, so the average power output from the rectifier P_R is calculated as the DC current multiplied by the DC rectified voltage, given by Equation (5.16). The current paths are shown in Figure 5.3. The DC path through the inverter is omitted for clarity.

$$P_R = V_{DC} I_{DC} = \frac{2{V_{pk}}^2 G(n)}{\pi R_L} \tag{5.16}$$

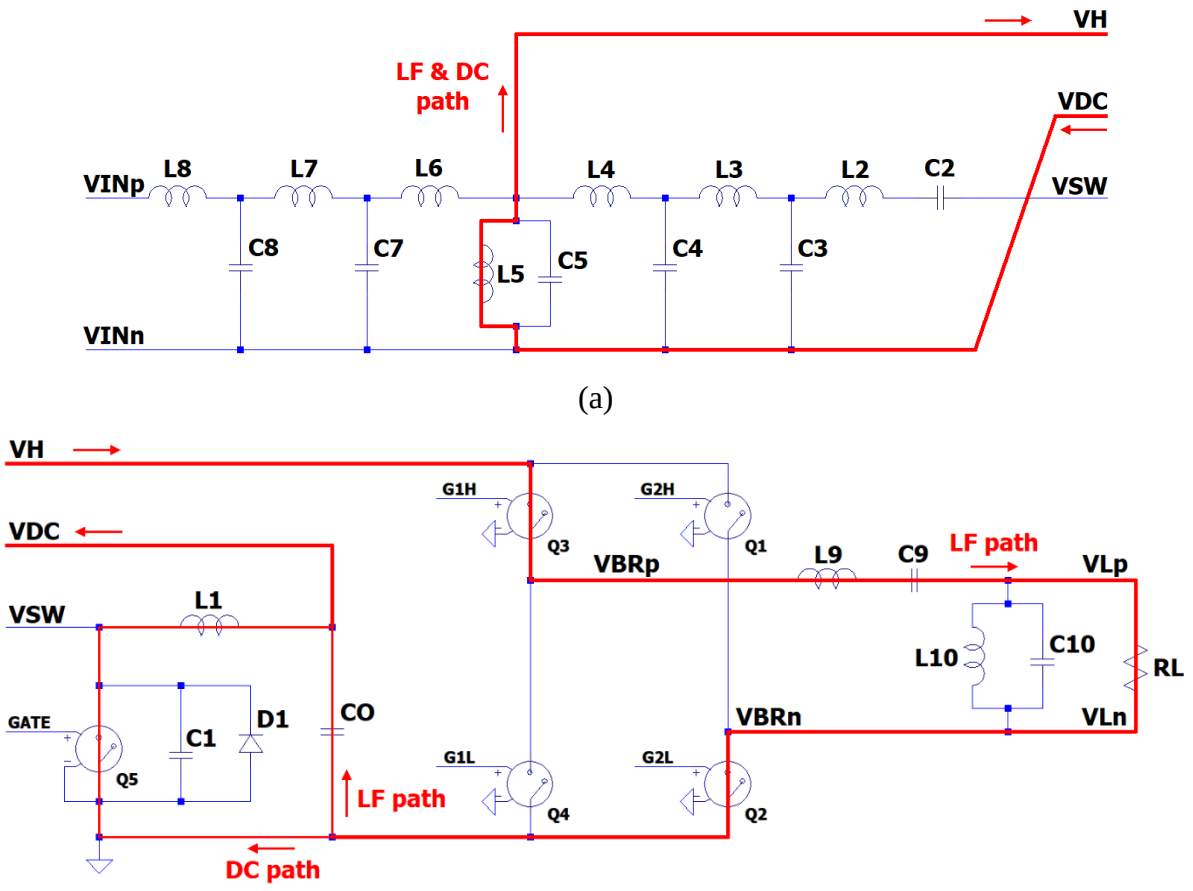


Figure 5.3: Path taken by low-frequency and DC current in the wave-shifting converter. a) Path through the DC pass inductor; b) Path through the rectifier and inverter.

Comparing the equations for the rectifier and inverter power reveals that less power flows through the rectifier than through the inverter. From Equations (5.14) and (5.16), the ratio of rectifier power to inverter power is given by Equation (5.17) and is plotted in Figure 5.4. The rectifier power is less than the inverter power, but at large values of n the rectifier power rapidly approaches equality with the inverter power.

$$P_R/P_H = \frac{(n^2-1)}{n^2} \tag{5.17}$$

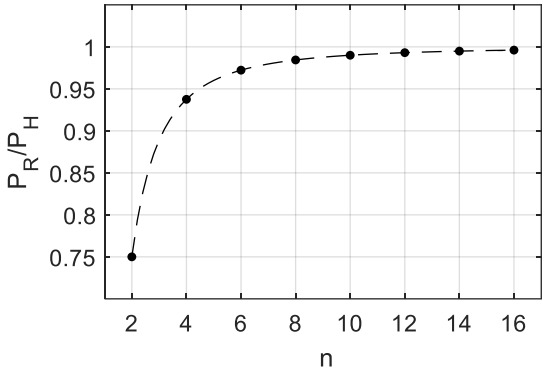


Figure 5.4: Ratio of rectifier power to inverter power as a function of n.

5.4 Power Capability

Power capability is defined as the ratio of average output power to the product of maximum switch voltage and current. In the wave-shifting converter, the power capability of the rectifier and inverter can be calculated separately.

5.4.1 Rectifier Power Capability

The power capability of the Class-E rectifier itself is calculated in [19] and has a maximum value of $c_{pR} = 0.0981$ which occurs at 50% duty cycle. However, as shown in Section 5.3.2, the power output of the wave-shifting converter is higher than the rectifier power. Hence, the power capability of the rectifier within the wave-shifting converter (c_p) is determined from Equations (5.14) and (5.16) and is given by:

$$c_p = c_{pR} P_R/P_H = \frac{c_{pR} n^2}{(n^2-1)} \tag{5.18}$$

Where c_{pR} is the power capability of the rectifier alone, and c_p is the power capability of the rectifier in the wave-shifting converter. The maximum value of c_p is 0.1332 which occurs at $n = 2$.

5.4.2 Inverter Power Capability

From Equation (5.8), the peak voltage across the inverter switches is $2V_{pk}$. From Equation (5.10), the peak current is I_M. Therefore, the inverter power capability c_{pH} is given by:

$$c_{pH} = {P_L}\Big/{2V_{pk}I_M} = \frac{G(n)}{4} \tag{5.19}$$

Substituting Equation (5.15) into Equation (5.19), the minimum value of c_{pH} is obtained as ${1}/{\pi} \approx 0.3183$, which occurs at large values of n. Comparing the limiting values of c_p and c_{pH} shows that the performance of the wave-shifting converter is limited by the rectifier switch, regardless of the frequency division factor. Therefore, the power capability of the entire converter is equal to c_p.

5.4.3 Overall Power Capability

For the 27.12 MHz experimental unit discussed in Chapter 4, a maximum power output of 21.6 W was delivered to a 20 Ω resistive load at an efficiency of 82.5%. The rectifier switch used in the experimental prototype is the EPC2012C GaNFET, which is rated 200 V and 5 A. The power capability of the converter with $n = 16$ obtained from Equation (5.18) is $c_p = 0.0985$. So, the theoretical maximum power output from the designed wave-shifting converter is 98.5 W. However, from [19], at a duty cycle of 50%, the ratio of peak switch voltage to DC voltage is 3.562 and the ratio of peak switch current to output current is 2.862. For the design value of a 20 Ω nominal load, the equivalent resistance at the rectifier output is 24.66 Ω (see Equation (5.26)). The rectifier output current resulting in a maximum switch current of 5 A is 5 / 2.862 = 1.747 A. Hence, the rectifier with the chosen switch can deliver a maximum of 75.27 W, and the converter can deliver a maximum of 75.56 W to a 20 Ω load.

The actual output power achieved by the converter is much less than the calculated maximum value primarily due to thermal limitations. The underlying cause is the rectifier harmonic

distortion discussed in Section 4.3.3. As the supply voltage is increased, a loss of ZVS causes excessive switch heating. Although the rectifier switch peaks are below the rated switch voltage, the supply voltage cannot be increased because of heating.

5.5 Impedances

The impedances at various points in the circuit can be determined analytically as a function of the load resistance.

5.5.1 Inverter Impedance

The impedance looking into the output filter is determined as the mean square of the voltage $v_{Br}(t)$, divided by the average load power over one half cycle of the output frequency. Since the square of the inverter input voltage equals the square of the inverter output voltage, the inverter input impedance R_H seen from $v_H(t)$ equals the impedance looking into the filter from $v_{Br}(t)$. An expression for R_H is derived using Equation (5.8).

$$R_H = \frac{2}{T_L P_H}\int_0^{T_L/2} {v_H}^2(t)dt = \frac{2{V_{pk}}^2}{T_L P_H}\int_0^{T_L/2}(1-\cos(\omega_0 t))^2 dt \tag{5.20}$$

Where T_L is the output period.

Simplifying, $$(1-\cos(\omega_0 t))^2 = 1.5 - 2\cos(\omega_0 t) + 0.5\cos(2\omega_0 t) \tag{5.21}$$

$$R_H = \frac{3{V_{pk}}^2}{2P_H} = \frac{3R_L}{G(n)^2} \tag{5.22}$$

The input impedance of the inverter seen from $v_S(t)$ is denoted R_D. It is relevant because some power flows directly from the source to the inverter. The average value of this power is denoted P_D, and is equal to the difference between the average inverter power and rectifier power as in Equation (5.23). From Equations (4.14) and (5.17), the expression for P_D in Equation (5.24) is obtained.

$$P_D = P_H - P_R \tag{5.23}$$

$$P_D = \frac{{V_{pk}}^2 G^2(n)}{2n^2 R_L} \tag{5.24}$$

The impedance R_D consumes power P_D when $v_S(t)$ is applied. Thus, Equation (5.25) for R_D is obtained.

$$R_D = \frac{\left(V_{pk}/\sqrt{2}\right)^2}{P_D} = \frac{n^2 R_L}{G^2(n)} \tag{5.25}$$

5.5.2 Rectifier Impedance

Considering the rectifier output power calculated in Equation (5.16), the equivalent resistive load at the rectifier output is given by:

$$R_{eq} = {V_{DC}}^2 \Big/ P_R = \frac{\pi R_L}{2G(n)} \tag{5.26}$$

The resistance seen looking from $v_S(t)$ into the rectifier impedance-matching network is proportional to R_{eq}. In terms of $v_S(t)$, the average power flowing into the rectifier is given by Equation (5.27).

$$P_R = \frac{\left(V_{pk}/\sqrt{2}\right)^2}{R_R} \tag{5.27}$$

Substituting Equation (5.27) into Equation (5.26) results in the impedance R_R seen looking from $v_S(t)$ into the rectifier impedance-matching network. The expression for R_R is given in Equation (5.28).

$$R_R = \frac{R_{eq}}{2} = \frac{\pi R_L}{4G(n)} \tag{5.28}$$

Resistance R_R accounts for the power that flows through the rectifier, which is most of the converter power. As n increases, R_R approaches the value $\pi^2 R_L/16$.

5.5.3 Input Impedance

The input impedance of the wave-shifting converter at the operating frequency f_0 can be derived in terms of the load resistance and frequency division factor. The input impedance is defined at the output of the source impedance-matching network, looking into the converter. This impedance may be transformed to match any source by the appropriate selection of the input impedance-matching network.

Finally, the input impedance of the converter R_S is the parallel combination of the rectifier input impedance R_R and the inverter input impedance R_D given by Equation (5.29). Note that as n increases R_D becomes large, so R_S rapidly approaches equality with R_R.

$$R_S = \frac{R_R R_D}{R_R + R_D} = \frac{R_L}{G^2(n)} \tag{5.29}$$

5.6 Component Reduction

Some improvements are possible to the wave-shifting converter as originally described, which reduce the size and number of reactive components in the circuit. These changes have the benefit of increasing the system efficiency and power density. This section presents a simulation of the changes as a proof-of-concept; however, the changes were not implemented experimentally.

5.6.1 Combined Impedance Transformers

The rectifier and input impedance transformers together form a three-port network that connects the supply, inverter and rectifier. As described above, the network consists of four impedance inverters containing a total of six inductors and four capacitors.

An alternate three-port network that accomplishes the same task may be constructed from three LCL impedance inverters in a Y configuration (L_8-C_8-L_7, L_{3b}-C_4-L_4, and L_{3a}-C_3-L_2). This construction eliminates one capacitor and reduces the size of the inductors. A partial schematic showing the impedance-matching Y-network and rectifier is shown in Figure 5.5. Note that some component labels are redefined in this circuit.

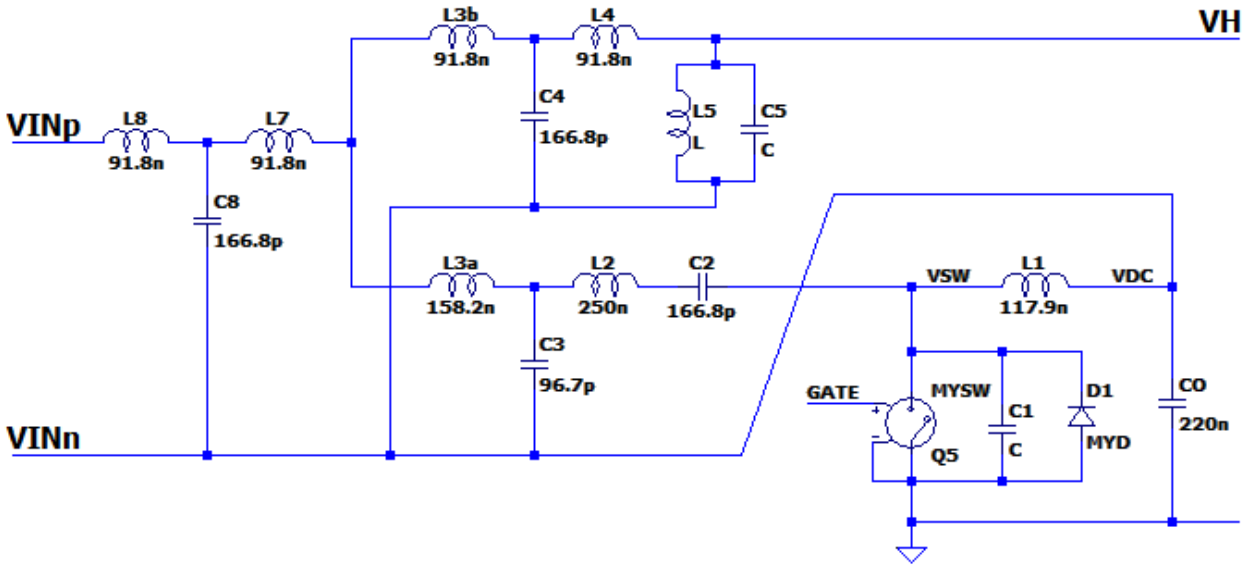


Figure 5.5: Combined impedance-matching network.

The previously determined value of L_3 is used here, but it is split into L_{3a} and L_{3b}, where $L_3 = L_{3a} + L_{3b}$ and $L_{3b} = L_4$. The values of L_7 and L_8 are equal, and resonant with C_8. These are chosen to achieve the desired input impedance.

5.6.2 Removal of DC Blocking Capacitor

The purpose of the DC-blocking capacitor C_2 is to allow a DC voltage difference between the rectifier switch node and the source. As described in Section 3.3.2, the RF source is connected across the rectifier filter inductor L_1, so there is necessarily no DC voltage present across the source. This renders C_2 redundant. To reduce component count, C_2 and its resonant inductor L_{2a} can be removed, leaving a smaller value of $L_2 = L_{2b}$. The input reactance of the rectifier can be corrected by adjusting the impedance transformer output inductor L_2.

5.6.3 Confirmation Simulation for Improved Converter

To prove that the modified circuit works as intended, a simulation was performed with a modified circuit based on the 27.12 MHz model developed in Chapter 4. The component values of the Y-network are given in Table 5.1. These values give the correct rectifier voltage gain such that $V_{pk} = V_{DC}$, and the same input impedance of 50 Ω.

Table 5.1: Component values in the impedance transformer Y-network.

Component	Value	Component	Value
L_2, L_{3a}	160 nH	C_3	215 pF
L_{3b}, L_4	90 nH	C_4	383 pF
L_7, L_8	93 nH	C_8	370 pF

Some performance metrics for the original and the modified converter models are compared in Table 5.2, for a supply voltage of 50 V peak and a resistive load of 20 Ω. Both models achieve ZVS for the rectifier and inverter switches. The performance of both models is not significantly different, but the modified circuit has smaller inductors.

Table 5.2: Comparison of original and modified converter performance.

Value	Original	Modified
Input impedance	48.8 Ω	49.4 Ω
Peak rectifier switch voltage	108 V	112 V
DC voltage	25.0 V	24.8 V
DC current	1.02 A	0.95 A
Load power	25.3 W	24.8 W

5.7 Balanced Configuration

The basic wave-shifting converter topology discussed in this work is an unbalanced configuration, requiring a two-terminal input with one grounded terminal. A more desirable arrangement is the balanced configuration, having a three-terminal input with a grounded center-tap.

5.7.1 Double-Negative Version of the Wave-Shifting Converter

A balanced version of the wave-shifting converter may be realized by joining two unbalanced converters together by their negative input terminals. This is referred to as the “double-negative” balanced configuration. The two rectifiers may have their DC outputs bussed together to reduce

ripple voltage, and both inverters use this as a ground reference (see Section 3.3.2). Each inverter has one of the input terminals (after the input impedance matching network) as a positive input. A block diagram of the double-negative balanced configuration with representative voltage waveforms is shown in Figure 5.6.

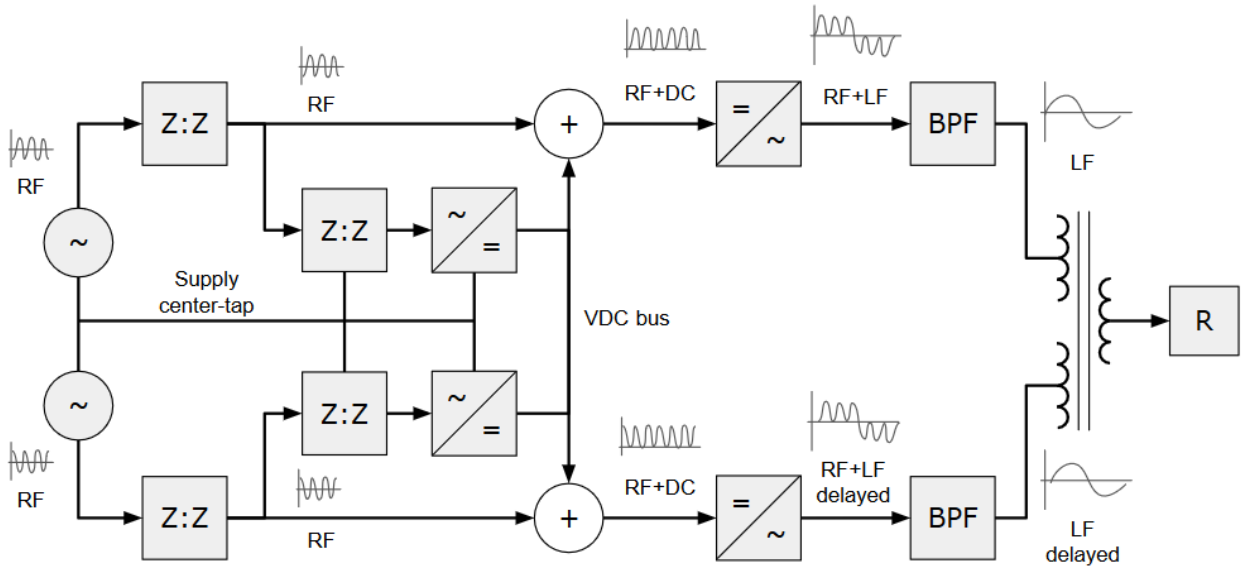


Figure 5.6: Block diagram of the double-negative balanced wave-shifting converter configuration.

The disadvantage of this method is that there is a phase delay between the two branches, since the voltages present at the inverter inputs have opposite phase. Specifically, the valleys of the waveforms during which the voltage is zero do not occur simultaneously for both inverters, hence the switching instants are different for both inverters. The minimum phase delay is $T_0/2$ (although the designer may choose any odd-integer multiple of $T_0/2$).

For large frequency division factors, the phase delay will be small in proportion to the output frequency and may be ignored. In this case, both inverter outputs may be connected to a single isolation transformer with dual primary windings, and a single secondary winding feeding a single low-frequency rectifier.

However, for small frequency division factors, the phase delay between the inverter outputs is significant, and so each requires a separate isolation transformer and low-frequency rectifier in the isolated rectifier system. The dual-primary transformer would be unsuitable in this case

because it would create reactance between the two branches. As discussed in Section 5.2.2, the wave-shifting converter cannot tolerate a reactive load.

A proposed alternative for small frequency division factors is to bridge the inverter outputs as shown in Figure 5.7, where RL1 and RL2 represent the transformer dual primary windings. In this arrangement, the fundamental components of both primary voltages are in phase, but the waveforms are skewed slightly. Further work on this arrangement is outside the scope of the current research.

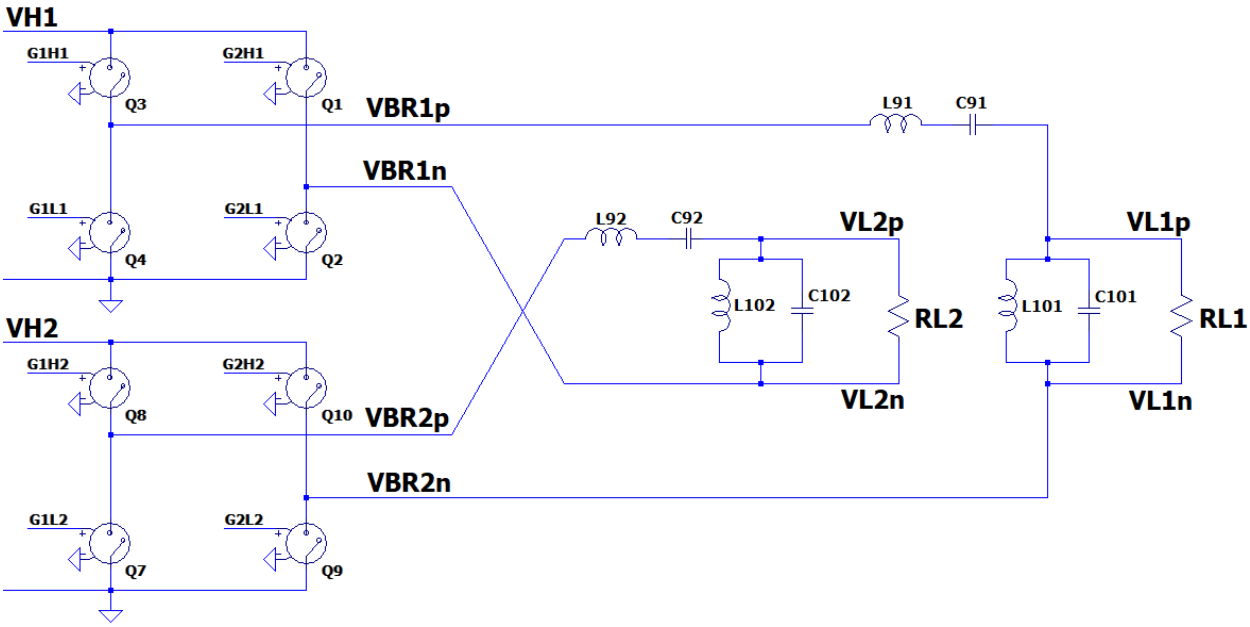


Figure 5.7: Two inverters with bridged loads.

5.7.2 Simulation of the Balanced Configuration

The double-negative balanced converter of Figure 5.6 was simulated using ideal components and a frequency division factor of n = 16. Some important waveforms in both branches of the circuit from the simulation are shown in Figure 5.8, with solid lines representing the top branch and dashed lines representing the bottom branch. The phase delay of $T_0/2$ between the inverter outputs can be seen in the load current plot of Figure 5.8 (d).

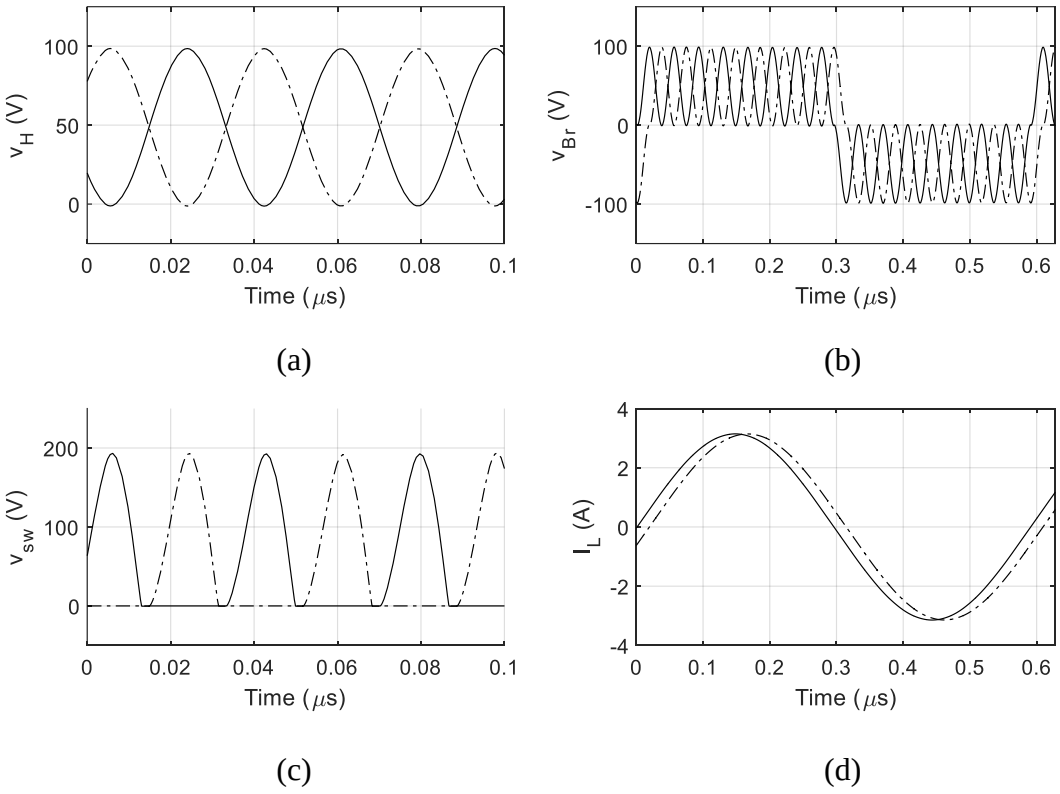


Figure 5.8: Voltage and current waveforms in the double-negative balanced converter. a) Inverter input voltage; b) Inverter output voltage; c) Rectifier switch node voltage; d) Load current.

5.8 Design of the Wave-Shifting Converter at 40.68 MHz

In this work a target operating frequency of 27.12 MHz has been assumed since current developments in capacitive wireless power transmission are exploring 27.12 MHz systems, but with an eye to 40.68 MHz.

It can be shown that the developed wave-shifting converter topology can be adapted to other operating frequencies. Here a simulation model is created with an operating frequency of 40.68 MHz and a frequency division factor of n = 32.

5.8.1 Component Values of the 40.68 MHz Wave-Shifting Converter

The converter is designed following the same procedure as in Section 3.3. Models of appropriate real GaNFET switches and diodes are chosen. The designed component values are given in Table 5.3. The simulation results from this model are presented in this chapter.

Table 5.3: Component values of the 40.68 MHz wave-shifting converter.

Component	**Value**	**Component**	**Value**
L_1	115.1 nH	C_1	79.7 pF
L_2	90 nH	C_2	483 pF
L_3	90 nH	C_3	263 pF
L_4	31.7 nH	C_4	483 pF
L_5	66 nH	C_5	232 pF
L_6	66 nH	C_O (DC capacitor)	220 nF
L_7	200 nH	C_7	233 pF
L_8	134 nH	C_8	114 pF
L_9	6009 nH	C_9	2608 pF
L_{10}	1043 nH	C_{10}	15000 pF
Rectifier diode D_1	C3D1P7060Q	GaNFET switches Q_1-Q_5	EPC8010

The power capability of the converter is determined by the switch selection, and the switch selection is influenced by the required switch capacitance. The 40.68 MHz Class-E rectifier requires C_1 = 79.7 pF. The EPC8010 GaNFET is chosen which has a typical output capacitance of C_{OSS} = 25 pF at 50 V. This switch has a maximum voltage of 100 V and a maximum continuous current of 4 A. From [19], the power capability of the Class-E rectifier with 50% duty cycle is c_p = 0.0981, so the maximum rectifier power capability with this switch is 39.2 W (= 0.0981 · 100 · 4). The power capability of the switch decreases with increasing load. For the parallel rectifier diode D_1, the C3D1P7060Q silicon carbide (SiC) diode is chosen which has a capacitance of 14 pF at 50 V.

5.8.2 Simulation Results at 40.68 MHz

The 40.68 MHz rectifier was simulated with resistive loads of 20 Ω, 25 Ω, and 50 Ω; and with supply voltages of 20 to 60 V peak in 10 V increments. The peak rectifier switch voltage in the simulated 40.68 MHz converter is plotted in Figure 5.9. The rectifier voltage is proportional to the supply voltage and is not affected by the load, since the rectifier is load-independent. The

maximum rated switch voltage is 100 V, so this converter is limited to a peak supply voltage of about 47 V.

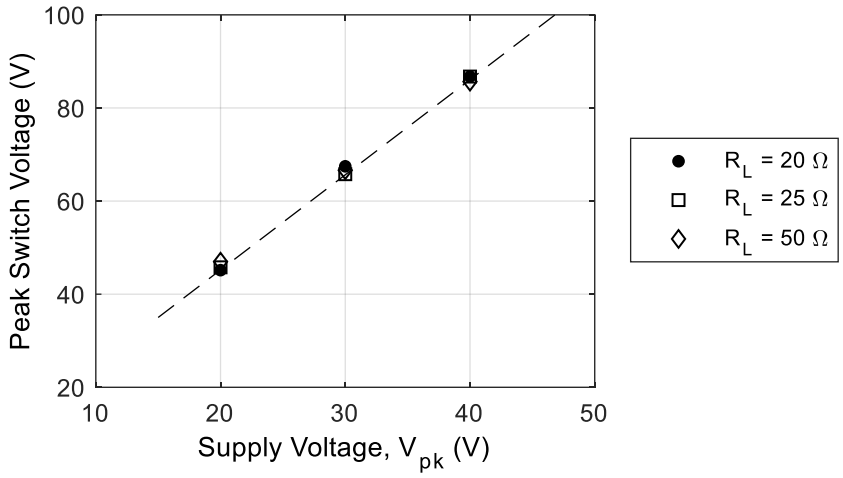


Figure 5.9: Rectifier switch voltage stress in 40.68 MHz wave-shifting converter.

The power delivered to the load is plotted in Figure 5.10. Considering the practical switch voltage limitation, the maximum power that can be delivered to a 20 Ω load at a supply voltage of 47 V is 23 W, which is just 72% of the expected value based on the power capability. The reason for the discrepancy is the imperfect switch node voltage waveform. Whereas the nominal ratio of peak switch voltage to DC voltage is 3.562 [19], ratios between 3.90 and 4.35 were observed in the simulation runs. Hence, the power capability of the simulated converter is less than nominal.

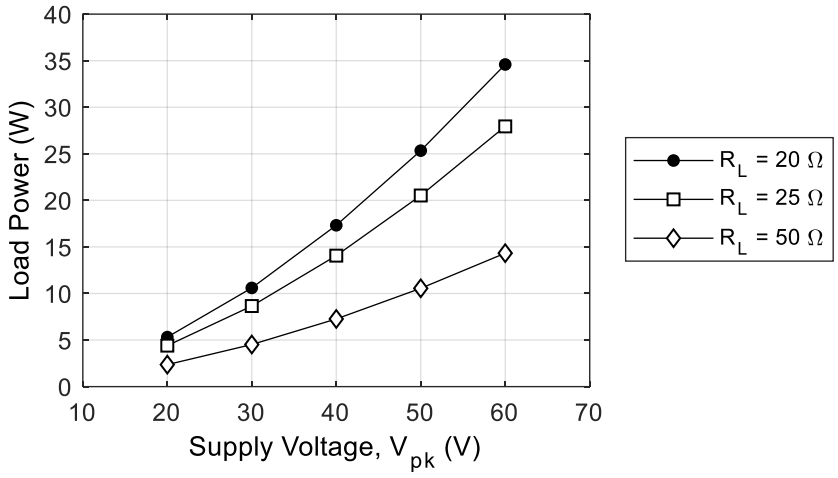


Figure 5.10: Load power in the simulated 40.68 MHz wave-shifting converter.

The impedance R_S seen at the load-side of the supply impedance transformer was measured in the simulated 40.68 MHz converter. The image impedance is consistent, varying by only 35% when R_L = 20 Ω and 51% when R_L = 50 Ω, as the supply voltage is changed by a factor of 3. The simulated and calculated values are plotted in Figure 5.11, which confirms the accuracy of the calculated values.

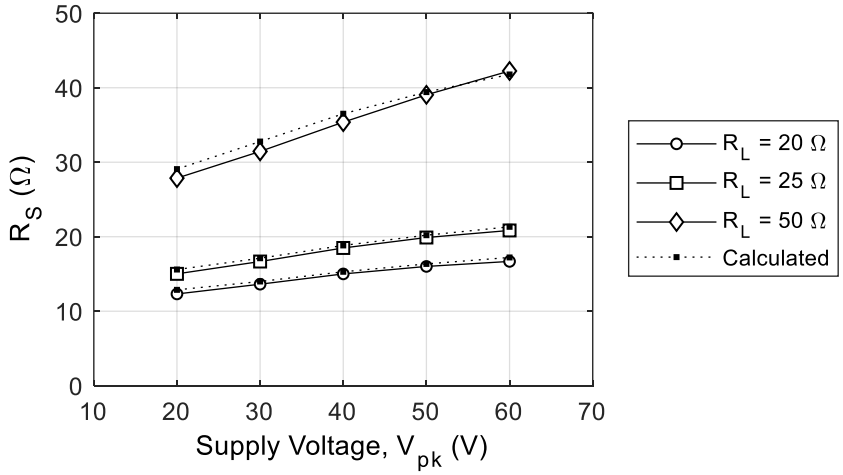


Figure 5.11: Image impedance seen at $v_S(t)$ node in 40.68 MHz wave-shifting converter.

5.9 Summary

In this chapter, a mathematical description of the wave-shifting converter operation has been derived. Expressions for the power and power capability have been determined. The impedances

seen at various points in the circuit have been determined in terms of the converter parameters and load. These impedances are important to achieve high power throughput when interfacing the converter with other components of known characteristic impedance.

Some modifications have been proposed to improve the density of the wave-shifting converter, by combining or removing redundant passive components. Simulation confirms that the modifications are plausible, although the modified converter has not been tested experimentally.

A balanced configuration of the wave-shifting converter is proposed to gain compatibility with balanced capacitive couplers. The “double-negative” balanced configuration is a practical version, despite challenges interfacing to the isolation transformer.

Lastly, a 40.68 MHz model of the wave-shifting converter with an output frequency of 1.27 MHz was developed and tested, to prove the scalability of the design. Models of real GaNFET switches are used for realism.

The 40.68 MHz converter performance generally agrees with the expected behaviour. The maximum load power in the simulated converter is limited by the imperfect rectifier switch node voltage, which has higher-than-nominal peaks. The simulated 40.68 MHz converter achieves a load power of 23 W without exceeding the rated switch voltage, which is 72% of the expected power capability. The simulated converter input impedance is in good agreement with the calculated values from the previous chapter, which confirms that the analysis is correct.

6 High-Frequency Transformer

The wave-shifting converter is intended to be used with an isolated transformer in a complete isolated CPT rectifier system. An experimental transformer was constructed to demonstrate its operation with the wave-shifting converter. The transformer design is based on the proposed design in [13]; however, it is wirewound rather than wire-bonded, which is feasible due to its unity turns ratio. The transformer was constructed from 20 AWG solid copper wire on a T90 iron powder toroidal core, and copper-clad wiring board (see Figure 6.1).

The experimental transformer is not highly optimised, hence it has somewhat poor efficiency. Nevertheless, it effectively demonstrates the operation of the converter with an isolated load.

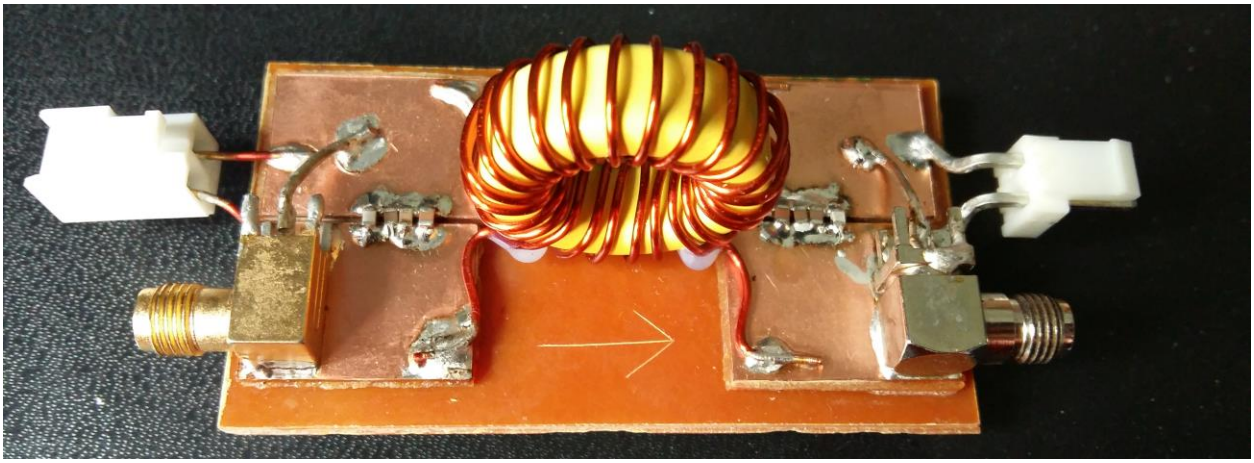


Figure 6.1: Transformer with shunt capacitors. The toroid measures 25 mm in diameter.

A lossy transformer model representing Figure 6.1 is shown in Figure 6.2. The experimental transformer was characterized using a vector network analyzer. Some parameters of the lossy transformer model of Figure 6.2 were populated by direct measurement, while others were estimated. The values in Table 6.1 were measured at 1.695 MHz.

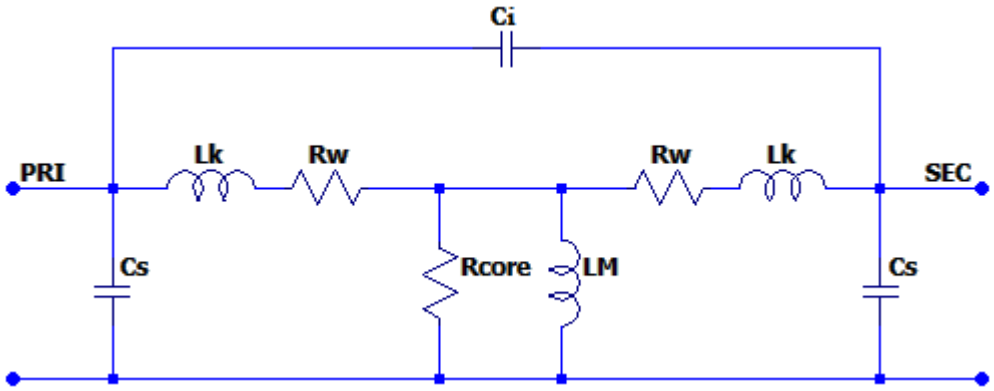


Figure 6.2: Lossy model of the 1:1 transformer.

Table 6.1: Measured values of the experimental transformer.

Port	**Condition**	**Measurement**	
Primary	Open secondary	11.91 Ω	1113.5 nH
	Shorted secondary	102.3 mΩ	248.5 nH
Secondary	Open primary	11.98 Ω	1119.8 nH
Between windings	Shorted primary and shorted secondary	-	13.63 pF

Since the transformer has a 1:1 turns ratio and is physically symmetrical, the primary and secondary component values in the circuit model are assumed to be equal. Using this assumption and the above measurements, an iterative solver was used to characterize the transformer (see Appendix A).

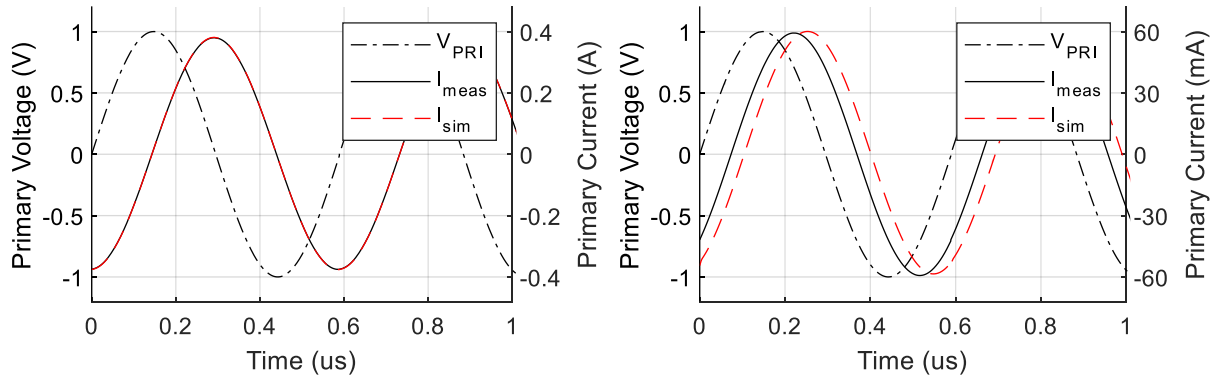
Starting from the lossless transformer model (a T-network of 3 inductors), and assuming that the model is symmetrical, it was found that a leakage inductance of 132 nH and a mutual inductance of 985 nH agrees with the measured values. This was used as the starting point for the solver. The resulting component values are given in Table 6.2.

Table 6.2: Numerical solver component values for transformer circuit model.

Variable	Symbol	Initial Value	Solver Output
Winding resistance	R_w	102.3 mΩ	28.3 mΩ
Leakage inductance	L_k	132 nH	128 nH
Magnetizing inductance	L_M	985 nH	1445 nH
Core loss	R_{core}	500 Ω	33.3 Ω
Winding self-capacitance	C_s	10 pF	360 pF
Interwinding capacitance	C_i	Omitted due to solver limitation.	

6.1 Circuit Model Validation

The circuit model of the transformer was validated by simulation in LTspice. With the secondary winding shorted, the simulated image impedance is identical to the measured value, as shown in Figure 6.3 (a). The simulated primary current with an open secondary winding has the correct amplitude but differs in phase by 33 ns (5.6 % of one cycle) as shown in Figure 6.3 (b). This is equivalent to an image impedance of 7.5 Ω and 1421 nH, whereas the measured value was 11.91 Ω and 1113.5 nH.



(a) (b)

Figure 6.3: Measured and simulated results: (a) Short-circuit test; (b) Open-circuit test.

6.2 Reactance Compensation

With a nominal load of 20 Ω, the image impedance seen at the transformer primary is 8.0 Ω plus 698 nH. This load is significantly reactive and is expected to cause stability problems for the wave-shifting converter, as established in Section 5.2.2.

To achieve efficient operation at nominal frequency, the transformer was compensated with external capacitors to achieve a non-reactive image impedance. The purpose of compensating the transformer in this way is to prevent distortion of the converter voltage and current waveforms.

Shunt capacitors were added to the transformer on the primary and secondary windings. The purpose of these is to achieve parallel resonance with the leakage inductance, thus presenting a resistive image impedance at the primary, when a resistive load is connected at the secondary.

The constructed transformer was tuned to achieve a resistive image impedance at the nominal load of 20 Ω, by adding shunt capacitors of 3100 pF at both the primary and secondary windings. The compensated image impedance with a 20 Ω load is 12.7 Ω due to the transformer core losses, meaning that its efficiency is only 63.5%. The reactance seen at the primary deviates from zero as the load resistance is varied. The trajectory of the image impedance is plotted in Figure 6.4, for load resistances of 15, 20 and 25 Ω. The experimental values are given in Table 6.3.

Table 6.3: Measured image impedance of compensated transformer.

Load resistance (Ω)	**Image impedance**
15	10.7 Ω + 70 nH
20	12.7 Ω
25	14.4 Ω + 110 nF

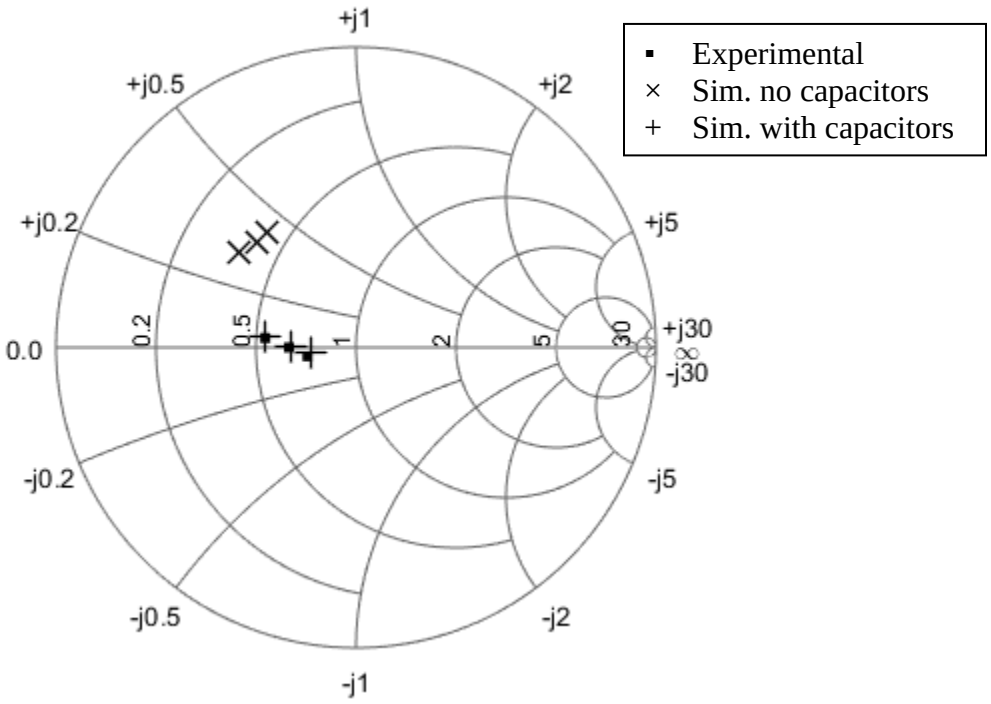


Figure 6.4: Image impedance of the compensated transformer.

6.3 Combination of Output Filter and Transformer

Using the transformer model developed above, it is shown that the wave-shifting converter output filter can be combined with the transformer to reduce component count. It is also shown that the compensated transformer with shunt capacitors outperforms the uncompensated transformer.

6.3.1 Method

A simulated ideal sine-wave source with a DC offset is connected to a full-bridge inverter composed of ideal switches. The input frequency is 27.12 MHz and the output frequency is 1.695 MHz. This source resembles the ideal inverter output voltage $v_{Br}(t)$ of the converter, with V_{pk} = 20 V. The source passes through the constant-K filter designed in Section 3.3.6. The transformer model is connected after the filter and loaded with a nominal 20 Ω resistive load. The complete simulation model is shown in Figure 6.5.

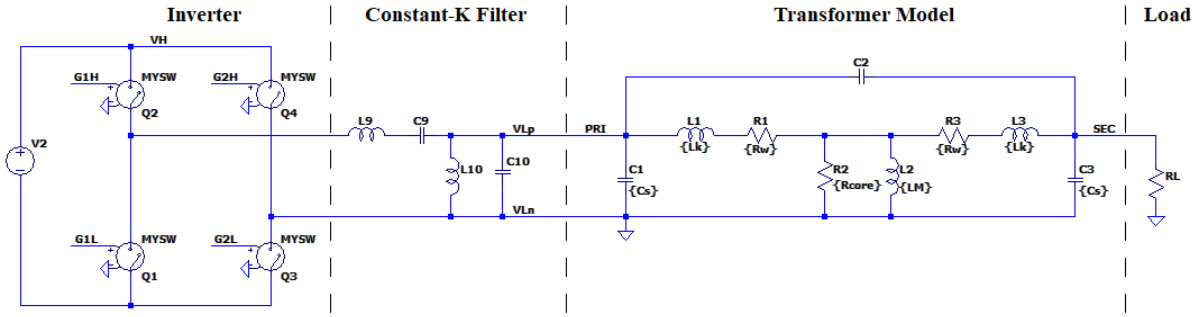


Figure 6.5: Output filter and transformer simulation model.

The load power and efficiency of the converter are considered in four scenarios as follows:

- Uncompensated transformer with reduced filter (removal of filter elements L_{10} and C_{10}).
- Uncompensated transformer with full filter.
- Compensated transformer with reduced filter (removal of filter elements L_{10} and C_{10}).
- Compensated transformer with full filter.

The power supplied by the source and the power consumed by the load are compared to determine the efficiency. It is assumed that the inverter and filter are lossless.

6.3.2 Results

Table 6.4 shows the simulation results for the four scenarios. It is observed that the compensated transformer improves the system power output and efficiency. The reason for this is the reduced reactance in the transformer image impedance, which results in lower losses due to circulating currents. This is shown by the primary currents and phases in Table 6.4. The compensated transformer eliminates the primary current phase lag, resulting in a smaller-magnitude current.

Table 6.4: Simulation results of output filter and transformer.

Test Condition	**Uncompensated Transformer**		**Compensated Transformer**	
	Load Power	**Efficiency**	**Load Power**	**Efficiency**
Reduced Filter	13.66 W	62.2%	16.29 W	64.4%
Full Filter	13.64 W	62.2%	16.28 W	64.4%
	Primary Current	**Phase Angle**	**Primary Current**	**Phase Angle**
Both Filters	1.65 A RMS	43° lag	1.40 A RMS	0°

It is also shown that the performance is not significantly affected by removing the resonant pair L_{10} and C_{10}, since the transformer leakage inductance and shunt capacitance form a similar resonant pair. It is noted that removing this pair results in slightly more harmonic content in the transformer primary voltage. The harmonic content, normalized to the magnitude of the fundamental component, is compared in Figure 6.6. For the full filter, the frequency components at $3f_L$ and $5f_L$ are less than 0.7% of the fundamental, while for the reduced filter they are less than 1.4%. Higher-frequency harmonics are negligible. Thus, the reduced filter performs sufficiently well and offers a reduction in component count.

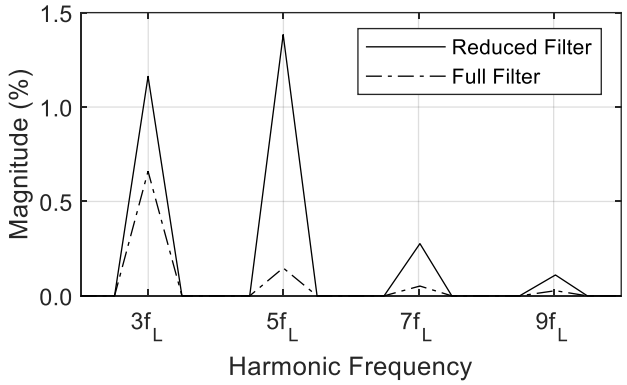


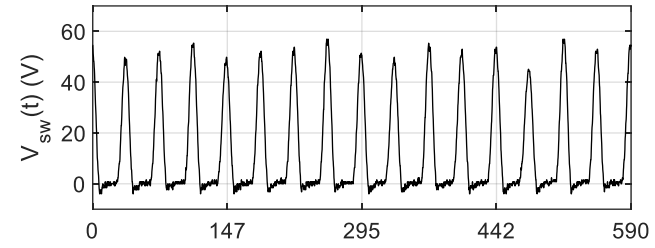
Figure 6.6: Simulated harmonic content of transformer primary voltage.

6.4 The Wave-Shifting Converter with the Isolation Transformer

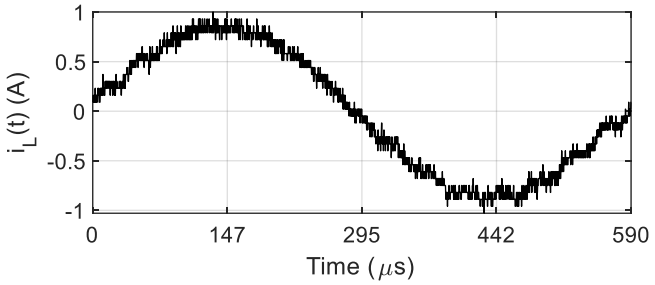
The experimental transformer was connected to the wave-shifting converter output to demonstrate that the system operates as expected with the transformer load. The experimental

converter delivered 7.4 W to a 20 Ω non-inductive load. The DC voltage was 12.3 V and the peak switch voltage was 56.9 V.

The switch voltage and transformer secondary current are shown in Figure 6.7. The switch voltage waveform has the same shape with minor harmonic distortion as was observed without the transformer in the circuit. Therefore, the insertion of the transformer does not interfere with the stability of the converter.



(a)



(b)

Figure 6.7: a) Rectifier switch voltage; b) Transformer secondary current.

6.5 Summary

The wave-shifting converter is intended to be used with an isolation transformer. An experimental prototype transformer was constructed and characterized using a vector network analyzer. An iterative solver was used to populate a lossy model of the transformer, and the model was validated by comparing simulations to the measured values.

The transformer was compensated to eliminate the reactance seen looking into the primary winding when a resistive load is connected. Shunt capacitors were added across the primary and secondary windings to resonate with the leakage inductance at the converter output frequency. It

has been shown that the compensated transformer achieves higher efficiency and power throughput than the uncompensated transformer. Moreover, the image reactance remains small as the load is varied.

It has also been shown that the resonant pair L_{10} and C_{10}, which forms part of the converter output filter, can be removed without significantly impacting the system performance. The compensated transformer has a similar filtering effect that makes L_{10} and C_{10} redundant.

7 Conclusion

A novel multi-megahertz, wave-shifting frequency converter has been proposed and tested in this work. The design is inspired by the line-frequency matrix converter, which inverts a sinusoidal input voltage to produce a lower output frequency. Although the matrix converter achieves zero-voltage switching by toggling at the zero-crossings, the voltage derivative is too high during the switching instants for multi-megahertz operation.

The developed wave-shifting converter circumvents the problem of voltage derivative by applying a DC offset to the input sine wave. The DC offset is equal to the amplitude of the input, resulting in a wave with its valleys at 0 V. Thus, the valleys have zero voltage and zero voltage-derivative, which makes operation at high frequency possible. It has been shown that the wave-shifting converter is feasible for operation at high frequencies in the tens of megahertz, and that it is compatible with the other components required to assemble an isolated rectifier in a capacitively-coupled wireless power system.

The DC voltage offset requires a resonant rectifier to be implemented. A load-independent Class-E rectifier design was selected, which has a minimal number of components. The load-independent rectifier behaves consistently as the load on the converter changes, which makes it more practically useful. The load-independent rectifier demands a synchronous switch, because in some loading conditions reverse current flows through the switch.

The inverter switching in the wave-shifting converter is synchronized to the rectifier. A single trigger circuit based on a voltage comparator feeds the rectifier and inverter gate drivers. The rectifier toggles at the input frequency, while the inverter toggles at the output frequency. The lower frequency signal that drives the inverter is derived from the trigger output by a digital clock divider.

Because the proposed wave-shifting converter is not an AC-DC-AC converter, it has the interesting property that the power flowing through its rectifier is less than that which is delivered to the load, especially at small values of the frequency division factor. In an application

requiring a relatively small change in frequency, this would be advantageous from an efficiency point of view. The converter as developed requires many inductors which have a significant contribution to the overall power losses in the circuit. However, the efficiency can be improved and the size of the components can be reduced by combining the impedance transformer networks. Furthermore, it has been shown that the output filter can be reduced to a single inductor-capacitor pair by taking advantage of the filtering effect of the isolation transformer.

In all aspects, the requirements placed on the rectifier switch are more demanding than the requirements for the inverter switches. The rectifier switch experiences higher peak voltages than the inverter switches, and must have low output capacitance.

The wave-shifting converter feeds a combined sine wave and DC voltage into an inverter, and this produces a voltage waveform containing odd harmonics of the output frequency. These harmonics create challenges for the stability of the rectifier and the quality of the output power. The distribution of harmonics has been calculated; it has been shown that the harmonic content is related to the frequency-domain representation of a square wave. Harmonic content in the inverter output defines the output filter specification – the filter must pass the fundamental and stop the 3rd harmonic of f_L.

Analytical expressions for the image impedances at multiple points within the circuit have been derived. Thus, the input impedance of the converter can be expressed in terms of the load resistance which is valuable for interfacing with other circuits. Because of the harmonic content present at various nodes in the circuit, it is useful to calculate impedances as the mean square of voltage divided by the mean power ($R = v^2/P$). This is a robust approach that can also be used on simulation data, where the simpler Ohm's law formulation ($R = v/i$) results in singularities due to a time-varying current. The former equation is used multiple times in the analysis of the converter.

7.1 Future Work

In the future, it is desired to experimentally test the suggested improvements to the wave-shifting converter design. These fall into two categories; those that increase the stability of the converter, and those that improve the efficiency and power density.

Other future work calls for a complete system test including the wireless resonator, wave-shifting converter, isolation transformer and low-frequency rectifier. The system test would confirm the effectiveness of the isolation and would provide a benchmark for the total system power capacity and efficiency.

7.1.1 Stability Improvements

Instability of the rectifier was the most important problem encountered in the experiment. It is desired to test a more robust trigger circuit to eliminate subharmonic oscillation at higher power levels.

7.1.2 Power Density Improvements

The power density of the converter can be increased by reducing the size and number of reactive components. First, the DC-blocking capacitor C_2 at the rectifier input can be removed, and the L_2 inductance can be reduced correspondingly. Second, combining the impedance transformers into a Y-network as discussed in Section 5.6.1 is expected to increase efficiency at the cost of more complicated tuning.

Some improvements to the circuit board layout are suggested. Better thermal management is needed for the rectifier switch since it is the hottest component in the experimental prototype. In the existing experimental unit, the rectifier switch is connected to a small copper area of only about 2 cm^2, which is inadequate for passive heat dissipation. The power capacity of the experimental converter was limited by the rectifier switch temperature. Furthermore, parasitic inductance between the rectifier and inverter should be reduced. To be precise, the length and loop area of the low-frequency and DC current paths of Figure 5.3 should be minimized.

7.1.3 Experimental Testing of Double-Negative Balanced Configuration

It is desired to test the balanced configuration of the wave-shifting converter configuration of Section 5.7 experimentally. This could be performed practically by joining the two existing 27.12 MHz unbalanced experimental units at their ground and V_{DC} nodes.

There are two options for implementing the isolation transformer in the balanced configuration, as discussed in Section 5.7. The simpler option is to use two independent isolation transformers

and low-frequency rectifiers. The other option is to construct a dual-primary transformer that would be fed by both inverters, and this would require the inverters in each branch to be synchronized with each other.

For the dual-primary transformer, it is recommended to build a modified trigger circuit with inputs from both rectifiers being compared by a single voltage comparator. The comparator output should be passed through inverting- and non-inverting logic buffers to drive the synchronous switches of both rectifiers. This arrangement would ensure that the rectifiers are driven with equal duty cycle and opposite phase. Independent RC adjustments should be included for both branches.

Lastly, a single clock divider should drive both inverters, with an appropriate delay introduced between the two branches. Using a single clock divider is the most robust way to keep the inverters synchronized with each other, rather than attempting to synchronize two independent clock dividers.

7.1.4 Positive-Negative Balanced Configuration

An alternate version of the balanced converter may be realized, having one positive and one negative rectifier. In this version, there are positive and negative inverters, each fed by its respective rectifier and input terminal. A block diagram of the positive-negative configuration is shown in Figure 7.1.

In the positive-negative version, the voltages present at the inverter inputs are symmetrical to each other about the 0 V axis, and thus both inverters may operate in-phase. (The inverters could also operate out-of-phase by an integer multiple of T_0.) The benefit of this version over the double-negative configuration of Section 5.7 is that this version is compatible with a dual primary transformer, regardless of the frequency division factor.

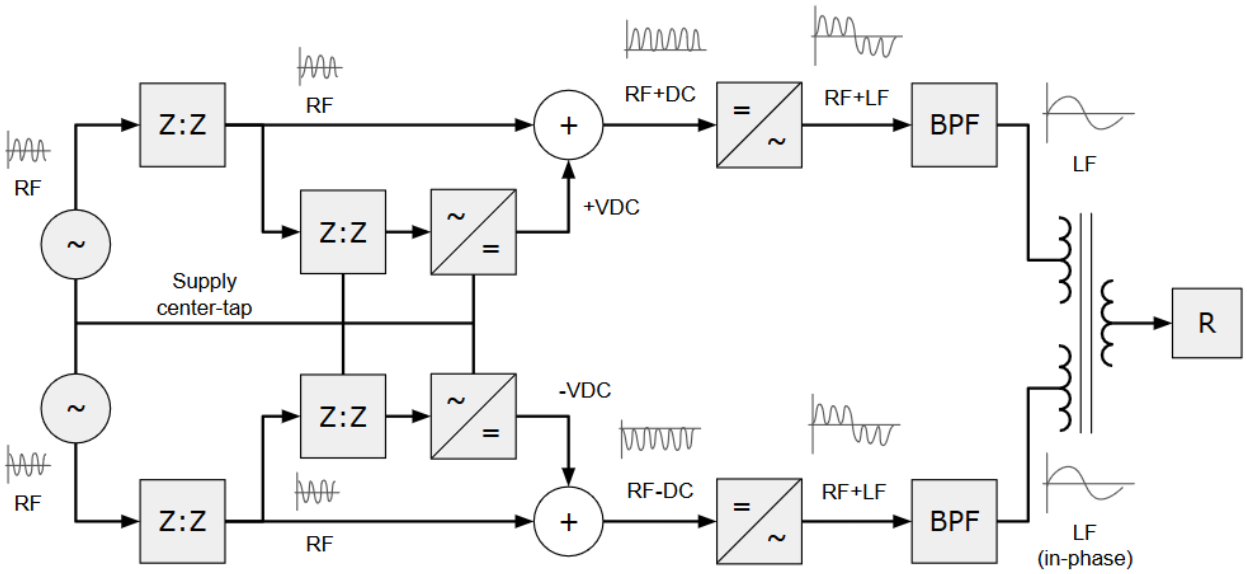


Figure 7.1: Block diagram of the positive-negative balanced wave-shifting converter configuration.

A major drawback of the positive-negative configuration is that the $+V_{DC}$ inverter has high-frequency voltage at its negative input terminal. Practical H-bridge drivers are typically referenced to the negative input terminal of the H-bridge, so electric field emissions from the gate driver's local ground plane would be a problem. To make this work would also require an isolated DC-DC converter for logic supply. In the future a suitable inverter may be developed to make the positive-negative configuration more practical.

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Appendix A: Passive Network Solver

A small Java program was written to assist with characterization of the experimental transformer and with filter designs. The program takes as input a passive two-terminal network consisting of series or shunt resistors, capacitors, and inductors. Some "evaluators" are defined, each having a set of test conditions and an optimization criterion. The network is evaluated by each evaluator, resulting in a unitless real number referred to as "merit". A merit of 1 means that the network perfectly satisfies the evaluation criteria, while a merit of 0 means that the network is unsatisfactory. Various evaluators are combined to yield a network with specific behaviour.

In each design iteration, one or more component values are adjusted by a small amount, and the product of all merits from all evaluators is calculated. If the total merit is greater than the previous best, the changes are kept, otherwise they are discarded. The program traverses all combinations of adjustments up or down until no further improvements to the network are possible, after which the adjustment size is decreased, and iteration continues. The program stops after a fixed number of iterations.

The solver program is alpha software and has no user interface. Different networks and evaluators are entered in the source code and compiled directly. The program results are displayed as text in the Java console.

The source code for the solver is available on the author's GitHub website: https://github.com/tseary/FilterNetwork.

A sample output from the program is shown below, which was used to estimate component values for the experimental transformer based on VNA measurements:

```
ImpedanceEvaluator[TestCondition[load=R6 1.000 mOhm resistor, f=1.695 MegHz], ideal
Zin = 0.102 + j2.647]
       merit = 0.9999993327307733
ImpedanceEvaluator[TestCondition[load=R7 1.000 MegOhm resistor, f=1.695 MegHz],
ideal Zin = 11.950 + j11.896]
```

```
       merit = 0.804970258952531
ImpedanceEvaluator[TestCondition[load=R7 1.000 MegOhm resistor, f=1.795 MegHz],
ideal Zin = 12.650 + j12.598]
       merit = 0.8198076781728217
ImpedanceEvaluator[TestCondition[load=R7 1.000 MegOhm resistor, f=1.595 MegHz],
ideal Zin = 11.250 + j11.194]
       merit = 0.7887054129587827

Stopped after 67962 iterations.
Network of 8 components:
 |-C--| shunt  C1 359.9 pF capacitor
 |    R series R3 28.32 mOhm resistor
 |    L series L2 128.4 nH inductor
 |-L--| shunt  L4 1.445 uH inductor
 |-R--| shunt  R5 33.28 Ohm resistor
 |    L series L2 128.4 nH inductor
 |    R series R3 28.32 mOhm resistor
 |-C--| shunt  C1 359.9 pF capacitor

Input Z (shorted secondary) = 0.102 + j2.647
observedZinShort = 0.102 + j2.647

Input Z (open secondary) = 7.287 + j15.206
observedZinOpen = 11.950 + j11.896
```