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COMPARISON OF MIXED ANALOG-DIGITAL SIMULATORS

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1. INTRODUCTION

The rapid growth of application specific integrated circuits (ASICs) and the need to fabricate chips that work the first time, have created a demand for simulators capable of analyzing both analog and digital circuits at varying levels of detail and accuracy [1-5]. Most of today's simulation programs are unable to model and simulate both the digital and analog components of a typical ASIC. The result is insufficient simulation before fabrication and an increased number of design cycles necessary for a successful design.

This paper examines the background, requirements, and several approaches to mixed analog-digital simulators; it also presents the results of benchmarking two commercially available and one public domain mixed analog-digital simulators on a 4-bit successive approximation analog-digital converter which has been fabricated. The results are presented in a consistent manner which allows realistic comparisons to be achieved between the various simulators. The capabilities of mixed analog-digital simulators which are required to meet the needs of ASICs are identified.

2. MIXED ANALOG-DIGITAL SIMULATION

Mixed analog-digital simulation implies the capability to analyze circuits containing both analog and digital components in a single simulator. The implementations of mixed analog-digital simulation vary widely. In general, three approaches exist. These methods are (1) use an analog simulator to perform both analog and digital simulation [6,7], (2) use a digital simulator to perform both digital and analog simulation [8,9], and (3) use both a digital and analog simulators coupled together; the degree of coupling and timing coordination distinguishes from several such examples [10-12]. In the first method, the digital elements are usually analyzed by the same mechanisms as the analog ones, which results in too accurate but also too inefficient simulation. The second approach extends the digital (discrete) methods to analog elements which usually provides quite efficient but rather inaccurate simulation. Only the coupled approach can combine the advantages of analog (accurate) and digital (efficient) simulations, however, this usually depends upon the level of coupling. Loosely coupled simulators basically execute two independent simulation programs (analog and digital) that "communicate" whenever they need information from the other part of the circuit; they are relatively simple to design but perform simulation of mixed analog-digital circuits neither really accurately nor efficiently. Tightly coupled or integrated simulators [5] "synchronize" the two simulation mechanisms at the level of internal timesteps and time event control, so they can easily avoid any redundant evaluations without any loss of accuracy.

It is important to observe that multilevel simulation plays an important role in mixed analog-digital simulation. Multilevel simulation is defined as the ability to simulate various components of a circuit at different levels of abstraction [13]. No mixed analog-digital simulator will be capable of simulating typical ASICs without making use of simulation hierarchy.

It is equally important to note that simulation hierarchy occurs in the modeling rather than the simulation engine. Various levels of modeling have been described as circuit, macromodel (or functional), and behavioral. These levels can be distinguished by model primitives or structural implications [14]. This is a challenging problem because increasing level of model abstraction increases the efficiency of simulation, but reduces the accuracy. This tradeoff must be made in a manner that does not eliminate important model characteristics.

3. BRIEF DESCRITION OF SIMULATORS

SPICE-PAC [15]

SPICE-PAC is a public domain simulation package that has been derived from the SPICE-2G simulation program; it is a typical example of a modular tool with an "open" structure (as opposed, for example, to the SPICE program which is functionally "closed") which means that it can easily be integrated with other software tools like optimization methods, yield analyzers, or other simulators. By decomposing the simulation process into a number of relatively independent tasks, it allows users to control the analyses as well as data structures at different stages of simulation. SPPAC includes full SPICE-2G capabilities plus a hierarchical circuit description, dynamic redefinition of circuit elements, parameterized subcircuit calls, table driven elements, and several interfaces to user-defined extensions of element characteristics or circuit analyses.

One such extension has been built into SPICE-PAC's implementation of the time-domain analysis. After each successful (internal) timepoint solution, an "external" routine is called that may impose additional conditions and/or constraints on the solution. In particular, such external routine can perform simulation of the digital part of a circuit (if the required conditions are satisfied; e.g., if there is a change in the input signals). And since the routine can be defined, redefined and modified by users, a very flexible mechanism is provided that allows very efficient simulation at any level of abstraction. However, the

flexibility is achieved at the cost of convenience; since each application potentially requires an independent external control, and this external control cannot be implemented without expert knowledge of simulation details and technicalities, quite often a simpler, less efficient but more convenient solution will be sought.

A truly integrated tightly coupled simulator composed of an analog and digital simulation engines offers reasonable efficiency, flexibility and "user-friendliness" required by typical applications. YADIS [16] integrated at the level of time-event control with SPICE-PAC is an example of integrated tightly coupled mixed analog-digital simulator that uses multilevel thresholders and voltage sources with piecewise linear characteristics triggered by digital signals for analog-to digital and digital-to-analog conversions, respectively.

PSPICE [10]

PSPICE program is an analog simulator with a "digital simulation" option that provides a 28-state, event-driven logic simulation. Digital circuit elements are included in the input files in the same way as the analog elements, and it is the simulator's task to recognize all analog-digital interfaces and perform the conversion of signals.

PSPICE recognizes three kinds of nodes, analog, digital and interface nodes. The type of a node is determined by the type of the devices connected to it. If all the devices are digital (analog), the node is digital (analog); if there is a mix of devices then it is an interface node. For analog nodes PSPICE calculates node voltages; for digital nodes it calculates logic states; for interface nodes PSPICE automatically creates interface blocks which depend upon logic families used in digital circuitry (the libraries of digital components include definitions of interface blocks).

Digital nodes have only three levels, "0", "1" and "X" (or "unknown"), but each level can be combined with one of four strengths, "forcing", "driving", "weak" and "high-Z". This creates 12 so called states. In addition, there are 16 states used to describe in more detail nodes that are driven with conflicting signals.

Most digital components use two models, the timing model that describes the device's timing characteristics, and the in-out model that specifies the device's loading and driving characteristics. The propagation delays are set by the sum of the delays of the timing model and additional delays determined by the circuit's loading. Loading delays are calculated for each device by looking at the connections and their capacitances; these calculations are performed only once, during initial preprocessing of the circuit.

SABER [6]

SABER is a commercial simulator developed to provide a multilevel modeling capability in analog circuits and systems. It has been extended to include digital models which are interfaced with the simulator through the model interface. The primary advantage of SABER is its ability to conveniently use higher level analog models. SABER is an example of an analog simulator extended to digital simulation.

4. THE BENCHMARK CIRCUIT

The example chosen to benchmark the above simulators needed to be representative of ASIC circuits, be fabricated, and to have information available about the design. The circuit chosen was a three-bit flash analog-to-digital converter. It met the necessary requirements and had the advantage of being extended in complexity by simply increasing the number of bits. The three-bit flash converter is shown in Fig.1.

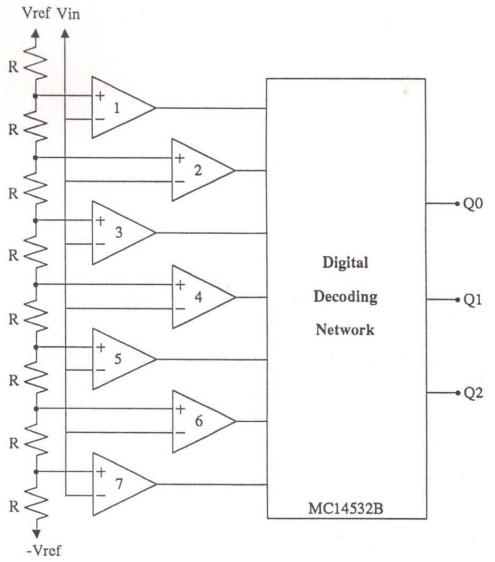

Fig.1. 3-bit flash analog-to-digital converter.

The converter consists of ananalog front-end and a digital back-end. The front-end is composed of a resistor string and $2^n - 1$ comparators where n is the number of bits. The back-end is a Motorola M14532B 8-bit priority encoder. Each comparator compares the input voltage to a fraction of the reference voltage. The decision of each comparator is used as an input to the digital decoding network. Table 1 shows the number of components and the modeling level ased in the simulations. The "standard" delay of 10ns is used for all digital elements.

Elements	Number of Elements	Model Level
Resistor	8	SPICE model
Transistor	140	SPICE model
Logic gate	30	SPICE model
Resitor	8	SPICE model
Comparator	7	macromodel
Logic gates	30	gate delay

Tab.1. Component summary.

The comparator was modeled at the device and macro level. This allowed for the comparison between circuit complexity and modeling level. The circuit level of the comparator is shown in Fig.2 and the macromodel of the comparator is shown in Fig.3.

All simulations were run on a SUN 3/260 to allow for realistic side-by-side comparison of the simulation times.

5. TRANSIENT ANALYSIS OF A RAMPED INPUT

The simulation performed was a transient analysis from 0s to 1s (with as increment of 0.1s). The inputwas

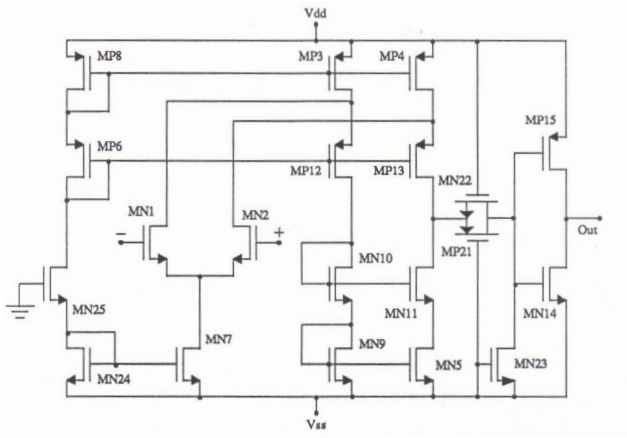

Fig.2. Two-stage cascode CMOS comparator.

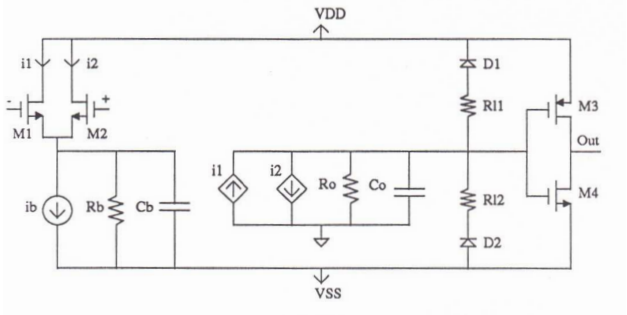

Fig.3. Macromodel of CMOS comparator.

"ramped" from -2.5V to +2.5V over the simulation period. The purpose of this simulation was to verify the functionality of the converter as this analysis took the converter through all of the bit transitions. Ideally, switching of the output bits should take place at 0.125s, 0.250s, 0.375s, 0.500s, 0.625s, 0.750s and 0.875s. The large timestep allowed for determining if the converter's output was correct for "discrete" voltages. A DC sweep would have been used but SABER's digital models are only good for time-domain analysis. The results reveal each simulator's ability in handling a complex circuit and a long transient run. Simulation times (in seconds) are shown in Table 2 and a sample output is shown in Fig.4.

	Modeling level	
Simulator	circuit	macro
SPICE-PAC (3)	1544.02	213.70
SPICE-PAC (7)	2812.16	362.24
PSPICE	2030.62	537.23
SABER	5390.00	365.00

Tab.2. Simulation times for a ramped input.

SPICE-PAC

In SPICE-PAC, the accuracy of analog-to-digital conversion is controlled by aparameter that determines the accuracy of the conversion. The results are shown for two values of this parameter; the value 3 corresponds to (approximately) 10value, 7, corresponds to 1

At the circuit level simulation, the "inaccurate" results (parameter = 3) showed switching of the output bit at

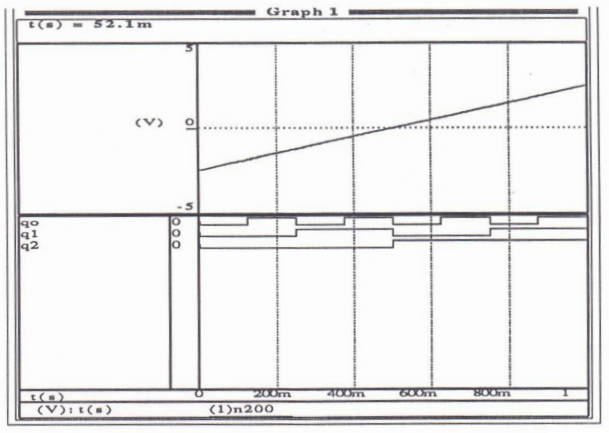

Fig.4. Waveforms for ramped input.

0.128s, 0.253s, 0.378s, 0.503s, 0.631s, 0.751s and 0.876s. For the conversion parameter equal to 7, the reults were 0.125s, 0.250s, 0.376s, 0.500s, 0.625s, 0.750s and 0.875s which are almost ideal.

Very similar values were obtained at the macrolevel of simulation in significantly reduced simulation times.

PSPICE

The results of the circuit level simulation showed that switching occurred at the ideal times.

The macromodel level simulation results were also ideal. All of the bits switched at the proper times.

SABER

At the circuit level simulation, the density (accuracy/speed trade off) was increase to 300 and NSDEN, the Newton step density, was increased to 4. The results for the circuit level simualtion showed switching at the ideal times.

At the macro level simulation, the density was set to 16 and NSDEN was set to 1 (default). The results showed that switching occurred at the ideal times.

6. TRANSIENT ANALYSIS OF A STEP INPUT

The simulation performed was a transient analysis from 0μs tp 20μs with the im=nput voltage switched from -2.5V at 1μs to 5mV at 1.01μs. Ideally, the corresponding digital outputs should switch from 000 to 100. However, because of dlays in comparators and in digital elements, the output will be invalid during a certain period of time. The simulation reveals the dynamic aspects of the circuit (delay in output change with respect to input) and the ability of each simulator in characterizing these aspects. The simulation times (in seconds) for this analysis aer shown in Tab.3.

	Modeling level	
Simulator	circuit	macro
SPICE-PAC (3)	1343.26	300.12
SPICE-PAC (7)	1573.70	318.88
PSPICE	1062.40	210.33
SABER	4350.00	144.00

Tab.3. Simulation times for a step input.

SPICE-PAC

As before, two values of the conversion parameter were used, namely 3 and 7. The differences in the corresponding simulation times are less significant in this case as the number of conversions is much smaller than for the ramped input.

For the circuit level simulation, the delays (between actual and ideal switching times) of 2.53μs and $2.47'mu$s were observed; at the macro level simulation, the delays were $2.65'mu$s and $2.56'mu$s for less and more accurate convesions, respectively.

PSPICE

The results of the circuit level simulation were consistent with the expected results. The simulator showed that 2.69μs of delay occurred before the output stabilized at 100.

The results of the macro level simulation are similar to the circuit level simulation. The simular gave a delay of 2.62μs before the output stabilized.

SABER

In the circuit level simulation, The density (accuracy/speed trade off) was increased to 300 and NSDEN was increased to 4. The results are consistent with the expected results. A delay time of 2.56μs was observed before the output stabilized.

The macro level simulation was similar. The density was increased to 16 and NSDEN was set to the default value, 1. A delay time of 2.75μs was observed.

7. CONCLUSIONS

Two commercially available (PSPICE and SABER) and one public-domain (SPICE-PAC) simulators with mixed analog-digital simulation capabilities were used to perform the same set of analyses for a 3-bit flash analog-to-digital converter used as a benchmark example. The results obtained for this circuit indicate that the macromodel is quite accurate as the simulations at the circuit level and the macrolevel are practically the same. On the other hand, the simulation times for the circuit level are four ro ten times greater than for the macro level; the same ratio for SABER is in the range of several tens.

The strong points of SABER seem to be in the modeling flexibility; it handles different models quite efficiently while at the circuit level it is clearly outperformed by both PSPICE and SPICE-PAC.

SPICE-PAC is basically a circuit level simulator which (presently) cannot take advantage of "inactive" periods during time domain analysis; in the case of step input, long time intervals are inactive while SPICE-PAC still performs all the internal timestep analyses. This inadequacy could be corrected be setting some SPICE-PAC's parameters, howver, no "adjustments" were made in order to preserve consistency between the simulation.

All simulations were performed with the default values of tolerances. At the circuit level of simulations, initial conditions were used in the case of SPICE-PAC because of some convergence problems in the initial transient solution. At the circuit level simulation in using PSPICE, some limits on the number of iteration steps wwre increased in order to avoid convergence difficulties.

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