FIT-2, AN EXTRACTION PROGRAM BASED ON THE SPICE-PAC SIMULATION SOFTWARE

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Accurate and reliable simulation of a circuit behaviour cannot be obtained without adequate device models. FIT–2 is an interactive program for extraction of transistor parameters for SPICE–like circuit simulators. It is based on a circuit simulator rather than an explicit set of model equations. Several optimization methods are built into the program to provide robust as well as efficient fitting of device characteristics. Flexibility of the approach is obtained by specification of extraction details in the data sets rather than the extraction procedure. Several directions for further research are identified.

1. INTRODUCTION

Reliable circuit simulation cannot be obtained without accurate specification of circuit elements and device models. Existing device models use large sets of parameters, values of which must be properly determined to represent device characteristics accurately. Usually these parameters cannot be determined by direct measurements because of highly nonlinear device models; popular extraction methods use iterative techniques to minimize differences between measurement data and model behaviour in the full range of operating conditions.

There are several approaches to parameter extraction:

- extraction methods can be general or specialized; specialized methods extract subsets of model parameters only, for example, model resistances, or capacitances [CFG], or DC parameters [IG];
- parameter extraction can be direct or iterative; direct methods approximate model equations by linear functions and determine the values of parameters graphically or by solving linearized equations; iterative methods fit the model equations to a set of measured characteristics by minimizing an objective function that characterizes the fit [DS,CCLL,Gar]; quite often a mixed approach is used in which some parameters are extracted using the direct methods, and remaining by an iterative procedure [DJ,IG];
- iterative methods can be equation-based or simulation-based; equation-based methods use a set of model equations to obtain device responses that correspond to measurement data [DS,EGMT]; in simulation-based approach, a circuit simulator (or its part that handles devices and their models) is used to provide circuit responses;
- simulation-based methods can be program-driven or datadriven; in program-driven approach the structure of the data as well as the sequence of processing steps are determined by the extracting software; data-driven approach is more flexible to use but also more difficult to implement as the extraction "strategy" is specified together with the measurement data, and the extracting program mainly recognized and executes extraction directives formulated in some sort of "high-level language".

The approach presented in this paper is iterative, simulation– based and data–driven; it uses an "open" circuit simulation tool rather than traditional set of model equations. Basic advantages of such an approach include:

- explicit model equations need not be known as the required circuit responses are provided by a general circuit simulation tool (additionally, potential inconsistencies between model equations used by the extractor and equations implemented in simulation tools are eliminated in this case),
- the same extractor can be used for a variety of devices and/or device models; the actual limitations are imposed by the tool used for circuit simulation rather than by the extractor,
- fitting can be performed not only for single devices (as is the case for equation-based extractors) but for any (sub)circuits as well; consequently, all packaging, mounting and fixture parasitics [EGMT] can easily be taken into account.

The paper describes the organization of data and the structure of the extraction program; it also discusses the formulation of the objective function in greater detail and identifies a number of further improvements. Extraction results for heterojunction bipolar transistors are used as an illustration of program capabilities.

2. INPUT DATA

Input data for the FIT–2 program are organized into three independent files: the circuit file, the variables file, and the measurement data. Typically, measurement data correspond to DC measurements, frequency–domain and/or time–domain measurements. Moreover, DC measurements are in CB or CE configurations, in forward or reverse mode.

The circuit file contains the description of a circuit that corresponds to the measurement environment (including all parasitics). If extraction is performed on a (sub)circuit level rather than for a single device (e.g., the transfer curve of an inverter is fitted rather than characteristics of transistors), the circuit file must describe the corresponding (sub)circuit as well as any measurement related components.

The following fragment shows the circuit description for extraction of DC parameters of a heterojunction bipolar transistor (CB and CE configurations, forward and reverse modes):

```
**** subcircuit TRPAR : transistor with parasitics
.SUBCKT TRPAR 1 2 3
QA 1 5 3 HBT
RBN 5 2 50
RFCB 1 2 1E8
RFCE 1 3 1E8
RFBE 2 3 1E8
CFCB 1 2 1E-16
CFCE 1 3 1E-16
CFCE 2 3 1E-16
.ENDS
```

.MODEL HBT NPN (IS=6.79D-24 BF=96.4 NF=1.057 VAF=229 IKF=5.05 ISE=1.44D-17 NE=1.67 BR=0.28 NR=1.060 VAR=104 IKR=1.00D-10 + ISC=1.38D-11 NC=2.21 RB=27.7 IRB=6.29D-3 RBM=15.30 RE=9.12 + RC=26.5 CJE=1.58D-13 VJE=1.80 MJE=0.50 TF=3.76D-12 XTF=01. VTF=100 ITF=0 PTF=0 CJC=1.09D-13 VJC=1.4 MJC=0.5 XCJC=0.15 + + TR=3.76D-12 CJS=0 VJS=0.75 MJS=0 XTB=0 EG=1.4 XTI=3.0 KF + AF=1.0 FC=0.5) **** CB forward and reverse XCB 101 102 103 TRPAR VE 0 103 0 VB 0 102 0 VC 0 101 0 **** CE forward and reverse; parameter: IB'DC XCE 201 202 0 TRPAR ECE 201 203 0 203 2.0 VCE 203 DC=4 0 DC=2E-4 TB 209 202 VIB 0 209 0 .END

The second file describes all variables and their lower and upper bounds (which are used as optimization constraints); it also contains the nominal values and the actual values of variables (initially actual values are equal to nominal values); the actual values - during extraction - are replaced by the results of optimization. For the circuit description shown above, the variables file contains all transistor model parameters as well as parasitics defined in the subcircuit TRPAR:

* var	min	nom	max	act
HBT'IS	1.0D-24	6.79000D-24	1.0D-23	6.79000D-24
HBT'BF	1.0D+01	9.64000D+01	1.5D+02	9.64000D+01
HBT'NF	1.0D+00	1.05700D+00	1.0D+00	1.05700D+00
HBT'VAF	1.0D+01	2.29000D+02	3.0D+02	2.29000D+02
HBT'IKF	1.0D+00	5.53000D+00	1.0D+01	5.53000D+00
HBT'ISE	1.0D-30	1.44672D-17	1.0D-16	1.44672D-17
HBT'NE	1.6D+00	1.66752D+00	1.8D+02	1.66752D+00
TRPAR.RBN	1.0D-03	5.0000D+01	1.0D+02	5.0000D+01
TRPAR.RFCB	1.0D+05	1.00000D+08	1.0D+10	1.00000D+08
TRPAR.RFCE	1.0D+05	1.00000D+08	1.0D+10	1.00000D+08
TRPAR.RFBE	1.0D+05	1.00000D+08	1.0D+10	1.00000D+08
TRPAR.CFCB	1.0D-16	2.56330D-15	8.0D-15	2.56330D-15
TRPAR.CFCE	1.0D-16	2.35640D-15	8.0D-15	2.35640D-15
TRPAR.CFBE	1.0D-16	5.61994D-15	1.0D-14	5.61994D-15

It should be noted that during the extraction process it is possible to store any partial results in a file, and subsequently use such stored results as the variables file; the extraction process can thus be stopped at any stage, its "state" saved, and restored when needed. This capability is the reason of dividing the circuit description and the specification of variables into two independent files.

The file of measurement data contains a sequence of data "groups", each group describing one type of measurement results such as DC–CB–F (DC measurements in CB configuration and forward mode), DC-CB-R, DC-CE-F, DC-CE-R, or AC (Sparameters) for a given bias point. Each data group is a rectangular table of numerical results that corresponds to one independent variable and a number of (dependent) results. For example, the following group:

!IDENT:ICVC-F(IB) !' PLAQUE: 129_19, DISPO: BIP, TYPE: T1C, POSIT: 8_5_1' : 11 Dec 1989 AT 22:11:17' !' DATE VCE 5.E-5 1.E-4 1.5E-4 2.E-4 2.5E-40.00 -4.993E-5 -9.990E-5 -1.499E-4 -1.999E-4 -2.499E-4 0.20 -4.899E-5 -9.798E-5 -1.468E-4 -1.954E-4 -2.438E-4 1.299E-4 1.963E-4 2.351E-4 2.570E-4 2.705E-4 0.40 4.936E-4 1.140E-3 1.556E-3 1.785E-3 1.934E-3 0.60

5.3 80	5.024E-4	1.314E-3	2.323E-3	3.394E-3	4.165E-3
0.600	5.039E-4	1.318E-3	2.339E-3	3.555E-3	4.961E-3
2920	5.048E-4	1.320E-3	2.343E-3	3.561E-3	4.972E-3
010	5.054E-4	1.321E-3	2.346E-3	3.563E-3	4.974E-3
5.260	5.060E-4	1.323E-3	2.348E-3	3.564E-3	4.976E-3
= 080	5.068E-4	1.324E-3	2.348E-3	3.566E-3	4.976E-3
.00	5.072E-4	1.325E-3	2.350E-3	3.566E-3	4.973E-3
2.40	5.082E-4	1.327E-3	2.352E-3	3.567E-3	4.970E-3
.80	5.091E-4	1.328E-3	2.354E-3	3.567E-3	4.968E-3
.20	5.096E-4	1.329E-3	2.355E-3	3.567E-3	4.963E-3
6.60	5.106E-4	1.331E-3	2.356E-3	3.567E-3	4.959E-3
.00	5.115E-4	1.332E-3	2.358E-3	3.567E-3	4.956E-3

2 2

2 3

3

4

describes (the !IDENT line) the DC measurements of the collector current in CE configuration and forward mode, with IB as the parameter (observe that IB must be a valid name of an independent current source in the circuit file because it is used by the extractor to set the values of this source during circuit simulation); similarly, VCE (in the line describing column headers) must be a valid name of an independent voltage source that is used for the voltage sweep in the DC analysis; the values of VCE can be arbitrarily distributed as SPICE-PAC can perform "data-driven" circuit analyses in which a table of explicit VCE values determines the DC analysis points. The remaining values in the header line are IB values associated with collector current curves as functions of VCE voltage.

There is no limit imposed on the number or composition of data groups; in fact, a section of one data group can be repeated (with more data points) as another data group to obtain better fit in regions which are believed to be more important or more difficult for fitting (e.g., initial parts of characteristics or highly nonlinear regions).

3. EXTRACTION THROUGH OPTIMIZATION

Extraction of transistor parameters can be formulated as an optimization problem [CCLL,DS,Gar,MMD,YCh] in which a nonlinear objective function \mathcal{F} is minimized with respect to the set of transistor parameters \mathcal{P} subject to a set of constraints \mathcal{C} . The objective function \mathcal{F} describes the fit of simulated device responses \mathcal{R} against a set of experimental measurement data \mathcal{D} . The results of optimization determine such a set of parameter values which minimizes the differences between the measurement and simulated data:

$$\begin{array}{ll} \text{minimize} & (\mathcal{F}(\mathcal{D},\mathcal{R}))\\ \mathcal{P}\\ \text{subject to } \mathcal{C} \end{array}$$

The set of measurement data can be regarded as a sequence of K data groups, and each data group is a rectangular table of numerical results comprising N_i rows and L_i columns, $1 \le i \le K$. The objective function $\mathcal{F}(\mathcal{D}, \mathcal{R})$ can thus be written as

$$\mathcal{F}(\mathcal{D},\mathcal{R}) = \frac{1}{K} \sum_{1 \le i \le K} \frac{1}{L_i} \sum_{1 \le j \le L_i} \frac{1}{N_i} f_i \left(\sum_{1 \le k \le N_i} e_i(D[i,j,k], R[i,j,k]) \right)$$

where D[i, j, k] is a measured value (in the *i*-th group, *j*-th column and k-th row and R[i, j, k] is the corresponding simulated result; e_i is one of the "standard" error functions such as the absolute value of the difference between D[i, j, k] and R[i, j, k], the square of this difference, the square of the relative difference, the absolute value of the difference between logarithms of D[i, j, k] and R[i, j, k], etc., and f_i is a function that is "complementary" to e_i , e.g., if e_i is the square function, f_i is the square root function, etc.

Error functions e_i are thus associated with data groups, and each data group can have a different error function associated with it. The formulation of the objective function "averages" the error

value in order to make it independent of the number of data points. Furthermore, the error functions e_i (and f_i) are usually selected in such a way that the errors for different data groups are within the same range of magnitude (e.g., CB characteristics are usually associated with logarithmic error functions); selection of error functions and their associations with data groups are specified in the input data.

4. FIT-2 PROGRAM

FIT-2 is an interactive simulation-based program for extraction model parameters for SPICE-like circuit simulators. It is based on the SPICE–PAC simulation package [Zub].

The FIT-2 program is composed of four major parts:

- the main segment that handles the interaction with a user, organizes presentation of extraction results and controls the remaining parts of the program;
- variables manager which controls the set of optimization variables; the lower and upper bounds of variables as well as their nominal and actual values can be modified by appropriate interactive commands, and the actual values are also updated after each optimization; the manager can select any subset of variables for subsequent optimization, as specified by appropriate interactive commands:
- data manager that stores all measurement data as well as corresponding simulation results (for the nominal and actual values of variables); it also provides selective extraction for any subset of groups and any subset of columns within a group, as indicated by appropriate interactive commands,
- optimizer which selects one of the optimization method and • adjusts optimization parameters accordingly, determines the starting point (using the nominal or actual values of selected variables) and invokes the optimization algorithm; for each evaluation of the objective function:
 - the values of optimization variables are used for updating corresponding parameters of the simulated circuit,
 - for each data group, group parameters (if any) are used for updating the control parameters of the simulated circuit (e.g., the bias point for AC simulations or the value of the base current for DC/CE simulations), and then
 - the corresponding simulation is performed (DC, AC or time-domain) and its results are used for evaluation of the objective function.

FIT-2 contains two different optimization techniques: (1) quite robust but rather slow simplex direct search method (as in [CCLL]), and (2) a more efficient but not-so-reliable guasi-Newton method based on approximated gradient information (E04JBF routine from the NAG library [Phil]). Normally, the initial optimization is performed by the simplex method as it is less sensitive to large changes of the objective function; the quasi-Newton method is most efficient in the neighborhood of the solution, so its typical application is in the second stage of optimization, after preliminary optimization performed by the simplex method.

A simple sequence of interactive commands for a selective extraction may be as follows:

data(1,2-5,6(1,3-5)) var(1,3,5-7,12)fit(nag,25,act)

where the data command selects groups 1, 2 to 5, and columns 1 and 3 to 5 of group 6; the var command performs the selections of variables, in this case variables 1, 3, 5 to 7, and 12 (as defined in the variables file); the variables can also be identified by their names, so - in the context of the variables file shown in section 2 - an equivalent variable selection is:

var(HBT'IS,HBT'NF,HBT'IKF-HBT'NE,HBT'ISC)

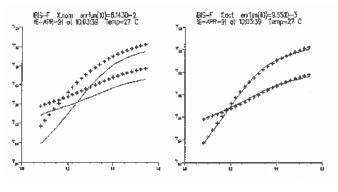
the fit command specifies the optimization step, in this case nag selects the routine E04JBF form the NAG library, 25 is the maximum number of the iteration steps, and act indicates that the actual values of variables are to be used as the starting point. More detailed descriptions of the program and its commands can be found in [ZK].

5. EXAMPLES

Extraction results for heterojunction bipolar transistors are used as an illustration of FIT-2's capabilities.

Fig.1, 2 and 3 show three groups of the measurement data (indicated by the "+" markers) together with the characteristics corresponding to the nominal values of transistor parameters (continuous lines) for DC measurements in CB configuration and forward mode (the collector and base currents), DC measurements in CE configuration and forward mode (4 different values of the base current), and AC measurements for all four S-parameters, respectively. It can be observed that the nominal values of parameters do not provide a reasonably good fit of transistor characteristics against the measurement data.

Fig.4, 5 and 6 show the same three groups of measurement data with extracted values of transistor parameters. It can be observed that transistor characteristics fit very closely to the measurement data; the values of error functions are equal to 0.010, 0.018, and 0.108, respectively.



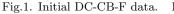


Fig.4. Fitted DC-CB-F data.

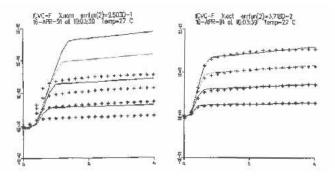


Fig.2. Initial DC-CE-F data. Fig.5. Fitted DC-CE-F data.

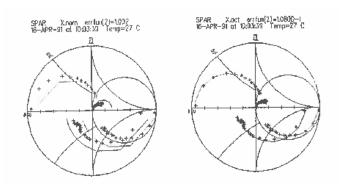


Fig.3. Initial AC data. Fig.6. Fitted AC data.

6. CONCLUDING REMARKS

Although a number of relationships between measurement data and extracted parameters are quite useful in parameter extraction [DJ,IG], practical experiments seem to indicate that a general extraction strategy may be rather difficult to find. Therefore a convenient formalism for higher–level specification of the extraction process can be very helpful in automation of this process. Elements of such higher–level specification have been implemented in FIT–2; some further extensions of this formalisms should be included in future versions of the program.

The set of transistor parameters is usually quite large; typically it contains more than 30 (electrical) parameters. However, the electrical parameters used in circuit simulation can be derived from a smaller set of technological and geometric parameters, that are more relevant to manufacturing processes. An interface has been incorporated into the FIT-2 program that accepts user-defined conversion of technological and geometric parameters (used as optimization variables) into electrical parameters (used as circuit variables).

Furthermore, it appears that different types (e.g., DC, AC) of (measurement and simulated) data are associated with subsets of the set of transistor parameters. The extraction process can be significantly simplified if selective optimizations are performed on small but relevant subsets of optimization variables, designated by different types of measurement data. Mechanisms for flexible selection of optimization variables as well as the measurement data are built into the FIT–2 program to support such selective optimizations.

Both optimization methods available in FIT-2 provide local optimization only, so in a case of numerous local minima, the starting point should be disturbed externally to cover as large part of the feasible space as seems reasonable. It appears, however, that local optimization algorithms are seldom satisfactory even when restarted from several randomly chosen initial points. Measurement error coupled with the large number of variables of a physically based circuit leads to an error function with many nonphysical local minima in addition to the global minimum [BST]. More general (and efficient) global optimization methods are needed but they are rather difficult to find. Simulated annealing [Rut] has recently been proposed as an alternative to gradient-descent methods. In simulated annealing, the actual values of variables are disturbed and the new error is calculated; it this error is smaller than the previous one, the new values replace the actual ones, as in descent methods. But, sometimes, in distinction to descent algorithms, the vector of variables with larger error may be accepted in accordance with a precise probabilistic criterion which becomes less tolerant of "bad" moves at late stages of the algorithm. The success of this algorithm depends on generating moves that are neither always accepted nor always rejected [Rut]. The method is

very promising but further research is needed to make it generally applicable.

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References

- [BST] G.L. Bilbro, M.B. Steer, R.J. Trew, C-R Chang, S.G. Skaggs, "Extraction of the parameters of equivalent circuits of microwave transistors using tree annealing"; IEEE Trans. on Microwave Theory and Techniques, vol.38, no.11, pp.1711-1718, 1990.
- [CCLL] P. Conway, C. Cahill, W.A. Lane, S.U. Lidholm, "Extraction of MOSFET parameters using the simplex direct search optimization method"; IEEE Trans. on Computer-Aided Design, vol.4, no.4, pp.694-698, 1985.
- [CFG] W.M. Coughran Jr., W. Fichtner, E. Grosse, "Extracting transistor charges from device simulations by gradient fitting"; IEEE Trans. on Computer-Aided Design, vol.8, no.4, pp.380-394, 1989.
- [DJ] A. Davies, A.K. Jastrzebski, "Parameter extraction technique for nonlinear MESFET models"; Proc IEEE Conf. on Microwave Theory and Techniques, pp.747-750, 1990.
- [DS] K. Doganis, D.L. Scharfetter, "General optimization and extraction of IC device model parameters"; IEEE Trans. on Electron Devices, vol.30, no.9, pp.1219-1228, 1983.
- [EGMT] M. Eron, J. Gerber, L. Mah, W. Tompkins, "MES-FET model extraction and verification techniques for nonlinear CAD applications"; Proc. 3–rd Asia–Pacific Microwave Conf., Tokyo, Japan, pp.321-324, 1990.
- [Gar] K. Garwacki, "Extraction of BJT model parameters using optimization method"; IEEE Trans. on Computer-Aided Design, vol.7, no.8, pp.850-854, 1988.
- [IG] A. Ibarra, J. Gracia, "Strategy for DC parameter extraction in bipolar transistors"; IEE Proceedings, vol.137, pt.G, no.1, pp.5-11, 1990.
- [MMD] W. Maes, K.M. DeMeyer, L.H. Dupas, "SIMPAR: a versatile technology independent parameter extraction program using a new optimized fit strategy"; IEEE Trans. on Computer-Aided Design, vol.5, no.2, pp.320-325, 1986.
- [Phil] J. Phillips, "The NAG library: a beginner's guide"; Oxford University Press 1987.
- [Rut] R.A. Rutenbar, "Simulated annealing algorithms: an overview"; IEEE Circuits and Devices Magazine, vol.5, no.1, pp.19-26, 1989.
- [YCh] P. Yang, P.K. Chatterjee, "An optimal parameter extraction program for MOSFET models"; IEEE Trans. on Electron Devices, vol.30, no.9, pp.1214-1219, 1983.
- [Zub] W.M. Zuberek, "SPICE–PAC version 2G6c an overview"; Technical Report #8903, Department of Computer Science, Memorial University of Newfoundland, St. John's, Canada A1C-5S7, 1989.
- [ZK] W.M. Zuberek, A. Konczykowska, "FIT-2, a simulationbased parameter extraction program for SPICE-like circuit simulators"; Technical Report (in preparation), Department of Computer Science, Memorial University of Newfoundland, St. John's, Canada A1C-5S7, 1991.