Design and Development of a MOSFET Driver Circuit for Phase-Shifted Zero-Voltage-Switching Full-Bridge DC-DC Converter

M. J. Khan[1,2] Graduate Student mjakhan@engr.mun.ca
M. T. Iqbal[1] Assistant Professor tariq@engr.mun.ca
J. E. Quaicoe[1] Professor jquaicoe@engr.mun.ca

[1]Faculty of Engineering and Applied Science; Memorial University of Newfoundland; St. John's, NL A1B3X5, Canada
[2] Corresponding Author

Abstract

This article presents an approach for analysis and design of MOSFET gate driver circuits for Phase-Shifted Zero-Voltage-Switching Full-Bridge (PS-ZVS-FB) DC-DC converters. Based on the critical requirements of the converter, the performance indices of an effective driver stage are identified. A brief overview of MOSFET driving basics is extended to a comparative analysis of several commonly used gate driver schemes. Design guidelines of a high-performance driver stage using off-the-shelf IC technology are presented. Tests were carried out on a setup consisting of IRFP2907 MOSFETs driven at 200 kHz and performance features based on the test results are highlighted. Finally, the possible limitations and indications for further improvement are discussed.

1.0 Introduction:

Full-bridge Zero-Voltage-Switching converters operated in Phase-Shifted mode are being considered as an attractive choice for medium to high power applications, especially in distributed generation (DG) and automotive systems. In general, this class of DC-DC converter is of high-power density, higher efficiency and can uniquely exploit the parasitic reactive elements within the power circuit for achieving soft-switching [1,2].

The issue of MOSFET driver design is no longer an unsolved problem by itself. However, there is always a scope for further investigation depending on a specific application, power level and switching frequency [3]. In addition to various typical requirements, a MOSFET driver circuit used in PS-ZVS-FB converter needs to accommodate a set of critical conditions as outlined below:

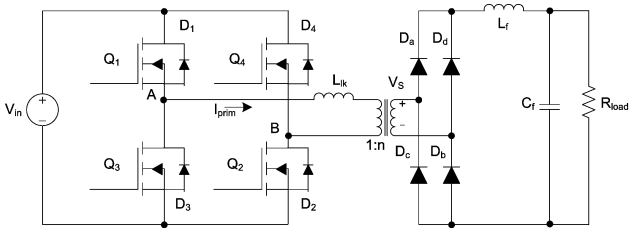


Fig. 1: Full-Bridge DC-DC converter

Dead time:

In a typical H-bridge configuration (Fig. 1), ZVS is achieved by utilizing the parasitic effects of the components (MOSFET output capacitance, Transformer capacitance and leakage inductance). Under such scheme, two legs of the bridge are driven with a phase shift (φ) against each other and with a certain dead time within two switches on the same leg (δ_{t1}, δ_{t2}) as shown in Fig. 2. This dead time along with the time taken for primary current to rise and reflect the secondary, create a dead zone between the voltages of either side of the transformer.

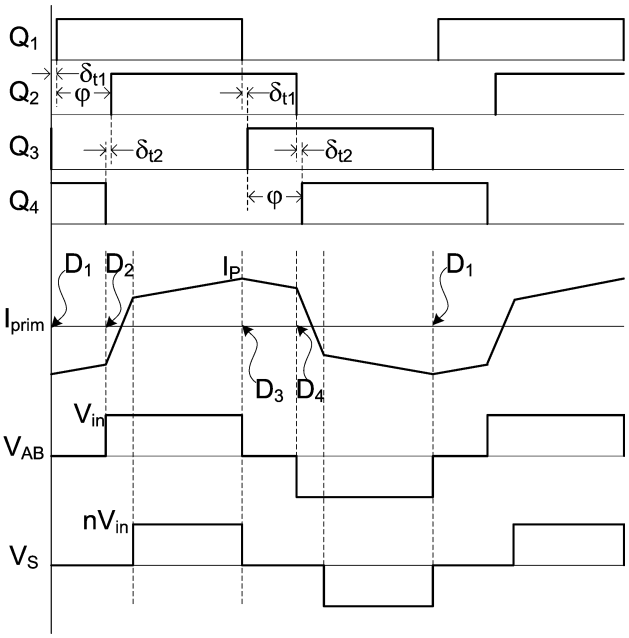


Fig. 2: Phase Shifted operation of FB-ZVS converter

Zero voltage turn on of the switches is achieved by allowing resonant discharge of the MOSFET output capacitance C_{MOS} using the energy stored in the transformer's leakage inductance L_{lk}. Prior to firing each MOSFET, the resonance between the reactive elements forces the corresponding anti-parallel diode to conduct, essentially putting zero voltage across the MOSFET. The minimum dead time required to enforce the resonance and

subsequent charging/discharging is different for the two legs of the bridge. Considering a finite transformer winding capacitance C_{TR} the minimum required dead time between switch Q_1-Q_3 and Q_4-Q_2 are given by [1]:

$$\delta_{t1} = \frac{4C_{MOS}V_{in} + C_{TR}V_{in}}{I_P} \quad (1)$$

$$\delta_{t2} = \frac{\pi}{2}\sqrt{L_{lk}(C_{MOS} + C_{TR})} \quad (2)$$

where I_P is the peak value of the primary current, which is the output filter inductor's peak current reflected to the primary.

Switching frequency

In order to achieve higher power density, smaller component size (transformer, filter etc.) and thereby reduced cost, high frequency operation of the power stage is desirable. Reports of PS-ZVS converters operating over a wide frequency range (50 - 500 KHz) are available in the literature [1,2]. Although MOSFETs are quite capable of switching at such high frequencies, the driver circuit itself may pose bottlenecks on faithfully carrying gating signals with a predefined dead time.

Power level

PS-ZVS converters are being used for medium (1 kW) to high power (50 kW) applications. Proper driving of the power circuit at such level is of great importance. For a constant voltage level and increasing power rating, MOSFETs generally display higher input capacitance and gate charge (Table 1). At higher frequencies, fast and effective charging/discharging of the MOSFETs' gate capacitance may become a significant issue.

Table 1: MOSFET characteristics [4]

MOSFET Name*	Continuous Drain Current I_D @ 25°C (A)	Static Drain-to-Source On-Resistance $R_{DS}(on)$ @10V (mΩ)	Total Gate Charge Q_g (nC)	Input Capacitance C_{iss} (pF)
IRFR2407	42	26.0	74.0	2400
IRF2807	82	13.0	106.7	3820
IRF1407L	100	7.8	160.0	5600
IRF3808L	105	7.0	150.0	5310
IRF1407	130	7.8	160.0	5600
IRF1607	142	7.5	210.0	7750
IRFP2907	177	4.5	410.0	13000

*Drain-to-Source Breakdown Voltage V_{BRDSS} = 75 V

The gate driver circuit must swiftly source and sink sufficient current such that the switches do not enter into the linear operating range possibly overheating the system and causing high power loss.

Full bridge configuration

The Full-Bridge configuration of the power stage consists of two high side (Q1, Q4) and two low side (Q2, Q3) MOSFETs. The reference nodes of the corresponding gate drives are different except for the two low side switches. The most common solution for driving such arrangement is to have isolated gating pulses referenced to the respective return paths. This calls for selection of a suitable isolation mechanism and investigation of its performance.

Phase shifting

The essence of the ZVS DC-DC converter operation is to introduce a phase shift between the switches of the left and right leg. This, along with other set of factors, dictates the effective duty ratio of the converter [1]. In order to achieve maximum range of phase shifting (ideally, 0-180°), the gate drive must carry the gating pulses from the signal source to the switch with minimum loss of duty ratio.

Apart from these critical issues attributed to the PS-ZVS-FB converter, other general issues for MOSFET drive design come into play. For commercial success of the converter itself, a low cost, modular and compact driver stage is desirable. Performance features such as, reliability, isolation, protection and noise immunity are also important. From a technical point of view propagation delay, EMI, power consumption and immunity from Miller effect may well dictate the success of the design.

The scope of this work is to design a rudimentary gate driver circuit that is flexible, simple and effective for high power PS-ZVS-FB converters. Based on a comparative analysis of several reported schemes, an alternative design has been attempted. This approach employs off-the-shelf IC technologies and may find application in various low cost schemes.

2.0 Analysis

Since MOSFETs are voltage driven devices, the prime objective of a driver circuit is to apply a voltage large enough to exceed the device threshold and switch it ON or vice-versa. Although voltage driven devices (such as, MOSFET, IGBT etc.) are relatively easier to operate against their current driven counterparts (BJT, SCR etc.), the gating requirements may not be very simple for many practical reasons. As shown in Fig. 3, to turn a MOSFET from OFF to ON state, the input capacitance C_{iss} needs to

be charged before the threshold V_{th} is exceeded by the driver circuit [5,6]. In order to force the device to act as a switch, the injection and extraction of the controlling charge needs to be fast enough so that the linear range of device operation is avoided. This requires a low impedance signal source. However, too low gate resistance may cause excessive ringing, current injection and subsequent power loss. On the contrary, high resistance may slow down the ON/OFF sequence and cause device overheating or shoot-through.

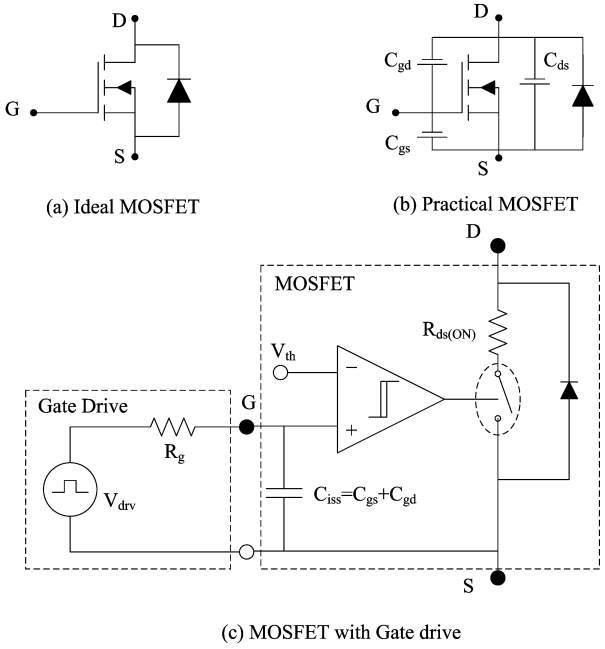


Fig. 3: MOSFET models and gate drive circuit

A simplified approximation of the magnitude of gate current I_g, gate resistance R_g and gate circuit power dissipation P_g is given using the following equations:

$$I_g = Q_g \frac{1}{t_{tx}} f_s \tag{3}$$

$$R_g = \frac{2}{3}\frac{1}{I_g} V_{drv} \tag{4}$$

$$P_g = Q_g V_{drv} f_s \tag{5}$$

where Q_g is the gate charge (C), f_s is the switching frequency (Hz) and t_{tx} is the total transition time (ON+OFF time) as a percentage of the switching frequency.

Since a typical gating circuit consists of a signal source, isolation and a possible current buffer, the accumulated effect of all these cascaded stages affects its performance.

Isolation between the signal source and switching device can be provided by a number of methods such as, pulse transformers, opto-couplers, photovoltaics, charge coupler or piezo actuators. However, transformers and opto-isolators are mature technologies and mostly preferred.

While a transformer based drive circuit provides very high voltage isolation with negligible propagation delay, upper limit on duty ratio handling and core saturation are its key drawbacks. Also, transformers can easily provide positive and negative gate voltage, which could help reduce the so-colled Miller effect [5]. IC based opto-isolators can also deliver high range of isolation voltage throughout a wide frequency band (DC-MHZ) with minimal circuit complexity. Generally, transformer isolators do not require separate power sources unlike opto-couplers.

With a view to investigating the performance of transformer based gating circuits applied in PS-ZVS-FB converters, two reported schemes are examined here [7,8]. The block diagrams of these transformer based gate drivers are shown in Fig. 4 and Fig. 5. Both are driven at 100 kHz and must use additional arrangement in conjunction with the transformer in order to preserve the essential dead time for ZVS operation.

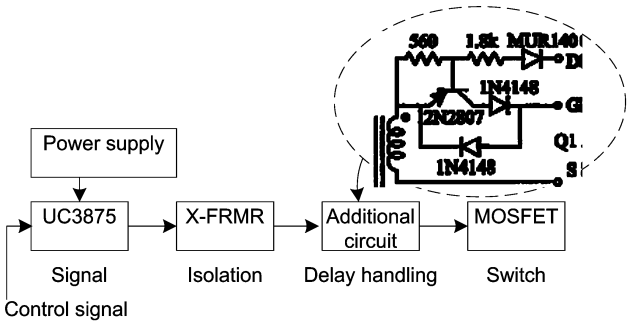


Fig. 4: PS-ZVS-FB driver as found in [7]

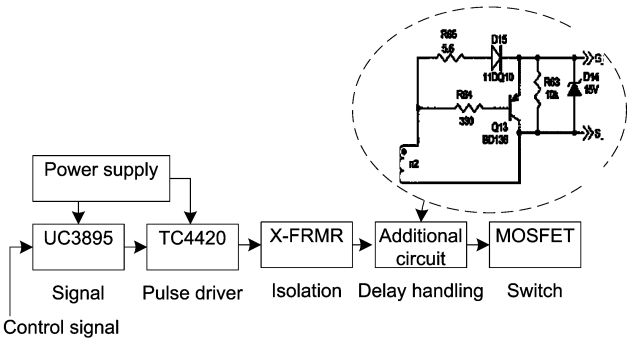
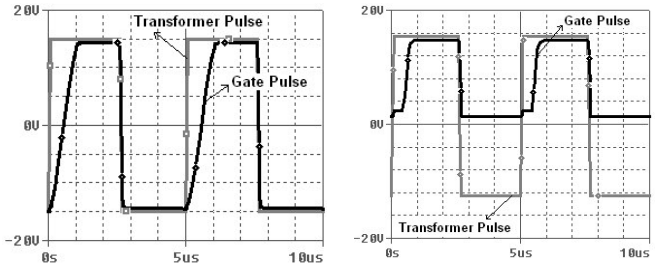


Fig. 5: PS-ZVS-FB driver as found in [8]

The arrangement in Fig.4 [7] may not be suitable for high power applications, as the current supplied to the MOSFETs must be delivered from the signal source. Generally, Phase Shifting ICs are not designed for such

high current injection. A modified method as shown in Fig.5 [8], which allows a current buffer between the signal source and the transformer, could be considered as a better option. Both circuits employ additional discrete components at the transformer output for preserving the dead time information at the expense of circuit complexity. Furthermore, simulations performed on these schemes at an elevated frequency (200 kHz) and higher MOSFET input capacitance (C_{iss} = 10000pF) indicates either slow rise time (Fig. 6(a)) or significant duty ratio loss (Fig. 6(b)). Practical implementation of these circuits may show even deteriorated performance due to the presence of non-ideal components.



(a) Scheme in [7] (b) Scheme in [8]

Fig. 6: Simulation of MOSFET gate drive at 200 kHZ.

Therefore, in contrast to the critical requirements for PS-ZVS-FB converters, these methods of MOSFET gate driving may not perform satisfactorily at high power/frequency ranges. An alternative strategy requiring minimal number of discrete components and utilizing off-the-shelf components is presented in the sections to follow.

3.0 Design Considerations and Implementation

The use of ICs is generally favored against a combination of discrete components. In addition to compactness, reliability and convenience, use of integrated circuits in the driver circuit would provide short propagation delay and smaller rise/fall time, which are essential for the application being considered. A complete IC based MOSFET gate driver, alternative options for component selection and design considerations are outlined in this section.

Since the ZVS converter is generally operated at high frequencies (50 kHz - 500 kHz), it is essential to generate the signals with sufficient noise immunity, pre-specified dead time and coordination. Instead of generating the signal using microcontrollers or custom built circuits, various commercial components such as UC 3875, UCC 3895 or ISL6551 could be used in that regard.

Many opto-couplers especially designed for MOSFET/IBGT gate drives are also commercially available. The HCPL 3120, HCPL 316J and IR2101 come with features such as, single switch drive, add-on protection and high/low drive, respectively. In addition to the built-in high current capabilities of these gate drive ICs, the addition of a separate current buffer stage might become necessary. This could be easily achieved by using bi-polar non-inverting totem-pole arrangements [3]. ICs such as TC4420 may provide such feature with adequate capability.

In order to supply isolated power to the opto-couplers and current buffers, a separate power supply module needs to be arranged. Miniature DC-DC converter ICs (e.g.: DCP022415) may well serve this purpose (Fig. 7).

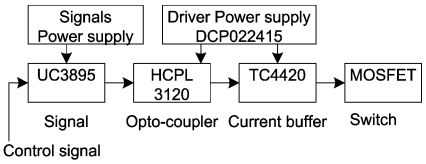
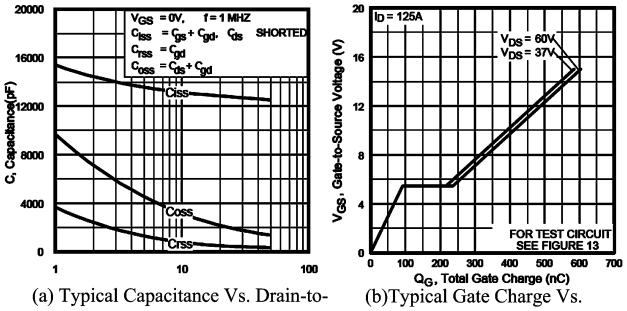


Fig. 7: IC based PS-ZVS-FB driver

In this work, a gating circuit is operated at 200 kHz for PS-ZVS-FB converter employing four IRFP 2907 MOSFETs. The key characteristics of these semiconductor devices are given in Table 1 and Fig. 8.



(a) Typical Capacitance Vs. Drain-to-Source Voltage (b)Typical Gate Charge Vs. Gate-to-Source Voltage

Fig. 8: IRFP 2907 capacitance and gate charge.

The magnitude of the required dead time for PS-ZVS operation could be found by equations (1) and (2) using the nominal values of Table 2.

Table 2: System Parameters

Parameter	Value
Input voltage, $V_{in} = V_{DS}$	48 V
Gate voltage, $V_{drv} = V_{GS}$	15 V
Peak primary current, I_P	5.5 A
Equivalent MOSFET capacitance, C_{MOS} (approx)	7 nF
Transformer parasitic capacitance, C_{TR} (approx)	150 pF
Transformer leakage inductance, L_{lk} (approx)	5 µH
Switching frequency, f_s	200 kHz
Total transition time, t_{tx}	10%

For this application, the desired dead times are: δ_1 = 250 ns and δ_2 = 300 ns. These parameters are implemented in

UCC 3895 phase shift controller IC to generate the four synchronized switching signals.

The HCPL 3120 has been chosen as the opto-coupler stage. Under the given operating conditions, an estimate of the driver current, gate resistance and power dissipation is found by equations (3)-(5). Although the value of I_g and R_g are well within the range (1 A and 10Ω, respectively), the power dissipation P_g is around 1.65 watt. Since, the absolute maximum rating of the IC is 295 mW, a separate buffer stage is required. The TC 4420 IC has been used for that purpose. The output resistance of this IC is around 2.5 Ω and no external gate resistor is used in this case. The block diagram of the driver circuit is shown in Fig. 7.

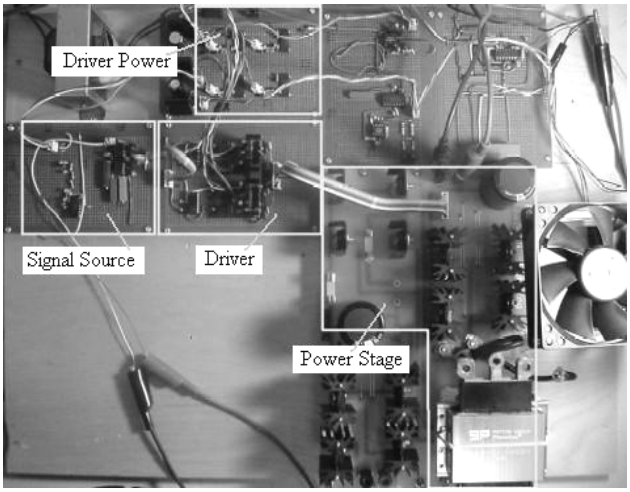


Fig. 9: Driver circuit as part of the power stage

The test setup showing the gate driver and DC-DC converter (which is a part of a bigger power converter) is given in Fig. 9.

4.0 Results

The tests were carried out primarily to investigate the performance of the gate driver circuit for PS-ZVS operation of the DC-DC converter. As indicated in the introductory section, effectiveness of the design with regard to dead time reproduction, propagation delay and phase shift range are considered. The converter is also subject to higher frequency operation in contrast to the reported designs [7,8].

In Fig. 10, the original signal (generated by UCC 3895) and the signal at the MOSFET gate is shown. There exists a noticeable propagation delay (~450 ns) and loss of steepness during signal transitions. The dead times for the legs containing Q_1-Q_3 and Q_2-Q_4 transistors are indicated in Fig 11 and 12, respectively. The preset values of 250 ns and 300 ns are faithfully reflected at the MOSFET gates. The finite rise time (~300 ns) and fall time (~ 250 ns) may also be taken into consideration and a new level of dead time can be calculated and applied, if required.

Fig. 10: Propagation delay

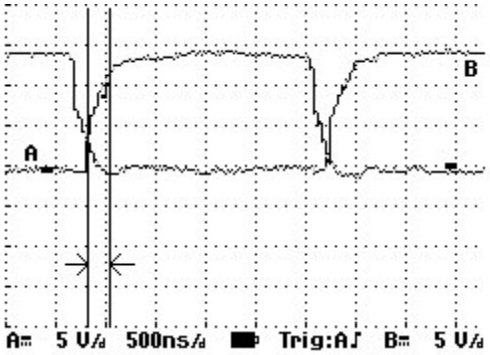


Fig. 11: Dead time in leg Q_1-Q_3

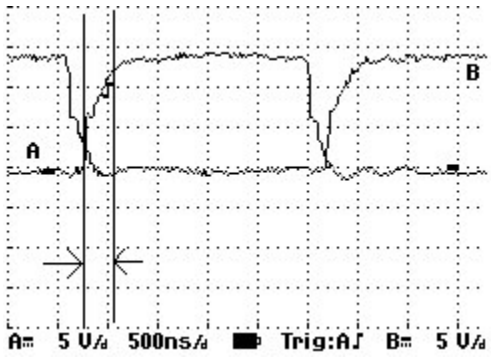


Fig. 12: Dead time in leg Q_2-Q_4

In Fig. 13, the gate voltage and corresponding crossover at the MOSFET output are shown in channel B and A, respectively. It signifies that even with a finite rise/fall time, the output voltage can switch its states with steeper slope. The associated high frequency ringing and gate voltage notches are common in such applications and are subject to further analysis [9].

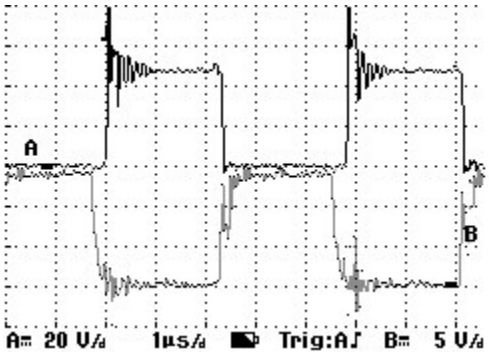


Fig. 13: Gate-source and drain-source voltage

In Fig. 14 and 15, phase shifting operation of the power stage is shown in terms of the output voltage. The mid range phase shifting (~ 50%) indicates a typical waveform for PS-ZVS-FB DC-DC converter operation. The maximum achievable phase shifting is around 95% as shown in Fig. 15.

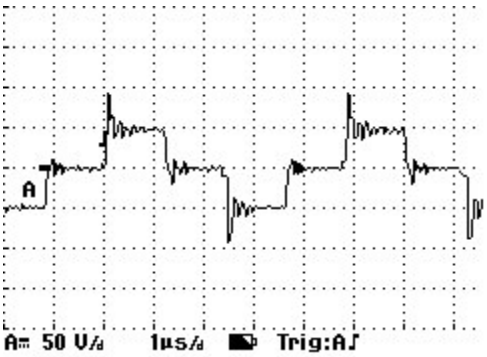


Fig. 14: Phase shifted operation (~ 50%)

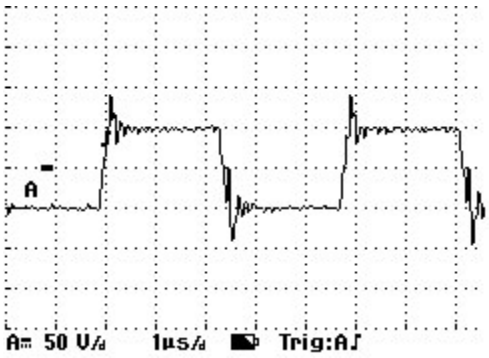


Fig. 15: Phase shifted operation (> 90%)

Observations on power dissipation of the driver circuit are charted on Fig. 16. The maximum loss with the H-bridge configuration is less than 8 watts.

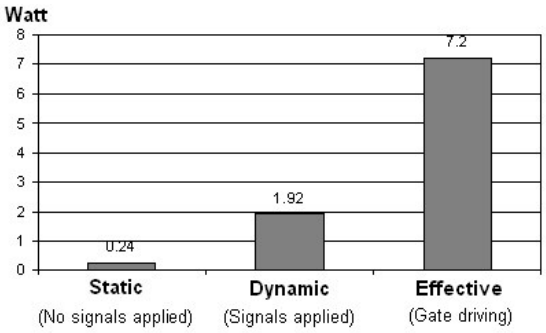


Fig. 16: Power dissipation in driver stage

This set of results indicates the satisfactory performance of the MOSFET driver circuit for PS-ZVS-FB operation at high frequencies. The circuit has been implemented using ICs and does not require transformer based coupling and associated add-on arrangements. Investigations on dv//dt protection, performance improvement, signal attenuation and upper limit of operating frequency could be considered as part of a continuing work.

5.0 Conclusion

In this work, an analysis and systematic approach for MOSFET driver circuit for PS-ZVS-FB DC-DC converters has been discussed. A comparative overview of the commonly used techniques and an alternative approach that effectively meets the critical requirements of such operation has been presented. Implementation, practical considerations and test results indicate that an off-the-shelf IC based system can perform satisfactorily for elevated frequency and power ranges. Further cost, performance and protection features may be incorporated in this design.

Acknowledgements
The authors would like to thank the Atlantic Canada Opportunities Agency (ACOA) for providing support for this research through the Atlantic Innovations Fund (AIF).

References

[1] J. A. Sabate, V. Vlatkovic, R. Ridley, F. C. Lee, and B. H. Cho, "Design considerations for high-voltage high-power full-bridge zero-voltage-switched PWM converter," Proc. IEEE APEC'90 Conf., pp. 275–284, 1990.

[2] L. H. Mweene et al., "A lkW, 500kHz, front end converter for a distributed power supply system," in APEC Conf Rec., 1989.

[3] Abhijit D. Pathak. "MOSFET/IGBT Drivers-Theory and Applications" Application Note available on www.ixys.com

[4] International Rectifier Inc. Available on www.irf.com

[5] Laszlo Balogh, “Design and Application Guide for High Speed MOSFET Gate Drive Cicruits”, Application Note available on www.ti.com

[6] P. T. Krein, *Elements of Power Electronics.* New York and Oxford: Oxford University Press, 1998. ISBN 0-19-511701-8.

[7] Marcelo Brunoro, Jos´E Luiz F. Vieira, “A High-Performance ZVS Full-Bridge DC–DC 0–50-V/0–10-A Power Supply with Phase-Shift Control”, IEEE Transactions on Power Electronics, Vol. 14, No. 3, May 1999.

[8] J.B. Ejea, A. Ferreres, E. Sanchis-Kilders, E. Maset, V. Esteve, J. Jordán, R. García, J.A. Carrasco, “Parallel Power Processing Applied to a High fficiency Battery Discharger Module for Space Power Systems”, 35th Annual IEEE Power Electronics Specialists Conference, Aachen, Germany, 2004.

[9] Alexander Fiel, Thomas Wu; “ MOSFET Failure Modes in the Zero-Voltage-Switched Full-Bridge”, Application Note available on International Rectifier Inc. www.irf.com