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Research Article

Modified Droop Method Based on Master Current Control for Parallel-Connected DC-DC Boost Converters

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Load current sharing between parallel-connected DC-DC boost converters is very important for system reliability. This paper proposes a modified droop method based on master current control for parallel-connected DC-DC boost converters. The modified droop method uses an algorithm for parallel-connected DC-DC boost converters to adaptively adjust the reference voltage for each converter according to the load regulation characteristics of the droop method. Unlike the conventional droop method, the current feedback signal (master current) for one of the parallel-connected converters is used in the inner loop controller for all converters to avoid any differences in the time delay of the control loops for the parallel-connected converters. The algorithm ensures that the load current sharing is identical to the load regulation characteristics of the droop method. The proposed algorithm is tested with a mismatch in the parameters of the parallel converters. The effectiveness of the proposed algorithm is verified using Matlab/Simulink simulation.

1. Introduction

In comparison to a single, high power, centralized power converter, parallel connection of low power converters offers several advantages. Some of these advantages are associated with the system performance such as higher efficiency, better dynamic response, and better load regulation. The other advantages are related to the system, which include expandability of output power and ease of maintenance [1].

For the operation of parallel DC-DC converters, the conventional droop method provides true redundancy because there is no interconnection between modules. However, effective load current sharing and voltage regulation are the main drawbacks of the droop method. A novel droop method proposed by Kim et al. [2] adaptively regulates a reference voltage to improve the load current sharing and properly regulate the output voltage. The output voltage variation in parallel-connected converters is caused by various conditions such as changes in load, input power, or measurement error in the voltage feedback signal [2, 3]. In general, the circulating current between modules could be initiated by a small mismatch in the output voltage which leads to unequal load current sharing between modules. Anand and Fernandes in [4] propose a modified droop controller to overcome the mismatch in output voltage due to the error in measurement of the voltage feedback signal. The circulating current measurement between converters is used to modify the nominal voltage which reduces the error of the modules output voltage.

The operating point for parallel-connected converter is modified randomly and thus a new set of parameters for the controller must be calculated again. To overcome this issue, several control laws have been proposed in the literature [5–9]. One of these control laws is a nonlinear control, which enhances the power quality for condition of different loads. Mazunder and Kamisetty in [7] gave an experimental validation of the proposed control scheme in [5] for parallel-connected buck converters. The performance of the proposed control is demonstrated under the transient and steady state for two parallel converters. The operation of the two modules uses interleaving mode of operation which is achieved by phase shifting the ramp signals of the two modules by one half cycle.

One of the commonly employed methods for active current sharing control of parallel converters is the master-slave current control that uses an analog wireless communication or an intercommunication link between converters [10]. The master-slave current sharing control of parallel converters is demonstrated using analog wireless communication in [11]. It uses one converter to operate as master controller. The chosen converter operates in voltage controlled mode to regulate the output voltage which tracks the reference voltage. The other converters operate in current controlled mode to regulate their output currents. Those converters operate as slaves because the master controller obtains their reference current value based on the total load current. Slave converters receive the new reference current through a high-speed communication link [12, 13]. The high-speed communication between converters is used to minimize the time delay and improve the system performance. The high-speed communication link such as digital communication scheme increases the total cost, which makes it appropriate in medium and high-power applications. However, in some power applications, an analog controller with connecting wires experiences noise which makes it applicable only for low power applications where converters are located close to each other.

To achieve wireless power sharing between converters, a droop method with virtual resistance (VR) has been proposed [14]. The method implements tertiary level optimization control for parallel-connected DC-DC converter to enhance the efficiency of the droop method with VR. The decision variable, which is VR, is used to adjust the load current sharing between the converters. Stability analysis is used to examine the effect of varying VR on the dynamic performance. In [15] an improved droop method for parallel-connected converters is presented to enhance the current sharing accuracy. Although the other modified droop methods adjust the output voltage by making the slope of the droop method steeper such as virtual resistance, the improved droop method adjusts the output voltage set point for each converter based on a generated digital signal from a module experiencing the highest current. A few specific current set points in the improved droop method are selected in advance. If the module with the highest current reaches the set point, a digital signal is sent by the module to the other modules to regulate their output voltage. However, the module which sends a digital signal does not respond to a signal of the other module at the same set point. Once all the modules have generated one signal at the same set point, the output voltage regulation for that set point is terminated and a new process is started.

In general, any mismatch in the output voltage level of the parallel-connected DC-DC boost converter could initiate a circulating current. To avoid an initiation of circulating current, a synchronous switching for parallel-connected DC-DC boost converter could be used [16]. The synchronous switching forces the parallel-connected converters to operate in two operating modes only. This ensures that the switching of the parallel-connected converters is synchronized. Lab measurement of two parallel connected MPPT modules with no intercommunication link between the two modules is shown in Figure 1. In this setup, there is no synchronous switching for the two parallel connected 260 W PV modules with individual MPPT.

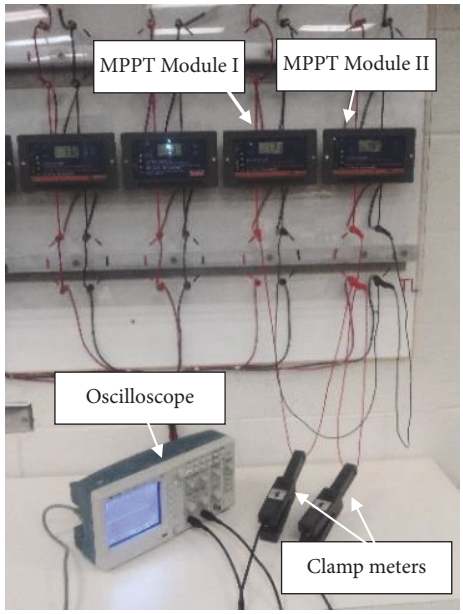

Figure 1: Two parallel-connected MPPT modules.

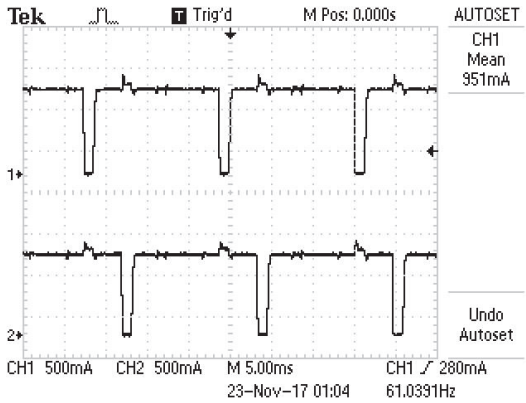

Figure 2: Output current for the two parallel-connected MPPT modules.

The outputs of the two MPPT modules are connected in parallel to the load. Also, the two clamp meters in Figure 1 monitor the currents from both MPPT modules. During a sunny day, the measurements of the currents for each module are shown in Figure 2.

It can be observed from Figure 2 that when a switch closes in one of the parallel-connected MPPT modules, the other MPPT module experiences higher current at the same time and vice versa. This is a clear evidence of circulating currents between the two MPPT modules. The asynchronous switching causes the undesired higher current for each one of the two MPPT modules. Moreover, there is no intercommunication link between the two MPPT modules to synchronize the switching and avoid circulating current.

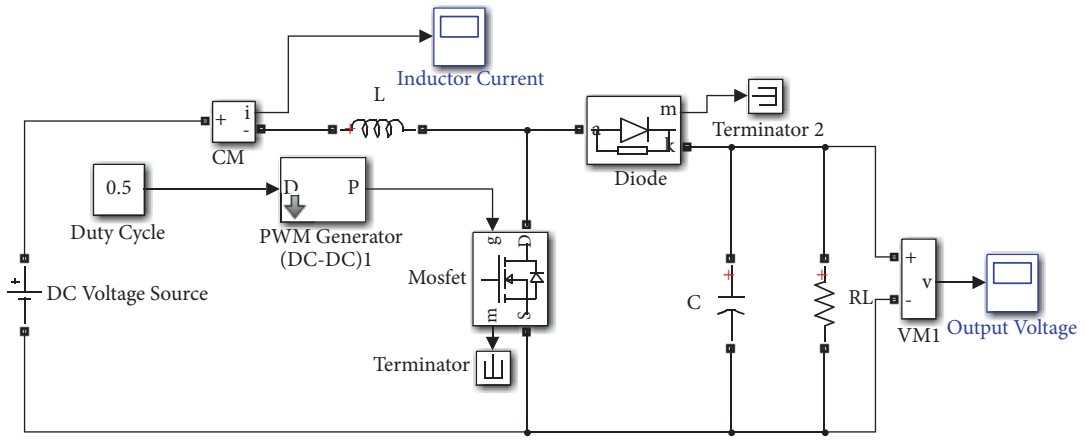

Figure 3: DC-DC boost converter.

In this paper, synchronous switching for the parallel-converter is achieved by intercommunication link between the modules. The proposed method based on master current control for parallel-connected DC-DC boost converters can synchronize the output voltage level during any change in the load condition. In this method, a linear control was implemented; thus the two parallel-connected converters are controlled using voltage controlled mode as the outer control loop and its reference voltage is adjusted by using the proposed algorithm. The algorithm inputs are the voltage measurement from the common dc bus of the parallel-connected converters and the current measurement of one converter (master current). However, the inner current loop control takes the chosen current measurement (master current) as feedback current signal for the two control loops. Therefore, the load current sharing is achieved based on the droop method. As the control loops for the parallel-connected converters have the same time delay, the output voltage levels for the parallel-connected converters are changed synchronously. This ensures no mismatch in the output voltage and no circulating current during changes in the load, in addition to minimizing the ripple in the output current waveforms.

2. DC-DC Boost Converter Design

The equivalent circuit of a DC-DC boost converter is shown in Figure 3. The DC-DC boost converter circuit consists of a DC power supply, inductor, MOSFET switch, diode, capacitor, and load resistance.

From the operating point of view, the DC-DC boost converter could be operated in Continuous Conduction Mode (CCM) and Discontinuous Condition Mode (DCM) [17]. The operation mode depends on the converters' parameters. For CCM, the parameters for the boost converter such capacitance, C, inductance, L, and duty cycle, D, can be obtained by the following expressions.

$$D = 1 - \frac{V_{in}}{V_{out}} \tag{1}$$

Table 1: Operating values for boost converter.

Parameters	DC-DC Boost Converter
Switching frequency $\boldsymbol{f_s}$	25 KHz
Inductance $\boldsymbol{L}$	15.986 mH
Capacitance $\boldsymbol{C}$	128.646 μF
Power $\boldsymbol{P}$	144 W

$$C = \frac{(I_{out} * D)}{(\delta * V_{out} * f)} \tag{2}$$

$$L = \frac{(V_{in} * D)}{(\delta * I_{in} * f)} \tag{3}$$

where the ripple limit (δ) is (1%). The boost converter parameters are obtained as shown in Table 1.

3. Design of PI Controller Using SISO Tool in Matlab

By considering a CCM, the boost converter in Figure 1 is switched between two states (ON/OFF). The inductor current (I_L) and the output voltage (V_{out}) waveforms with PWM at duty cycle of 0.5 are shown in Figure 4.

As shown in Figure 4, during the ON state the inductor current is increased, but the output voltage is decreased. Moreover, for the OFF state, the MOSFET switch is opened resulting in a decrease in the inductor current and increase in the output voltage. During one cycle (ON and OFF states), the state space averaging technique is employed over one switching cycle [18], and it is given by

$$\begin{bmatrix} \dot{i_L} \\ \dot{v_c} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-(1-D)}{L} \\ \frac{(1-D)}{C} & \frac{-1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_{in} \tag{4}$$

$$v_{out} = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} \tag{5}$$

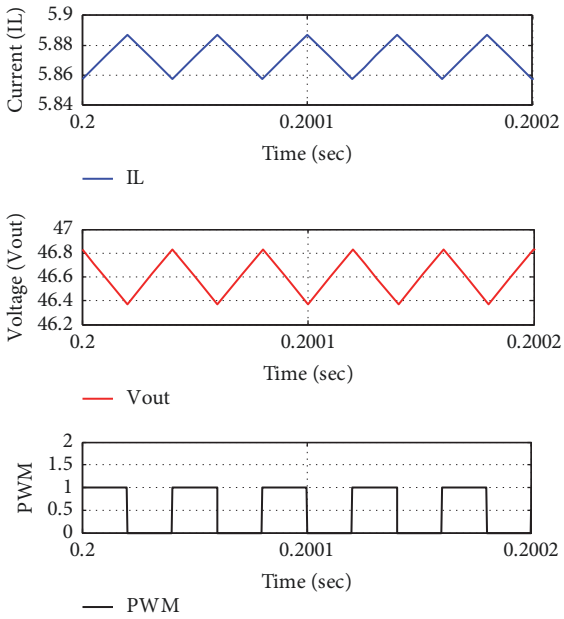

Figure 4: Waveforms of inductor current (I_L) and output voltage (V_{out}) in CCM.

For a small perturbation, the standard linearization technique is used as shown below:

$$\begin{aligned} i_L &= i_L + \tilde{i}_L \\ v_c &= v_c + \tilde{v}_c \\ d &= D + \tilde{d} \\ v_{in} &= v_{in} + \tilde{v}_{in} \end{aligned} \tag{6}$$

During the small signal analysis, the input voltage is considered to be constant. The DC-DC boost converter small signal model can be given by

$$\begin{bmatrix} \dot{\tilde{i}}_L \\ \dot{\tilde{v}}_c \end{bmatrix} = \begin{bmatrix} 0 & \dfrac{-(1-\mathrm{D})}{L} \\ \dfrac{(1-\mathrm{D})}{C} & \dfrac{-1}{RC} \end{bmatrix} \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_c \end{bmatrix} + \begin{bmatrix} \dfrac{V_c}{L} \\ \dfrac{-I_L}{C} \end{bmatrix} \tilde{d} \tag{7}$$

$$V_{out} = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_c \end{bmatrix} \tag{8}$$

The transfer function $\tilde{v}_0/\tilde{d}$ can be obtained from (7) and (8). Similarly, by replacing (8) with (9), the transfer function $\tilde{i}_{in}/\tilde{d}$ can be determined.

$$i_{in} = \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_c \end{bmatrix} \tag{9}$$

Table 2: Parameters of PI controller for boost converter.

	Gains	Type of Controller	
		$\mathrm{PI_{id}}$ Controller	$\mathrm{PI_{vi}}$ Controller
Converter	Proportional gain k_p	0.0809484	0.016874
	Integral gain k_i	20.756	12.98

The transfer functions G_{vi} for the outer loop and the inner loop G_{id} are given as

$$G_{vi} = \frac{-16\,(S - 235.8)}{(S + 971.7)} \tag{10}$$

$$G_{id} = \frac{3092.9\,(S + 971.7)}{\left(S^2 + 485.8 * S + 1.146 * 10^5\right)} \tag{11}$$

where v is the output voltage, i is the inductor current, and d is the duty cycle. However, Figure 5 shows the basic structure of PI_{vi} controller for the outer loop and PI_{id} for the inner loop.

Several methods such as Ziegler-Nicholas, loop shaping method, and frequency response can be used to design a PI controller [19, 20]. However, for simplicity, Sisotool from Matlab/Simulink is used to tune the controller and evaluate the suitability of stability. For the outer loop, the Sisotool command of the transfer functions G_{vi} is used in the control system toolbox to provide a graphical user interface for the bode plot and root locus as shown in Figure 6.

The zero in the right z plane for root locus of the boost converter does not affect the absolute stability of the system [21, 22]. By modifying the pole-zero pattern of the feedback controller, the closed-loop frequency response can be changed until the desired repose is obtained. To determine the $\mathrm{PI_{vi}}$ gains, the position of the root locus is modified online. The gains for the proportional and integral controller for the outer loop are given in Table 2. Similarly, the Sisotool command is used for the inner loop transfer function G_{id}. The graphical user interface is generated for the root locus and bode plot as shown in Figure 7.

For rise time of 0.002971 seconds, settling time of 0.0164 seconds, and overshoot less than 8%, the gains for $\mathrm{PI_{id}}$ are obtained for the DC-DC boost converter. The gains for the $\mathrm{PI_{vi}}$ and $\mathrm{PI_{id}}$ controllers are given in Table 2.

4. Proposed Method

A schematic diagram of two parallel-connected DC-DC boost converters is shown in Figure 8.

The two parallel-connected DC-DC boost converters in Figure 8 are connected to a common DC, with the load connected directly to the common DC bus. The output voltage and current for converters I and II are V_1, I_1 and V_2, I_2, respectively. Because converter I and converter II are connected to the common DC bus, the output voltages V_1 and V_2 are equal. Therefore, the output voltage of each converter is equal to the load voltage, and the load current is the sum of the output currents of both converters.

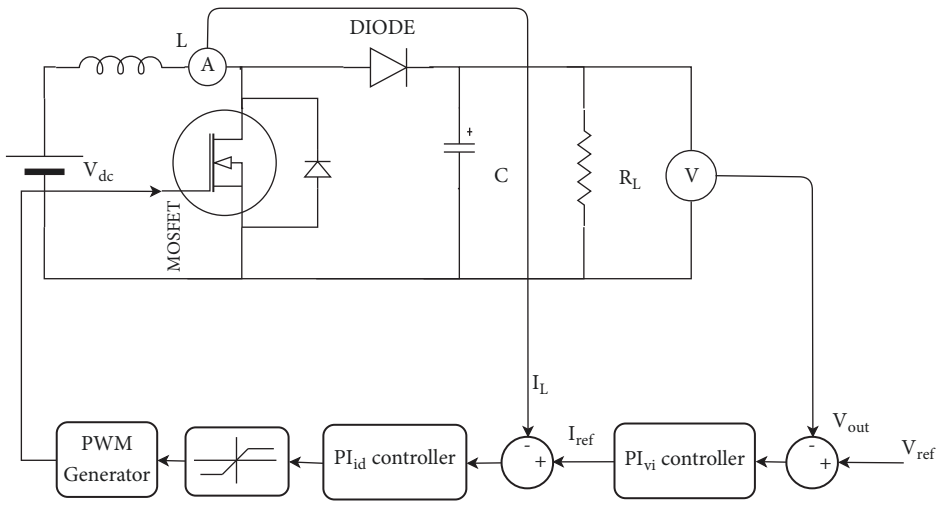

Figure 5: Basic structure of PI_{vi} and PI_{id}controllers for the two loops.

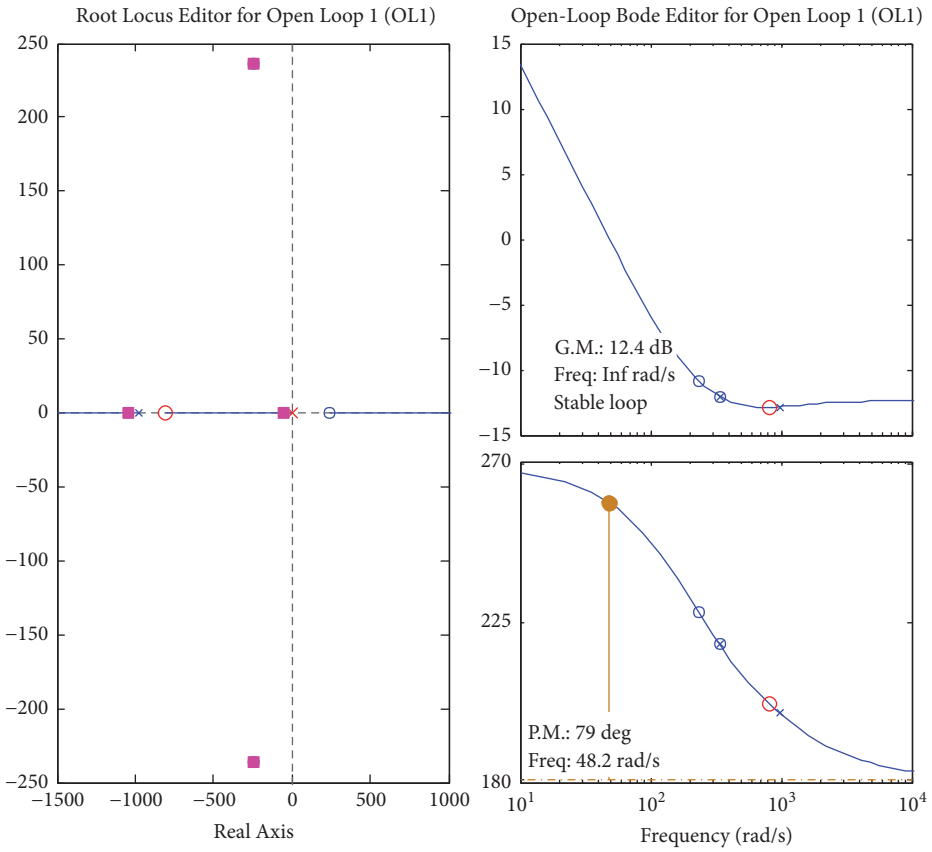

Figure 6: Root locus and open loop bode plots for the outer loop of boost converter.

Zero-circulating current in Figure 8 can be achieved by having zero mismatch in the output voltage during the changes in the load or the input power. The proposed method ensures synchronization in the output voltage level by adjusting the reference voltage according to the droop method. The outer voltage loop for each converter regulates the output voltage which would be in the level of the adjusted reference voltage. The inner control loop uses one of the converters' measured current signal as feedback current signal for the parallel-connected converters (master current control). The inner current loop needs interconnection current measurement between modules. However, to overcome the mismatch in the output voltage, the algorithm is used to adjust the reference voltage for the parallel-connected converters. Figure 9

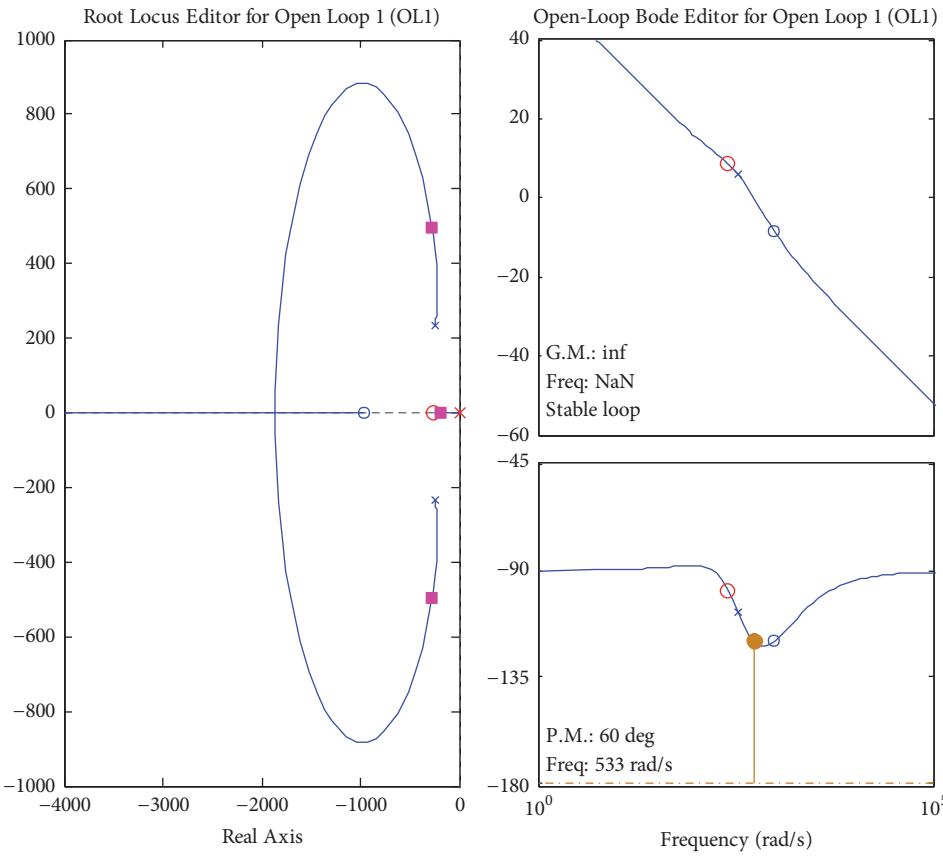

Figure 7: Root locus and open loop bode plots for the inner loop of boost converter.

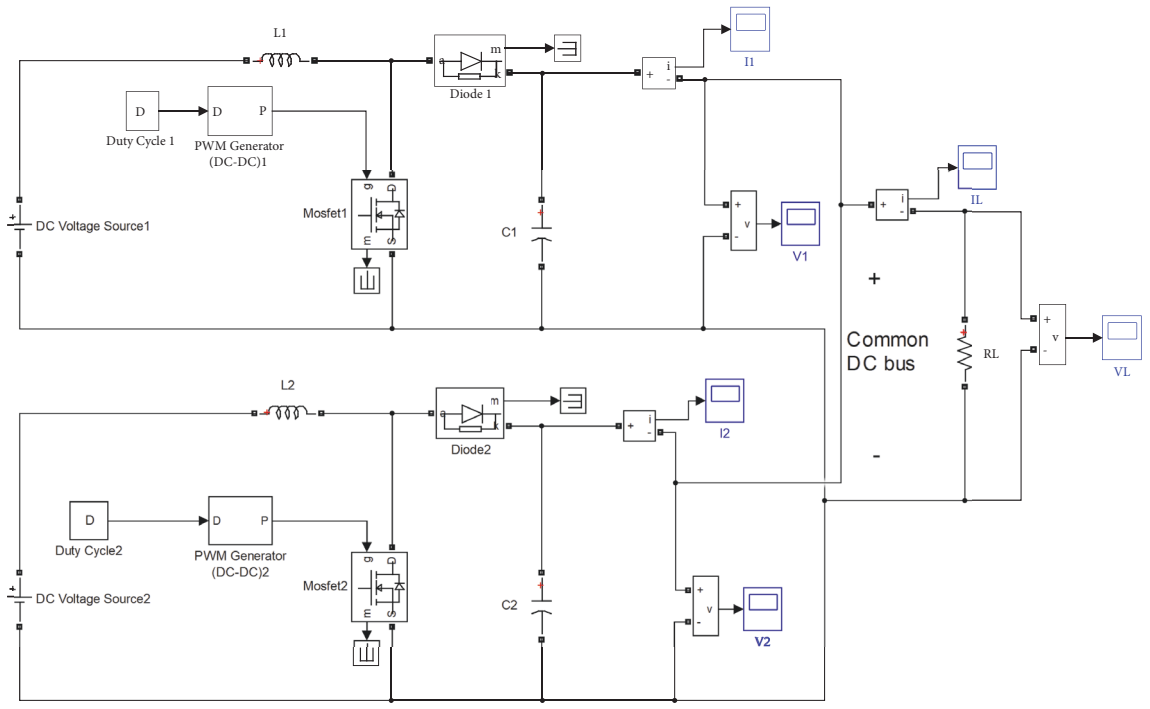

Figure 8: Schematic diagram of the two boost parallel-connected converters.

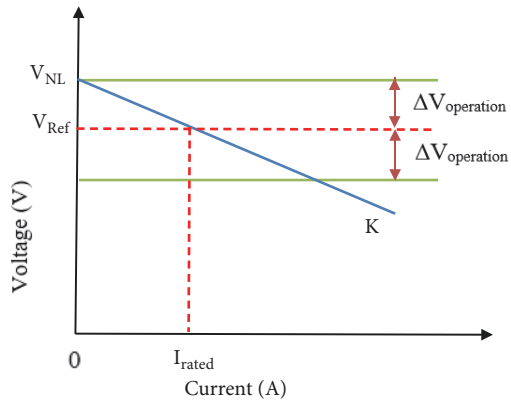

Figure 9: Load regulation characteristic of the droop method with gain of K.

shows the general load regulation characteristics of the droop method [23, 24].

As indicated in Figure 9, V_{NL} is the no-load voltage, V_{ref} is the reference voltage (rated operation voltage), $\Delta V_{operation}$ is the range of voltage that would allow the algorithm to adjust the reference voltage, and K is the droop gain of one of the converters. Therefore, if the output voltage is not within the operation range of the voltage $\Delta V_{operation}$, the reference voltage will be constant and equal to the rated voltage of the converter. From Figure 9, the output droops as the output current increases by

$$V_{out} = V_{NL} - K * I_{out} \tag{12}$$

where V_{out} is the output voltage at the DC bus, and I_{out} is the output current for one of the parallel converters.

Figure 10 shows the block diagram of the two parallel-connected boost converters with the proposed algorithm.

The proposed algorithm inputs are the measured output voltage at the common bus, the output current of one of the converters, and the reference voltage. The load regulation characteristics for the chosen converter are used to adjust the reference voltage during changes in load. Figure 11 shows the flowchart of the proposed algorithm.

From Figure 11, the first step in the proposed algorithm is to check if the output voltage is within the operating zone for the algorithm. If the absolute ΔV is not less than or equal to $\Delta V_{operation}$, ΔV_{ref} is set to zero, and the reference voltage remains at its rated value.

However, if the absolute ΔV is less than or equal to $\Delta V_{operation}$, the output current for the chosen converter is compared with the droop current (I_{droop}). The droop current is calculated based on the load regulation characteristics for the chosen converter as follows:

$$I_{droop} = \frac{(V_{NL} - V_{out})}{K} \tag{13}$$

$$\Delta I_{droop} = I_{droop} - I_{out} \tag{14}$$

ΔI_{droop} is the difference between the calculated droop current and the actual measurement of the chosen converter current. If the absolute ΔI_{droop} is less than or equal to a tolerance error $(1 * e^{-15})$, the operating point will be the same as the calculated operating point based on the load regulation characteristics for the chosen converter. Therefore, the reference voltage will remain at its rated value.

However, if the absolute ΔI_{droop} is not less than or equal to tolerance error $(1 * e^{-15})$, the reference voltage will be adjusted based on the load regulation characteristics for the chosen converter as

$$V_{droop} = V_{NL} - I_{out} * K \tag{15}$$

$$\Delta V_{ref} = V_{ref} - V_{droop} \tag{16}$$

ΔV_{ref} is the difference between the reference voltage and the calculated droop voltage based on the load regulation characteristics for the chosen converter. If ΔV_{ref} is a positive value, it will be subtracted from the reference voltage as shown in the block diagram of the parallel-connected converters, and it means that the output voltage needs to be lowered according to the load regulation characteristics of the droop method. In contrast, if ΔV_{ref} is negative value, it will be added to the reference voltage to increase the output voltage level.

5. Simulation Results and Discussion

Figure 12 shows droop characteristics of two identical parallel-connected DC-DC converters.

The load current sharing is identical because the droop gains of both converters are equal. The main reason for having the same droop gains is that there is no mismatch in the power stage of both converters. At different levels of the output voltage, the output current of the two converters would be shared equally. The simulation of the first case considers the two parallel-connected boost converters with no mismatch or zero mismatch in the power stage. The algorithm for the proposed method will adjust the reference voltage when the load changes. The PI controller parameters in Table 2 are used to obtain the results. In the first examined case, the load is changed from 16 Ω to 8 Ω by adding parallel resistances at 0.2 sec. The load resistance is further reduced from 8 Ω to 5.33 Ω at 0.4 sec. Figure 13 shows the output voltage at the common dc bus.

The output voltage in Figure 13 is adjusted by the proposed algorithm according to the load regulation characteristics of the droop method. The proposed algorithm adjusts the reference voltage when the load changes and provides synchronization of the output voltage level of the parallel converters. Therefore, the load current sharing will be equal based on the identical load regulation characteristics for the two converters as shown in Figure 10. The output current for each converter and the total load current are shown in Figure 14.

As shown in Figures 12, 13, and 14, when the load resistance is 16 Ω, the proposed algorithm adjusts the reference voltage according to the droop method. Because of the load resistance value of 16 Ω, the output voltage level is regulated by the algorithm to be 48.7V, and the output current of each

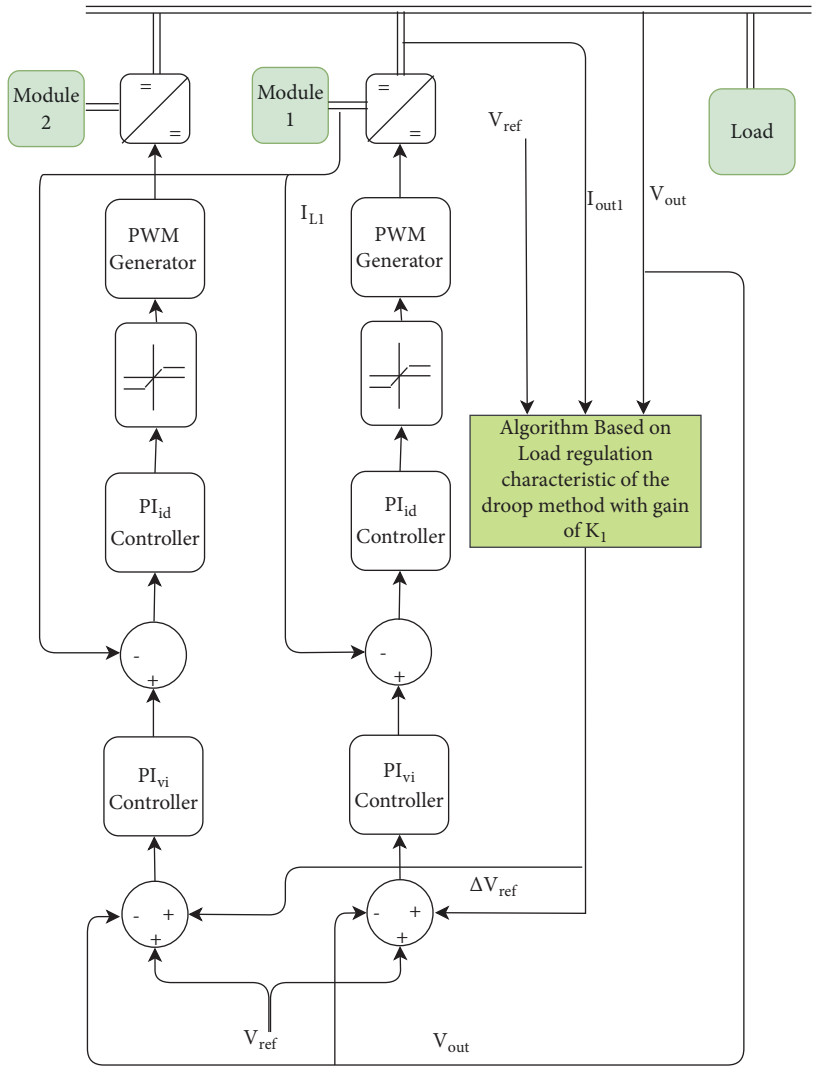

Figure 10: Block diagram of two parallel-connected converters with their control loops and the proposed algorithm.

converter is 1.5 A. Furthermore, when the load is changed from 16 Ω to 8 Ω at 0.2 sec., the proposed algorithm adjusts the reference voltage due to the new change in the load resistance. The output voltage level becomes 48 V, and the output current of each converter is 3 A for the period between 0.2 sec and 0.4 sec. At 0.4 sec. when the load resistance is further reduced to 5.33 Ω, the algorithm regulates the output voltage level to be 47.4 V, and the load current sharing of each converter is 4.425A. With no mismatch in the load regulation characteristics, the proposed method with its algorithm regulates the output voltage level synchronously which results in no mismatch in the output voltage and hence no circulating current.

However, the parameters for the two converters with mismatch in power stage of 10% and 20% of the DC-DC boost converter in Table 1 are given in Table 3. These parameters are implemented in cases two and three.

A second case with 10% mismatch in the load regulation characteristics of the two converters is shown in Figure 15.

Table 3: Operating values for boost converter.

Parameters	DC-DC Boost Converter with 10% mismatch	DC-DC Boost Converter with 20% mismatch
Switching frequency f_s	25 KHz	25 KHz
Inductance L	14.533 mH	13.322 mH
Capacitance C	141.51 μF	154.375μF
Power P	158.4 W	178.8 W

From Figure 15, the load current sharing between the two converters is not identical because of the 10% mismatch in the power stage of the two converters. The droop gains of both converters are different. Based on the mismatch in the load regulation characteristics, the two converters share the load current unequally. Similar to the first case, the load resistance is changed from 16 Ω to 8 Ω at 0.2 sec., and, at 0.4 sec., the

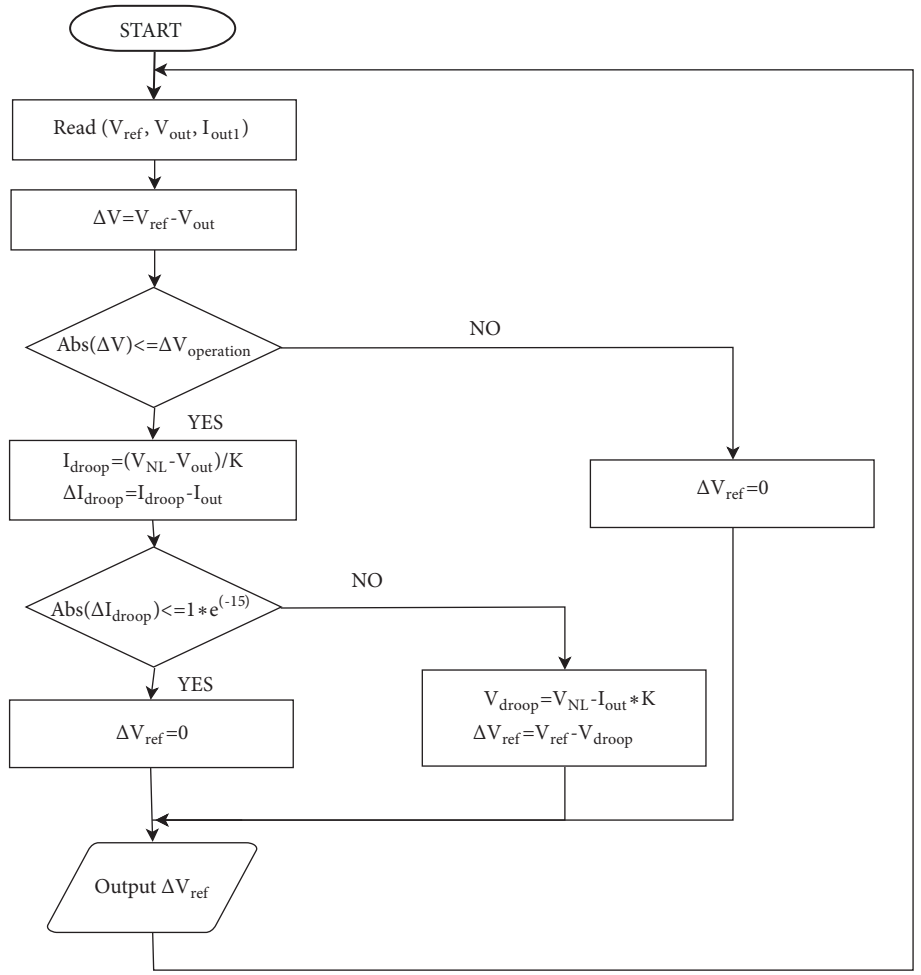

Figure 11: Flowchart of the proposed algorithm.

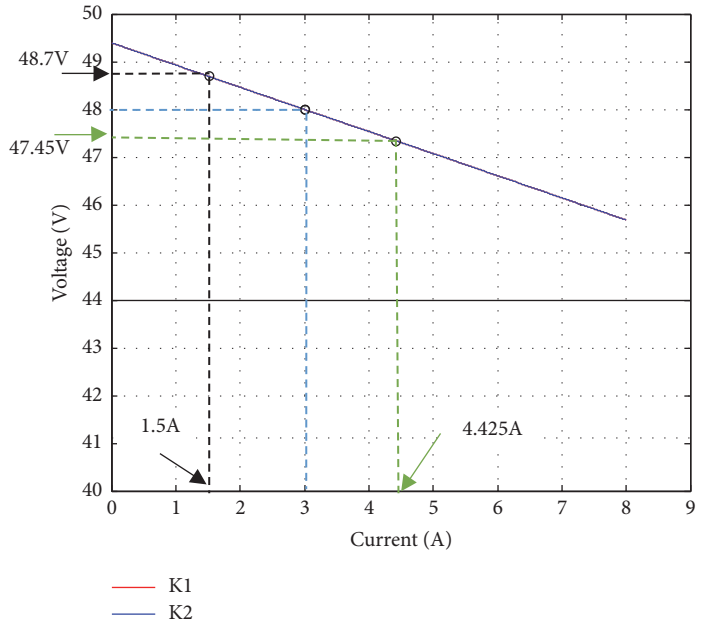

Figure 12: Zero mismatch in load regulation characteristic of the droop method for the two converters.

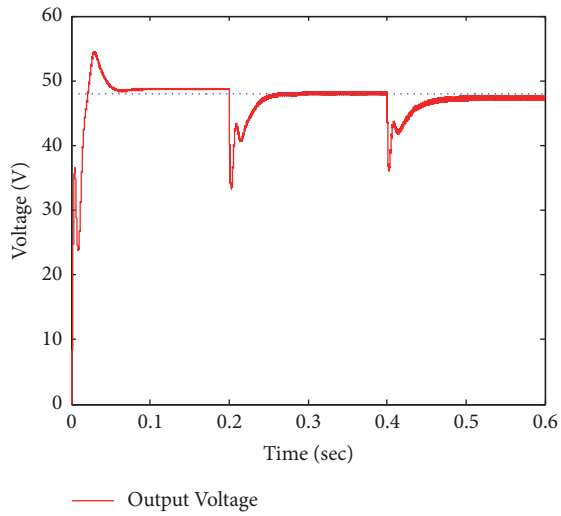

FIGURE 13: Output voltage at the common dc bus.

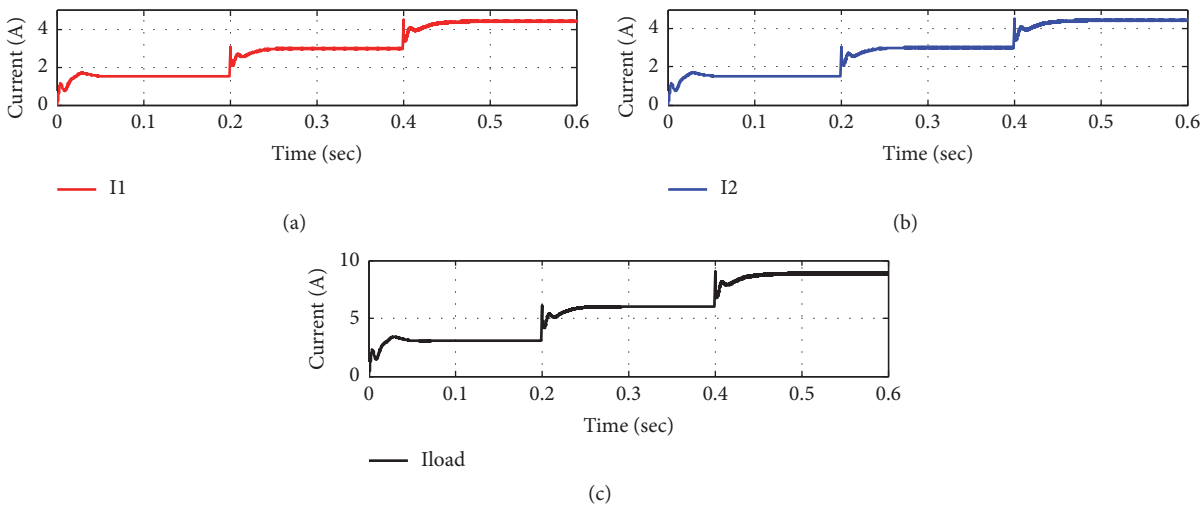

FIGURE 14: The output current from the simulation results of no mismatch case: (a) converter I output current; (b) converter II output current; (c) load current.

load resistance is decreased further from 8 Ω to 5.333 Ω. The output voltage at the common bus with 10% mismatch of the load regulation characteristic of the droop method is shown in Figure 16.

From Figure 16, the proposed algorithm adjusts the reference voltage according to load regulation characteristic of the two converters and it shows that the output voltage is regulated for changes in the load resistance. The output current for each converter and the load current are shown in Figure 17.

When the load resistance is 16 Ω, the regulated output voltage is 48.7 V and the load current sharing for converter I and converter II is 1.4 A and 1.6 A, respectively. Due to the change in the load resistance from 16 Ω to 8 Ω at 0.2 sec., the output voltage level is changed synchronously by the proposed algorithm for both converters to be 48 V. Converters I and II contribute 2.85 A and 3.15 A, respectively, to the total load current. Similarly, the change in the load resistance from 8 Ω to 5.33 Ω causes the proposed algorithm to regulate the output voltage at 47.4 V. The contributions to the load current from converters I and II are 4.2 A and 4.65 A, respectively.

A third case with 20 % mismatch of the load regulation characteristics is shown in Figure 18.

With a 20 % mismatch in the load regulation characteristics, the two converters share the load current unequally. The third case is also simulated with the changes in the load resistance from 16 Ω to 8 Ω at 0.2 sec and from 8 Ω to 5.33 Ω at 0.4 sec. As shown in Figure 19, the output voltage level is regulated by the proposed algorithm.

The output voltage is regulated to be 48.7 V when the load resistance is 16 Ω. When the load resistance is changed to 8 Ω, the algorithm adjusts the output voltage to the new level of 48 V. With transition in the load resistance from 8 Ω to 5.33 Ω at 0.4 sec., the algorithm regulates the output voltage level to be 47.4 V. The load current is shared based on the 20% mismatch

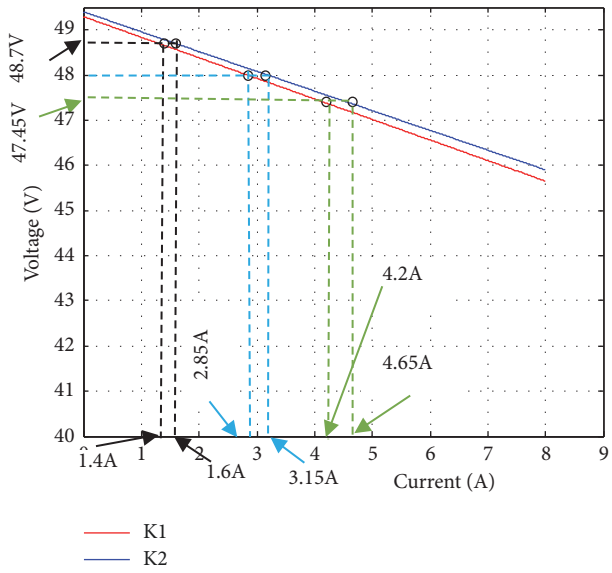

Figure 15: 10% mismatch in load regulation characteristic of the droop method for the two converters.

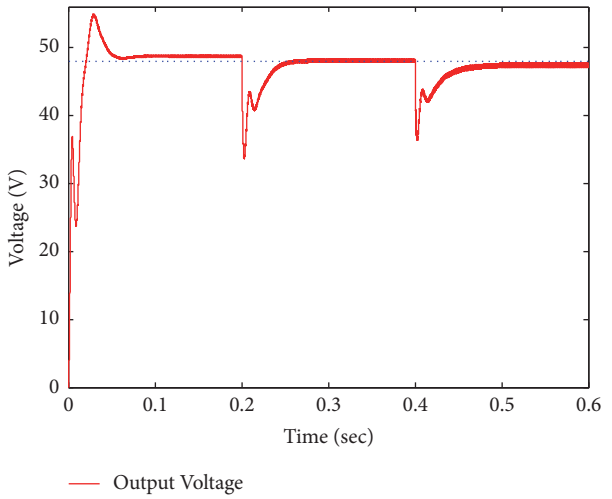

Figure 16: The output voltage at the common dc bus with 10% mismatch in the load regulation characteristics of the droop method.

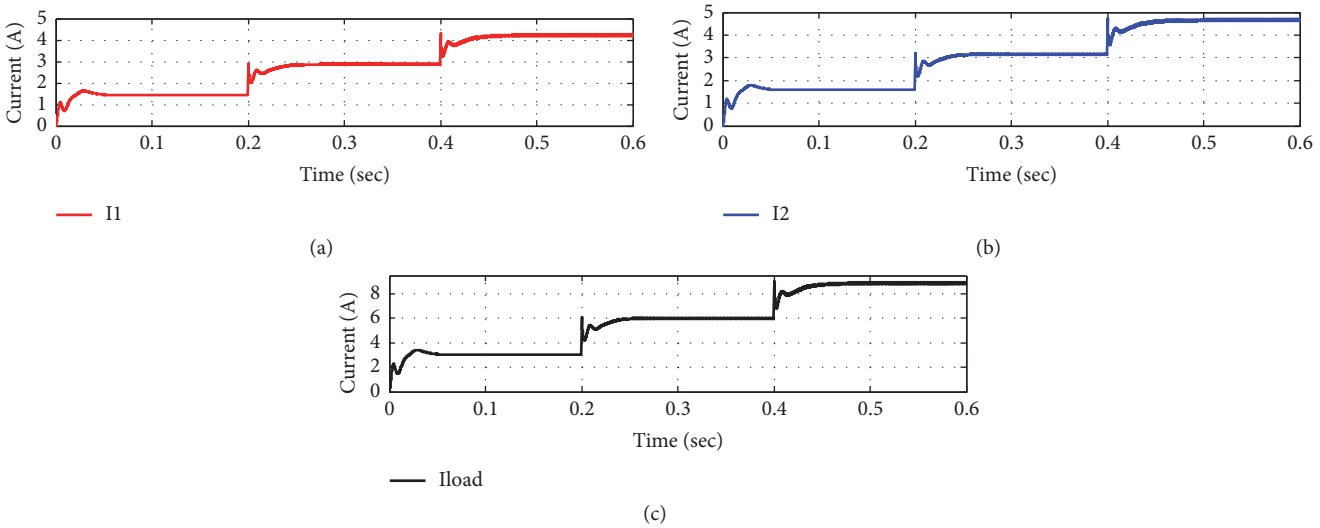

Figure 17: The output current from the simulation results of 10% mismatch case: (a) converter I output current; (b) converter II output current; (c) load current.

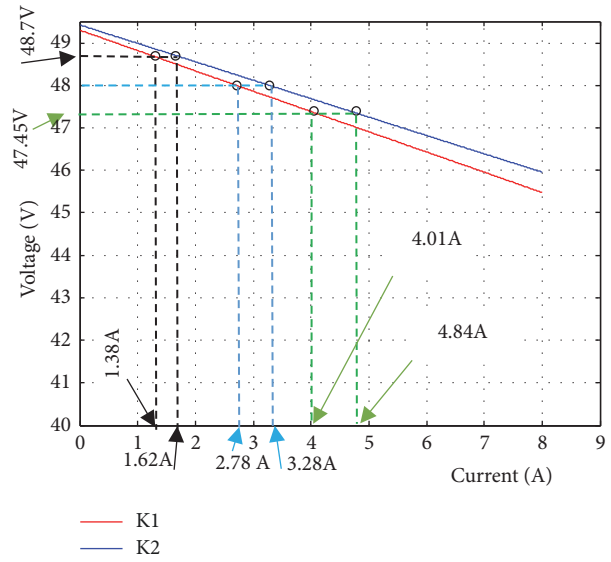

Figure 18: 20% mismatch in load regulation characteristic of the droop method for the two converters.

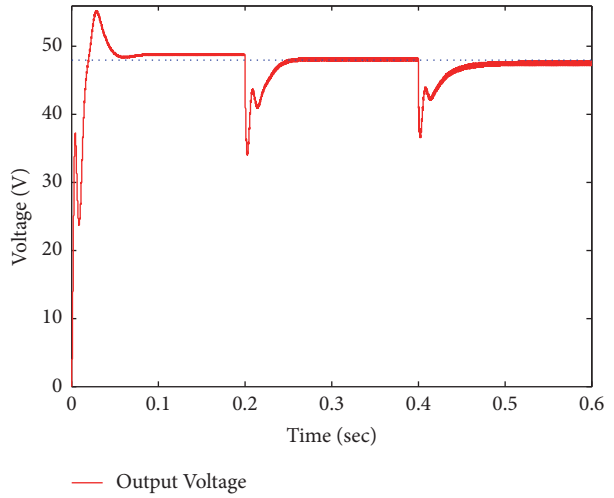

Figure 19: Output voltage with reference voltage.

in the load regulation characteristic for both converters as shown in Figure 20.

As indicated in Figure 20, when the output voltage is adjusted by the proposed algorithm to 48.7 V, the contribution of current for converters I and II to the total load current is 1.38 A and 1.62 A, respectively. However, before 0.4 sec, the load current sharing for converter I is 2.78 A and for converter II is 3.28 A. This is at a regulated output voltage of 48 V. Moreover, when the load is changed from 8 Ω to 5.33 Ω, the new regulated output voltage is 47.4 V. The load current sharing between converter I and converter II is 4.01A and 4.84A, respectively.

This paper presents a proof-of-concept methodology through simulations. In a subsequent paper, experimental results of the performance of two parallel-connected boost converters, which incorporate the proposed modified droop method based on the master current control, will be presented.

6. Conclusion

The simulation cases of the proposed method with its algorithm are presented. The modified droop method based on master current control is verified using Matlab/Simulink simulation. The proposed algorithm adjusts the output voltage according to the load regulation characteristic of the parallel-connected converters. The proposed method ensures that the output voltage level of the two parallel converters is identical, thus avoiding circulating current at the DC bus. Three cases involving no mismatch, 10% mismatch, and 20 % mismatch of the power stage are considered in order to examine the proposed method and its algorithm. The results demonstrate

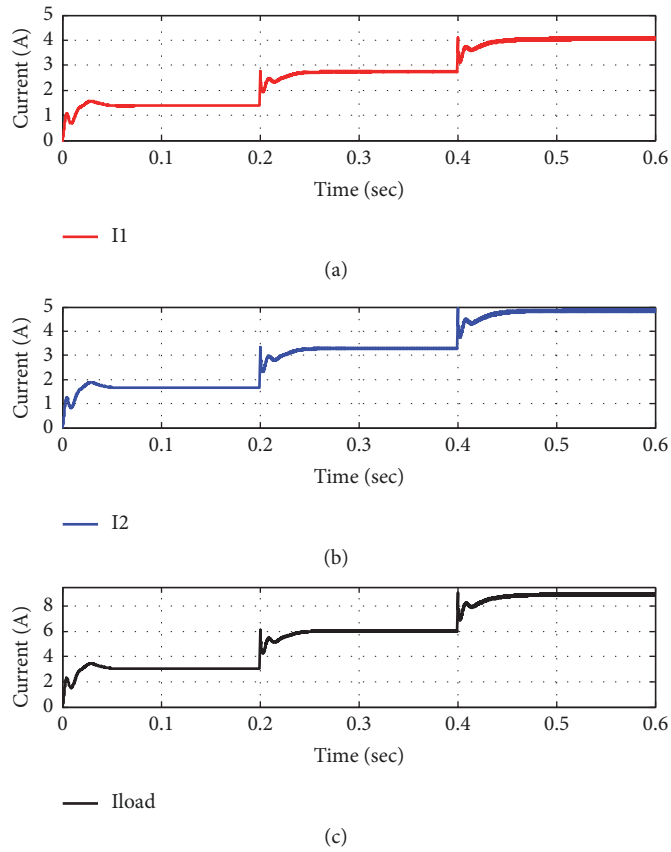

FIGURE 20: The output current from the simulation results for optimized control case. (a) Converter I output current; (b) converter II output current; (c) load current.

the effectiveness of the proposed method and its algorithm.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

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