Analysis and Design of a Dual Series-Resonant DC-DC Converter

by

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A thesis submitted to the

School of Graduate Studies

in partial fulfilment of the

requirements for the degree of

Doctor of Philosophy

Faculty of Engineering and Applied Science

Memorial University of Newfoundland

May 2016

St. John's Newfoundland

Abstract

DC-DC conversion systems are vital components in DC distribution systems, renewable energy generation systems, telecommunication systems, and portable electronics devices. The extensive applications of DC-DC converter have resulted in continuous improvement in the topologies and control methods in these converters. The challenge is to build a converter that improves factors such as efficiency of conversion and power density with a simple topology, which incorporates simplified switching and control schemes and fewer numbers of active and passive components to reduce the manufacturing cost. This thesis addresses this challenge by proposing an alternative topology of a DC-DC converter based on dual series-resonant circuits.

The proposed topology operates under zero voltage switching (ZVS) and zero current switching (ZCS) conditions to reduce the switching losses. It achieves two degrees of freedom (i.e., duty ratio and switching frequency) to control the output voltage of the converter, which results in both step-down and step-up voltage conversions. The number of active components is limited to two semiconductor switches and two rectifying diodes, which reduces the manufacturing cost of the converter. Detailed analytical analysis is carried out using the extended describing function methodology to characterize the steady state and small signal operation of the converter. Small-signal transfer functions are developed and used to propose a simple closed-loop control scheme to control the output voltage of the converter. An experimental 10 V, 40 W prototype of the proposed converter

is built and tested to investigate its operation and confirm its features. The improvement in the efficiency of the converter and power transfer capability of the proposed dual series-resonant converter compared with the traditional single series-resonant circuit, which is used in the interleaved topologies are experimentally verified. In addition, soft switching operation of the converter is realized and a simple control scheme is developed to control the output voltage of the converter. A detailed and step-by-step design procedure is developed, which can be used to customize the design of the converter for different levels of power and voltage.

It is shown that the proposed dual series-resonant DC-DC converter provides significant improvement regarding power density, efficiency of power conversion, simplicity of switching and control schemes, and reduced number of converter components resulting in a low cost and compact converter.

Acknowledgement

I convey my sincerest appreciation and gratitude to my supervisor, Dr. John Quaicoe for his invaluable guidance, support, and positive attitude. I am indebted to him for his commitment and assistance during the course of this Ph.D. program. I would like to thank the other members of my supervisory committee: Dr. Benjamin Jeyasurya and Dr. Tariq Ibal for their valuable advice into the research program.

Generous financial supports from School of Graduate Studies (SGS) and Natural Sciences and Engineering Research Council of Canada (NSERC) for this Ph.D. program are greatly appreciated.

I would like also to send my appreciation to Dr. Leonard Lye, Associate Dean of the Graduate Studies for all the efforts he put to ensure a smooth administrative operation for graduate programs at the Faculty of Engineering and Applied Science.

Finally, I would like to thank my family and friends for their support and encouragement through the entire time of this Ph.D. program.

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List of Abbreviations

ADC	Analog Digital Converter
API	Application Programming Interface
CCM	Continues Current Mode
DCM	Discontinuous Current Mode
DG	Distributed Generation
eGaN	Enhancement-Mode Gallium Nitride
EMI	Electromagnetic Interference
GUI	Graphical User Interface
IC	Integrated Circuit
IDE	Integrated Design Environment
IGBT	Insulated Gate Bipolar Transistor
LRC	Load Resonant Converters
MOSFET	Metal Oxide Silicon Field Effect Transistor
MRC	Multi-Resonant Converters
PLECS	Piece-wise Linear Electrical Circuit Simulation
PRC	Parallel Resonant Converter

PSoC	Programmable System on Chip
PWM	Pulse Width Modulation
QRC	Quasi-Resonant Converters
SAR	Successive Approximation Register
SiC	Silicon Carbide
SPDT	Single-Pole Double Throw
SRC	Series Resonant Converter
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching
ZCT	Zero Current Transition
ZVT	Zero Voltage Transition

List of Symbols

a_n	The n^{th} cosine coefficient of the Fourier expansion of the magnetizing inductor voltage
A_n	The n^{th} cosine coefficient of the Fourier expansion of the $sgn(i_{Lr1}+i_{Lr2})$
b_n	The n^{th} sine coefficient of the Fourier expansion of the magnetizing inductor voltage
B_n	The n^{th} sine coefficient of the Fourier expansion of the $sgn(i_{Lr1}+i_{Lr2})$
B	Buffer
C_{Boot}	Bootstrap capacitor
C_c	Clamping capacitor
C_o	Output capacitor
C_{Q1}	Drain-to-source capacitor of *Q1*
C_{Q2}	Drain-to-source capacitor of *Q2*
$C_{r1}=C_{r2}$	Resonant capacitors
C_s	Snubber capacitor
d	Duty ratio of *Q2*
D1, D2	Output rectifying diodes

$DQ1$	Anti-parallel diode of *Q1*
$DQ2$	Anti-parallel diode of *Q2*
D_{Boot}	Bootstrap diode
D_s	Snubber diode
F	Normalized switching frequency (f_{sw} / f_r)
f_r	Resonant frequency
f_{sw}	Switching frequency
i_{Lm}	Magnetizing inductor current of L_m
i_{Lr1}	Resonant inductor current of L_{r1}
i_{Lr2}	Resonant inductor current of L_{r2}
i_{NLr}	Normalized resonant inductor current
i_{nFCLr}	The n^{th} cosine coefficient of the Fourier expansion of the resonant inductor current
i_{nFSLr}	The n^{th} sine coefficient of the Fourier expansion of the resonant inductor current
I_{GSS}	Gate-to-source forward leakage current
I_{LK}	Bootstrap circuit leakage current
I_{QBS}	Bootstrap circuit quiescent current

I_{SW}	Steady state current of an ideal switch
$I_{Lr1}^{T_x}$	Resonant inductor current of L_{r1} at $t=T_x$
$I_{Lr2}^{T_x}$	Resonant inductor current of L_{r2} at $t=T_x$
J_1 & J_2	Shunt jumpers
K_I	Integral gain of the controller
$L_{r1}=L_{r2}$	Resonant inductors
L_m	Magnetizing inductance of the transformer
L_s	Snubber inductor
N	Turns ratio of the transformer (N_s / N_p)
N_p	Primary winding turns
N_s	Secondary winding turns
ω_r	Angular resonant frequency of L_r and C_r
ω_m	Angular resonant frequency of L_m and C_c
ω_s	Angular switching frequency
Q1, Q2	Semiconductor switches
Q_g	Total gate charge
Q_{gd}	Gate-to-drain charge
Q_{gs}	Gate-to-source charge

Q_{LS}	Total charge required by the internal level shifter of the gate driver
Q_{sw}	Switching charge
R_o	Output load
R_{Boot}	Bootstrap resistor
R_s	Snubber resistor
θ	Phase angle between $sgn(i_{Lr1}+i_{Lr2})$ and v_{Lm} waveforms
$t_{d\text{-}on}$	Turn-on delay time of an ideal switch
T_s	Time period ($T_s = 1 / f_{sw}$)
$T_{new}(s)$	Resultant transfer function with higher order components
V_{aux}	Auxiliary voltage
V_B	Bootstrap voltage
v_{Cr1}	Resonant capacitor voltage of C_{r1}
v_{Cr2}	Resonant capacitor voltage of C_{r2}
v_{NCr}	Normalized resonant capacitor voltage
v_d	Input DC voltage
v_o	Output DC voltage
v_{Cc}	Clamping capacitor voltage
v_{Lm}	Magnetizing inductor voltage

v_{nFCCr}	The n^{th} cosine coefficient of the Fourier expansion of the resonant capacitor voltage
v_{nFSCr}	The n^{th} sine coefficient of the Fourier expansion of the resonant capacitor voltage
$V_{Cr1}^{T_x}$	Resonant capacitor voltage of C_{r1} at $t=T_x$
$V_{Cr2}^{T_x}$	Resonant capacitor voltage of C_{r2} at $t=T_x$
V_S	Switch node voltage
V_{SW}	Steady state voltage of an ideal switch
ζ	Damping ratio
Z_o	Characteristic impedance ($Z_o = \sqrt{L_r / C_r}$)

Chapter 1

Introduction

1.1 Background

Electrical converters play a vital role in our everyday life by shaping the electrical power of electrical sources to meet the needs of consumers and requirements of loads. The electric output power of a source can be AC (single-phase or three-phase, 50 Hz or 60 Hz) or DC (nearly fixed voltage from a battery source or a variable voltage from a renewable energy source). On the other hand, the requirement of the load can be AC or DC power and it varies in a very wide range with respect to the level of voltage and value of the frequency. Among different electrical converter platforms, DC-DC power converters are

gaining extensive attention in research and industry. On a system level, the rapid growth of distributed generation (DG) units based on renewable energy sources and the trend of moving toward DC electrical distribution systems have made an important role for DC-DC converters utilizing green energy resources for customers and in the future electric power distribution system. On a device level, due to the extensive penetration of portable electronic devices such as laptops and cell phones, high-efficient and compact DC-DC converters are an essential part of the device to convert the voltage of the battery to required voltage levels of the devices. It is projected that the market of DC-DC converters will experience a considerable growth from 3.9 billion USD in 2014 to 5.0 billion USD in 2019 with a compound annual growth rate of 4.9% [1].

This growth demands overall improvement in switching techniques of the converters with respect to traditional methods and solutions to address the needs of today's industry. Since the advent of pulse width modulation (PWM) technique in the 1970s, this technique has been widely used as the main switching technique in DC-DC converters. In this technique, the switching action happens based on the comparison between a carrier signal and a control signal. In other words, in PWM switching method, the switching action occurs regardless of the on-state current or off-state voltage of the switch. Because of such a hard switching scheme, during turn-on instant of the switch and after sending the trigger-on command to the switch and passing the turn-on delay time ($t_{d\text{-}on}$), the current of the switch starts to increase from zero and reaches its final value I_{SW}. During this interval, the voltage drop across the switch (V_{SW}) either remains constant (for an inductive load) or starts to decrease simultaneously (for a resistive load). Based on the duality concept, similar

variations occur during turn-off action. These variations are shown in Figure 1.1, assuming linear current and voltage variations.

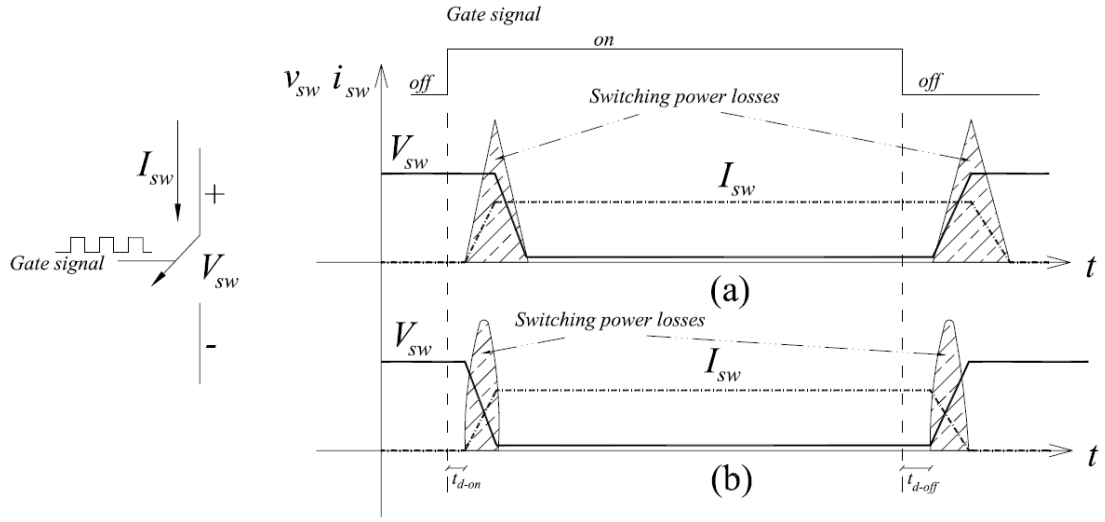


Figure 1.1: Simplified waveforms of voltage and current of the switch during switching instants: a) inductive load, b) resistive load.

This phenomenon causes non-zero product of voltage and current of the switch during switching transitions, which increases the switching power losses, heats up the switch, poses a limitation for high switching frequency operation, deteriorates the efficiency, and increases the electromagnetic interference (EMI) profile of the converter.

Considerable efforts have been made to reduce the switching losses and increase the efficiency of the converter. Using snubber circuits is one of the solutions to reduce the switching losses. In these circuits, either the capacitor (in turn-off snubbers) or the inductor (in turn-on snubbers) mitigates *dv/dt* or *di/dt* associated with the switch, respectively. However, as illustrated in Figure 1.2, even with the use of snubber circuits, the product of

voltage and current of a switch during the switching instants can be quite significant, especially at high values of switching frequency. The problems of switching losses and EMI associated with high switching frequency can be overcome with soft switching methods, whereby, the value of voltage or current during switching instants is kept at zero or very close to zero, leading to significant reduction in switching losses.

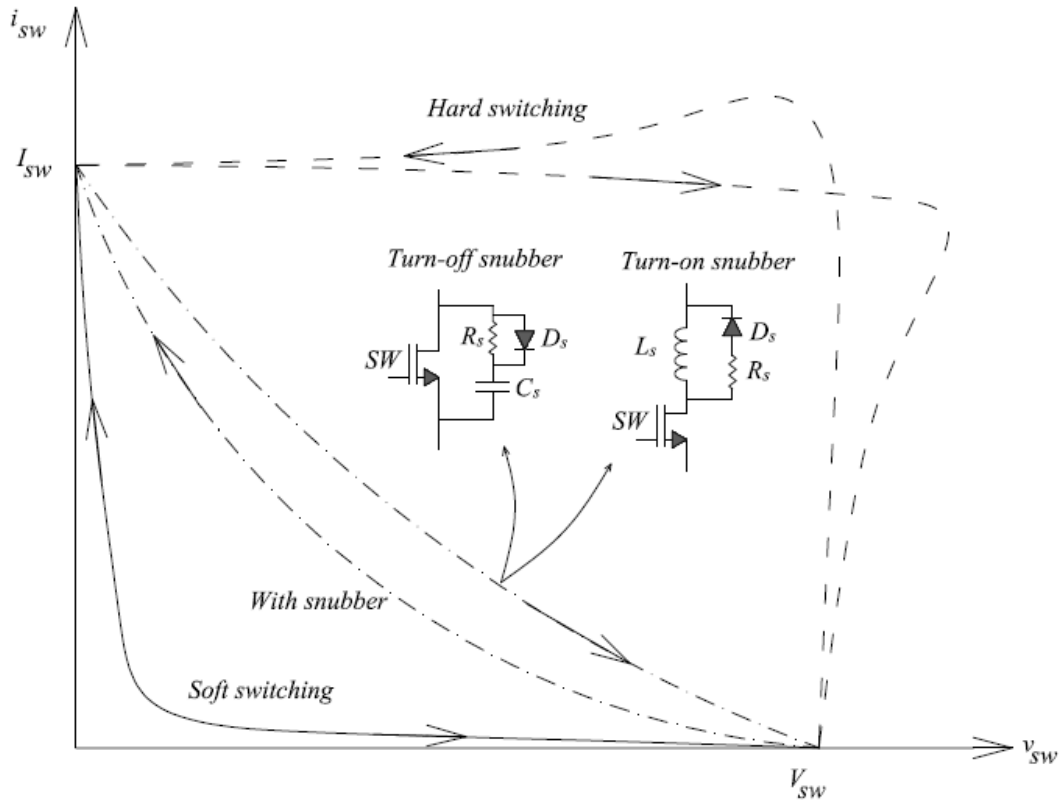


Figure 1.2: Locus of voltage-current variations during switching instants.

Considering the locus of voltage and current of the switch during switching instants for the soft switching case and comparing that with the hard switching method and the snubber case in Figure 1.2, it is noticed that the product of voltage and current is considerably smaller for the soft switching case compared with other two switching approaches,

signifying considerable mitigation in the switching losses. In addition, both conducted and radiated EMI are mitigated due to the reduction of switching transients (*dv/dt* and *di/dt*) [2]-[6].

Since the 1980s, various soft switching methods and topologies have been proposed to solve the problem of switching losses in DC-DC converters such as quasi-resonant converters (QRC), multi-resonant converters (MRC), load resonant converters (LRC), and zero voltage transition (ZVT) and zero current transition (ZCT) converters [7]-[14]. Each of these methods has its own limitations; however, the superior advantage is the achievement of zero voltage switching (ZVS) or zero current switching (ZCS) features that can result in reduction of the switching losses, increase in the power density, and decrease in the EMI level.

1.2 Motivation

Extensive efforts have been made to miniaturize the size and improve the performance of DC-DC converters. The total size, overall efficiency, reliability, manufacturing cost, and the complexity of the topology and control scheme of a DC-DC converter are the most important factors in the evaluation of the performance of a converter. Different research contributions have attempted to improve one or more of the mentioned factors.

In order to make the size of the converter more compact and smaller, increasing the switching frequency and subsequently, operating under soft switching conditions are inevitable. Operating at high switching frequency allows smaller size of passive components to be utilized for the construction of the converter. However, another aspect of

miniaturizing and making the size of the converter more compact is at the converter-topology level, where the topology of the converter is able to transfer more power to the output-connected load without adding interleaved stages, which increases the power transfer capability of the converter at the cost of increasing the size and number of the components used in the topology. By increasing the power transfer capability without adding extra components or stages to the topology of the converter, the power density can be increased. In addition, the total manufacturing cost of the converter can be reduced since the power rating of the converter is increased.

The goal of this research is to develop an alternative DC-DC converter topology that meets the requirements of high efficient, compact topology, reduced manufacturing cost, and simple control scheme. The goal will be achieved through the following objectives:

1. Propose a topology that is capable of increasing the output power transfer of the converter;

2. Develop an analytical methodology to obtain expressions for steady-state and stability characterization of the converter;

3. Design and construct a prototype of the converter and carry out experimental measurements to validate the performance of the converter.

4- Propose a step-by-step procedure to customize the design of the converter for different operating conditions (i.e., output power, input voltage, switching frequency, etc.).

In order to meet the requirements of high overall efficiency, miniaturization, reduced manufacturing cost, versatile applications, and simple control scheme, it is expected that the proposed converter will have the following features:

1. Operate under ZVS and ZCS in order to enable high switching frequency operation and reduced losses to achieve high efficiency;

2. Improve the output power transfer without increasing the number of switching devices and passive components, so as to improve the power density, miniaturize the topology, and reduced manufacturing cost of the converter;

3. Achieve both step-up and step-down output voltage conversion ratios to enhance the versatility and wide utilization of the converter;

4. Regulate the output voltage through either duty ratio control or switching frequency control to accommodate two degrees of freedom to control the output voltage.

1.3 Outline of the Thesis

A survey of the literature on different soft switching DC-DC converters is given in Chapter 2. The development of the proposed topology is given in Chapter 3. In this chapter the proposed DC-DC converter topology, operating principles, and features are presented and the proper operation of the converter under different scenarios is investigated by simulation. Detailed analysis of the proposed topology with respect to: (i) large signal analysis and steady state conditions, and (ii) small signal and stability analysis are presented in Chapter 4. In this chapter, the behavior of the converter is characterized and modeled using the extended describing function methodology to obtained models of the

converter. The analytical models are subsequently simplified and used to design a control scheme to regulate the output voltage of the converter. Experimental results of a 10 V, 40 W prototype of the proposed DC-DC converter are presented and the final comparison between simulation results, analytical modeling result, and the experimental results are given to validate the consistency between simulations and analytical modeling, with experimental results. A systematic procedure for the design of the converter for any level of power or voltage is presented in Chapter 6. The design procedure can be used as a reference guide to customize the proposed topology for different applications. Finally, in Chapter 7 the major outcomes, specific contributions, and further extensions to this research work are discussed.

Chapter 2

Literature Review

By increasing the switching frequency in DC-DC power converters, the size of the passive components can be reduced; consequently, the converter can be miniaturized. However, the drawbacks of increasing the switching frequency are higher stress on the switching devices, more switching losses, increased vulnerability to the parasitic components in the circuit, and higher level of EMI. Due to these drawbacks, the benefits of operating at high switching frequencies cannot be achieved in traditional hard switching schemes. Using soft switching technique in a switching circuit mitigates the aforementioned disadvantages and makes it feasible to increase the switching frequency. Different methods have been

introduced and implemented for numerous topologies of DC-DC power converters to reduce the switching losses and improve the overall efficiency of the converter. The objective of this chapter is to introduce briefly these methods and topologies. This brief introduction is followed by a discussion of the relevant research contributions for soft switching DC-DC power converter topologies, highlighting the advantages, disadvantages, and limitations of each topology in order to establish the context and demonstrate the rationale for this research work.

2.1 Basic Resonant DC-DC Converter Topologies

2.1.1 Quasi-Resonant Converter (QRC)

Both soft switching general forms of ZVS and ZCS can be achieved in these types of converters. The family of quasi-resonant converters (QRC) can be constructed by replacing the power switch in a traditional PWM converter with either ZVS or ZCS resonant switches [7], [8]. Figure 2.1 and Figure 2.2 show the topologies of zero-voltage and zero-current resonant switches, respectively.

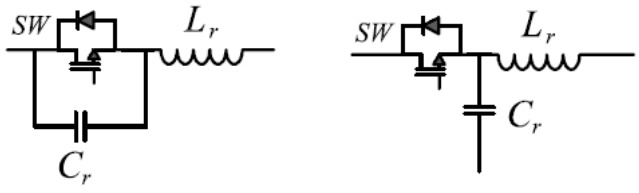


Figure 2.1: Zero-voltage resonant switches.

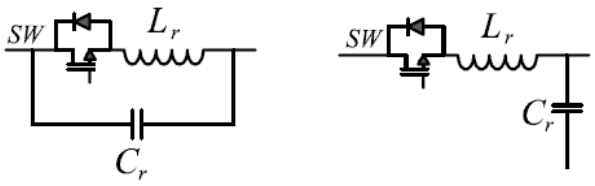


Figure 2.2: Zero-current resonant switches.

It is worth noting that the topologies of the ZVS and ZCS resonant switches are duals. As an example, Figure 2.3 and Figure 2.4 show the topologies of QRC-ZVS and QRC-ZCS buck converter topologies, respectively. These two topologies are achieved by replacing the power switch in a simple PWM buck converter with ZVS or ZCS resonant switches.

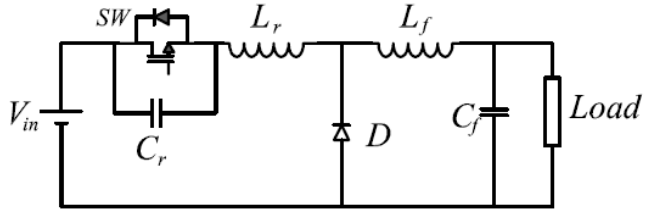


Figure 2.3: QRC-ZVS DC-DC buck converter.

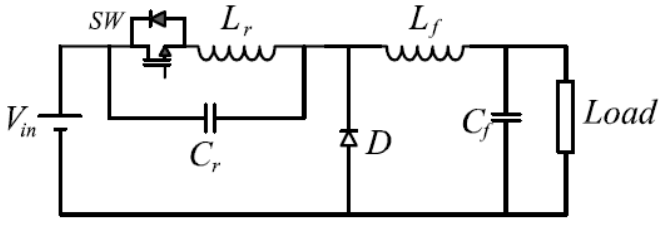


Figure 2.4: QRC-ZCS DC-DC buck converter.

Despite the fact that the topologies of both QRC-ZVS and QRC-ZCS converters are derived based on the simple PWM DC-DC converter, QRC-ZVS and QRC-ZCS are controlled by switching frequency rather than duty ratio. This results in the dependency of the efficiency of the converter on the switching frequency and adds more complexity to the control scheme. Kwon et al. [15] proposed an isolated topology of a single-switched quasi-resonant DC-DC converter. Although the proposed topology employs only one semiconductor switch that operates under ZVS condition, the free-wheeling diode experiences hard-switching at turn-on transitions. Besides, input power is transferred to the output load during only one of the four operational modes of the converter, which reduces the power density of the converter. An isolated ZVZCS quasi-resonant CLL DC-DC converter was proposed by Ryu, et al. [16], in which the switching frequency varies slightly in response to 70% variation in the load. However, during the discharging mode of the resonant capacitor, which is the longest mode of the operation of the converter, only the output capacitor supplies the load current. As a result, the converter experiences high output voltage ripple and partial power transfer to the output load. Consequently, improvements in the performance of the converter are achieved at the expense of increased output voltage ripple for large loads and reduction in the power density of the converter.

2.1.2 Load Resonant Converter (LRC)

Two well-known topologies of this class of converters are series resonance converter (SRC) and parallel resonance converter (PRC). The resonant tank is connected between a half-bridge or full-bridge inverter stage and a diode rectification stage. Figure 2.5 and Figure 2.6 show the topology of SRC and PRC, respectively. Depending on the switching

frequency, the converter operates in either the discontinuous current mode (DCM) or continuous current mode (CCM). Table 2.1 shows the soft switching conditions for both the SRC and PRC converters under DCM and CCM conditions.

A drawback of these converters is that output voltage regulation is achieved by changing the switching frequency. Optimization of the output filter becomes a challenge under variable switching frequency operation, since the filter needs to be designed for the worst-case scenario. An alternative topology of the SRC converter was proposed by Ting, et al. [17], which enables fixed switching frequency operation. The proposed topology consists of four switches in a full bridge configuration and an extra inductor between the legs of the full bridge that makes the converter bulky. The SRC converter operates only as a step-down converter and it exhibits poor voltage regulation. For the case of the PRC, the problem of circulating current poses a difficulty especially for a wide range of input voltage variations. Operation of the converter in CCM results in almost sinusoidal current, and the peak values of the inductor current and capacitor voltage can be reduced by increasing the switching frequency. However, both PRC and SRC converters need relatively large resonant inductor that makes the converter bulky [11].

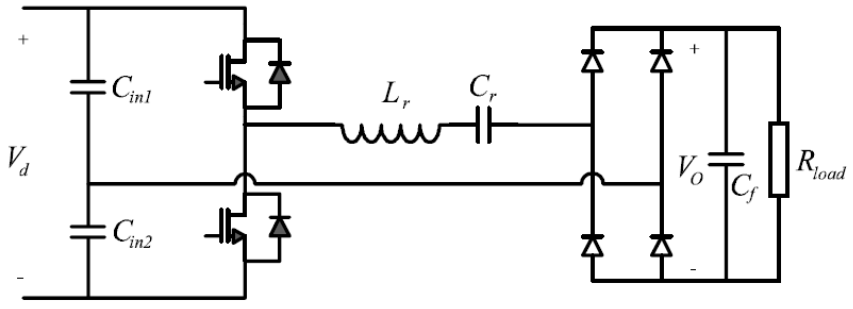


Figure 2.5: Series resonant converter (SRC).

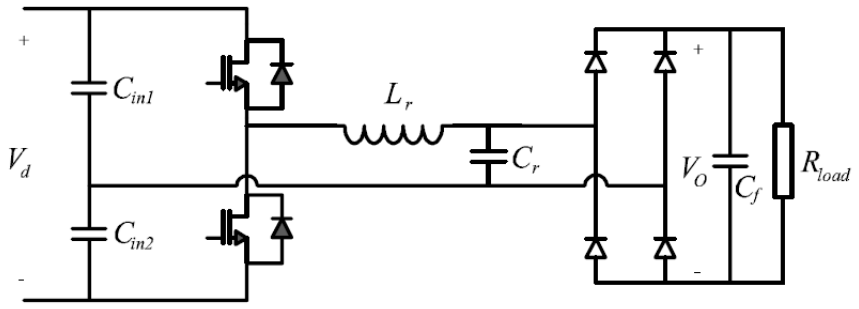


Figure 2.6: Parallel resonant converter (PRC).

Table 2.1: Soft switching conditions for load resonant converter.

	Series-Loaded Resonant Converter			Parallel-Loaded Resonant Converter		
	Discontinuous Mode (DCM)	Continuous Mode (CCM)		Discontinuous Mode (DCM)	Continuous Mode (CCM)	
	$\omega_s < 0.5\omega_r$	$0.5\omega_r < \omega_s < \omega_r$	$\omega_s > \omega_r$	$\omega_s < 0.5\omega_r$	$0.5\omega_r < \omega_s < \omega_r$	$\omega_s > \omega_r$
ZC turn on	Yes	No	Yes	Yes	No	Yes
ZC turn off	Yes	Yes	No	Yes	Yes	No
ZV turn on	No	No	Yes	Yes	No	Yes
ZV turn off	Yes	Yes	No	Yes	Yes	No

2.1.3 Multi-Resonant Converter (MRC)

For non-isolated multi-resonant converter (MRC) topologies, the underlying principle of the topologies is the same as QRCs, i.e., the power switch in a traditional PWM converter is replaced by a multi-resonant network. By doing this, one of the limitations of QRCs, which is soft switching operation for either the semiconductor switch or output diodes, can

be overcome. Figure 2.7 and Figure 2.8 show the zero-voltage multi-resonant (ZV-MR) and zero-current multi-resonant (ZC-MR) networks, respectively [8], [9].

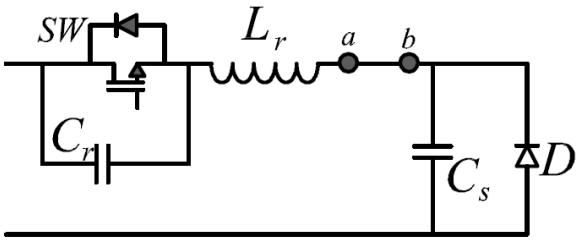


Figure 2.7: Zero-voltage multi-resonant (ZV-MR) network.

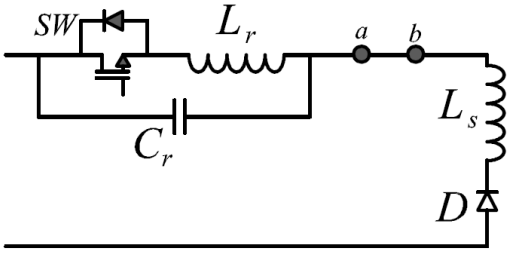


Figure 2.8: Zero-current multi-resonant (ZC-MR) network.

Depending on the converter topology, passive components may exist between node *a* and node *b*. The topologies of ZVS-MRC and ZCS-MRC buck converters are depicted in Figure 2.9 and Figure 2.10, respectively. For isolated converters, as for example the forward ZVS-MRC, the leakage inductance of the transformer is utilized as the inductance L_r in Figure 2.7. For the resonant networks shown in Figure 2.7 and Figure 2.8, the duality concept is applicable. Still the problem of output voltage regulation in the case of wide range of variation in the input voltage exists in the ZVS-MRC and ZCS-MRC. In order to

overcome the problem of variable switching frequency in MRCs, phase-shift control method has been proposed to regulate the output voltage [10]; however, this has been achieved at the expense of increased circuit complexity (i.e., implementation of auxiliary circuits) and complex control scheme.

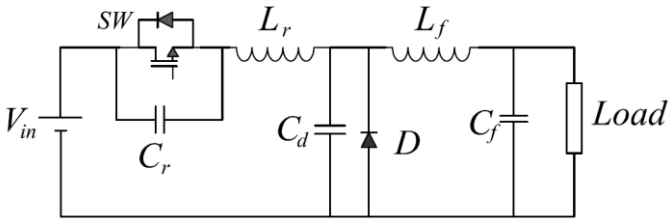


Figure 2.9: ZVS-MRC buck converter.

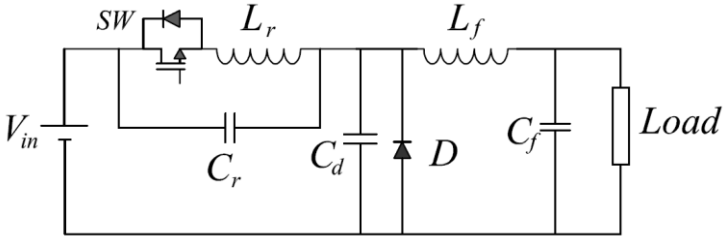


Figure 2.10: ZCS-MRC buck converter.

The isolated topologies of MRC can be achieved by adding extra passive components (capacitor and/or inductor) on the primary side of the isolating transformer in load resonant converter topologies. Depending on the number and type of the additional components, several topologies can be derived. Two very well-known topologies of three-element MRCs are the LLC (i.e., two inductors (LL) and one capacitor (C)) and LCC (i.e., two capacitors (CC) and one inductor (L)) converters, which are shown in Figure 2.11 and

Figure 2.12, respectively. Using transformers with two identical windings on the secondary side, these converters can be constructed with two diodes at the output.

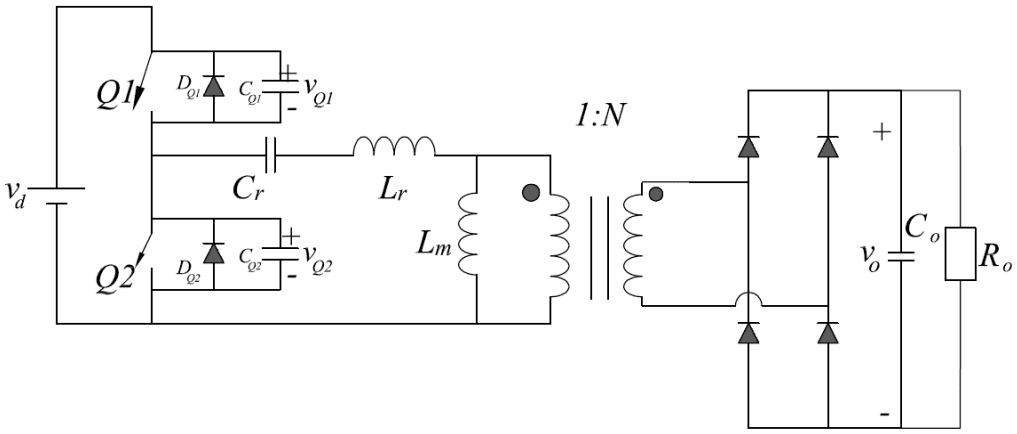


Figure 2.11: Multi resonant LLC DC-DC converter.

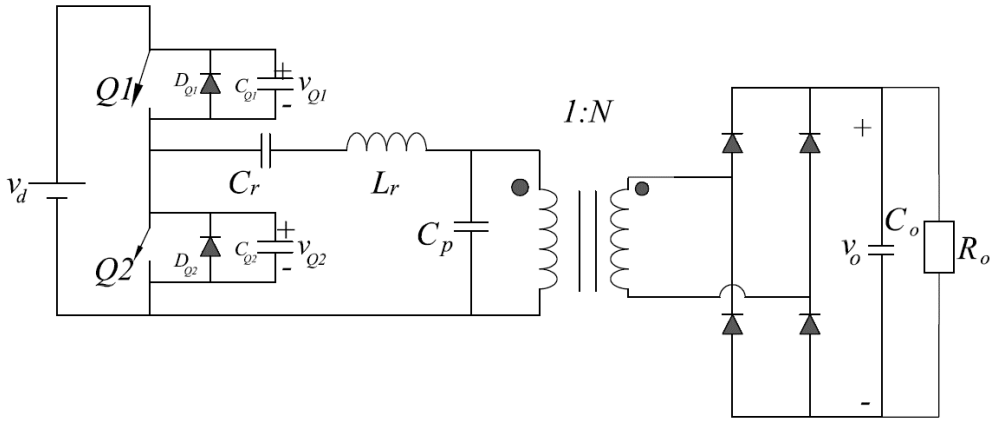


Figure 2.12: Multi resonant LCC DC-DC converter.

Depending on the value of the parallel capacitor, the LCC converter behaves similar to either PRC, if $C_r >> C_p$, or SRC, if C_p is very small. Therefore, LCC combines the characteristics of both SRC and PRC topologies. The LLC topology can regulate the

output voltage over wide range of input voltage and it operates under ZVS condition over its entire load range [18]. In addition, the overall size of the converter is smaller since the size of the output filter is reduced [19]. Furthermore, it has been reported that the LLC topology exhibits better performance compared with the LCC topology since the efficiency is more flat as the switching frequency varies [20]. The basic problems with these two topologies are: 1) the regulation of the output voltage, which is achieved under a variable switching frequency scheme; 2) the overall efficiency of the converters drops when the switching frequency is far away from the resonant frequency [21]-[25]. In general, the efficiency of the LLC converter drops when the switching frequency decreases, whereas the efficiency of the LCC topology drops when the switching frequency increases [26]. Although higher efficiency for wider range of switching frequency has been reported in the literature [27], [28], the improvements have been achieved by adding more active and passive components. The increase in the number of components and the size of the converter reduce the total power density of the converter. Besides, the control scheme of the converter becomes more complicated as the number of active components increases.

2.1.4 Zero-Voltage Transition and Zero-Current Transition Converters (ZVT & ZCT)

Zero-Voltage Transition (ZVT) and Zero-Current Transition (ZCT) converters can be constructed using auxiliary resonant circuits in parallel with the main switch of the converter [12], [13]. The corresponding auxiliary resonant circuits for both ZVT and ZCT

converters are shown in Figure 2.13 and Figure 2.14, respectively. For non-isolated converters, the main switch (*SW*) needs to be replaced with the switch networks shown in Figure 2.13 and Figure 2.14. The topologies of ZVT-boost converter and ZCT-boost converter are shown in Figure 2.15 and Figure 2.16, respectively. For these converters, output voltage regulation is achieved by using a constant frequency PWM switching scheme. An advantage of this class of converters is that soft switching operation can be achieved and the voltage and the current stresses on the main switch can be maintained within a safe margin [12]-[14]. Despite the developments of ZVT and ZCT for non-isolated converters [14], [29]-[30], the development of ZVT and ZCT techniques for isolated converters is challenging. The reason is that for isolated DC-DC converters, the auxiliary resonant circuits are such that the leakage inductance of the transformer cannot be utilized as a resonant component in the converter. This makes the design of the transformer difficult, as it needs to be constructed with minimum leakage inductance.

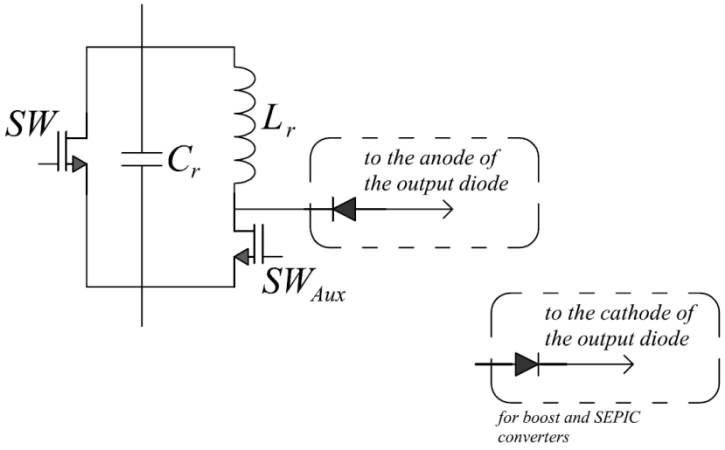


Figure 2.13: Auxiliary network for zero voltage transition (ZVT).

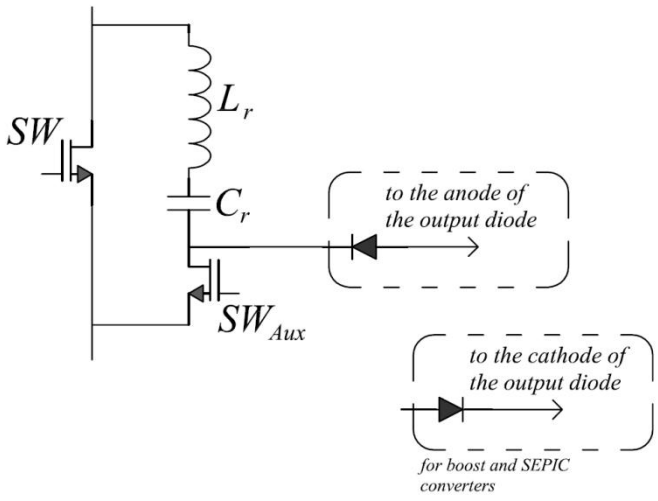


Figure 2.14: Auxiliary network for zero current transition (ZCT).

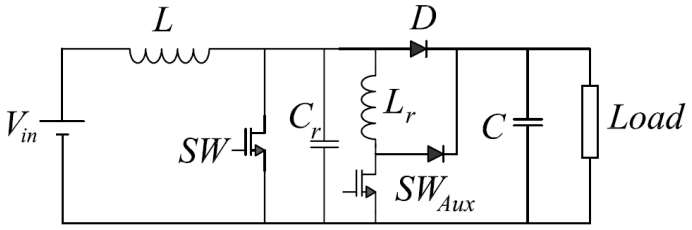


Figure 2.15: ZVT-boost converter.

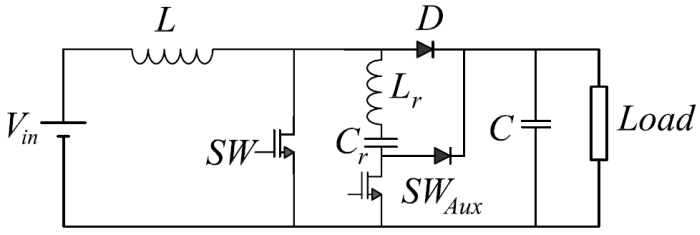


Figure 2.16: ZCT-boost converter.

2.2 Transformer-Based DC-DC Converters

Among the several topologies for soft switching DC-DC converters that are proposed to meet new requirements and industry standards, isolated converters are preferred due to the galvanic isolation, reliability, safety, and protection requirements in accordance with IEEE Standard 519 and 1547 [31]. Numerous topologies of isolated DC-DC converter have been proposed in the literature [32]-[41].

Zheng, et al. [42] proposed an isolated single-switch DC-DC converter that has the capability to transfer power to the output load during the entire operating modes of the converter. A drawback of the converter is the use of hard switching operation, which results in high switching losses. An improved topology that uses a zero current resonant network to achieve soft switching operation was proposed later [43]. The proposed topology utilizes the leakage inductance of the isolating transformer, and along with the capacitor and inductor of the zero current resonant network, it forms an LCL network. Experimental results show improvement in the efficiency of the proposed converter; however, the maximum efficiency of the converter is achieved at almost half load and the efficiency drops at the full load condition.

A full-bridge topology of the series resonant converter with the ability of direct power transfer to the output has been proposed [44]. ZVS operation for semiconductor switches and ZCS operation for output diodes are interesting features of the topology. However, this topology consists of four semiconductor switches at the primary side of the transformer and one bidirectional switch at the secondary side. Besides the increased conduction

losses, the control scheme of the converter becomes more complicated since the bidirectional switch controls the power flow and voltage conversion ratio.

The forward resonant converter is another category of the isolated resonant DC-DC converters that are popular because of their low cost, simple structure, and ZVS operational characteristics [45]-[47]. However, the drawbacks of the converters are forward transformer resetting and limitation on the range of duty ratio, which should be less than 0.5 in two-switch forward resonant converters [48]. This makes the application of two-switch forward resonant converters impossible when a wide range of voltage regulation is required. Some research contributions have addressed the aforementioned problems and have achieved increases in the range of duty ratio [49], [50]. However, either the soft switching operation is violated or the converter suffers from complexity in topology and control scheme and low power transfer capability. Interleaving technique is a well-know approach to increase the power transfer of the converter to the output load and reduce the ripple on the output capacitor, leading to choose a smaller output capacitor [51]-[66]. In this technique, identical stages of a converter are paralleled with each other, with one shared load at the output and one shared source at the input. The switching gate signals of stages are phase-shifted according to the number of the stages. As an example, a 2-stage interleaving technique was proposed to increase the power transferred to the load in one complete cycle of operation [66]. The increased power transfer was achieved at the cost of doubling the total number of passive and active components of the converter. Therefore, the overall power density of the converter remains almost unchanged, while the control scheme becomes more complicated.

Flyback converters bring considerable improvements from the point of view of simplicity of the topology, low parts count, and wide range of operation. This type of converter is the isolated version of the buck-boost converter, in which a flyback transformer provides the task of isolation. However, flyback converters suffer from poor transformer utilization and not having high power density since the power cannot be delivered to the output during all modes of operation. Using clamp capacitors at the primary side of the transformer improves the utilization of the transformer by providing energy balance across the magnetizing inductor of the transformer. Due to its simple topology, and small size, active clamping flyback converters have been considered a good solution to achieve ZVS and ZCS operations [67], [68]. However, the problem of partial power transfer to the output load remains a challenge for active clamping flyback converters. Several efforts have been made to improve the power density of the flyback converters [69], [70]. The challenge is to achieve increased power transfer without additional or auxiliary active components.

2.3 Objective of the Research

The objective of this work is to propose an alternative topology, referred to as a dual series-resonant DC-DC converter that achieves increased overall efficiency, improved power density, reduced number of active semiconductor components, and simplified control scheme to regulate the output voltage. The proposed converter should provide both ZVS and ZCS for semiconductor switches and output diodes, respectively. This would make the operation at higher frequencies feasible and would lead to increased converter efficiency. The topology should be capable of transferring power to the output load during both positive and negative cycles of operation, thereby increasing the power density of the

converter without introducing more switching components and using techniques such as interleaving method. The number of semiconductor components is to be kept to minimum (not more than two switches), leading to reduced cost of the converter. With a two-switch topology, the possibility of complementary switching operation can be exploited to simplify the control scheme. Finally, the proposed topology should be capable of providing output voltage regulation through a single-loop, voltage-feedback control scheme. To the best of the author's knowledge, a converter topology that incorporates the aforementioned features has not been addressed in the literature.

2.4 Summary

This chapter gave a categorized introduction about the common topologies of resonant DC-DC converters. Some of the typical and fundamental topologies and techniques for soft switching approaches in DC-DC converters were presented. The advantages, disadvantages, and limitations of each topology were discussed. This was followed by an extensive review of recent proposed topologies in the literature. The discussions led to the realization of the common technical challenges, and the necessity to propose a new topology to address those challenges regarding DC-DC converters. The subsequent chapters are devoted to the development, analysis, experimental validation, and design of the proposed converter topology.

Chapter 3

Dual Series-Resonant DC-DC Converter

Increasing the power density of DC-DC power electronic converters is always an on-going demand for customers since the preference is always given to small and miniaturized equipment and gadgets. Operation at high switching frequency leads to smaller and more compact DC-DC power electronic converters; however, the downsides are more switching losses, higher EMI, and fewer options for the semiconductor switching devices.

Increasing the power transfer capability of the DC-DC power electronics converters is the other aspect of power density. A low cost solution to increase the rated power of DC-DC power electronics converters is always interesting to manufacturing companies.

Techniques such as interleaving methods increase the power transfer capabilities of the DC-DC converters; however, it is associated with higher manufacturing cost because of more components that are used in the interleaved DC-DC converters. In addition, the overall size and weight of the circuit inevitably increase with this approach.

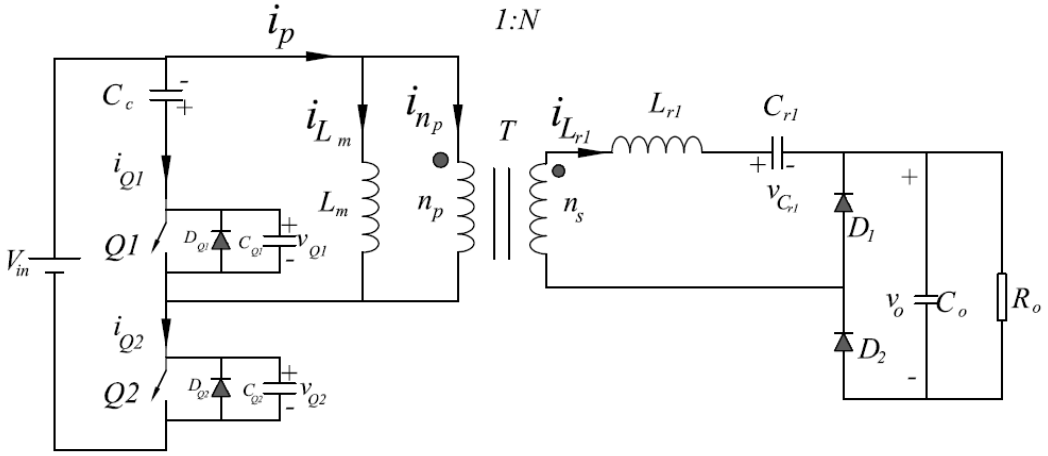
In this chapter, the proposed dual series-resonant DC-DC converter is presented. The main objective of the proposed topology is to increase the power density of the DC-DC converter (i.e., increase the power transfer capability of the converter without significantly increasing the number of components). The details of the operation of the proposed converter during each mode are described and the soft switching feature of the converter is theoretically demonstrated. In addition, the improvement in the power transfer capability of the converter is demonstrated. The operation of the converter under different scenarios is investigated in the PLECS simulation environment to confirm the feasibility of the proposed topology. Finally, the importance and merits of operating the converter in the continuous current mode (CCM) are elaborated and the boundary condition between the discontinuous current mode (DCM) and CCM is presented.

3.1 Development of the Proposed Topology

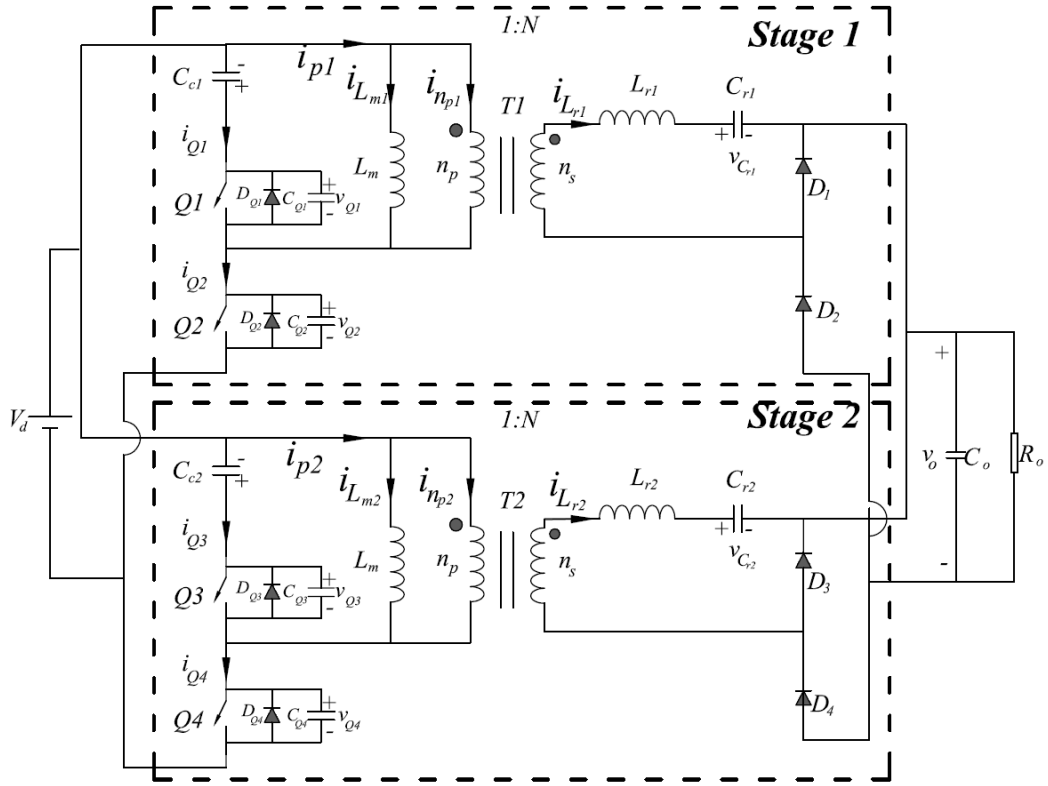
The proposed converter is based on the basic topology, which is shown in Figure 3.1 (a). This figure shows an isolated DC-DC converter, which transfers input power to the output load during half cycle of its operation when *D2* is on. During the other half cycle of operation, the resonant current i_{Lr1} circulates in the secondary side of the transformer through *D1*. Figure 3.1 (b) shows an attempt to improve the power transfer capability of

the converter using an interleaved approach [66]. For this topology, either Stage 1 or Stage 2 continuously supplies current to the load in the 2-stage interleaved converter. The operation of the 2-stage interleaved converter involves the implementation of a phase delay between the switching signals for each stage. Experimental results of the interleaved topology show that the power transferred to the output load increases [66]; however, this is achieved at the cost of doubling the number of semiconductor switches, diodes, transformers, and passive components. As a result, the footprint of the circuit becomes bigger and the power density of the converter deteriorates. Besides, the manufacturing cost of the converter increases and the implementation of the switching signals become more complicated.

The second stage in Figure 3.1 (b) performs a complementary stage to supply the load current through *D4* when i_{Lr2} is positive and i_{Lr1} is negative and circulates in the secondary winding in *T2* through *D1*. However, if *D1* participated to supply the load current in a symmetrical form during the negative cycle of the operation, then the need for the second stage in an interleaved approach is eliminated. This will require a transformer with two separate and identical secondary windings, where each winding is connected to a separate and identical series resonant circuit. This topology, referred to as the dual series-resonant topology, will provide continuous power transfer to the load without increasing the number of switching devices and complexity of the gate signal generating system.



(a)



(b)

Figure 3.1: Resonant DC-DC converter: a) single-stage series resonant circuit, b) 2-stage interleaved solution to improve the power transfer capability.

3.1.1 Description of the Proposed Topology

The proposed dual series-resonant DC-DC converter is shown in Figure 3.2. This figure shows an isolated transformer with three windings, one winding on the primary side and two separate windings on the secondary side. The primary has N_p turns and each secondary windings has $N_{s1}=N_{s2}=N_s$ turns. The turns ratio of the transformer (N) is defined as the ratio of the number of turns of the secondary winding to the number of turns of the primary winding ($N=N_s / N_p$). The magnetizing inductor of the transformer (L_m) is shown at the primary side. Two switches (Q_1 and Q_2) and one clamping capacitor (C_c) are connected in series at the primary side of the transformer. The switches are triggered in a complementary manner based on PWM switching scheme. At the secondary side of the transformer, each of the two secondary windings is connected to a series-resonant circuit (i.e., L_{r1} and C_{r1} to N_{s1}, L_{r2} and C_{r2} to N_{s2}). The connection of the secondary windings is such that the positive polarities of the windings, marked by a dot, are connected to the series resonant circuits, while the negative polarity nodes form a common connection point. The output load (R_o) and output capacitor (C_o) are connected to the series-resonant circuits through a half-bridge rectifying diode stage (*D1* and *D2*). The windings at the secondary side of the transformer are considered to be identical and the passive components in each series-resonant circuit are considered to be identical (i.e., $L_{r1}=L_{r2}$, and $C_{r1}=C_{r2}$). This results in energy distribution balance at the secondary side of the transformer. In reality, there are always mismatches between the values of the resonant inductors and resonant capacitors. The effects of mismatches between these components will be discussed through the experimental investigation in Chapter 5.

The positive polarities of voltages are shown with ± sign and the positive polarity of branch currents are shown with black arrows.

3.1.2 Principle of Operation

Before describing the operating modes of the converter, it is necessary to list the following assumptions:

- The parasitic components of all electrical connections and the turn-on resistances of the switches and diodes are neglected.
- All capacitors and inductors are assumed ideal.
- The two windings at the secondary side of the transformer are identical.
- Except for the dead-time interval between switching instants, the switching action of *Q1* and *Q2* is complementary and *D* is the duty ratio of *Q2*.
- The output capacitor and the clamping capacitor are much larger than the resonant capacitors.
- The internal capacitors of the switches are much smaller than the resonant capacitors.
- The magnetizing inductor of the transformer is much larger than the resonant inductors.
- The normalized switching frequency is more than two (i.e., $F=f_{sw}/f_r>2$).
- In the descriptions given below, the first resonant circuit refers to the resonant circuit formed by L_{r1} and C_{r1}, while the second resonant circuit refers to the resonant circuit formed by L_{r2} and C_{r2}.

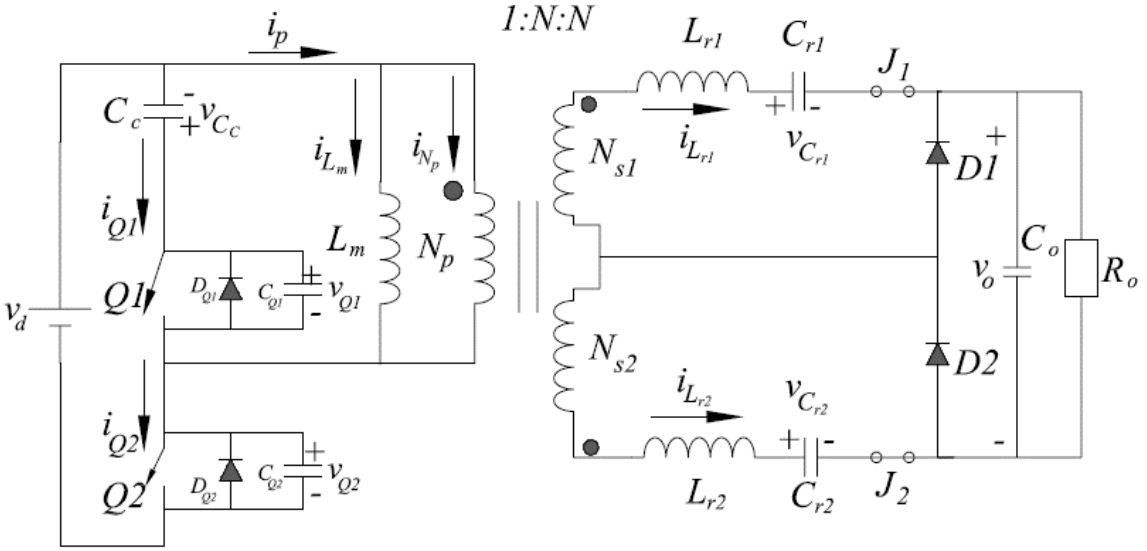


Figure 3.2: Proposed dual series-resonant DC-DC converter.

The operation of the converter is occurred in six different modes as described below:

Prior to *Mode I* ($t=T_0^-$): *Q2* is off; *Q1* is on and conducts the current $i_{Q1}= -i_p$ at the primary side of the transformer; i_{Lm} is positive but is decreasing; i_{Lr1} and i_{Lr2} are negative (therefore i_{Np} is also negative) and *D1* conducts while *D2* is off.

Mode I ($T_0<t<T_1$): At $t=T_0$, *Q1* is triggered off and C_{Q1} starts to charge by $i_{Q1.}$ Therefore, the voltage drop across *Q1* increases from zero to V_d+V_{Cc}, where V_{Cc} is the clamping capacitor voltage. Meanwhile, the voltage drop across *Q2* decreases from V_d+V_{Cc} to zero. As soon as the voltage drop across *Q2* equals zero, D_{Q2} turns on. Therefore, *Q2* can be triggered on at ZVS condition. Due to the small value of C_{Q1}, this time interval is very short and can be neglected. During this mode, the primary current of the transformer (i_p)

can be assumed constant. Figure 3.3 shows the direction of currents during this mode with red dashed lines.

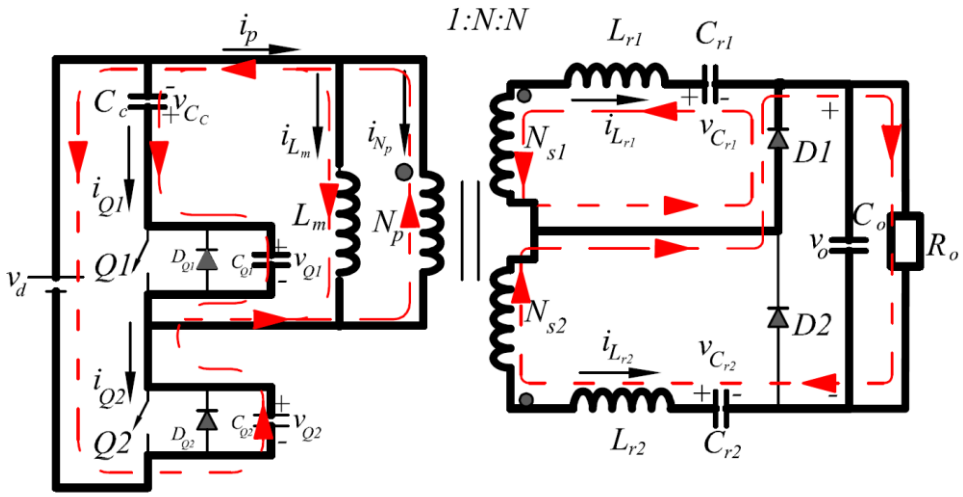


Figure 3.3: Dual series-resonant DC-DC converter - *Mode I.*

Mode II ($T_1<t<T_2$): During this mode, *Q1* is off; the voltage at the primary side of the transformer is equal to V_d. D_{Q2} conducts the negative current of i_p, and both i_{Np} and i_{Lm} increase. On the secondary side, *D1* conducts the resonant currents $i_{Lr1}+i_{Lr2}$, which are both negative values start to increase. The resonant capacitor voltages keep decreasing. Figure 3.4 shows the current paths during this mode. Assuming a fixed voltage at the output of the converter, Figure 3.5 shows the equivalent circuits on the secondary side of the transformer for each of the resonant circuits. This figure shows that during *Mode II*, the voltage on each of the secondary windings is equal to NV_d. While in the first series resonant circuit the resonant current i_{Lr1} circulates in the circuit, the current i_{Lr2} in the second series resonant circuit supplies the load current. If the initial resonant inductor

currents and resonant capacitor voltages at the beginning of this mode ($t=T_1$) are shown with $I_{Lr1}^{T_1}$, $I_{Lr2}^{T_1}$, $V_{Cr1}^{T_1}$, and $V_{Cr2}^{T_1}$, then (3.1)-(3.4) show the expressions for the resonant inductor currents and resonant capacitor voltages in the time domain during this mode. This mode ends when $i_{Lr1}+i_{Lr2}$ becomes zero. In other words, at the end of this mode, *D1* turns off naturally and *D2* turns on at ZCS condition and conducts the resonant currents.

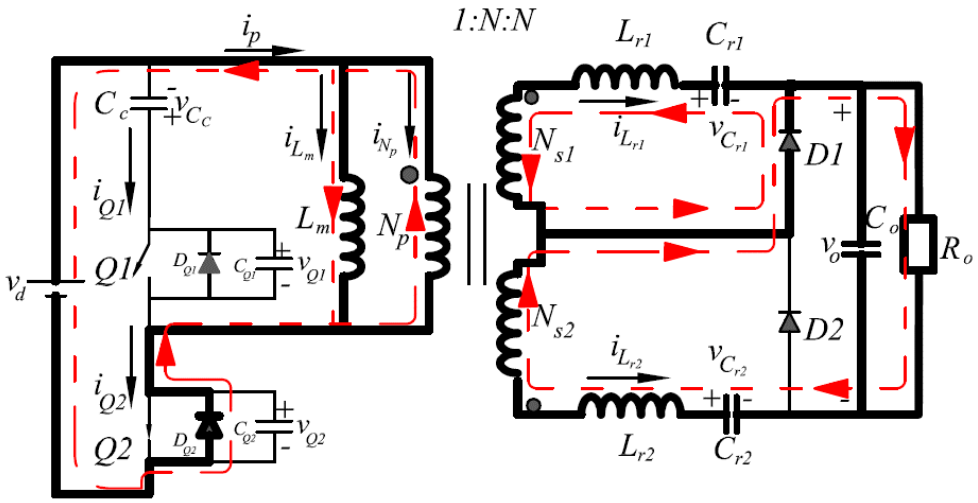
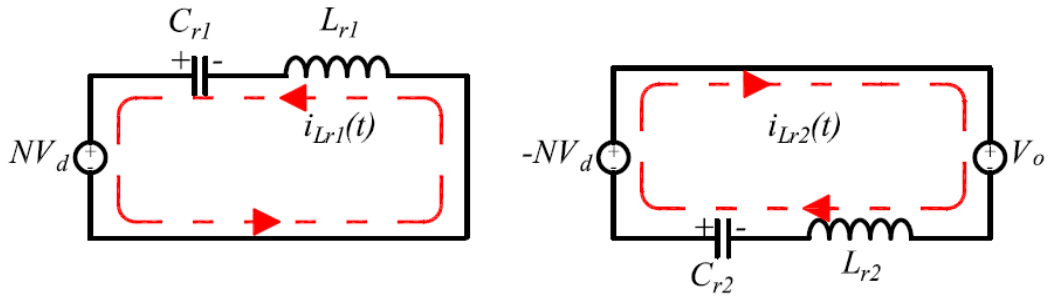


Figure 3.4: Dual series-resonant DC-DC converter - *Mode II.*



(a) (b)

Figure 3.5: Equivalent resonant circuits on the secondary side of the transformer in *Mode II*: a) first series resonant circuit, b) second series resonant circuit.

$$i_{Lr1}(t) = I_{Lr1}^{T_1}\cos(\omega_r t) + \frac{NV_d - V_{Cr1}^{T_1}}{Z}\sin(\omega_r t) \tag{3.1}$$

$$v_{Cr1}(t) = NV_d - (NV_d - V_{Cr1}^{T_1})\cos(\omega_r t) + Z_o I_{Lr1}^{T_1}\sin(\omega_r t) \tag{3.2}$$

$$i_{Lr2}(t) = I_{Lr2}^{T_1}\cos(\omega_r t) + \frac{NV_d + V_o - V_{Cr2}^{T_1}}{Z_o}\sin(\omega_r t) \tag{3.3}$$

$$v_{Cr2}(t) = NV_d + V_o - (NV_d + V_o - V_{Cr2}^{T_1})\cos(\omega_r t) + Z_o I_{Lr2}^{T_1}\sin(\omega_r t) \tag{3.4}$$

where, Z is the characteristic impedance, ω_r is the angular resonant frequency, and N is the turn ratio of the transformer.

Mode III ($T_2<t<T_3$): At $t=T_2^+$, $i_{Lr1}+i_{Lr2}$ is positive and *D2* carries the load current in the positive cycle of operation while *D1* is off. On the primary side, i_{Np} becomes positive which makes i_p positive; therefore, *Q2* starts to carry the positive current i_p at the primary side of the transformer. The resonant inductor currents and resonant capacitor voltages

increase during this mode. Figure 3.6 shows the current paths during this mode. The voltage on each of the secondary windings remains at NV_d. Figure 3.7 shows the equivalent resonant circuits on the secondary side during this mode. As shown in Figure 3.6, during this mode, i_{Lr1} supplies the load current and i_{Lr2} circulates in the second series resonant circuit. Assuming that $V_{Cr1}^{T_2}$, and $V_{Cr2}^{T_2}$ are the initial values of the resonant capacitor voltages at the beginning of this mode, the corresponding expressions for the resonant inductor currents and resonant capacitor voltages in both circuits during this mode are shown in (3.5)-(3.8). Since the initial resonant inductor currents at the beginning of this mode are zero, the associated terms with initial resonant currents in these equations are zero. The operation continues until *Q2* is triggered off at $t=T_3$. Since the switching frequency is more than twice the resonant frequency ($F \geq 2$), i_{Lr1} and i_{Lr2} remain positive at the end of this mode.

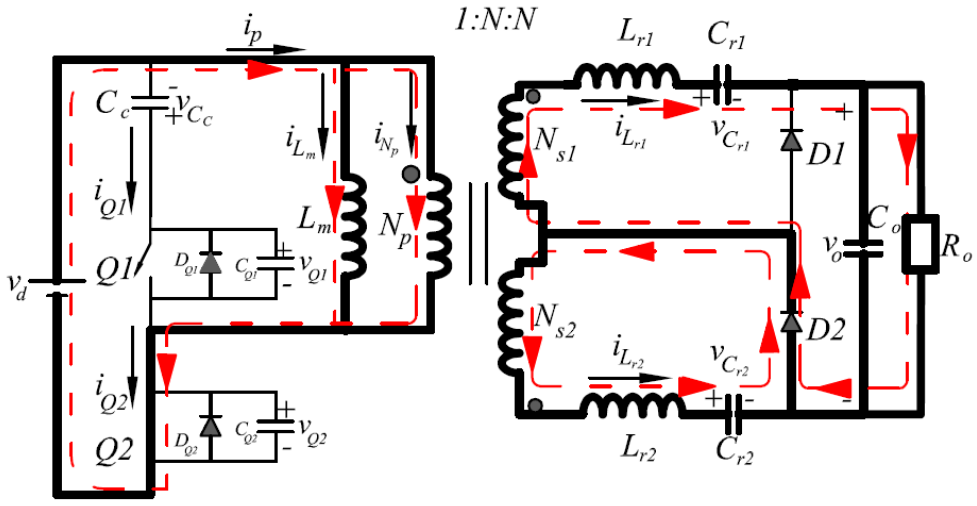
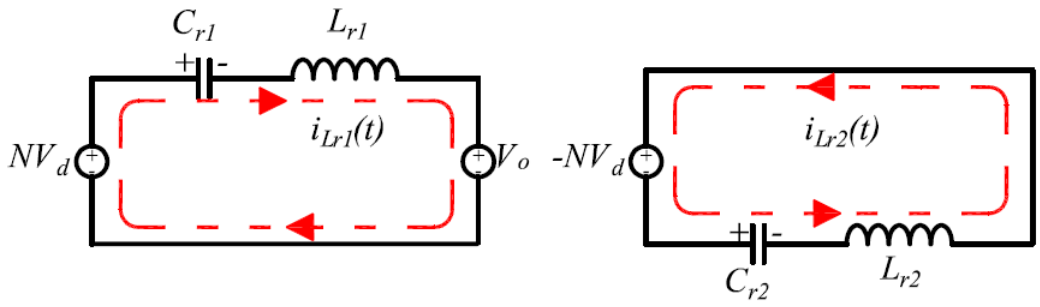


Figure 3.6: Dual series-resonant DC-DC converter - *Mode III.*



(a) (b)

Figure 3.7: Equivalent resonant circuits on the secondary side of the transformer in *Mode III*: a) first series resonant circuit, b) second series resonant circuit.

$$i_{Lr1}(t) = \frac{NV_d - V_o - V_{Cr1}^{T_2}}{Z_o}\sin(\omega_r(t - T_2)) \tag{3.5}$$

$$v_{Cr1}(t) = NV_d - V_o - (NV_d - V_o - V_{Cr1}^{T_2})\cos(\omega_r(t - T_2)) \tag{3.6}$$

$$i_{Lr2}(t) = \frac{NV_d - V_{Cr2}^{T_2}}{Z_o}\sin(\omega_r(t - T_2)) \tag{3.7}$$

$$v_{Cr2}(t) = NV_d - (NV_d - V_{Cr2}^{T_2})\cos(\omega_r(t - T_2)) \tag{3.8}$$

Mode IV ($T_3<t<T_4$): When *Q2* is triggered off, i_{Lr1} and i_{Lr2} are still positive, v_{Cr1} and v_{Cr2} keep increasing. On the primary side, i_p is positive; therefore, C_{Q2} conducts i_p and v_{CQ2} increases from zero to $V_{d+}V_{Cc}$. Simultaneously, v_{CQ1}, which was $V_{d+}V_{Cc}$, decreases and finally reaches zero and D_{Q1} starts to conduct the current. At this time, *Q1* can be triggered on at ZVS condition. This mode is the dual of *Mode I*. Figure 3.8 shows the current

directions during this mode. The time duration of this mode is negligibly small and the current i_p can be assumed constant.

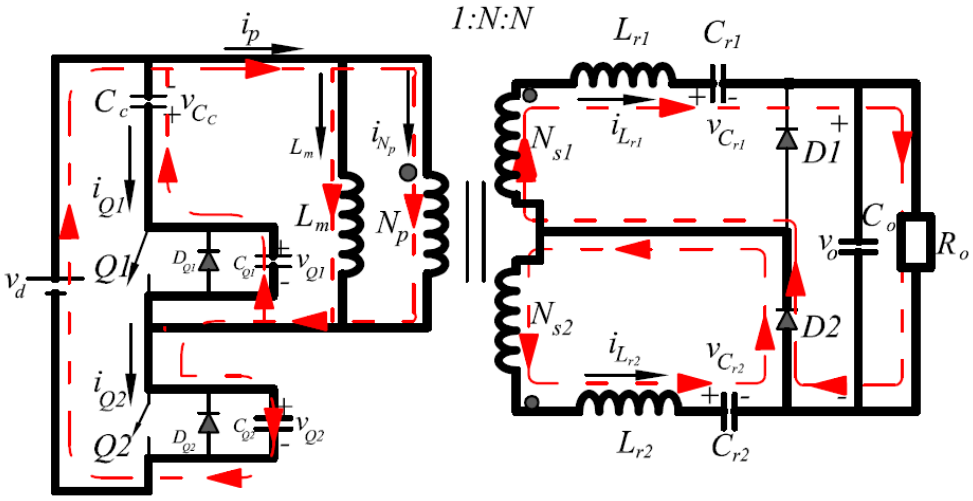


Figure 3.8: Dual series-resonant DC-DC converter - *Mode IV*.

Mode V ($T_4<t<T_5$): During this mode, the voltage at the primary side of the transformer is $-V_{Cc}$. On the primary side, i_p is still positive and is conducted by D_{Q1}. i_{Lm} and i_p start to decrease. On the other hand, i_{Lr1} and i_{Lr2} are still positive on the secondary side of the transformer and v_{Cr1} and v_{Cr2} keep increasing. However, due to the negative voltage across the secondary side of the transformer, the positive resonant currents start to decrease to zero. Figure 3.9 shows the converter during this mode and Figure 3.10 shows the equivalent resonant circuits on the secondary side of the transformer. During this mode, the voltage of each of the secondary windings is equal to $-NV_{Cc}$; i_{Lr1} continues to supply the load current and i_{Lr2} circulates in the second series resonant circuit. Assuming that $I_{Lr1}^{T_4}$, $I_{Lr2}^{T_4}$, $V_{Cr1}^{T_4}$, and $V_{Cr2}^{T_4}$ are the initial values of the resonant inductor currents and resonant

capacitor voltages in the series resonant circuits at the beginning of this mode, (3.9)-(3.12) show the time domain expressions for the resonant inductor currents and resonant capacitor voltages during this mode.

This mode ends when $i_{Lr1}+i_{Lr2}$ becomes zero.

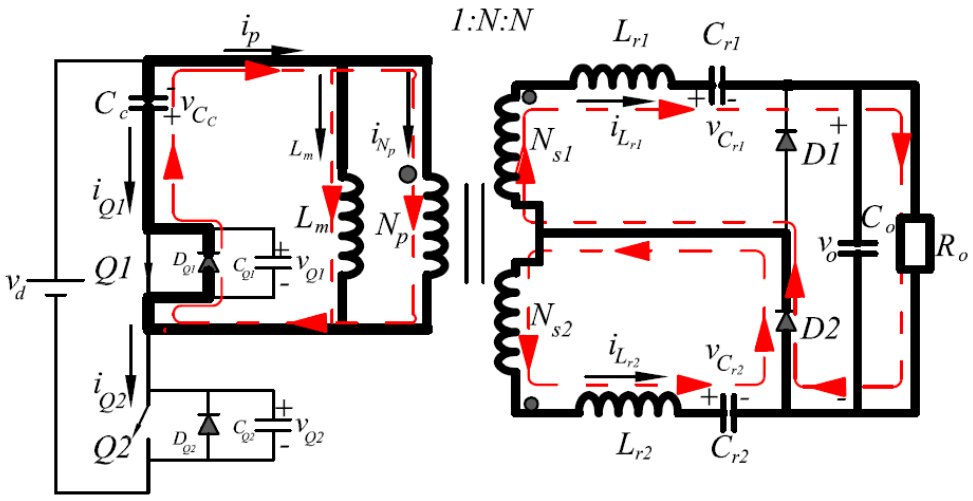
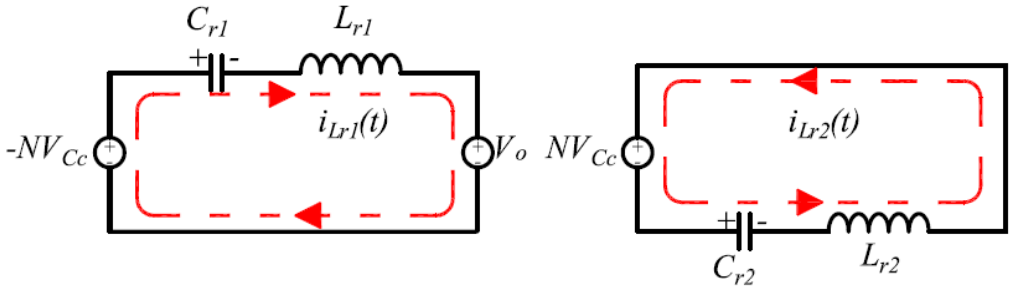


Figure 3.9: Dual series-resonant DC-DC converter - *Mode V*.



(a) (b)

Figure 3.10: Equivalent resonant circuits on the secondary side of the transformer in *Mode V*: a) first series resonant circuit, b) second series resonant circuit.

$$i_{Lr1}(t) = I_{Lr1}^{T_4}\cos(\omega_r(t-T_4)) + \frac{V_{Cc} - V_o - V_{Cr1}^{T_4}}{Z_o}\sin(\omega_r(t-T_4)) \tag{3.9}$$

$$v_{Cr1}(t) = V_{Cc} - V_o - (V_{Cc} - V_o - V_{Cr1}^{T_4})\cos(\omega_r(t-T_4)) + Z_o I_{Lr1}^{T_4}\sin(\omega_r(t-T_4)) \tag{3.10}$$

$$i_{Lr2}(t) = I_{Lr2}^{T_4}\cos(\omega_r(t-T_4)) + \frac{V_{Cc} - V_{Cr2}^{T_4}}{Z_o}\sin(\omega_r(t-T_4)) \tag{3.11}$$

$$v_{Cr2}(t) = V_{Cc} - (NV_{Cc} - V_{Cr2}^{T_4})\cos(\omega_r(t-T_4)) + Z_o I_{Lr2}^{T_4}\sin(\omega_r(t-T_4)) \tag{3.12}$$

Mode VI ($T_5<t<T_6$): At $t=T_5^+$, and on the secondary side of the transformer, $i_{Lr1}+i_{Lr2}$ are negative and v_{Cr1} and v_{Cr2} start to decrease. *D2* turns off naturally, and *D1* starts to conduct the resonant and load currents at ZCS condition in the negative cycle of operation. This makes i_{Np} and subsequently i_p negative and *Q1* conducts the current at the primary side of the transformer. Due to the negative voltage on the primary side, i_{Lm} keeps decreasing. Figure 3.11 shows the current paths during this mode and Figure 3.12 show the equivalent circuits on the secondary side of the transformer for each of the series resonant circuits. As shown in this figure, during this mode, i_{Lr2} of the second series resonant circuit supplies the load current while i_{Lr1} circulates in the first series resonant circuit. These variations continue until *Q1* is triggered off. At this stage, the converter returns to *Mode I* and repeats the cycle. Assuming that $V_{Cr1}^{T_5}$, and $V_{Cr2}^{T_5}$ are the initial values of the resonant capacitor voltages at the beginning of this mode, the corresponding expressions for the resonant inductor currents and resonant capacitor voltages in both circuits during this mode are shown in (3.13)-(3.16). The initial resonant inductor currents at the beginning of this mode

are zero; therefore, the associated terms with initial resonant currents in these equations are zero.

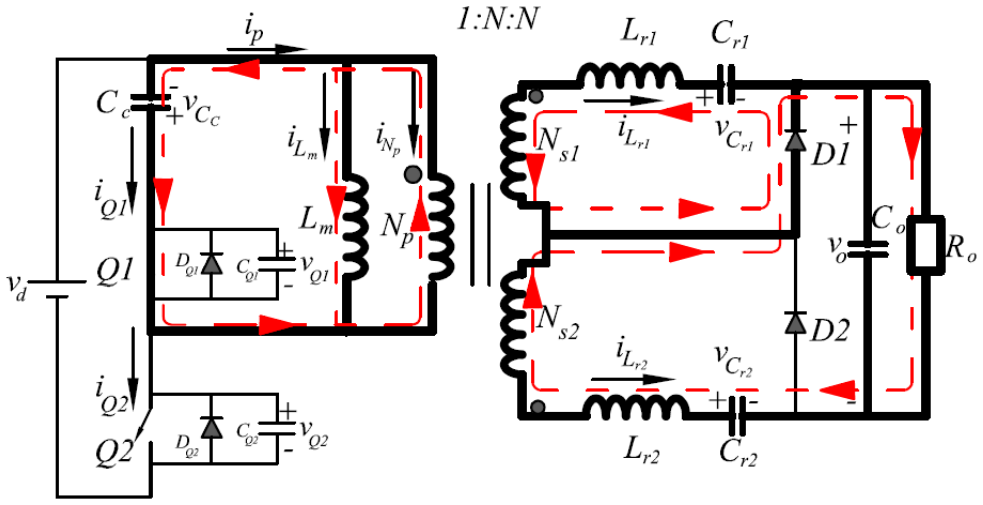


Figure 3.11: Dual series-resonant DC-DC converter - *Mode VI.*

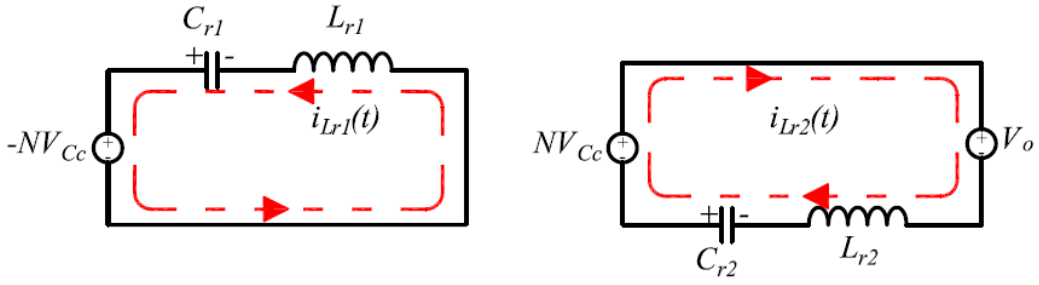


Figure 3.12: Equivalent resonant circuits on the secondary side of the transformer in *Mode VI*: a) first series resonant circuit, b) second series resonant circuit.

$$i_{Lr1}(t) = \frac{V_{Cc} - V_{Cr1}^{T_5}}{Z_o} \sin(\omega_r (t - T_5)) \tag{3.13}$$

$$v_{Cr1}(t) = V_{Cc} - (V_{Cc} - V_{Cr1}^{T_5}) \cos(\omega_r (t - T_5)) \tag{3.14}$$

$$i_{Lr2}(t) = \frac{V_{Cc} + V_o - V_{Cr2}^{T_5}}{Z_o} \sin(\omega_r (t - T_5)) \tag{3.15}$$

$$v_{Cr2}(t) = V_{Cc} + V_o - (V_{Cc} + V_o - V_{Cr2}^{T_5}) \cos(\omega_r (t - T_5)) \tag{3.16}$$

It is observed that during each mode, the following relationship between v_{Cr1} and v_{Cr2} is satisfied:

$$v_{Cr2}(t) = v_{Cr1}(t) + V_o \tag{3.17}$$

This relationship (3.17) holds true throughout the entire operation of the converter and it applies to the initial values of resonant capacitor voltages. In other words, assuming that $V_{Cr1}^{T_x}$ and $V_{Cr2}^{T_x}$ are the initial values of the resonant capacitor voltages at $t=T_x$, the following relationship can be realized at the beginning of each mode:

$$V_{Cr2}^{T_x} = V_o + V_{Cr1}^{T_x} \tag{3.18}$$

Employing (3.17) and (3.18) to the resonant inductor current expressions in each mode, it is found that the resonant inductor currents are equal throughout the entire operation of the converter. In other words:

$$i_{Lr1}(t) = i_{Lr2}(t) \tag{3.19}$$

This fact can be observed in Figure 3.13 where the key waveforms during one complete cycle of operation are shown. The resultant relationships between the resonant inductor currents and resonant capacitor voltages given in (3.17) and (3.19) will be confirmed in Chapter 4 through the use of the extended describing function analytical procedure to obtain the steady state model of the proposed dual series-resonant converter.

Using (3.18) and (3.19) in (3.1) to (3.17), the time duration of each mode can be obtained as follows:

$$T_0 = T_1 \approx 0 \tag{3.20}$$

$$\Omega_r T_2 = \arctan\left(\frac{\left(\frac{-DNV_d}{1-D} - V_{Cr1} \right)}{V_{Cr1} - NV_d} \sin\left(\Omega_r (T_s - T_5)\right) \right) \tag{3.21}$$

$$T_3 = T_4 \tag{3.22}$$

$$T_4 = DT_s \tag{3.23}$$

$$\Omega_r T_5 = \Omega_r DT_s + \arctan\left(\frac{\left(NV_d - V_{Cr1} - V_o\right)}{\frac{DNV_d}{1-D} + V_{Cr1} + V_o} \sin\left(\Omega_r (DT_s - T_2)\right) \right) \tag{3.24}$$

$$T_6 = T_s \tag{3.25}$$

where, Ω_r is the large signal part of the angular resonant frequency (ω_r).

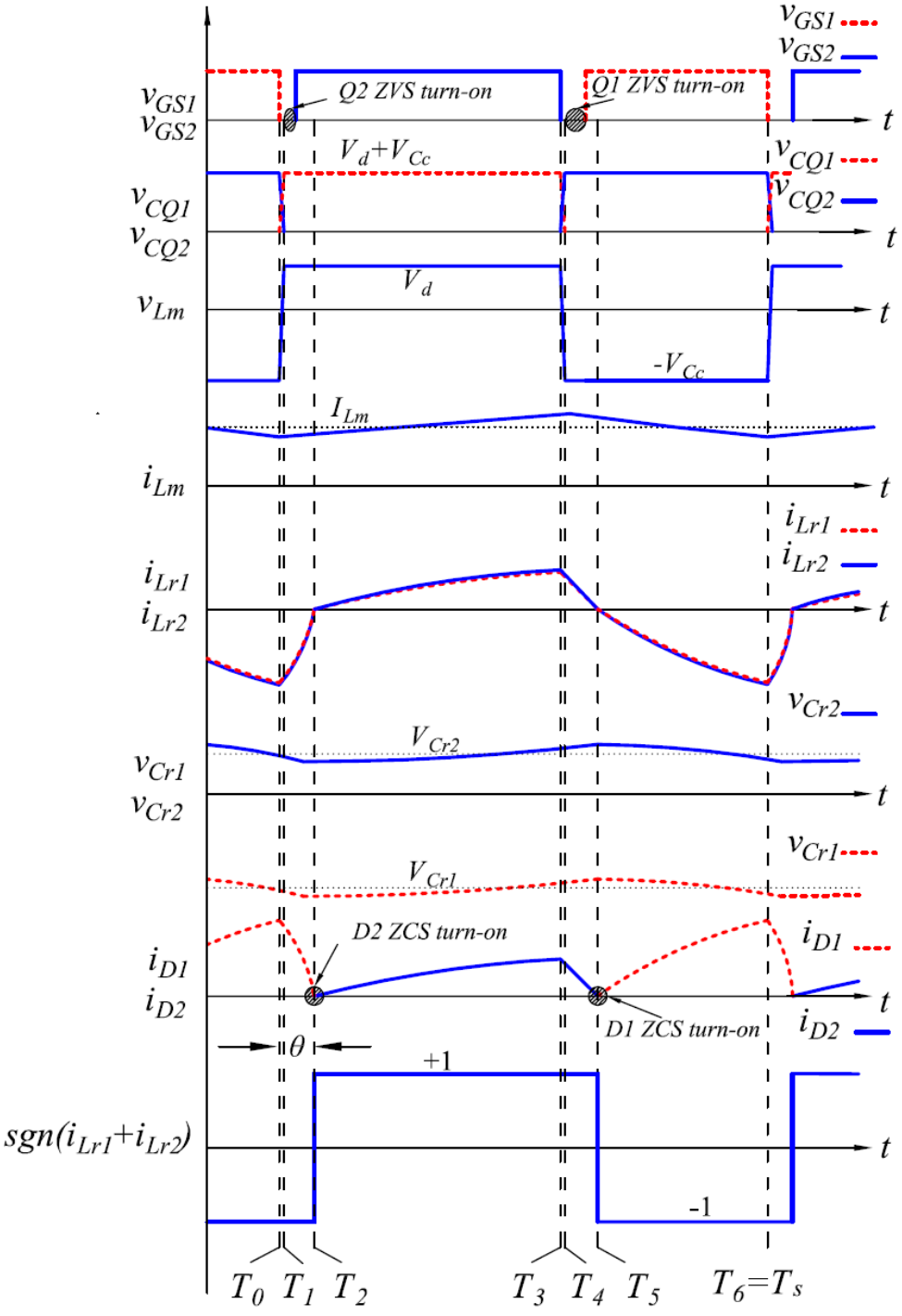


Figure 3.13: Key waveforms of the dual series-resonant DC-DC converter.

3.2 Simulation Case Study

In order to confirm the feasible operation of the proposed dual-series resonant DC-DC converter under different operating conditions (i.e., duty ratio, switching frequency, and loading condition), a series of simulations are implemented using PLECS [71] software to verify the proper operation of the proposed converter in steady state condition. Figure 3.14 shows the simulation setup in PLECS environment.

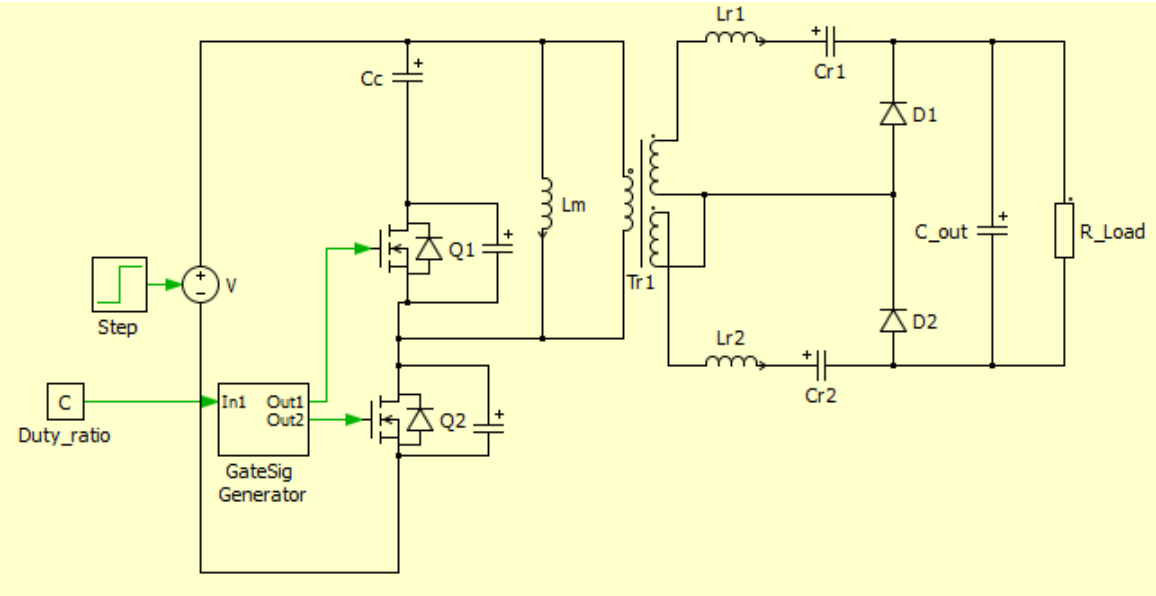


Figure 3.14: Simulation setup in PLECS environment.

The input voltage is modeled as a constant DC voltage and the output load is modeled as a resistor. The simulation parameters are as follows:

$N=1$, $L_{r1}=L_{r2}=4\ \mu H$, $C_{r1}=C_{r2}=1\ \mu F$, $C_o=100\ \mu F$, $C_c=10\ \mu F$, $L_m=70\ \mu H$, and $V_d=10\ V$.

The duty ratio of *Q2* is varied from *D*=0.3 for case study I to *D*=0.6 case study II. Figure 3.15 shows the gate signals, resonant inductor currents, resonant capacitor voltages, and the output voltage of the converter.

It is observed that by increasing the duty ratio of *Q2*, the output voltage of the converter increases for V_o=8.84 V to V_o=17.8 V. Therefore, the output voltage can be controlled by changing the duty ratio of the switching signals. In the simulation, the inductor resonant currents of i_{Lr1} and i_{Lr2} are equal during the operation of the converter, and the absolute values of the resonant capacitor voltages increase.

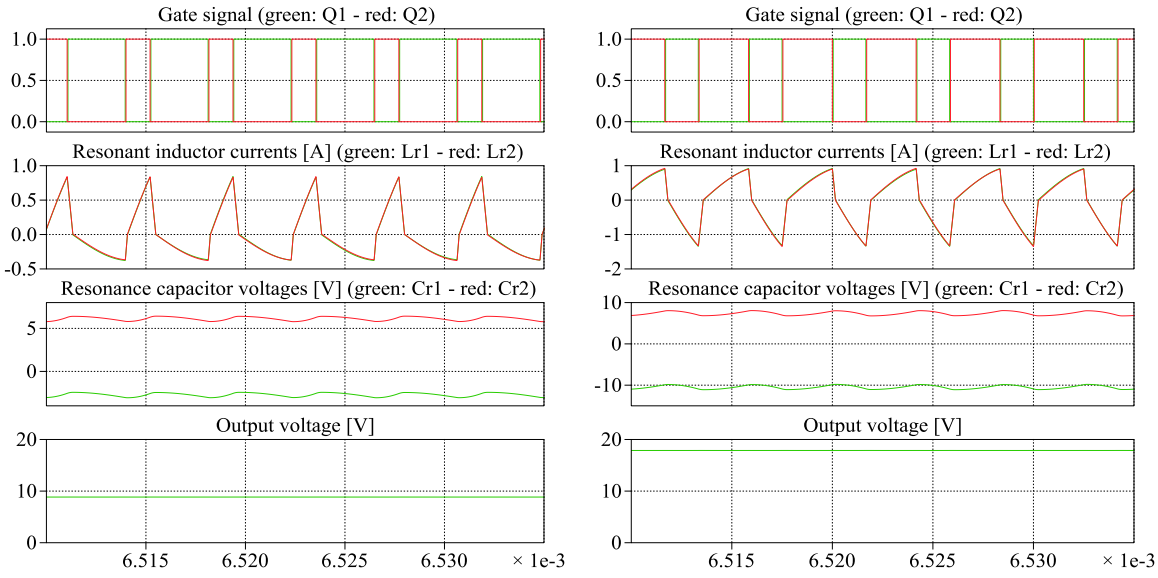


Figure 3.15: Simulated operation of the dual series-resonant DC-DC converter under different values of duty ratio (R_o=30 Ω, f_{sw}=240 kHz): a) *D*=0.3 (case study I), b) *D*=0.6 (case study II).

The operation of the converter under different switching frequencies is simulated and Figure 3.16 shows the results of the simulation. In this scenario, the switching frequency is changed from f_{sw}=240 kHz for case study III to f_{sw}=400 kHz for case study IV. It is observed that by increasing the switching frequency, the output voltage of the converter decreases from V_o=16.24 V to V_o=13.63 V, indicating that the switching frequency can also be used to control the output voltage. The absolute values of the resonant capacitor voltages decrease; however, resonant inductor currents remain equal with each other.

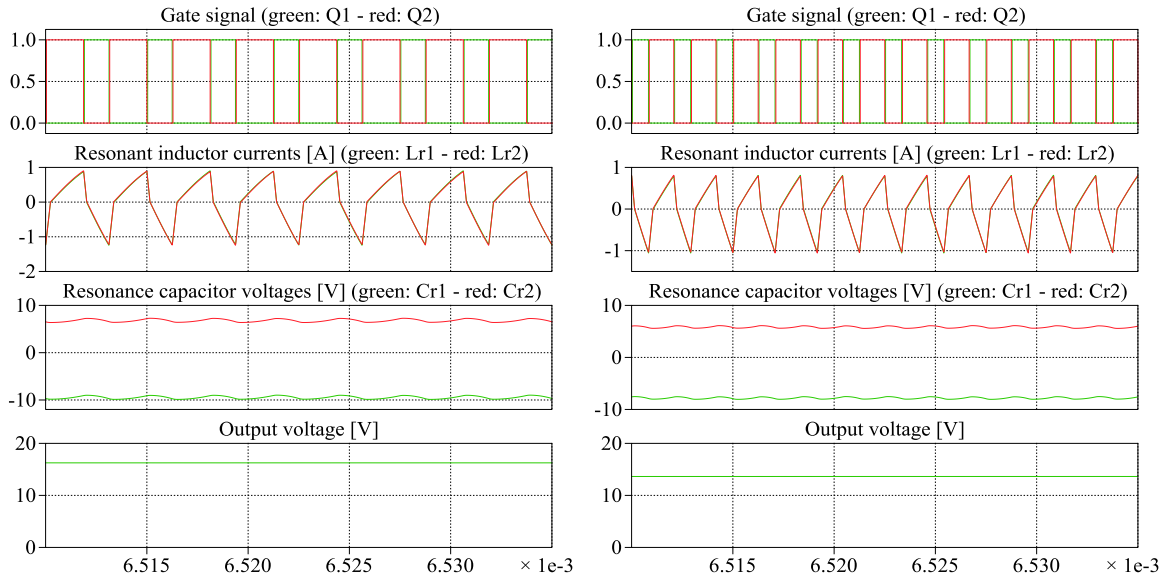


Figure 3.16: Simulated operation of the dual series-resonant DC-DC converter under different switching frequencies (D=0.6, R_o=30 Ω): a) f_{sw}=320 kHz (case study III), b) f_{sw}= 480 kHz (case study IV).

Figure 3.17 shows the effect of different loading conditions on the operation of the converter. It is shown that by reducing the value of the output load from R_o=30 Ω for case

study V to R_o=15 Ω for case study VI, the inductor resonant currents increase and the value of the output voltage decreases from V_o=11.46 V to V_o=9.2 V. In this case, the absolute values of resonant capacitor voltages decrease. This behaviour was expected as the converter is from the series-resonant class.

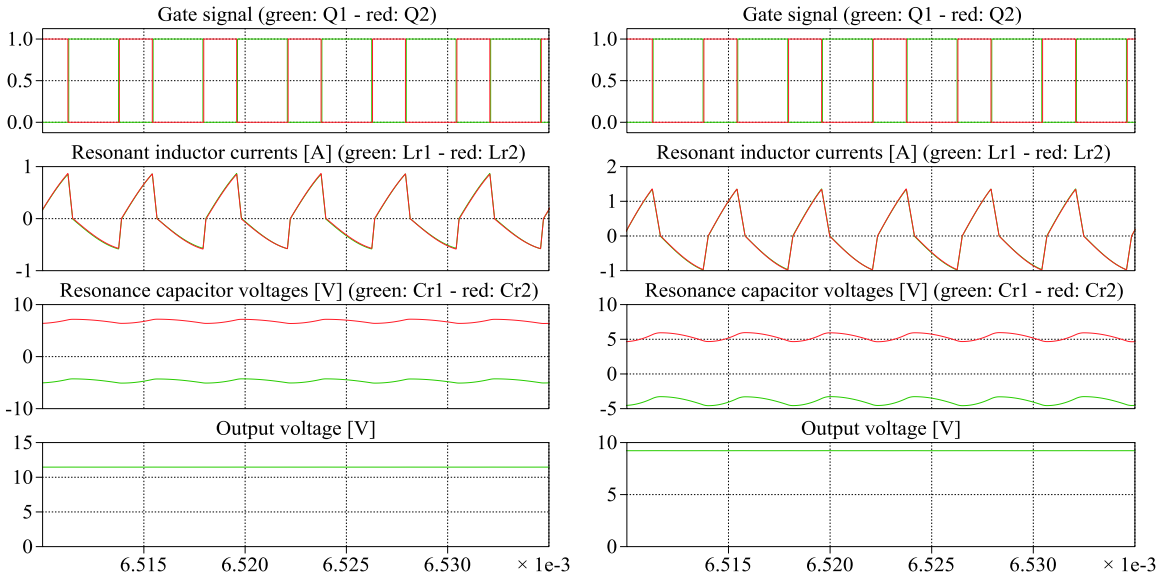


Figure 3.17: Simulated operation of the dual series-resonant DC-DC converter under different loading conditions (D=0.4, f_{sw}=240 kHz): a) R_o=30 Ω (case study V), b) R_o=15 Ω (case study VI).

Table 3.1 lists the steady state the values of the fundamental components of the resonant inductor currents (I_{1FLr1} and I_{1FLr1}), DC components of resonant capacitor voltages (V_{Cr1} and V_{Cr1}), and DC values of the output voltage (V_o) for each scenarios of the simulation. The higher components in resonant inductor currents and resonant capacitor voltages are neglected in Table 3.1.

Table 3.1: PLECS simulation results in the steady state.

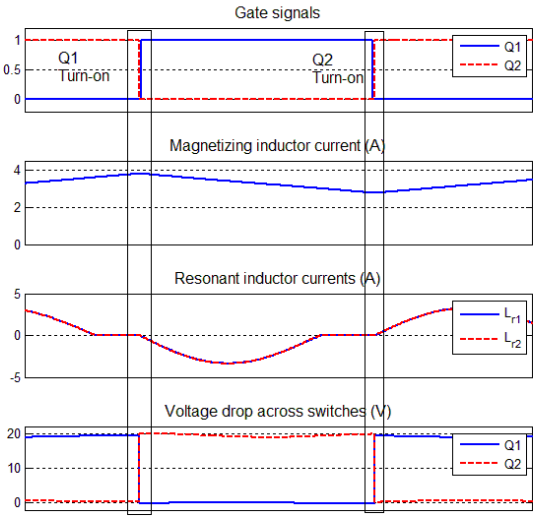
	I_{1FLr1}= I_{1FLr2} [A]	V_{Cr1} [V]	V_{Cr1} [V]	V_o [V]
Case study I f_{sw}=240 kHz, D=0.3, R_o=30 Ω	0.433	-2.72	6.14	8.84
Case study II f_{sw}=240 kHz, D=0.6, R_o=30 Ω	0.90	10.50	7.40	17.87
Case study III f_{sw}=320 kHz, D=0.6, R_o=30 Ω	0.82	-9.45	6.81	16.24
Case study IV f_{sw}=480 kHz, D=0.6, R_o=30 Ω	0.71	-7.86	5.86	13.71
Case study V f_{sw}=240 kHz, D=0.4, R_o=30 Ω	0.58	-4.66	6.80	11.46
Case study VI f_{sw}=240 kHz, D=0.4, R_o=15 Ω	0.95	-3.88	5.33	9.21

3.3 Boundary Condition Between CCM and DCM

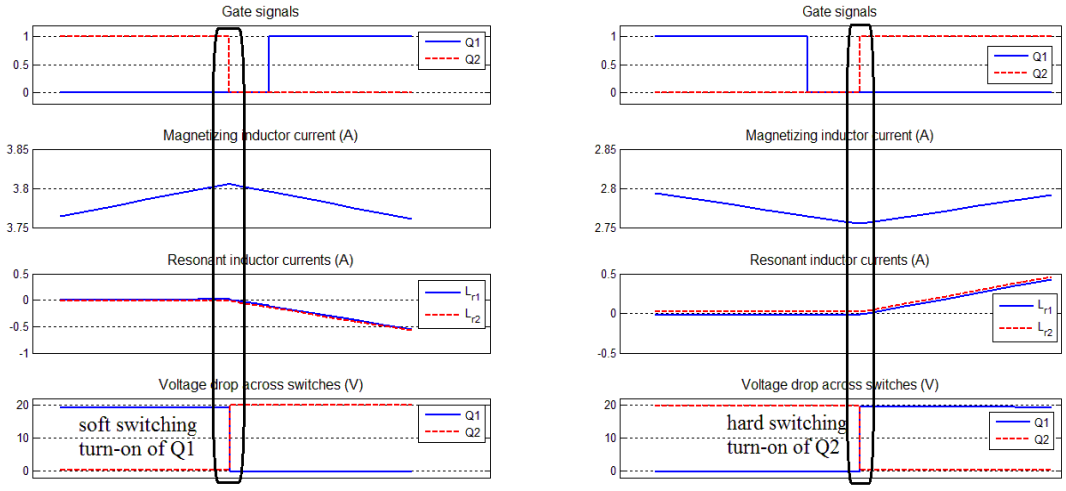
In order to ensure ZVS operation of both switches, it is crucial to operate the converter in the continuous current mode (CCM). Otherwise, the turn-on operation of *Q2* would not occur under ZVS condition. Figure 3.18 shows the simulation results of the gate signals, magnetizing inductor current, resonant inductor currents, and voltage drop across the switching devices in a discontinuous current mode (DCM) operation. The resonant inductor currents on the secondary side of the transformer reach and remain zero before the switching action occurs.

Therefore, only the magnetizing inductor current, which is positive, flows on the primary side of the transformer, and the direction of i_p would not change. Having these conditions, the voltage drops across C_{Q1} and C_{Q2} before triggering *Q2* on would be equal to zero and V_d+V_{Cc}, respectively. Consequently, the turn-on operation of *Q1* would always occur at

ZVS condition; however, *Q2* will experience hard-switching turn-on since D_{Q1} is on prior to triggering *Q2*. These operations are highlighted in Figure 3.18 (b) and Figure 3.18 (c). According to Figure 3.18 (b), the voltage drop across switches changes at the turn-off instant of *Q1* and v_{CQ2} becomes zero during the dead-time interval, which makes the turn-on of *Q1* at zero voltage condition. However, due to the positive current of i_p, during turn-on of *Q2*, D_{Q1} conducts and C_{Q2} cannot discharge to zero; therefore, the turn-on of *Q2* occurs at hard-switching condition. Operation in DCM would result in increased switching losses with associated reduction in the converter efficiency. The DCM conditions are shown in Figure 3.19, where the current flow in the circuit prior to the turn-on of *Q1* and *Q2* is shown.



(a)



(b) (c)

Figure 3.18: DCM operation of the converter: a) one complete cycle, b) *Q1* turn-on condition, and c) *Q2* turn-on condition.

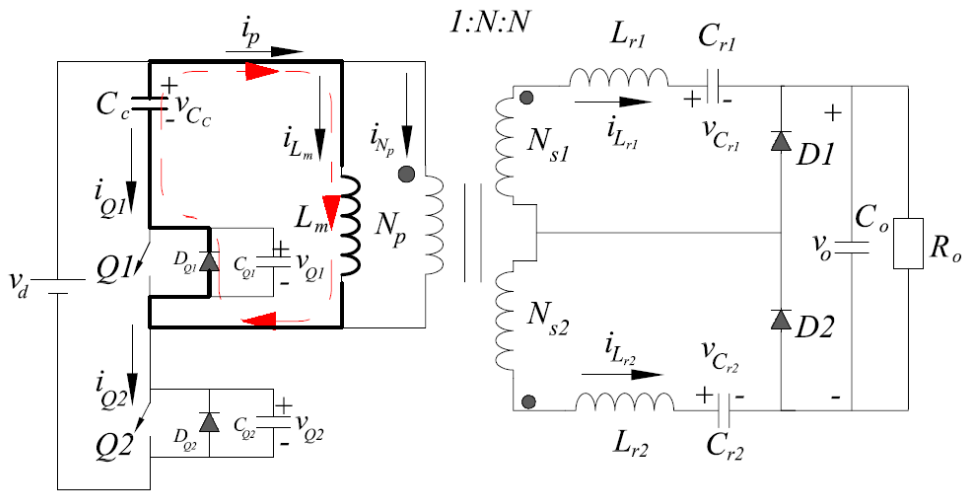


Figure 3.19: Current flow in DCM operation during the dead time.

It is preferable to operate the converter in CCM condition for the reasons given above. In order to ensure CCM operation the switching frequency should be high enough to trigger the switches before the resonant currents on the secondary side of the transformer reach zero. This depends not only on the resonant frequency of the series resonant circuits, but also on the duty ratio of the PWM switching signals. In order to guarantee CCM operation of the converter, the switching frequency of the converter should be at least twice the resonant frequency, i.e.:

$$F = \frac{f_{sw}}{f_r} \geq 2 \tag{3.26}$$

3.4 Summary

The development of the proposed dual series-resonant topology to overcome the limitations of the existing topologies and techniques was discussed. The principle of operation of the proposed dual series-resonant DC-DC converter was described. The

description included both qualitative and quantitative description of each mode of operation. Equivalent circuits showing the directions of current flow and the states of the active devices, time domain expressions, and ideal waveforms for each mode were presented. ZVS and ZCS operation of the switches and output diodes during the operational modes of the converter were demonstrated. It was shown that the proposed dual series-resonant converter is capable of continuous power transfer to the load throughout the entire modes of operation. The feasibility of the operation of the proposed converter was confirmed using PLECS simulation. The boundary between DCM and CCM operation of the proposed converter was investigated and it was shown that in order to guarantee ZVS operation of the switches, it is necessary to operate the converter in CCM.

Chapter 4

Analysis of the Dual Series-Resonant DC-DC converter

The proposed topology of the dual series-resonant DC-DC converter presented in Chapter 3 is investigated to model its steady state and small signal behavior. The objective of this chapter is to develop accurate and detailed models of the converter to predict and investigate its steady state and small signal behavior. The results of the steady state and small signal models of the converter are essential aids to characterize the converter and develop a control scheme to control its output voltage.

Several techniques are available to model and analyze resonant DC-DC converters. State-space averaging is the most well-known method to analyze and model PWM based DC-DC converters [72]. The necessary assumption of a small ripple condition during the averaging interval in the state-space averaging approach is not valid for resonant converters; hence, the state-space averaging technique cannot be utilized to analyze and model the proposed dual series-resonant DC-DC converter. A sampled data approach was proposed in 1986 as a standard method to model and analyze resonant converters [73]. Despite the proven effectiveness of the sampled data approach in modeling different topologies of resonant converters, this method does not provide an in-depth, thorough, and parametrical approach to model the converter to be used to design of the converter [74], [75]. The extended describing function analysis method provides a mixed time-domain and frequency-domain analyses and a parametrical approach, which makes this method a powerful approach to model and analyze resonant converters [75]. Hence, this method is used to model and analyze the proposed dual series-resonant DC-DC converter.

Although this method inevitably involves some approximations of neglecting higher order harmonics in the state-space variables, in Appendix A, it is demonstrated that these approximations do not affect the accuracy of the developed models. The time-domain and frequency-domain analyses of the extended describing function lead to the development of steady state and 7^{th} order small signal models that provide insightful understanding of the operation of the converter. For example, the developed steady state model reveals that the output voltage of the converter can be regulated with two degrees of freedom (i.e., duty ratio of the PWM switching signal and switching frequency) in both step-down and step-

up voltage conversion regimes. The 7th order small signal models are discussed and the order to the control-to-output transfer function is reduced to a 3rd order model which is used to develop a single-loop, voltage-feedback control scheme to control the output voltage of the converter.

The developed steady state and small signal models are used in Chapter 6 to develop a parametric and systematic approach to the design of the converter.

4.1 Extended Describing Function

In order to implement the extended describing function, it is necessary to decompose the state-space variables into DC and/or AC components. The proposed converter consists of seven energy-storage components, i.e., two resonant circuits (L_{r1}, C_{r1}, L_{r2}, and C_{r2}), a magnetizing inductor (L_m), a clamping capacitor (C_c), and an output capacitor (C_o). The state variables of the system can be defined in a general form as follows:

$$i_{Lr1}(t) = \sum_{n=1,2,...} i_{nFSLr1}(t)\sin(nF\omega_r t) + i_{nFCLr1}(t)\cos(nF\omega_r t) \tag{4.1}$$

$$i_{Lr2}(t) = \sum_{n=1,2,...} i_{nFSLr2}(t)\sin(nF\omega_r t) + i_{nFCLr2}(t)\cos(nF\omega_r t) \tag{4.2}$$

$$v_{Cr1}(t) = v_{Cr1} + \sum_{n=1,2,..} v_{nFSCr1}(t)\sin(nF\omega_r t) + v_{nFCCr1}(t)\cos(nF\omega_r t) \tag{4.3}$$

$$v_{Cr2}(t) = v_{Cr2} + \sum_{n=1,2,...} v_{nFSCr2}(t)\sin(nF\omega_r t) + v_{nFCCr2}(t)\cos(nF\omega_r t) \tag{4.4}$$

$$i_{Lm}(t) = i_{Lm} \tag{4.5}$$

$$v_{Cc}(t) = v_{Cc} \tag{4.6}$$

$$v_o(t) = v_o \tag{4.7}$$

where, *F* is the normalized switching frequency and *n* is the order of the harmonic.

The resonant inductor currents have been decomposed into sine and cosine terms; resonant capacitor voltages have been approximated with a DC signal and the AC parts has been decomposed into sine and cosine terms. However, based on the initial simulations that were carried out for different scenarios, it was observed that the magnetizing inductor current, clamping capacitor voltage, and output capacitor voltage contain very small and negligible AC terms on their DC components; therefore, these signals have been approximated only by DC components. For the sake of simplicity, it is necessary to obtain the Fourier series of some of the key waveforms in one complete cycle of the operation before introducing the state-space equations.

1. Voltage at the primary side of the transformer:

The variation of the voltage at the primary side of the transformer in one complete cycle is shown in Figure 4.1. It is noticed that during *Mode II* ($T_1 < t < T_2$) and *Mode III* ($T_2 < t < T_3$), the voltage at the primary side of the transformer is equal to V_d and during *Mode V* ($T_4 < t < T_5$) and *Mode VI* ($T_5 < t < T_6$), the voltage at the primary side of the transformer is equal to $-V_{Cc}$. The transition times of the voltage between V_d and $-V_{Cc}$ that occur in *Mode I* and *Mode IV* are neglected since the time intervals for these two modes are very short compared with the other modes. The Fourier expansion of the voltage at the primary side of the transformer can be given as follows:

$$v_{Lm}(t) = a_0 + \left(v_d + v_{Cc}\right) \sum_{n=1,2,\ldots} a_n \cos(nF\omega_r t) + b_n \sin(nF\omega_r t) \tag{4.8}$$

where,

$$a_0 = Dv_d - (1-D)v_{Cc} \tag{4.9}$$

$$a_n = \frac{\sin(2\pi mD)}{n\pi} \tag{4.10}$$

$$b_n = \frac{1-\cos(2\pi mD)}{n\pi} \tag{4.11}$$

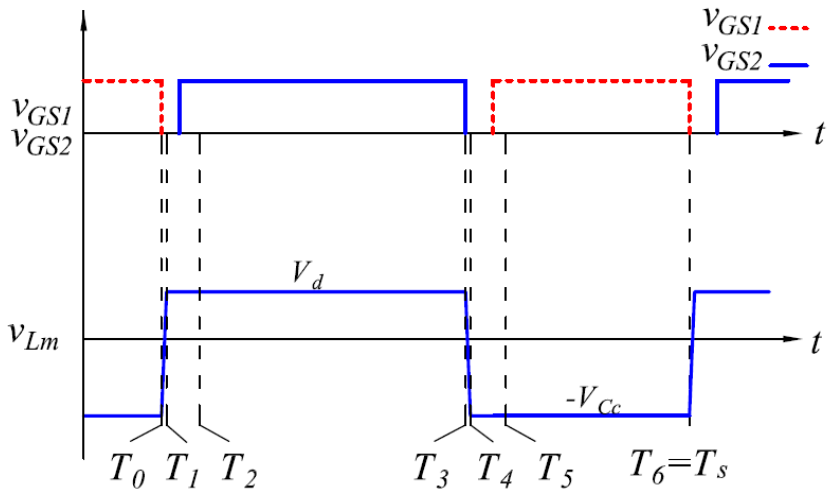


Figure 4.1: Gate signals and voltage at the primary side of the transformer.

where, *D* is the large signal of duty ratio (*d*) of the PWM switching signal.

2. Step function of the derivative of ($-i_{Lr1}$-i_{Lr2}):

This function is used to determine the state-space equations for the clamping capacitor. Between *Mode I* to *Mode III*, both resonant inductor currents are increasing. Hence, the derivative of ($-i_{Lr1}$-i_{Lr2}) is negative and the step function returns zero. However, between *Mode IV* to *Mode VI*, the resonant inductor currents of i_{Lr1} and i_{Lr2} are decreasing; therefore, the derivative of ($-i_{Lr1}$-i_{Lr2}) is positive and the step function returns unity. Figure 4.2 shows the waveform of this function during one complete period. The Fourier expansion of this function is obtained as follows:

$$u\left(\frac{d}{dt}\left(-i_{Lr1}(t)-i_{Lr2}(t)\right)\right)=(1-D)-\sum_{n=1,2,\ldots}\left(a_n\cos(nF\omega_r t)+b_n\cos(nF\omega_r t)\right) \tag{4.12}$$

a_n and b_n have been given in (4.10) and (4.11).

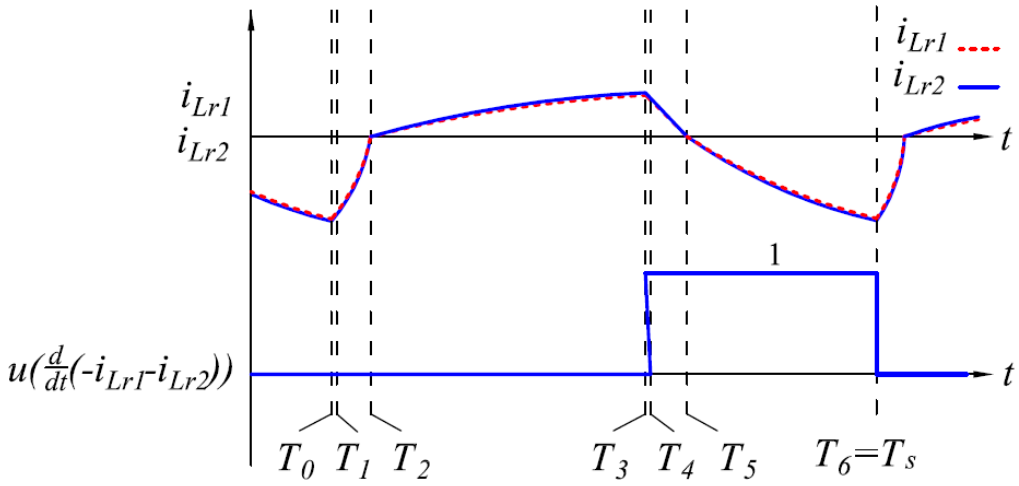


Figure 4.2: Resonant inductor currents and $u\left(\frac{d}{dt}\left(-i_{Lr1}-i_{Lr2}\right)\right)$.

3. Sign function of (i_{Lr1}+i_{Lr2}):

The variation of $sgn(i_{Lr1}+i_{Lr2})$ during one complete cycle of operation is shown in Figure 4.3. During *Mode III*, *Mode IV*, and *Mode V*, it equals +1 and during *Mode I*, *Mode II*, and *Mode VI* it equals -1. Therefore, $sgn(i_{Lr1}+i_{Lr2})$ can be decomposed into the Fourier series as follows:

$$\text{sgn}(i_{Lr1}(t)+i_{Lr2}(t))=A_0+\sum_{n=1,2,\ldots}A_n\cos(nF\omega_r t)+B_n\sin(nF\omega_r t) \tag{4.13}$$

where,

$$A_0=\frac{2T_5-2T_2-T_s}{T_s} \tag{4.14}$$

$$A_n = \frac{2}{n\pi}\left(\sin\left(\frac{2n\pi(T_5 - T_0)}{T_s}\right) - \sin\left(\frac{2n\pi(T_2 - T_0)}{T_s}\right)\right) \tag{4.15}$$

$$B_n = \frac{2}{n\pi}\left(-\cos\left(\frac{2n\pi(T_5 - T_0)}{T_s}\right) + \cos\left(\frac{2n\pi(T_2 - T_0)}{T_s}\right)\right) \tag{4.16}$$

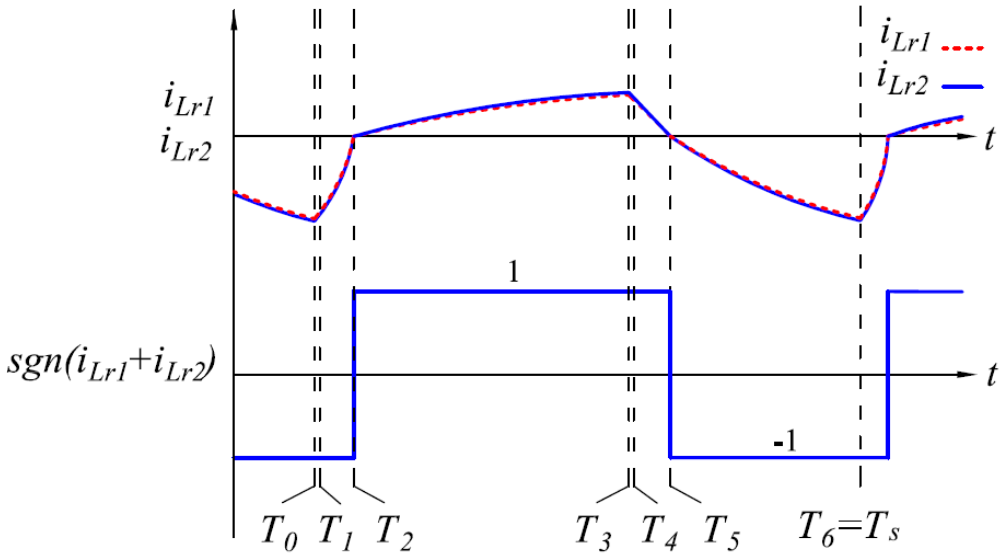


Figure 4.3: Resonant inductor currents and $sgn(i_{Lr1}+i_{Lr2})$.

4.2 State-Space Equations

The state-space equations for the converter in general form are obtained as follows:

$$C_{r1}\frac{dv_{Cr1}(t)}{dt} = i_{Lr1}(t) \tag{4.17}$$

$$C_{r2}\frac{dv_{Cr2}(t)}{dt} = i_{Lr2}(t) \tag{4.18}$$

$$L_{r1}\frac{di_{Lr1}(t)}{dt} = -v_{Cr1}(t) - \frac{v_o(t)}{2}\left(1+\text{sgn}(i_{Lr1}(t)+i_{Lr2}(t))\right) + Nv_{Lm}(t) \tag{4.19}$$

$$L_{r2}\frac{di_{Lr2}(t)}{dt}=-v_{Cr2}(t)+\frac{v_o(t)}{2}\left(1-\text{sgn}(i_{Lr1}(t)+i_{Lr2}(t))\right)+Nv_{Lm}(t) \tag{4.20}$$

$$L_m\frac{di_{Lm}(t)}{dt}=v_{Lm}(t) \tag{4.21}$$

$$C_c\frac{dv_{Cc}(t)}{dt}=u\left(\frac{d}{dt}\left(-i_{Lr1}(t)-i_{Lr2}(t)\right)\right)\times\left(i_{Lm}+N\left(i_{Lr1}(t)+i_{Lr2}(t)\right)\right) \tag{4.22}$$

$$C_o\frac{dv_o(t)}{dt}=\frac{1}{2}(i_{Lr1}(t)-i_{Lr2}(t))+\frac{1}{2}(i_{Lr1}(t)+i_{Lr2}(t))\text{sgn}(i_{Lr1}(t)+i_{Lr2}(t))-\frac{v_o}{R_o}+i_o(t) \tag{4.23}$$

where, *sgn*(·) and *u*(·) are the sign and step functions, respectively.

With the converter represented as a general block diagram, the input signals are shown in Figure 4.4. The inputs of the system can be expressed in the form of a constant large signal and a small signal, as shown in (4.24)-(4.27).

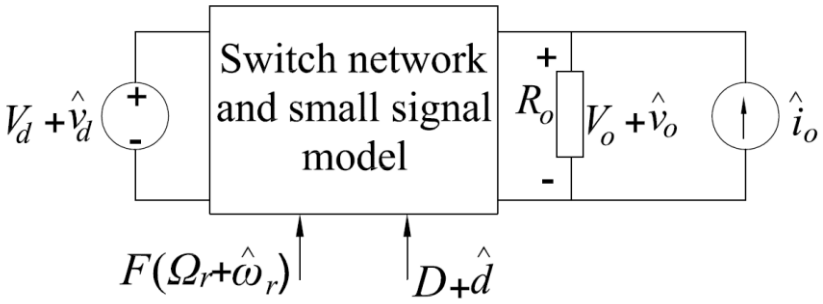


Figure 4.4: General representation of the converter.

$$v_d=V_d+\hat{v}_d \tag{4.24}$$

$$d=D+\hat{d} \tag{4.25}$$

$$\omega_s=\Omega_s+\hat{\omega}_s=F\omega_r=F(\Omega_r+\hat{\omega}_r) \tag{4.26}$$

$$i_o = \hat{i}_o \tag{4.27}$$

where, ω_s is the angular switching frequency and i_o represents small variation in the output load.

Combining the decomposed form of the state-space signals of (4.1)-(4.7) and (4.24)-(4.27) with the state-space equations (4.17)-(4.23) and using the pre-defined signals in (4.8), (4.12) and (4.13), the general form of the state-space equations can be obtained as follows:

$$C_{r1}\sum_{n=1,2,..}\left(\begin{array}{l}\left(\frac{d}{dt}v_{nFSCr1}(t)-nF\omega_r v_{nFCCr1}(t)\right)\sin(nF\omega_r t)\\ +\left(\frac{d}{dt}v_{nFCCr1}(t)+nF\omega_r v_{nFnCr1}(t)\right)\cos(nF\omega_r t)\end{array}\right) = \sum_{n=1,2,..}\left(i_{nFSLr1}(t)\sin(nF\omega_r t)+i_{nFCLr1}(t)\cos(nF\omega_r t)\right) \tag{4.28}$$

$$C_{r2}\sum_{n=1,2,..}\left(\begin{array}{l}\left(\frac{d}{dt}v_{nFSCr2}(t)-nF\omega_r v_{nFCCr2}(t)\right)\sin(nF\omega_r t)\\ +\left(\frac{d}{dt}v_{nFCCr2}(t)+nF\omega_r v_{nFnCr2}(t)\right)\cos(nF\omega_r t)\end{array}\right) = \sum_{n=1,2,..}\left(i_{nFSLr2}(t)\sin(nF\omega_r t)+i_{nFCLr2}(t)\cos(nF\omega_r t)\right) \tag{4.29}$$

$$\begin{aligned}&L_{r1}\sum_{n=1,2,..}\left(\begin{array}{l}\left(\frac{d}{dt}i_{nFSLr1}(t)-nF\omega_r i_{KnCLr1}(t)\right)\sin(nF\omega_r t)\\ +\left(\frac{d}{dt}i_{nFCLr1}(t)+nF\omega_r i_{nFSLr1}(t)\right)\cos(nF\omega_r t)\end{array}\right)=\\ &-v_{Cr1}-\sum_{n=1,2,..}\left(v_{nFSCr1}(t)\sin(nF\omega_r t)+v_{nFCCr1}(t)\cos(nF\omega_r t)\right)-\\ &\frac{v_o}{2}\times\left(1+A_0+\sum_{n=1,2,...}\left(A_n\cos(nF\omega_r t)+B_n\sin(nF\omega_r t)\right)\right)+\\ &N\left(a_0+\sum_{n=1,2,...}\left(a_n\cos(nF\omega_r t)+b_n\sin(nF\omega_r t)\right)\right)\end{aligned} \tag{4.30}$$

$$L_{r2}\sum_{n=1,2,..}\begin{pmatrix}\left(\frac{d}{dt}i_{nFSLr2}(t)-nF\omega_r i_{nFCLr2}(t)\right)\sin(nF\omega_r t)\\+\left(\frac{d}{dt}i_{nFCLr2}(t)+nF\omega_r i_{nFSLr2}(t)\right)\cos(nF\omega_r t)\end{pmatrix}=$$
$$-v_{Cr2}-\sum_{n=1,2,...}\left(v_{nFSCr2}(t)\sin(nF\omega_r t)+v_{nFCCr2}(t)\cos(nF\omega_r t)\right)+$$
$$\frac{v_o}{2}\times\left(1-A_0-\sum_{n=1,2,...}\left(A_n\cos(nF\omega_r t)+B_n\sin(nF\omega_r t)\right)\right)+$$
$$N\left(a_0+\sum_{n=1,2,...}\left(a_n\cos(nF\omega_r t)+b_n\sin(nF\omega_r t)\right)\right) \quad (4.31)$$

$$L_m\frac{d}{dt}i_{Lm}(t)=a_0+\left(v_d+v_{Cc}\right)\sum_{n=1,2,...}a_n\cos(nF\omega_r t)+b_n\sin(nF\omega_r t) \quad (4.32)$$

$$C_c\frac{d}{dt}v_{Cc}(t)=\left((1-d)+\sum_{n=1,2,..}a_n\cos(nF\omega_r t)+b_n\sin(nF\omega_r t)\right)\times$$
$$\left(-i_{Lm}-N\sum_{n=1,2,..}\left(\left(i_{nFSLr1}(t)+i_{nFSLr2}(t)\right)\sin(nF\omega_r t)+\left(i_{nFCLr1}(t)+i_{nFCLr2}(t)\right)\cos(nF\omega_r t)\right)\right) \quad (4.33)$$

$$C_o\frac{d}{dt}v_o(t)=\frac{1}{2}\sum_{n=1,2,..}\left(\left(i_{nFSLr1}(t)-i_{nFSLr2}(t)\right)\sin(nF\omega_r t)+\left(i_{nFCLr1}(t)-i_{nFCLr2}(t)\right)\cos(nF\omega_r t)\right)+$$
$$\left(\frac{1}{2}\sum_{n=1,2,..}\left(\left(i_{nFSLr1}(t)+i_{nFSLr2}(t)\right)\sin(nF\omega_r t)+\left(i_{nFCLr1}(t)+i_{nFCLr2}(t)\right)\cos(nF\omega_r t)\right)\right)\times$$
$$\left(A_0+\sum_{n=1,2,...}A_n\cos(nF\omega_r t)+B_n\sin(nF\omega_r t)\right)-\frac{v_o}{R_o}+i_o \quad (4.34)$$

Moreover, each signal can be written as the summation of large signal and small signal terms for both AC and DC parts as follows:

$$i_{nFSLr1}(t)=I_{nFSLr1}+\hat{i}_{nFSLr1} \quad (4.35)$$

$$i_{nFCLr1}(t)=I_{nFCLr1}+\hat{i}_{nFCLr1} \quad (4.36)$$

$$i_{nFSLr2}(t) = I_{nFSLr2} + \hat{i}_{nFSLr2} \tag{3.37}$$

$$i_{nFCLr2}(t) = I_{nFCLr2} + \hat{i}_{nFCLr2} \tag{4.38}$$

$$v_{nFSCr1}(t) = V_{nFSCr1} + \hat{v}_{nFSCr1} \tag{4.39}$$

$$v_{nFCCr1}(t) = V_{nFCCr1} + \hat{v}_{nFCCr1} \tag{4.40}$$

$$v_{nFSCr2}(t) = V_{nFSCr2} + \hat{v}_{nFSCr2} \tag{4.41}$$

$$v_{nFCCr2}(t) = V_{nFCCr2} + \hat{v}_{nFCCr2} \tag{4.42}$$

$$v_{Cr1} = V_{Cr1} + \hat{v}_{Cr1} \tag{4.43}$$

$$v_{Cr2} = V_{Cr2} + \hat{v}_{Cr2} \tag{4.44}$$

$$i_{Lm} = I_{Lm} + \hat{i}_{Lm} \tag{4.45}$$

$$v_{Cc} = V_{Cc} + \hat{v}_{Cc} \tag{4.46}$$

$$v_o = V_o + \hat{v}_o \tag{4.47}$$

By equating AC and DC terms of (4.28)-(4.34), and dividing each equation into large signal and small signal components (4.35)-(4.47), the steady state and small signal analyses can be derived as described in the following sections.

4.3 Steady State Analysis

For a given operating point $\{V_d, D, \Omega_s, R_o\}$, the following steady state solutions can be derived from the large signal analysis:

$$I_{nFCLr1} = I_{nFCLr2} \tag{4.48}$$

$$I_{nFSLr1} = I_{nFSLr2} \tag{4.49}$$

$$V_{Cr1} = -\frac{V_o}{2}(1 + A_0) \tag{4.50}$$

$$V_{Cr2} = +\frac{V_o}{2}(1 - A_0) \tag{4.51}$$

$$V_{Cc} = \frac{D}{1-D} V_d \tag{4.52}$$

$$I_{nFCLr1} = \frac{-V_{nFSCr} - \frac{V_o}{2} B_n + N\left(\frac{V_d + V_{Cc}}{n\pi}\right)\left(1 - \cos(2n\pi D)\right)}{-L_{r1} nF\Omega_r} \tag{4.53}$$

$$I_{nFSLr1} = \frac{-V_{nFCCr} - \frac{V_o}{2} A_n + N\left(\frac{V_d + V_{Cc}}{n\pi}\right)\left(\sin(2n\pi D)\right)}{L_{r1} nF\Omega_r} \tag{4.54}$$

$$V_{nFSCr1} = \frac{I_{nFCLr1}}{nF\Omega_r C_{r1}} \tag{4.55}$$

$$V_{nFSCr2} = \frac{I_{nFCLr2}}{nF\Omega_r C_{r2}} \tag{4.56}$$

$$V_{nFCCr1} = -\frac{I_{nFSLr1}}{nF\Omega_r C_{r1}} \tag{4.57}$$

$$V_{nFCCr2} = -\frac{I_{nFSLr2}}{nF\Omega_r C_{r2}} \tag{4.58}$$

$$I_{Lm} = \frac{N}{(1-D)} \sum_{n=1,2,\ldots} \left[I_{nFCLr1} a_n + I_{nFSLr1} b_n \right] \tag{4.59}$$

$$V_o = \frac{R_o}{2} \sum_{n=1,2,\ldots} \left[I_{nFCLr1} A_n + I_{nFSLr1} B_n \right] \tag{4.60}$$

It is observed that all the state-space variables are not completely in terms of input signals $\{V_d, D, \Omega_s, R_o\}$. For example, the output voltage is a function of the output load, resonant currents, and the Fourier components of $sgn(i_{Lr1}+i_{Lr2})$. However, an approximate expression for the voltage conversion ratio of the converter can be obtained by assuming that the pulse widths of $sgn(i_{Lr1}+i_{Lr2})$ and $v_{Lm}(t)$ are equal, but with a phase difference between the two signals. This assumption can be visually realized as shown in Figure 4.5. In this figure, this phase difference is marked as θ and can be expressed as $\theta=2\pi.T_2/T_s$.

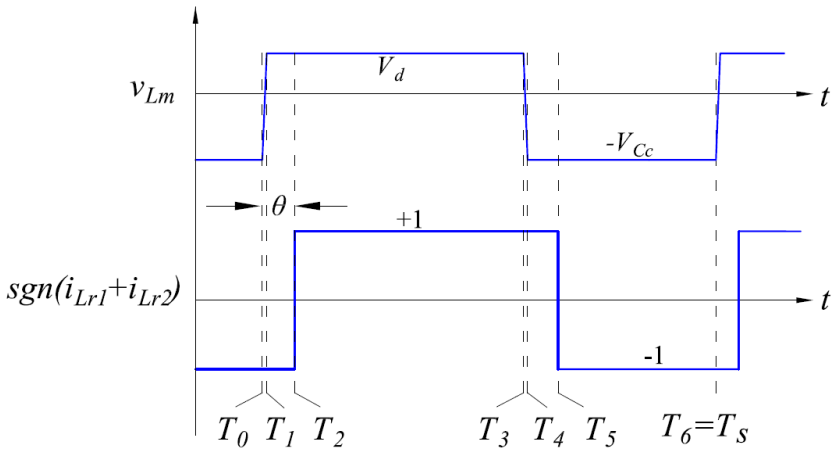


Figure 4.5: The phase angle between v_{Lm} and sgn($i_{Lr1}+i_{Lr2}$).

Applying these approximations to calculate the Fourier coefficients of $sgn(i_{Lr1}+i_{Lr2})$, the following terms are obtained:

$$A_0 \approx A_0' = 2D-1 \tag{4.61}$$

$$A_n \approx A_n' = \frac{2}{n\pi}\left(\sin(2\pi nD+n\theta)-\sin(n\theta)\right) \tag{4.62}$$

$$B_n \approx B_n' = \frac{2}{n\pi}\left(-\cos(2\pi nD + n\theta) + \cos(n\theta)\right) \tag{4.63}$$

Merging the steady state solutions of the resonant currents (4.53) and (4.54) with (4.60), and considering the first two components of the series (4.60), the output voltage is obtained as follows:

$$V_o = 2R_o\left(\frac{\left|V_o\angle\theta - \frac{NV_d}{1-D}\right|}{\pi^2\left(\Omega_s L_r + 1/\Omega_s C_r\right)}\left(1-\cos(2\pi D)\right) + \frac{\left|V_o\angle 2\theta - \frac{NV_d}{1-D}\right|}{(2\pi)^2\left(2\Omega_s L_r + 1/2\Omega_s C_r\right)}\left(1-\cos(4\pi D)\right)\right) \tag{4.64}$$

Equation (4.64) shows that the DC output voltage can be varied by the duty ratio (D) and switching frequency (Ω_s).

4.3.1 Simulation Results – State Space Trajectories

Figure 4.6 to Figure 4.8 show the state-space trajectories of the converter in the steady state condition for different operating conditions. The results of the large signal analysis show that the resonant inductor currents are equal, i.e. $I_{nFSLr1}=I_{nFSLr2}$ and $I_{nFCLr1}=I_{nFCLr2}$. Consequently, (4.55)-(4.58) demonstrate that the AC components of the resonant capacitor voltages are equal. This result is observed in the state-space trajectories, as the shapes of the trajectories of v_{Cr1} versus i_{Lr1} and v_{Cr2} versus i_{Lr2} are identical. This indicates that the AC components of the resonant inductor currents of i_{Lr1} and i_{Lr2} and the resonant capacitor voltages of v_{Cr1} and v_{Cr2} are equal. However, it is observed that the average values of the resonant capacitor voltages (V_{Cr1} and V_{Cr2}) are not equal. It can be realized from (4.50) and

(4.51) that the difference between v_{Cr1} and v_{Cr2} is equal to the output voltage of the converter as follows:

$$V_{Cr2} - V_{Cr1} = V_o \tag{4.65}$$

The above conclusion was reached in Chapter 3 from the time domain analysis of the operation of the converter.

Figure 4.6 shows the state-space trajectories for different switching frequencies. As the switching frequency increases, the trajectory tends to become a straight line and the centers of the trajectories of each resonant circuit move closer together. This signifies that there is less fluctuation in both resonant inductor currents and resonant capacitor voltages and decrease in the output voltage.

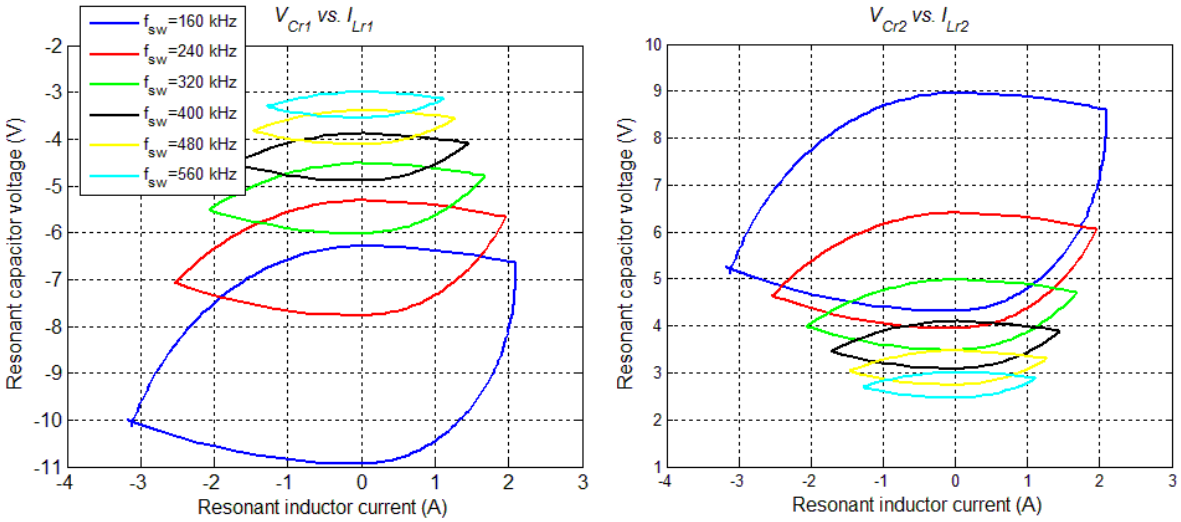


Figure 4.6: State-space trajectories for different switching frequencies

(D=0.6, R_o=10 Ω, V_d=10 V).

The state-space trajectories for different loading conditions are shown in Figure 4.7. As the output load resistor decreases, the resonant inductor currents increase and the resonant capacitor voltages decrease. The centers of the trajectories for higher value of loads move towards the origin, indicating the onset of short circuit condition.

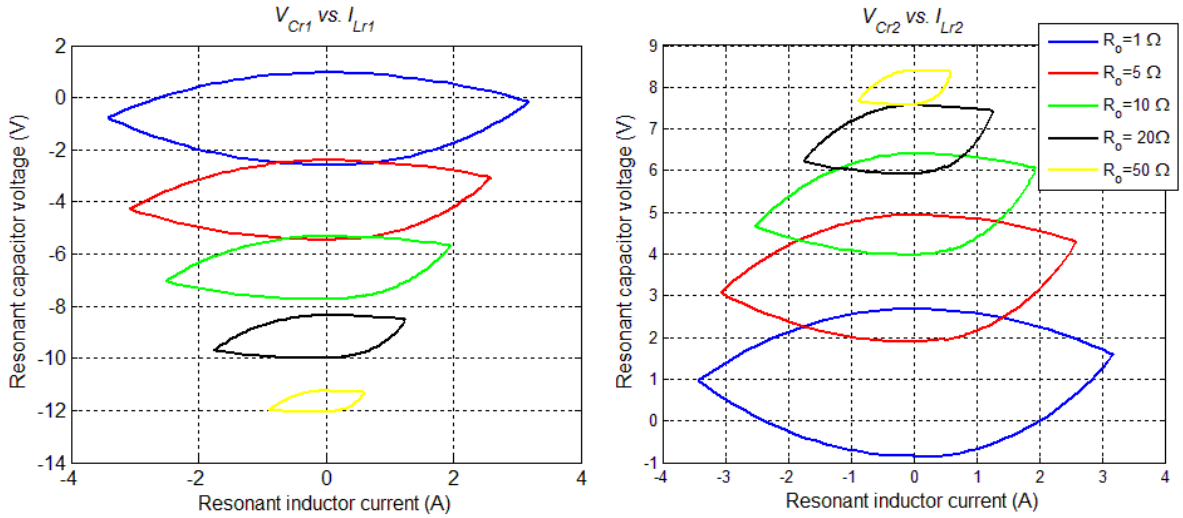


Figure 4.7: State-space trajectories for different loading conditions

(D=0.6, F=3, V_d=10 V).

Figure 4.8 shows the effect of the duty ratio of the switching signal on the state-space trajectories. Increasing the duty ratio of the switching signal results in the increase in both resonant inductor currents and resonant capacitor voltages. Besides, the centers of the trajectories move farther away from the origin, indicating increase in the value of output voltage of the converter.

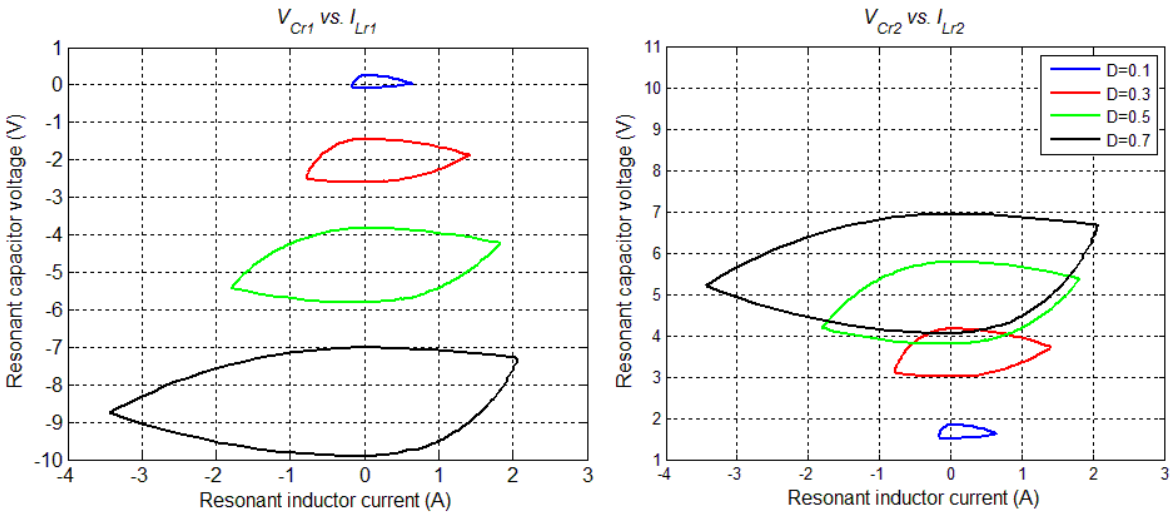


Figure 4.8: State-space trajectories for different duty ratios of the switching signal (R_o=10 Ω, F=3, V_d=10 V).

4.3.2 Simulation Results - PLECS and MATLAB

The steady state expression of the output voltage that is obtained from the developed model (4.64) is implemented in MATLAB and the results are compared with the simulation results from PLECS.

Figure 4.9 shows the voltage conversion ratio of the converter as a function of both duty ratio and switching frequency. It is observed that the predicted voltage conversion ratio based on the obtained expression in (4.64) is in good agreement with the simulation results. In addition, it is observed that the converter is capable of operating in step-down and step-up modes. Higher voltage conversion ratios can be achieved by reducing the switching frequency and increasing the duty ratio. The slight differences between the results from the PLECS simulation and analytical implementation in MATLAB are due to

the approximations described in the previous sections (i.e., the pulse widths of $sgn(i_{Lr1}+i_{Lr2})$ and $v_{Lm}(t)$ are equal, but with a phase difference between the two signals). The figure also shows that the deviation between the simulation and analytical results increases for duty ratios more than 0.7. This is because the pulse width of $sgn(i_{Lr1}+i_{Lr2})$ is no longer equal to the pulse width of $v_{Lm}(t)$ for D>0.7.

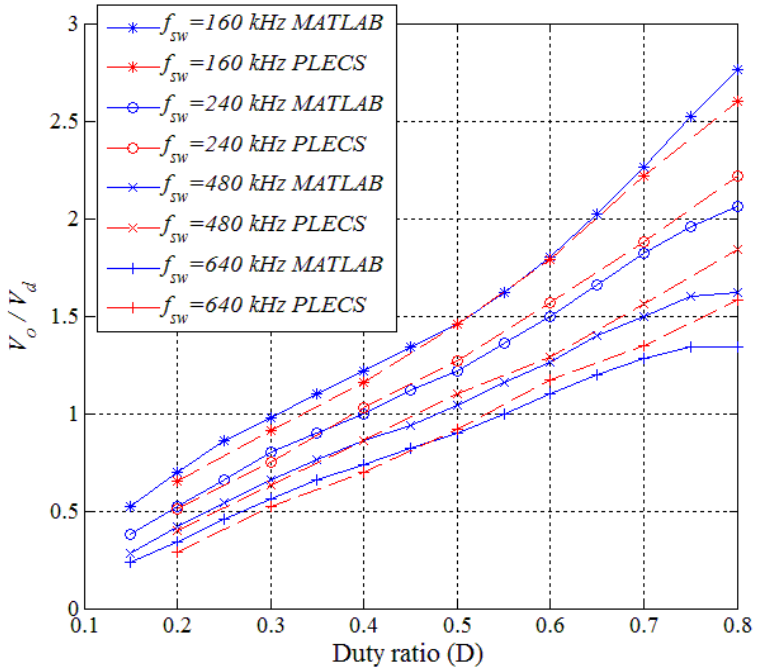


Figure 4.9: Simulation and modeling results of voltage conversion ratio versus duty ratio for different switching frequencies (V_d=10 V, R_o=30 Ω).

Table 4.1 compares the PLECS simulation results (also given in Table 3.1) with the results obtained from the extended describing function analytical approach in steady state condition for six different case studies introduced in Chapter 3. It is observed that the results from the analytical approach are in good agreement with simulation results for

different scenarios of operating condition of the converter. This comparison confirms the modeling procedure of the converter using extended describing function. In Chapter 6, the steady state results obtained from the analytical approach will be used to develop a design procedure to customize the converter for any level of power and voltage.

Table 4.1: Comparison between PLECS simulation and analytical modeling results.

	I_{1FLr1}= I_{1FLr1} [A]		V_{Cr1} [V]		V_{Cr1} [V]		V_o [V]	
	PLECS Results	Analytical Results	PLECS Results	Analytical Results	PLECS Results	Analytical Results	PLECS Results	Analytical Results
Case study I f_{sw}=240 kHz, D=0.3, R_o=30 Ω	0.433	0.465	-2.72	-2.76	6.14	5.83	8.84	8.60
Case study II f_{sw}=240 kHz, D=0.6, R_o=30 Ω	0.90	0.82	-10.50	-10.80	7.40	7.50	17.87	18.30
Case study III f_{sw}=320 kHz, D=0.6, R_o=30 Ω	0.82	0.79	-9.45	-10.65	6.81	7.54	16.24	18.20
Case study IV f_{sw}=480 kHz, D=0.6, R_o=30 Ω	0.71	0.70	-7.86	-8.90	5.86	6.39	13.71	15.30
Case study V f_{sw}=240 kHz, D=0.4, R_o=30 Ω	0.58	0.61	-4.66	-4.58	6.80	6.51	11.46	11.10
Case study VI f_{sw}=240 kHz, D=0.4, R_o=15 Ω	0.95	0.90	-3.88	-3.46	5.33	4.83	9.21	8.30

4.4 Small Signal Analysis

In order to obtain the small signal model of the converter, the small signal components on both sides of the state space equations ((4.28) – (4.34)) should be equated. However, these equations contain a series of infinite harmonic terms. Employing the extended describing

function would involve equating all terms that have identical harmonics. For an infinite number of harmonics, completing the small signal analysis and finding an analytical result by taking into account all harmonic components is a challenge. To simplify the analysis, only the fundamental components (i.e., n=1) of the state variables are considered and the higher harmonic components are neglected. In Appendix A, it is demonstrated that this assumption has a negligible effect on the response of the system, by comparing the frequency response of the developed model based on the fundamental components of the state space variables with the response of the system when all harmonic components are taken into account.

The state-space equations of the converter ((4.28) – (4.34)) can be represented in the general form as follows:

$$\frac{d\hat{x}}{dt} = A\hat{x} + B\hat{u} \tag{4.66}$$

$$\hat{y} = C\hat{x} \tag{4.67}$$

where,

$$\hat{x} = \left[\hat{i}_{1FSLr} \quad \hat{i}_{1FCLr} \quad \hat{v}_{1FSCr} \quad \hat{v}_{1FCCr} \quad \hat{i}_{Lm} \quad \hat{v}_{Cc} \quad \hat{v}_o\right]^T \tag{4.68}$$

$$\hat{u} = \left[\hat{v}_d \quad \hat{d} \quad \hat{\omega}_s \quad \hat{i}_o\right]^T \tag{4.69}$$

$$\hat{y} = \left[\hat{v}_o\right] \tag{4.70}$$

In (4.68), $\hat{i}_{1FSLr}$, $\hat{i}_{1FCLr}$, $\hat{v}_{1FSCr}$, and $\hat{v}_{1FCCr}$ represent the decomposed fundamental components of the resonant inductor currents and resonant capacitor voltages (n = 1). The state space matrices in (4.66) and (4.67) can be obtained by substituting (4.24)-(4.27) into

(4.28)-(4.34) and equating the small signals of *sin*(·), *cos*(·), and DC terms. The resulting state-space matrices in (4.66) and (4.67) are as follows:

$$A=\begin{bmatrix} 0 & F\Omega_r & -\frac{1}{L_r} & 0 & 0 & \frac{-Nb_1}{L_r} & \frac{-B_1'}{2L_r} \\ -F\Omega_r & 0 & 0 & -\frac{1}{L_r} & 0 & \frac{-Na_1}{L_r} & \frac{-A_1'}{2L_r} \\ \frac{1}{C_r} & 0 & 0 & F\Omega_r & 0 & 0 & 0 \\ 0 & \frac{1}{C_r} & -F\Omega_r & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1-D}{L_m} & 0 \\ \frac{Nb_1}{C_c} & \frac{Na_1}{C_c} & 0 & 0 & -\frac{(1-D)}{C_c} & 0 & 0 \\ \frac{B_1'}{2C_o} & \frac{A_1'}{2C_o} & 0 & 0 & 0 & 0 & -\frac{1}{R_oC_o} \end{bmatrix} \tag{4.71}$$

$$B=\begin{bmatrix} \frac{Nb_1}{L_r} & \frac{Na_1}{L_r} & 0 & 0 & \frac{D}{L_m} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{V_d}{(1-D)L_m} & \frac{I_{Lm}}{C_c} & 0 \\ nI_{1FCLr} & -nI_{1FSLr} & nV_{1FCCr} & -nV_{1FSCr} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{C_o} \end{bmatrix}^T \tag{4.72}$$

$$C=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{4.73}$$

A'_1, and B'_1 are the approximated fundamental Fourier coefficients of $sgn(i_{Lr1}(t)+i_{Lr2}(t))$; a_1 and b_1 are the Fourier coefficients of $v_{Lm}(t)$, the voltage across the magnetizing inductor at the primary side of the transformer.

The transfer functions of the converter can be obtained by transforming the state-space equations into the *s* domain, as follows:

$$T(s)=C(sI-A)^{-1}B \tag{4.74}$$

4.4.1 Qualitative Analysis of the Transfer Functions

By implementing (4.74), four transfer functions that relate the output voltage to the inputs of the system can be derived. These are: 1) input voltage-to-output ($\hat{v}_o(s)/\hat{v}_d(s)$); 2) duty ratio-to-output ($\hat{v}_o(s)/\hat{d}(s)$); 3) frequency-to-output ($\hat{v}_o(s)/\hat{\omega}_r(s)$); and 4) output current-to-output ($\hat{v}_o(s)/\hat{i}_o(s)$). The polynomial in the denominator of these transfer functions, which locates the poles of the system, is shown in (4.75).

$$\Delta = s^7 + \frac{1}{R_oC_o}s^6 + \frac{2(F^2+1)}{L_rC_r}s^5 + \frac{2(F^2+1)}{L_rC_rR_oC_o}s^4 + \frac{(F^2-1)^2}{{L_r}^2{C_r}^2}s^3 + \frac{(F^2-1)^2}{{L_r}^2{C_r}^2R_oC_o}s^2 + \frac{(1-D)^2(F^2-1)^2}{{L_r}^2{C_r}^2L_mC_c}s + \frac{(1-D)^2(F^2-1)^2}{{L_r}^2{C_r}^2L_mC_cR_oC_o} \tag{4.75}$$

Assuming that $L_m >> L_r$, and $\{C_c\ ,\ C_o\} >> C_r$, (4.75) can be reduced to the following expression:

$$\Delta = \left(s+\frac{1}{R_oC_o}\right)\left(s^2+(1-D)^2\Omega_m^2\right)\left(s^2+(F-1)^2\Omega_r^2\right)\left(s^2+(F+1)^2\Omega_r^2\right) \tag{4.76}$$

where,

$$\Omega_m = \frac{1}{\sqrt{L_mC_C}} \tag{4.77}$$

$$\Omega_r = \frac{1}{\sqrt{L_rC_r}} \tag{4.78}$$

It is observed that the system has one real pole and three imaginary double poles on the imaginary axis. Although all the complex poles in (4.76) are stated as purely imaginary poles, they have very small real parts that are small compared to the imaginary parts. In Section 4.5, it is shown that the real parts of the significant poles are effective in the stability analysis and need to be considered. The next sections investigate the four transfer functions of the system to determine their suitability for the control of the output voltage.

1. Input Voltage-to-Output Transfer Function ($\hat{v}_o(s)/\hat{v}_d(s)$)

This transfer function can be used to investigate the small variation in the output voltage caused by small variations in the input voltage.

$$\frac{\hat{v}_o(s)}{\hat{v}_d(s)} = K_v \frac{\left(s^2 + F^2\Omega_r^2\right)\left(s^2 + (1-D)\Omega_m^2\right)\left(s + z_1\right)}{\Delta} \tag{4.79}$$

where,

$$z_1 = \frac{F\Omega_r\left(B_1'a_1 - A_1'b_1\right)}{A_1'a_1 + B_1'b_1} \tag{4.80}$$

$$K_v = \frac{N\left(A_1'a_1 + B_1'b_1\right)}{2L_rC_o} \tag{4.81}$$

The pole-zero map of the input voltage-to-output transfer function is shown in Figure 4.10.

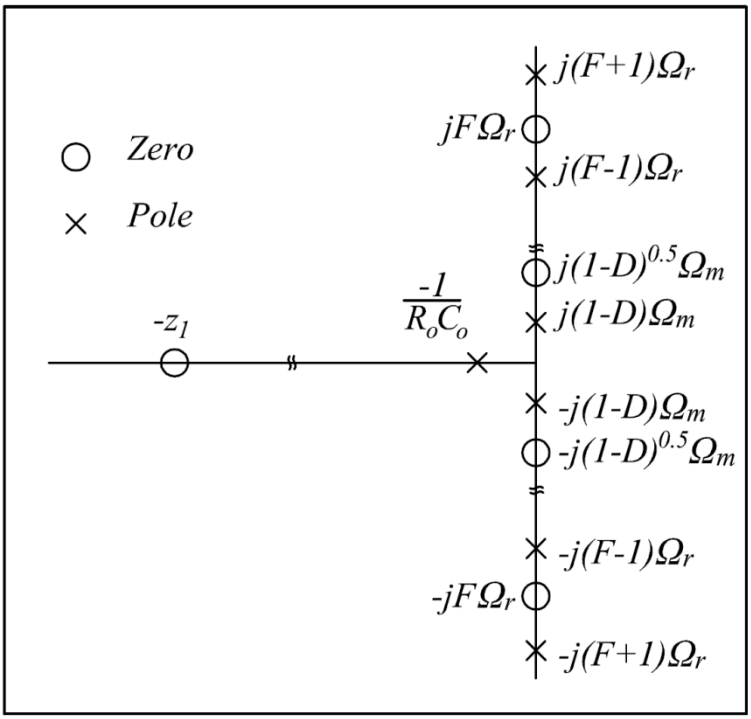


Figure 4.10: Pole-zero map of the input voltage-to-output transfer function.

2. Duty ratio-to-Output Transfer Function ($\hat{v}_o(s)/\hat{d}(s)$)

The duty ratio-to-output transfer function derived from (4.74) is as follows:

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = K_d \frac{\left(s^2 + F^2\Omega_r^2\right)\left(s+z_2\right)\left(s+z_3\right)}{\Delta} \tag{4.82}$$

where,

$$z_2 = \frac{F\Omega_r\left(B_1'a_1 - A_1'b_1\right)}{A_1'a_1 + B_1'b_1} \tag{4.83}$$

$$z_3 = \frac{V_d}{I_{Lm}L_m} \tag{4.84}$$

$$K_d = \frac{N\left(A_1' a_1 + B_1' b_1\right) I_{Lm}}{2 L_r C_c C_o} \tag{4.85}$$

It has one double imaginary zero and two real zeros. Figure 4.11 shows the pole-zero map of this transfer function.

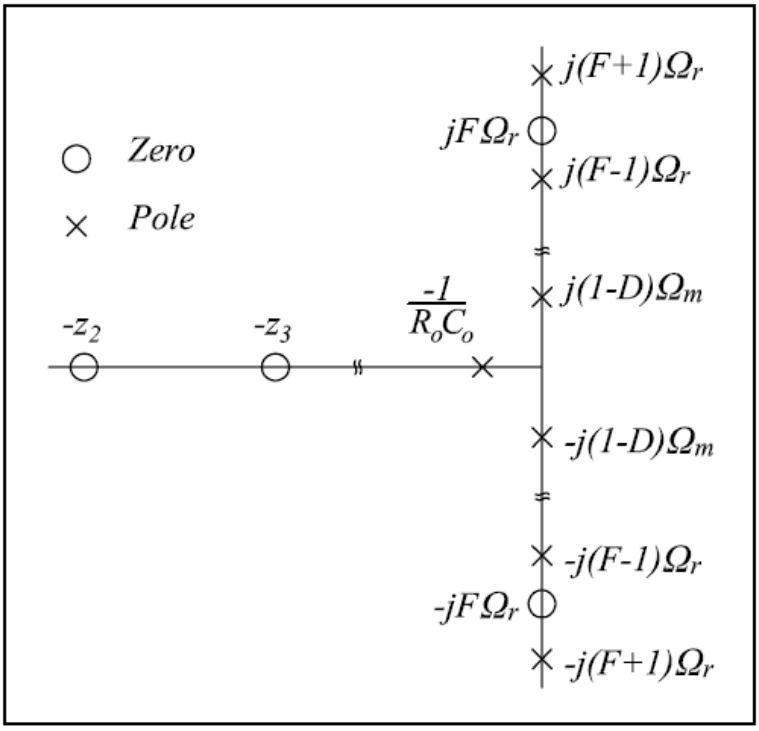


Figure 4.11: Pole-zero map of the duty ratio-to-output transfer function.

3. Frequency-to-Output Transfer Function ($\hat{v}_o(s)/\hat{\omega}_r(s)$)

Small variation in the output voltage caused by small variations in the switching frequency can be described by the frequency-to-output transfer function. The transfer function is as follows:

$$\frac{\hat{v}_o(s)}{\hat{\omega}_r(s)} = K_\omega \frac{\left(s^2 + F^2\Omega_r^2\right)\left(s^2 + (1-D)^2\Omega_m^2\right)(s + z_4)}{\Delta} \tag{4.86}$$

where,

$$K_\omega = \frac{F\left(I_{1FSLr}A_1' - I_{1FCLr}B_1'\right)}{2C_o} \tag{4.87}$$

$$z_4 = F\Omega_r \frac{I_{1FCLr}A_1' + I_{1FSLr}B_1'}{I_{1FSLr}A_1' - I_{1FCLr}B_1'} \tag{4.88}$$

As indicated in the pole-zero map of the transfer function in Figure 4.12, this transfer function has one real zero and two double imaginary zeros.

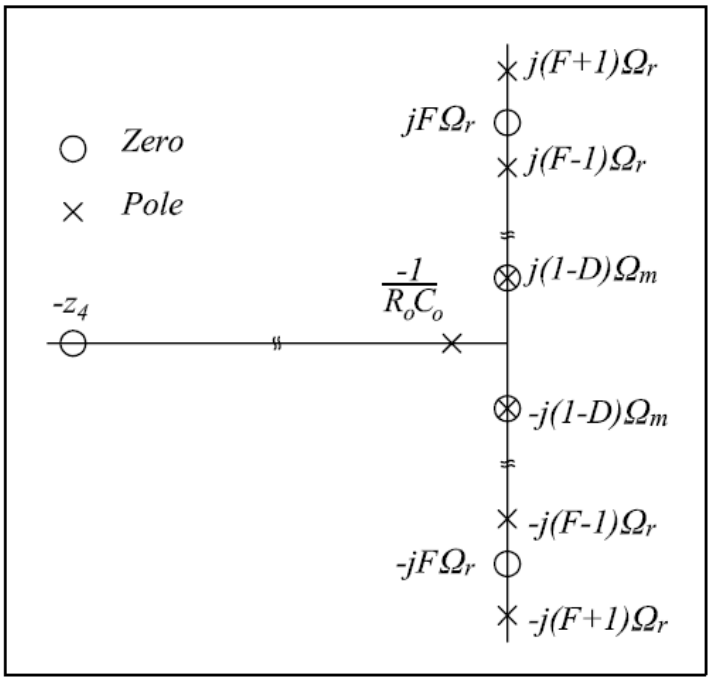


Figure 4.12: Pole-zero map of the frequency-to-output transfer function.

4. Output Current-to-Output Transfer Function ($\hat{v}_o(s)/\hat{i}_o(s)$)

The output current-to-output voltage transfer function is obtained as follows:

$$\frac{\hat{v}_o(s)}{\hat{i}_o(s)} = K_i \frac{\left(s^2 + (F+1)^2\Omega_r^2\right)\left(s^2 + (F-1)^2\Omega_r^2\right)\left(s^2 + (1-D)^2\Omega_m^2\right)}{\Delta} \tag{4.89}$$

where,

$$K_i = \frac{1}{C_o} \tag{4.90}$$

It is observed that the imaginary poles and imaginary zeros are co-located; therefore, the order of the output current-to-output voltage transfer function can be reduced to a first order, low pass filter as follows:

$$\frac{\hat{v}_o(s)}{\hat{i}_o(s)} = \frac{1/C_o}{s + \frac{1}{R_o C_o}} \tag{4.91}$$

Figure 4.13 shows the pole-zero map of this transfer function.

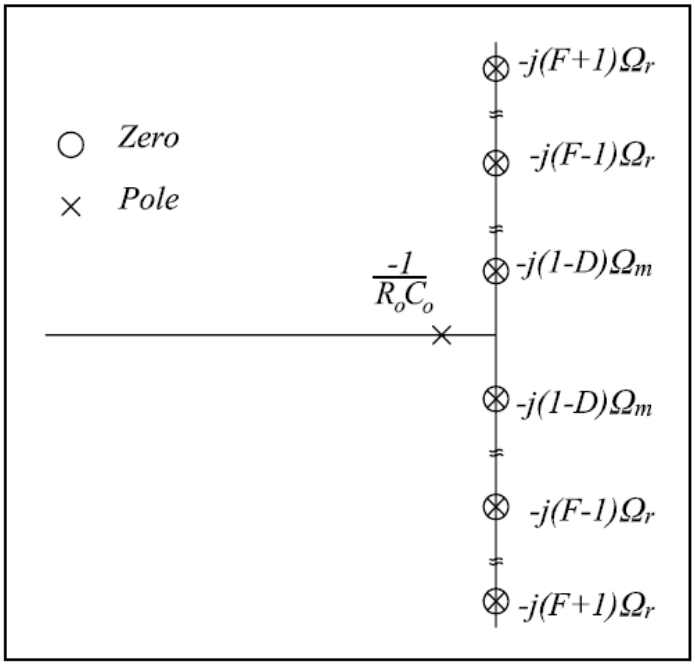


Figure 4.13: Pole-zero map of the output current-to-output transfer function.

The locations of all poles, zeros, and value of the gains of the transfer functions are summarized in Table 4.2.

Table 4.2: Small signal transfer functions of the system.

Transfer Function	Gain	Zeros	Poles
$\frac{\hat{v}_o(s)}{\hat{v}_d(s)}$	$\frac{N\left(A_1'a_1+B_1'b_1\right)}{2L_rC_o}$	$\pm jF\Omega_r$ $\pm j\sqrt{1-D}\Omega_m$ $-F\Omega_r\frac{B_1'a_1-A_1'b_1}{A_1'a_1+B_1'b_1}$	$\pm j(F+1)\Omega_r$ $\pm j(F-1)\Omega_r$ $\pm j(1-D)\Omega_m$ $-\frac{1}{R_oC_o}$
$\frac{\hat{v}_o(s)}{\hat{d}(s)}$	$\frac{N\left(A_1'a_1+B_1'b_1\right)I_{Lm}}{2L_rC_CC_o}$	$\pm jF\Omega_r$ $-F\Omega_r\frac{B_1'a_1-A_1'b_1}{A_1'a_1+B_1'b_1}$ $-\frac{V_d}{I_{Lm}L_m}$	
$\frac{\hat{v}_o(s)}{\hat{\omega}_r(s)}$	$\frac{F\left(I_{1FSLr}A_1'-I_{1FCLr}B_1'\right)}{2C_o}$	$\pm jF\Omega_r$ $\pm j(1-D)\Omega_m$ $-F\Omega_r\frac{I_{1FCLr}A_1'+I_{1FSLr}B_1'}{I_{1FSLr}A_1'-I_{1FCLr}B_1'}$	
$\frac{\hat{v}_o(s)}{\hat{i}_o(s)}$	$\frac{1}{C_o}$	$\pm j(F+1)\Omega_r$ $\pm j(F-1)\Omega_r$ $\pm j(1-D)\Omega_m$	

4.4.2 Selection of Transfer Function to Control the Output Voltage

Among the four transfer functions that can be employed to regulate the output voltage with respect to a fixed reference voltage in a closed-loop control scheme, the duty ratio-to-output and frequency-to-output transfer functions would be preferred, since the duty ratio and switching frequency can be tuned using most controller platforms. Between the two control schemes, the duty ratio-to-output transfer function is preferred for the following reasons:

1. The value of the gain and the location of one of the zeros of the frequency-to-output transfer function are dependent on the fundamental components of the Fourier expansion of the resonant inductor current (i.e., I_{1FSLr} and I_{1FCLr}). Although the RMS value of the fundamental component of the resonant inductor current can be calculated using (4.92), finding the phase angle of the resonant inductor current and consequently, calculating I_{1FSLr} and I_{1FCLr}, is a challenge. On the other hand, although it appears that the value of the gain and the location of one of the zeros of duty ratio-to-output transfer function is dependent on I_{Lm}, in the next section it is shown that this dependency can be removed by reducing the duty ratio-to-output transfer function to a 3rd order system.

$$I_{Lr} = \frac{\pi V_o}{2R_o\sqrt{1-\cos(2\pi D)}} \tag{4.92}$$

2. Implementation of a control scheme to control the duty ratio is easier than implementation of a control scheme to control the switching frequency. A simple PWM chip with fixed frequency can be used to generate the pulse signals that feed the driver of the switches. In the case of more sophisticated controller platforms such as FPGA and DSP, the frequency of the generated pulse can be varied by either changing the frequency of the clock of the PWM block or changing the number of bits of the PWM block depending on the available features of the controller platform. In either case, the implementation of a variable switching frequency control scheme is not straightforward. On the other hand, the duty ratio of the PWM pulse can be updated during each repetition without changing the

basis of the control algorithm (i.e., frequency of the clock and the number of bits of the PWM block).

From the point of view of simplicity and ease of implementation, the duty ratio-to-output transfer function is chosen for the implementation of a closed-loop control scheme for the proposed converter and hereinafter, it is called control-to-output transfer function. The control scheme would be able to regulate the output voltage in the case of step changes in the output load or input voltage of the converter.

4.4.3 Control-to-Output Transfer Function Simplification

In order to provide additional insight into the performance of the converter under duty ratio control scheme, a reduced order model of the control-to-output transfer function is derived. Considering all the poles on the imaginary axis, as listed in Table 4.2, it is expected that the response of the system will fluctuate without any damping behavior around the steady state value. Figure 4.14 depicts a case study where the PLECS simulation results and the step response of the control-to-output transfer function of the 7^{th} order system in (4.82) are compared. From the PLECS simulation results, it is seen that the output voltage of the converter exhibits damping behavior and reaches a steady state value after some initial damped fluctuations. However, the step response of the control-to-output transfer function behaves as an undamped fluctuation around the steady sate value of the output voltage.

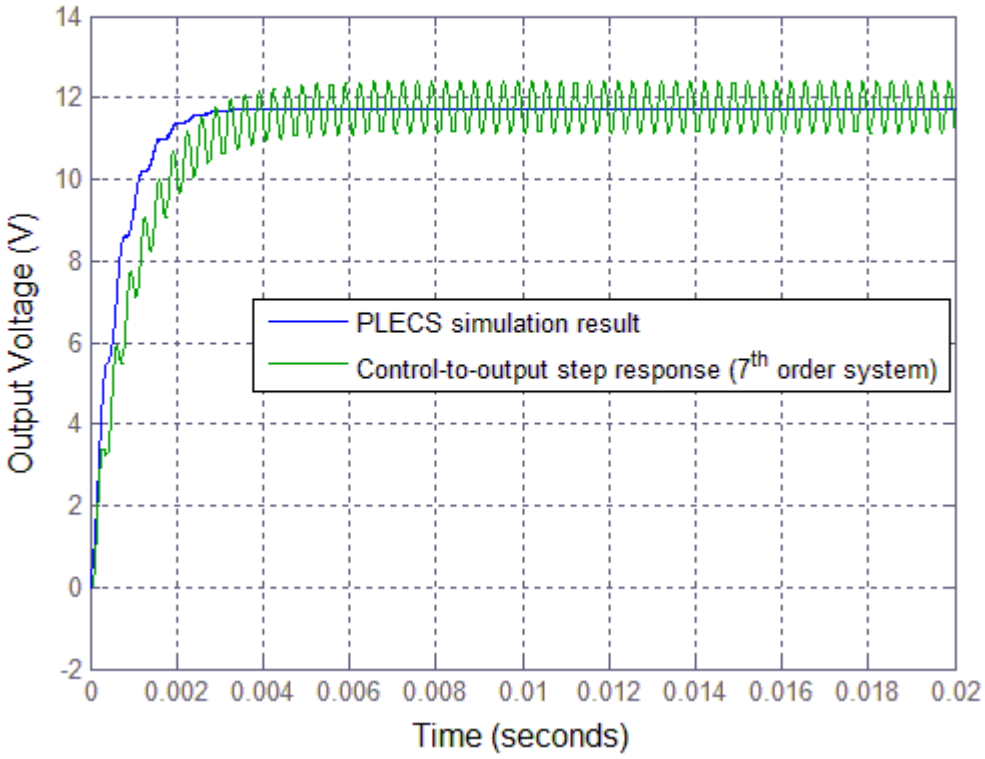
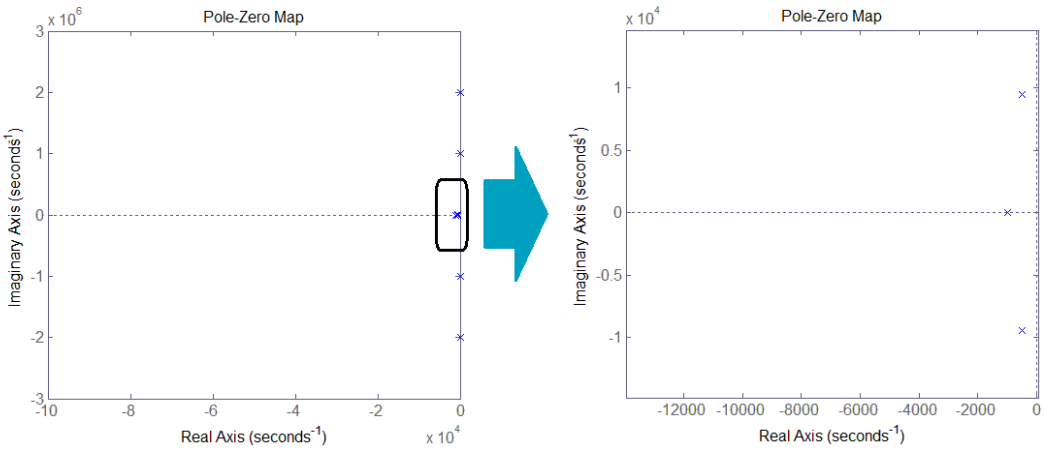


Figure 4.14: Comparing the step response of the 7th order system in (4.82) with the PLECS simulation result (R_o=10 Ω, F=3, D=0.6).

This observation suggests that at least one of the double imaginary poles of the system have a non-zero real part, which helps the system to damp the fluctuations around the steady state value of the output voltage and has been omitted during implementation of the extended describing function. A closer look at the pole-zero map of the control-to-output transfer function reveals that the double imaginary poles associated with Ω_m have a small real part, which establishes a damping ratio (ζ). Figure 4.15 shows the map of the poles of the control-to-output transfer function. From the enlarged window of this figure, it is

noticed that the poles associated with Ω_m do not occur exactly on the imaginary axis; instead, these poles have a real part, which is very small compared to the imaginary part. This yields a small damping ratio, which needs to be considered in the analysis due to its role in damping the fluctuations of the output voltage.



(a) (b)

Figure 4.15: The complex poles associated with Ω_m (R_o=10 Ω, F=3, D=0.75): a) all the existing poles, b) enlarged window.

Therefore, the polynomial in (4.76) can be rewritten as follows:

$$\Delta' = \left(s + \frac{1}{R_o C_o}\right)\left(s^2 + 2\zeta(1-D)\Omega_m s + (1-D)^2\Omega_m^2\right)\left(s^2 + (F-1)^2\Omega_r^2\right)\left(s^2 + (F+1)^2\Omega_r^2\right) \tag{4.93}$$

Other double imaginary poles (i.e., $\pm j(F+1)\Omega_r$ and $\pm j(F-1)\Omega_r$) occur at relatively high frequencies. Even if these poles exhibit the same damping behavior, the dynamic behaviour of the system is determined by the poles associated with Ω_m, which occur at much lower frequencies. Therefore, the poles associated with Ω_r can be considered totally

on the imaginary axis and without real parts. Hence, the poles of the transfer function can be expressed as follows:

$$p_1 = -\frac{1}{R_o C_o} \tag{4.94}$$

$$p_2, p_3 = -\zeta(1-D)\Omega_m \pm j(1-D)\Omega_m\sqrt{1-\zeta^2} \tag{4.95}$$

$$p_4, p_5 = \pm j(F-1)\Omega_r \tag{4.96}$$

$$p_6, p_7 = \pm j(F+1)\Omega_r \tag{4.97}$$

The modified control-to-output transfer function is as follows:

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{\frac{N\left(A_1'a_1 + B_1'b_1\right)I_{Lm}}{2L_r C_c C_o}\left(s^2 + F^2\Omega_r^2\right)\left(s + F\Omega_r\frac{B_1'a_1 - A_1'b_1}{A_1'a_1 + B_1'b_1}\right)\left(s + \frac{V_d}{I_{Lm}L_m}\right)}{\left(s + \frac{1}{R_o C_o}\right)\left(s^2 + 2\zeta(1-D)\Omega_m s + (1-D)^2\Omega_m^2\right)\left(s^2 + (F-1)^2\Omega_r^2\right)\left(s^2 + (F+1)^2\Omega_r^2\right)} \tag{4.98}$$

From (4.94)-(4.97), it is observed that the poles and zeros of the transfer function occur at relatively high frequencies, except for p_1, p_2, and p_3 in (4.94) and (4.95). This observation can be used to effectively reduce the order of the transfer function from a 7th order system to a 3rd order system which is expressed as follows:

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{K_d'}{\left(s + \frac{1}{R_o C_o}\right)\left(s^2 + 2\zeta(1-D)\Omega_m s + (1-D)^2\Omega_m^2\right)} \tag{4.99}$$

The gain of the 3rd order system is determined from (4.98) as follows:

$$K_d' = \frac{N\left(A_1'a_1 + B_1'b_1\right)I_{Lm}}{2L_rC_cC_o}\frac{\left(F^2\Omega_r^2\right)\left(F\Omega_r\dfrac{B_1'a_1 - A_1'b_1}{A_1'a_1 + B_1'b_1}\right)\left(\dfrac{V_d}{I_{Lm}L_m}\right)}{\left((F-1)^2\Omega_r^2\right)\left((F+1)^2\Omega_r^2\right)} \approx \frac{NV_d\left(B_1'a_1 - A_1'b_1\right)}{2F\Omega_rL_rL_mC_cC_o} \qquad (4.100)$$

Figure 4.16 shows the step response of the modified 3rd order system along with the simulation results from PLECS. It is seen that the reduced order system gives a more accurate prediction of the behavior of the response of the system compared with PLECS simulation results.

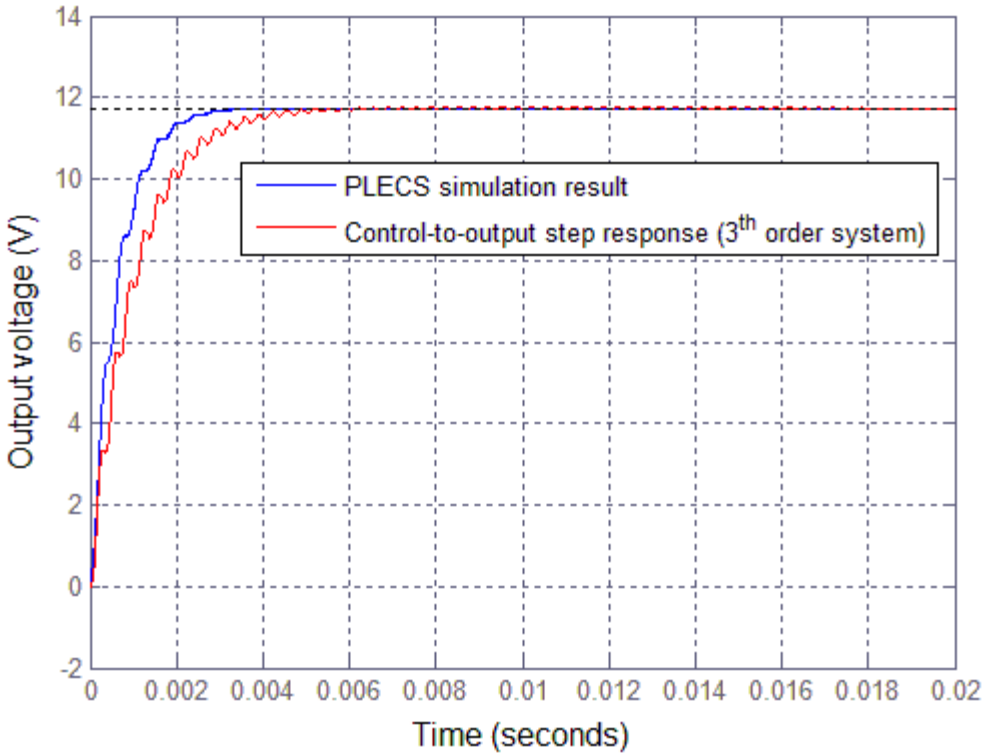


Figure 4.16: Comparing the step response of the 3rd order system in (4.100) with the PLECS simulation result (R_o=10 Ω, F=3, D=0.6).

4.5 Design of the Control Scheme

The objective of this section is to develop a closed-loop control scheme to control the output voltage of the converter in order to investigate the transient behavior of the converter. The control scheme should be simple and effective to control the duty ratio of the switching signals, in order to maintain a fixed and controllable voltage at the output with respect to a fixed reference voltage and in response to any changes in the output load or input voltage.

4.5.1 Single-Loop, Voltage-Feedback Control Scheme

The objective of the control scheme has been defined to keep the output voltage of the converter fixed during the operation and with respect to variations in the input signals of the converter. Since the output voltage of the converter is to be controlled by variation of the duty ratio, the voltage-feedback control technique used in conventional PWM DC-DC converters can be used for the proposed converter. Therefore, a single-loop, voltage-feedback control scheme is designed to feedback the output voltage in a closed-loop configuration and to establish the error signal with respect to the reference voltage. Figure 4.17 shows a simple closed-loop control scheme for output voltage regulation. It is observed that the output voltage of the converter is sampled as the feedback signal and the error of the system is passed through an integral block and finally the corrected duty ratio is fed to the converter to update the duty ratio of the switching signals.

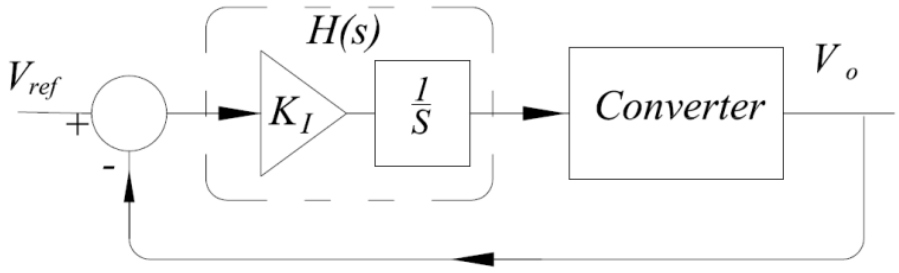


Figure 4.17: The single-loop, voltage-feedback control scheme to control the output voltage of the converter.

The coefficient of the integral block (K_I) determines the type of response of the system. Figure 4.18 shows the root locus of the compensated system. As the value of K_I increases, the real poles of the compensated system start to move closer to each other. The imaginary poles also start to move closer to the real axis. The locations of the real poles are more sensitive to the value of K_I. The first breakaway point ($K_{I\text{-}th}$) occurs on the real axis and is the threshold gain between the overdamped and underdamped response. Since this breakaway point occurs at s=-0.5/R_oC_o, the value of the threshold gain can be calculated as follows:

$$K_{I-th} = -s\frac{\hat{d}(s)}{\hat{v}_o(s)}\bigg|_{s=-\frac{0.5}{R_oC_o}} = \frac{(1-D)^2 F\Omega_r L_r}{2NV_d(B_1'a_1 - A_1'b_1)R_o^2C_o} \tag{4.101}$$

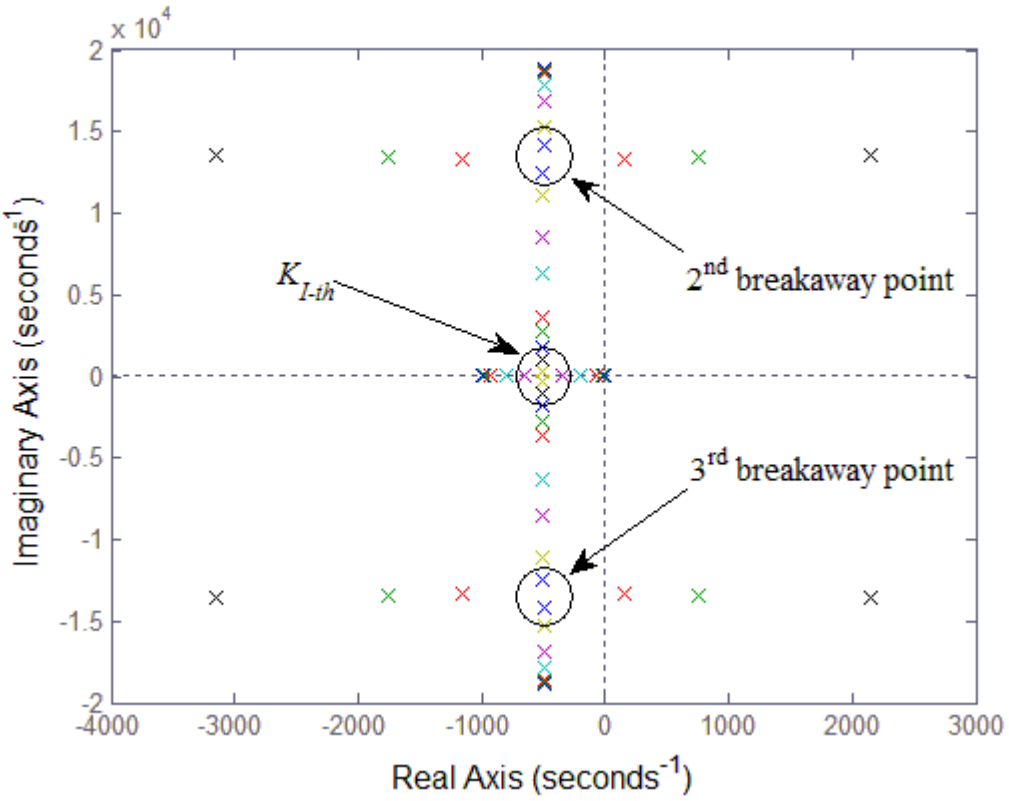


Figure 4.18: Root locus of the compensated control-to-output transfer function (R_o=10 Ω, F=3, D=0.6).

As K_I increases more than $K_{I\text{-}th}$, the response of the system becomes underdamped. It experiences significant overshoots and undershoots as a result of small tolerances in K_I close to the second and the third breakaway points. Increased values of K_I leads to the second and third breakaway points and promptly moves the poles of the compensated system to the right half plane, which makes the system unstable. Figure 4.19 shows the response of the system for overdamped, critically damped and underdamped cases.

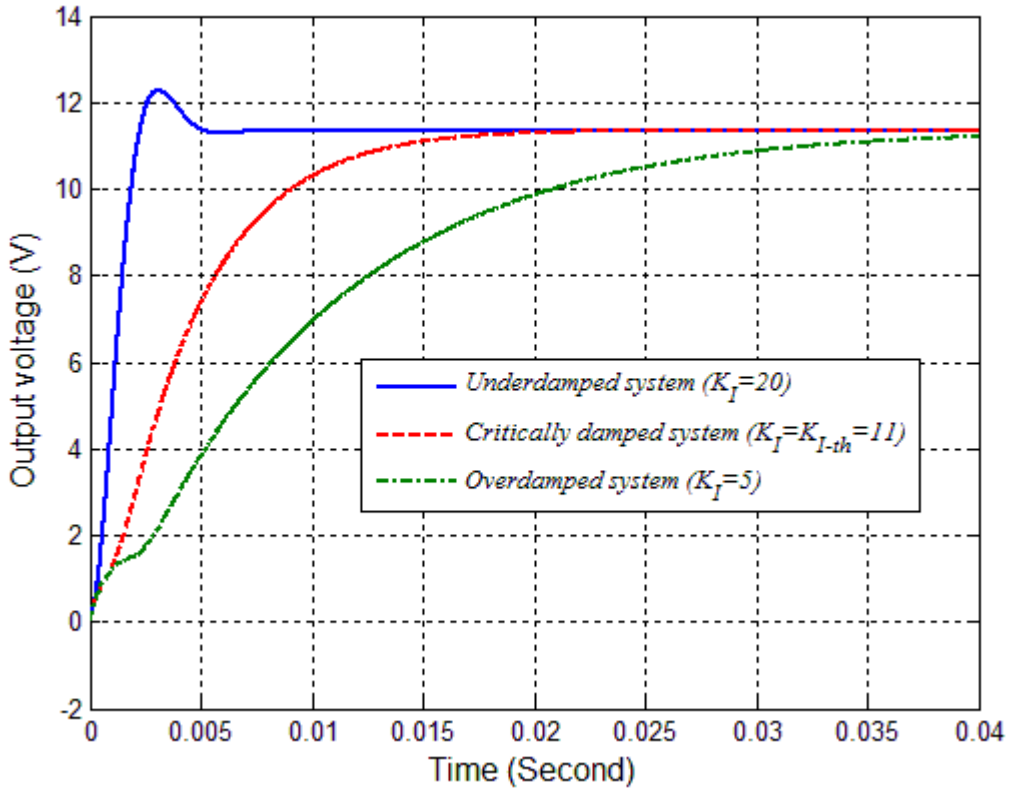
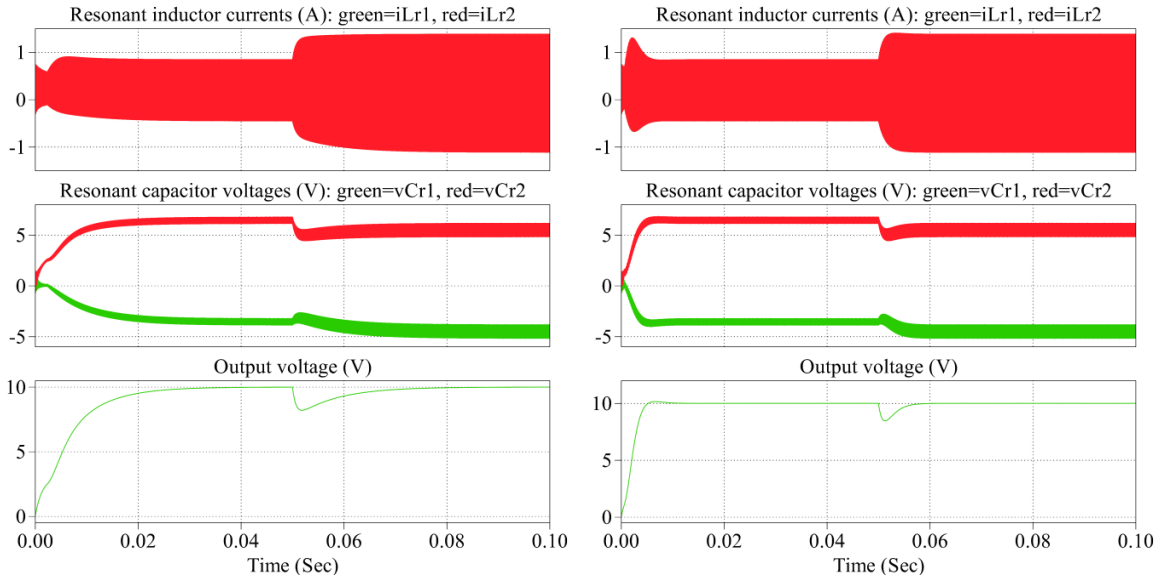


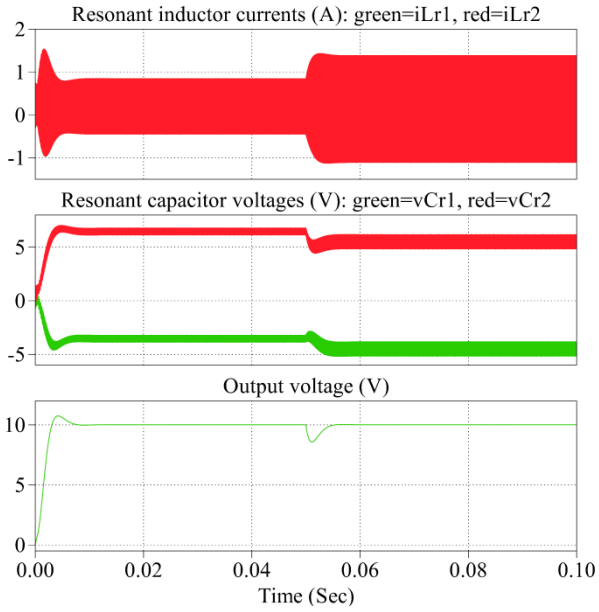
Figure 4.19: Overdamped, critically damped and underdamped responses in a closed-loop control scheme (R_o=10 Ω, F=3).

In order to examine the effect of the integral gain on the response of the system, simulations are carried out for two different cases: 1) a step change in the output load of the converter, and 2) a step change in the input voltage of the converter. Figure 4.20 shows the PLECS simulation results for the resonant inductor currents, resonant capacitor voltages, and the output voltage of the converter when the output load of the converter suddenly decreases by 50% from R_o=30Ω to R_o=15 Ω for three different types of response (i.e., overdamped, critically damped, and underdamped responses). It is seen that for all

three cases, the output voltage is regulated to 10 V after the change in the output load. Figure 4.21 shows the output voltage regulation for a step change in the input voltage from V_d=10 V to V_d=7 V. Again, it is noticed that for all three types of responses, the output voltage is regulated to 10 V after the change in the input voltage. In both case studies, it is observed that increasing the value of the integral gain reduces the damping ratio of the response as shown in Figure 4.18. The poles of the compensated system start to move away from the first breakaway point ($K_{I\text{-}th}$). This results in a faster system response and reduced settling time. In the vicinity of the $K_{I\text{-}th}$, the value of the damping ratio is not very sensitive to the value of the gain. Therefore, in order to avoid significant underdamped overshoots and undershoots, an integral gain with a value close to $K_{I\text{-}th}$ should be used.

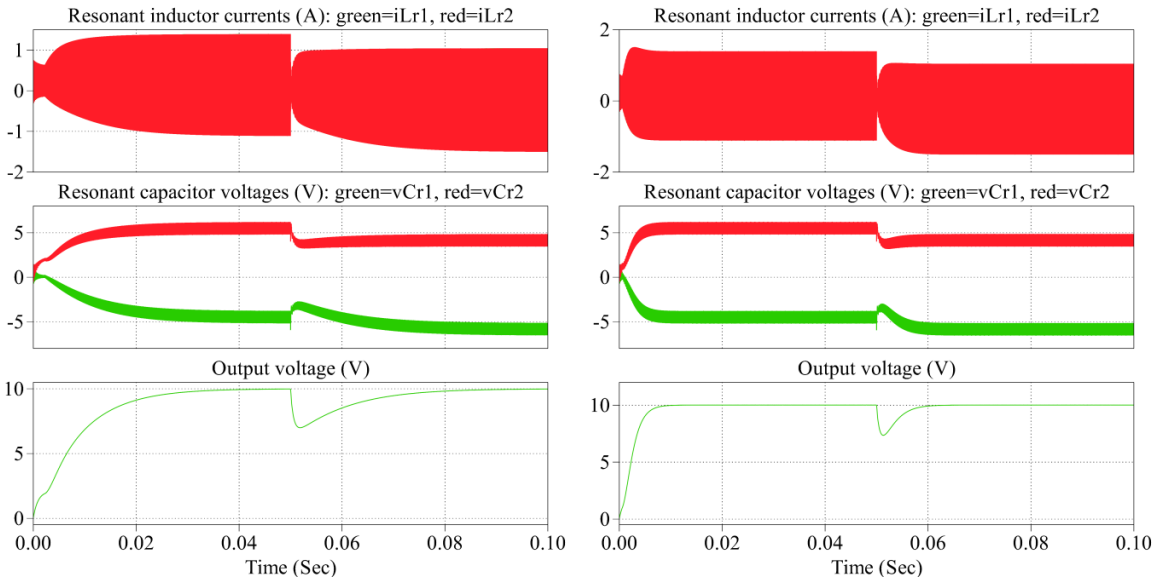


(a) (b)

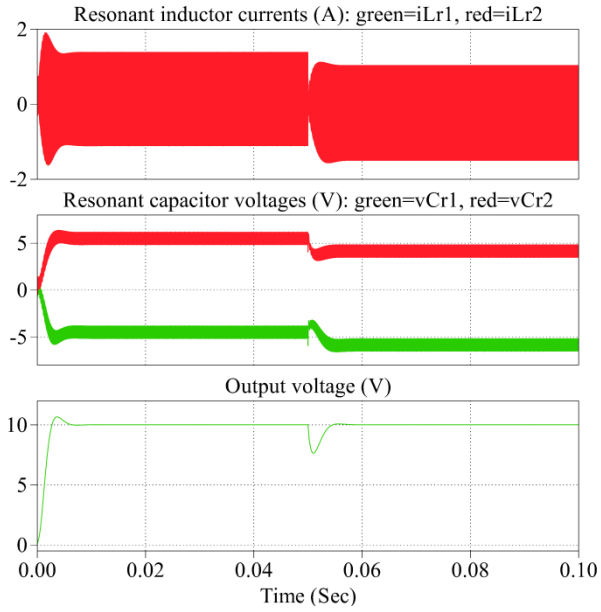


(c)

Figure 4.20: Step changes in the output load from R_o=30 Ω to R_o=15 Ω: a) overdamped response, b) critically damped response, and c) underdamped response.



(a) (b)



(c)

Figure 4.21: Step changes in the input voltage from V_d=10 V to V_d=7 V: a) overdamped response, b) critically damped response, and c) underdamped response.

4.6 Summary

This chapter investigated the analytical approach to model the converter and analyze the steady state and small signal operation of the proposed converter. The extended describing function was used as the modeling tool due to its significant advantages of providing an in-depth understanding of the operation of the converter and the effects of the components on the steady state and small signal operation of the converter. The analytical modeling approach yielded complete solutions of the steady state operation of the converter. It was observed that the output voltage of the converter can be changed through duty ratio of the switching signal and the switching frequency. A series of simulation-based investigations

were carried out to compare the results from the steady state analytical model with PLECS simulation results. It was demonstrated that the analytical model of the converter using the extended describing function approach was able to predict the output voltage of the converter accurately.

Small-signal models of the converter using the extended describing function approach were developed. Transfer functions of the output voltage of the converter with respect to small signal variation of input signals (input voltage, duty ratio, switching frequency, and output current) were developed. The duty ratio-to-output voltage transfer function was selected for the implementation of the control scheme. The 7^{th} order control-to-output transfer function was reduced to a 3^{rd} order model by removing the non-significant poles and zeros, which do not affect the response of the converter due to their occurrence at very high frequencies. An effective single-loop, voltage-feedback control scheme was then developed to control the output voltage with respect to a reference voltage. The performance of the closed-loop control of the converter was investigated for sudden step changes in the input voltage and the output load of the converter. Based on the simulation results the threshold gain of the controller was established, and the simple single-loop voltage-feedback control scheme was found effective for output voltage regulation when the converter is subjected to step changes in the input voltage and load resistor.

Chapter 5

Experimental Prototype of the Dual Series-Resonant DC-DC Converter

In Chapter 4, the implementation of the extended describing function approach for the proposed dual series-resonant DC-DC converter yielded a set of equations that describes the steady state and small signal operation of the converter. The accuracy of the developed analytical models was verified by comparing the modeling results in MATLAB with the simulation results in PLECS.

An experimental prototype of the proposed dual series-resonant DC-DC converter is constructed in order to examine the operation and features of the proposed converter. This chapter begins with the description of the components chosen to build a 40 W, 10 V experimental prototype. Based on the footprint of the selected components and the topology of the converter, a two-layer PCB is designed using Altium Designer [76] and populated to construct the experimental prototype. The performance of the prototype is examined in both open-loop and closed-loop configurations and the experimental results are presented. The ZVS operation of the switches and ZCS operation of the output diodes are experimentally verified and the improvement in the power transfer capabilities of the proposed dual series-resonant converter and the efficiency of the conversion are examined and compared with the traditional single-series resonant topology.

5.1 Selection of the Components

- *Switching devices*: The operation of the proposed dual series-resonant converter needs to be investigated over a wide range of switching frequency. For this purpose, MOSFETs are used as the switching devices due to their suitable performance at high switching frequencies. For this experimental prototype, 200V, 32A Infineon MOSFET IPP320N20N3 G is selected due to its relatively low gate charge (Q_{gs} = 8 nC, Q_{gd} = 3 nC, Q_{sw}= 5 nC, and Q_g= 22 nC) compared with other MOSFETs with the same rating [77].

  Planar Transformer: The planar transformer is required to operate reliably over a wide range of switching frequency (between 100 kHz and 700 kHz). It must have at least two identical separate windings on the secondary side of the transformer, and

the voltage rating of the windings needs to be high enough for the maximum possible voltage at the primary side of the transformer, which depends on the duty ratio of the PWM switching signal and the input voltage as stated in (5.1).

$$V_p = V_d + V_{Cc} = \frac{V_d}{1-D} \tag{5.1}$$

The chosen transformer is the Midcom 750341142 from Wurth Electronics, which has a turns ratio, N=1. Figure 5.1 shows the winding configuration of this transformer [78].

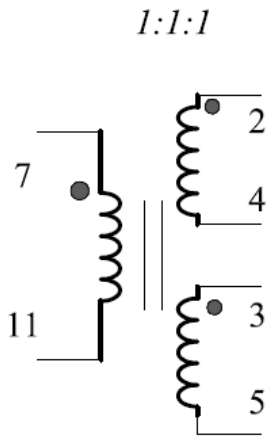


Figure 5.1: Winding configuration of Midcom 750341142 planar transformer.

- *Voltage Transducer*: In a closed-loop configuration, the output voltage needs to be measured as the feedback signal for the purpose of voltage regulation. The chosen voltage transducer is LV25-P from LEM due to its excellent accuracy and low response time [79]. Figure 5.2 shows the configuration of the transducer. As stated in the datasheet of the transducer, resistor R_1 should be

high enough to limit the primary current of the transducer to 10mA. Since the maximum voltage level for analog ports of most of the controller platforms is +5 V, the measured voltage of the transducer needs to be scaled down enough to a value less than +5 V in order to avoid damage to the controller. The combination of R_1 = 3300 Ω and R_M = 100 Ω are chosen that limits the primary current to 10 mA and scales down the measured output voltage with a factor of K=14, which keeps the feedback voltage to the controller between 0V and 5V as the output voltage of the converter varies up to 70V.

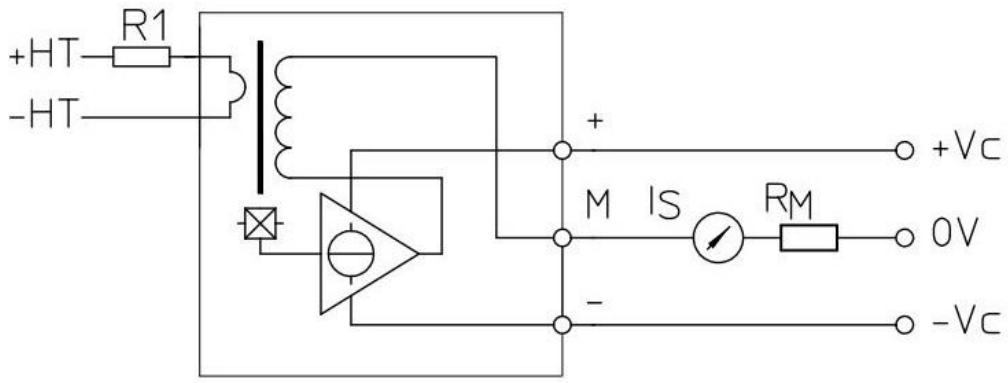


Figure 5.2: Configuration of the voltage transducer LEM LV25-P [79].

- *MOSFET Driver and Driver Circuitry*: The MOSFET driver chip is the 200V, IRS2011PBF device from International Rectifier (currently Infineon) [80]. Figure 5.3 shows the MOSFET drive circuitry, in which the capacitors, resistors, and diode of the drive circuitry are shown. Pins named as *HI* and *LI* are the input pins of the driver and are connected to the gate signal generator.

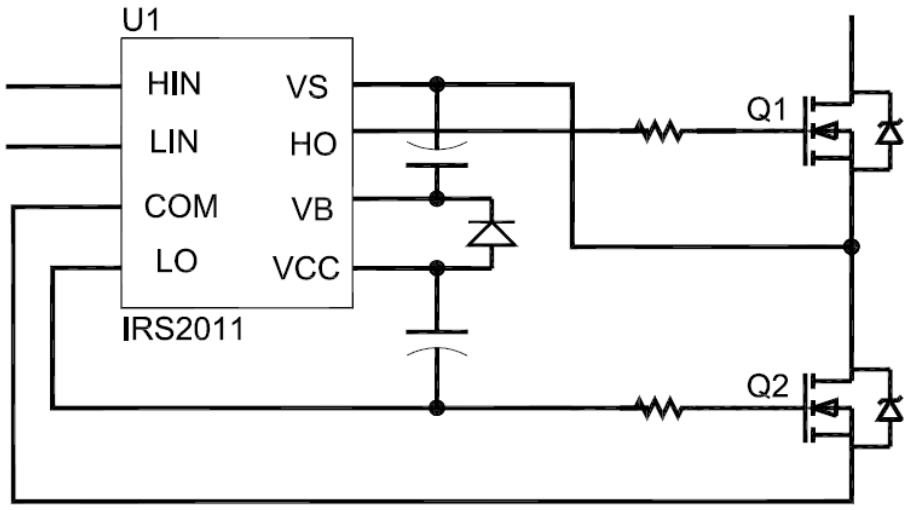


Figure 5.3: IRS2011PBF MOSFET driver wiring diagram [80].

- *Controller Platform*: PSoC 5LP from Cypress development kit [81] is selected as the controller platform to generate the gate signals of the MOSFET driver. PSoC 5LP development kit is equipped with CY8C5868AXI 32-bit ARM Cortex-M3 CPU core with digital and analog peripheral in a single chip. With two dedicated 12-bit 1000ksps SAR ADC, this platform offers precise and fast signal acquisition, signal processing, and control. The PSoC Creator Integrated Design Environment (IDE) programming tool, in which the components in its library (such as ADCs, PWM blocks, Clock blocks, etc.) can be set in a graphical user interface (GUI) is used to configure and program analog and digital peripherals of the PSoC device. A complete list of application programming interface (API) is available to change and modify the settings of all components in C language [82]. Figure 5.4 shows the development kit.

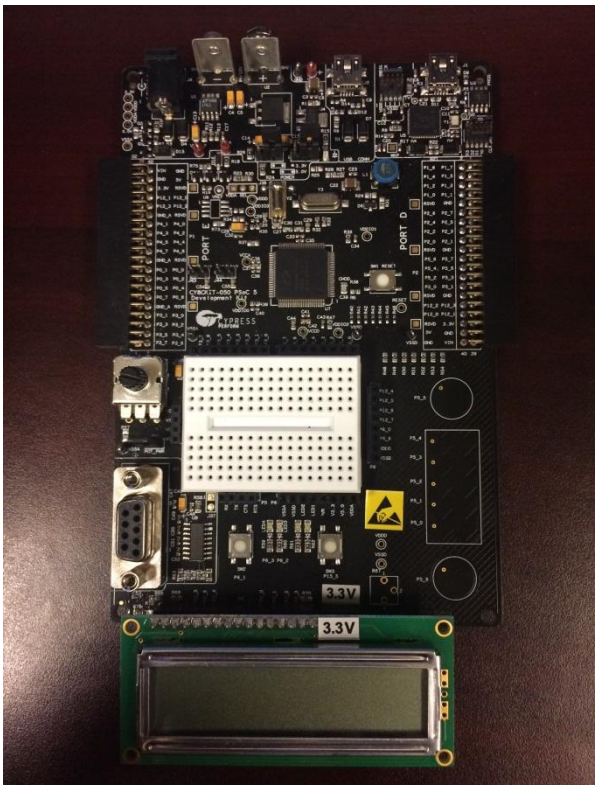


Figure 5.4: PSoC 5LP development kit.

- *Output Diodes*: The output diodes are RF2001T4S from ROHM, which are suitable for very fast switching applications with 30 nSec reverse recovery time [83].

The list of all the components and part number and/or values is listed in Table 5.1. Figure 5.5 shows the overall implementation of the prototype in Altium Designer.

Table 5.1: Parameters of the experimental prototype.

Parameter	***Part No. / Value***
MOSFET switches	IPP320N20N3
Transformer	Wurth Electronics Midcom 750341142 (L_m = 70 µH, N =1)
Output diodes	RF2001T4S
Driver and bootstrap circuit	IRS2011
Voltage transducer	LV 25-P
Series resonant circuit (L_{r1} –C_{r1})	C_{r1}=1 µF - L_{r1}=4 µH
Series resonant circuit (L_{r2} –C_{r2})	C_{r2}=1 µF - L_{r2}=4 µH
Output capacitor	100 µF
Clamping capacitor (C_c)	10 µF
Gate signal generator	PSoC 5LP

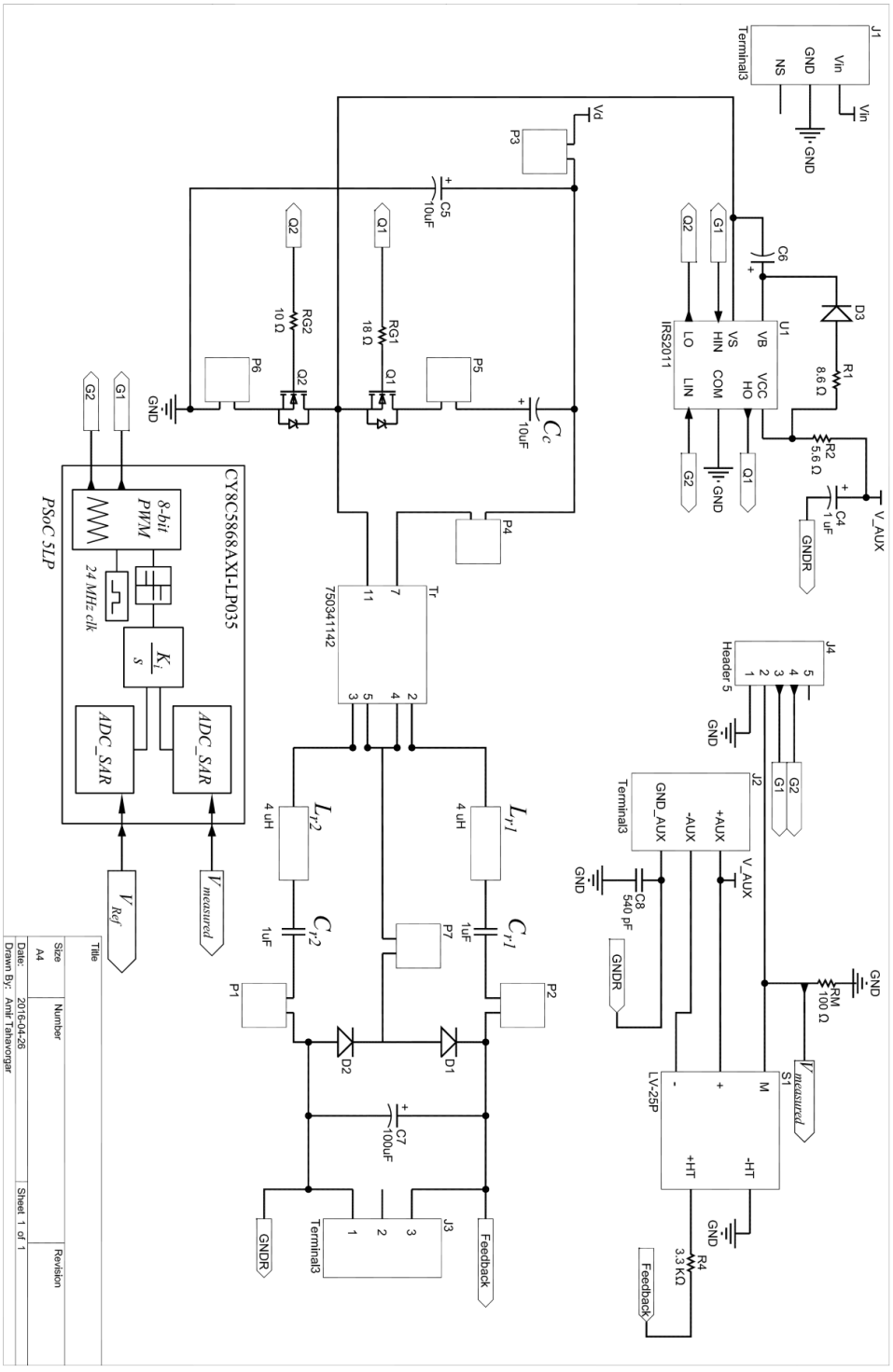


Figure 5.5: The layout of the prototype dual series-resonant DC-DC converter in Altium Designer.

As shown in Figure 5.5, the detailed topology consists of four terminals identified as follows:

- J1 is the input of the converter, which is connected to the input voltage source;
- J2 is the auxiliary voltages terminal for the MOSFET driver and the voltage transducer;
- J3 is the output of the converter, which is connected to the load; and
- J4 is the signaling terminal, which is connected to the controller platform.

The implemented topology consists of several shunt jumpers, identified as P in Figure 5.5. Currents are measured by replacing the shunt jumper with the current probe amplifier.

Figure 5.6 shows the designed two-layer PCB in Altium Designer. The size of the board is 1100 mm × 1000 mm. The copper tracks on the top and bottom layers are shown with red and blue colors, respectively. Figure 5.7 shows the picture of the populated PCB, and Figure 5.8 is the image of the prototype and the experimental set up of the converter showing the instrumentations used in the experimental measurements.

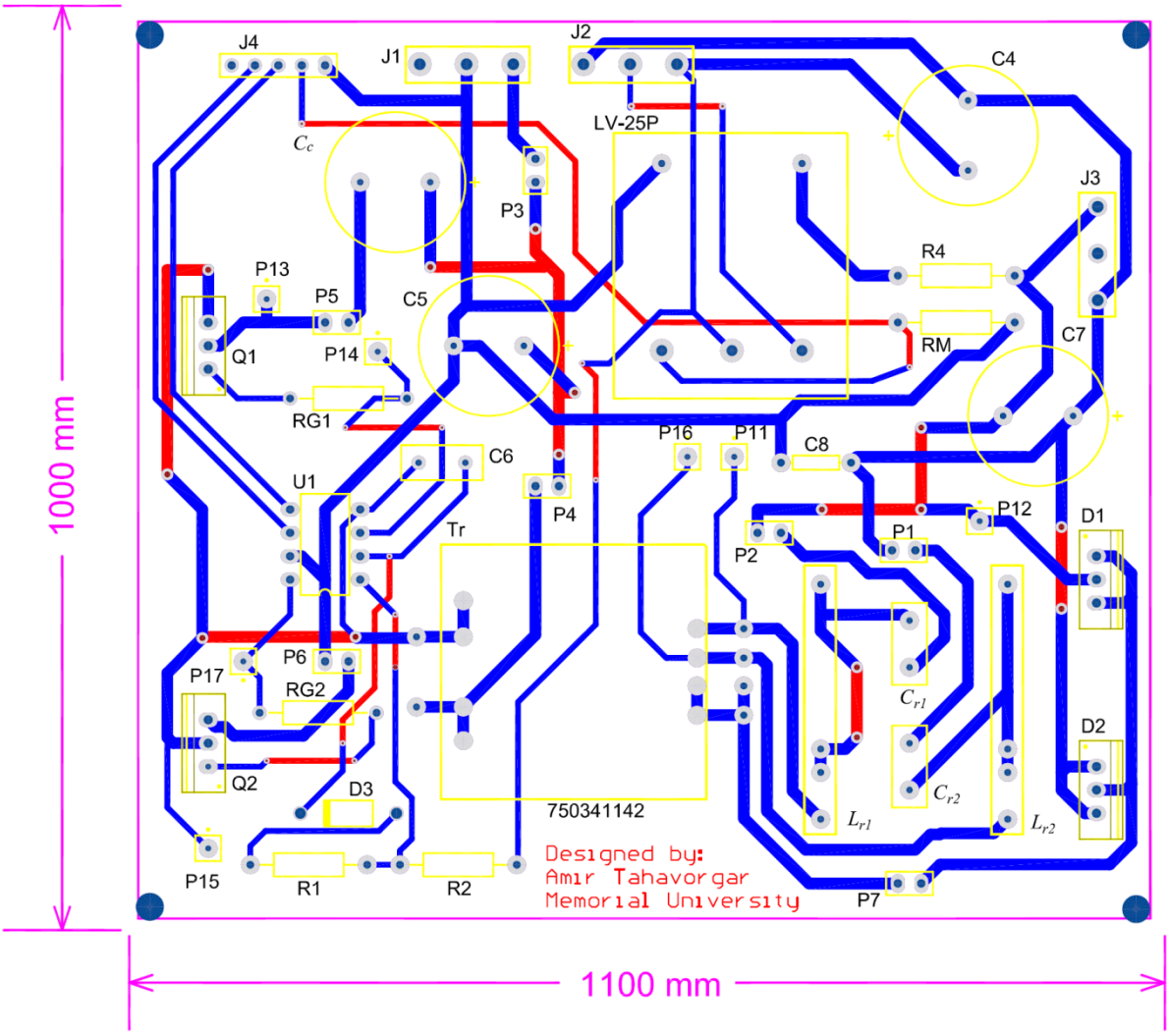
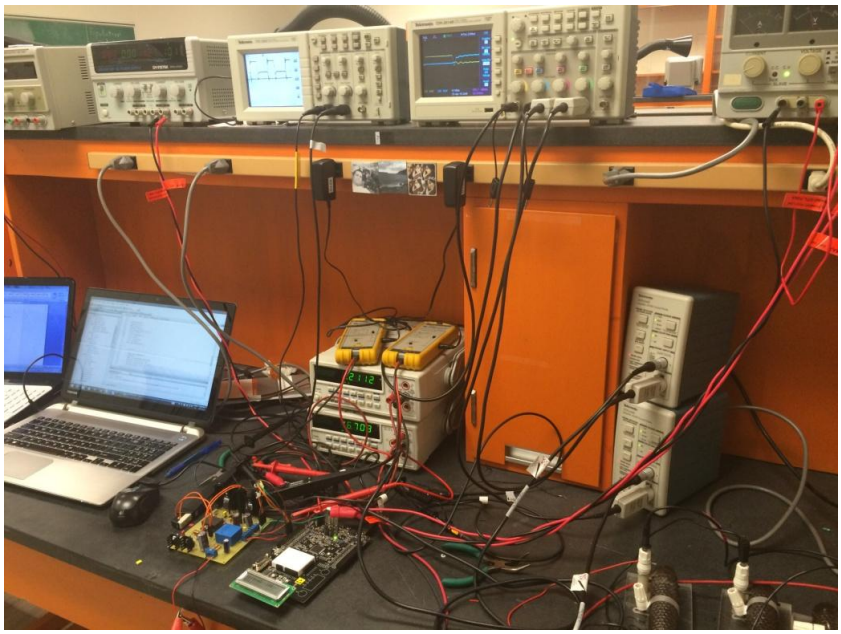


Figure 5.6: Designed PCB in Altium Designer environment.

(a)



(b)

Figure 5.7: a) Prototype of the proposed dual series-resonant DC-DC converter, b) experimental setup.

5.2 Open-Loop Operation - Experimental Results

For open-loop operation, the voltage transducer is bypassed and the gate signals are generated by PSoC 5LP, regardless of the measured output voltage by the transducer. An 8-bit PWM block in PSoC 5LP is used to generate the PWM signal. Figure 5.8 shows the schematic configuration of the PSoC Creator that is implemented for the open-loop operation. The experimental waveforms for the open-loop experiment are obtained for the following operating conditions:

V_d=10V, f_{sw}=240 kHz (F=3), and R_o=30Ω. Next, the experimental results of the six case studies listed in Table 4.1 are compared with the simulation and analytical modeling results.

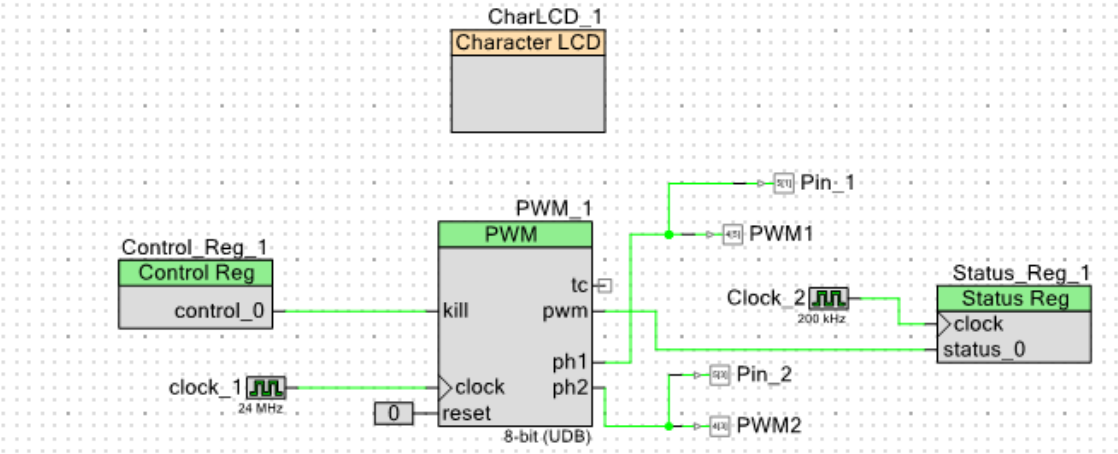


Figure 5.8: Schematic configuration of the PSoC Creator for the open-loop experiment.

The gate signals of the PSoC 5LP are shown in Figure 5.9. In PSoC 5LP, two shunt jumpers set the level of the output rail voltage. Depending on the position of the jumpers,

the output voltage rail is either 5V or 3.3V. For this experiment, the PSoC 5LP settings are adjusted to generate 5 V as the high-level voltage on the output rail. Figure 5.10 shows the measured gate-to-source voltages of the MOSFETs.

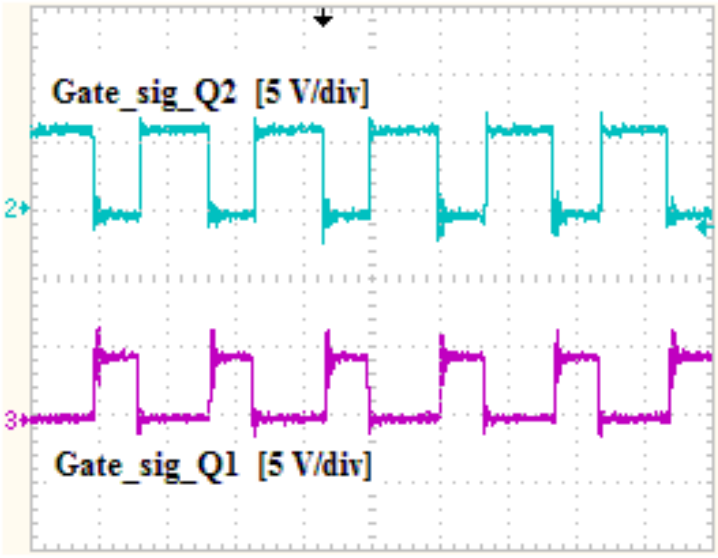


Figure 5.9: Gate signals for the MOSFET driver.

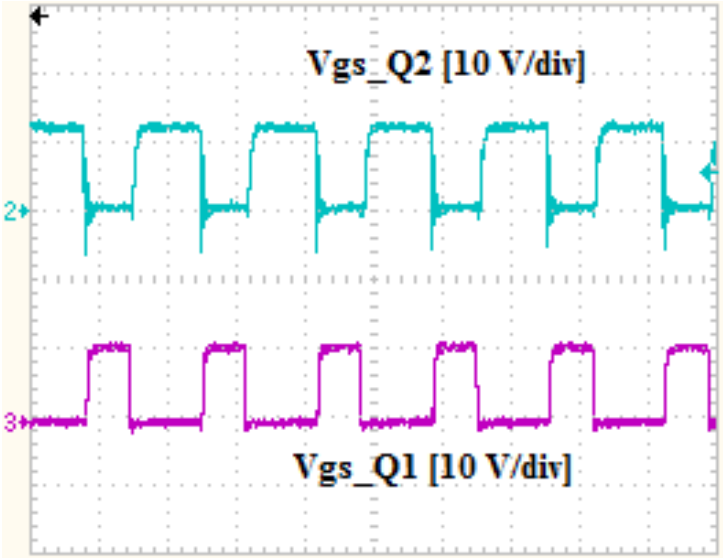
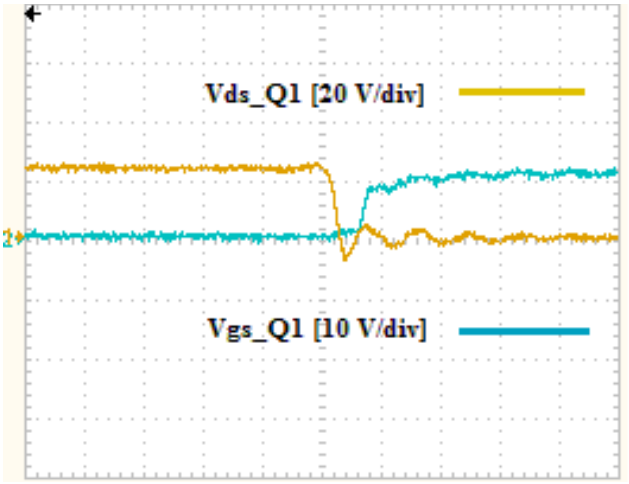
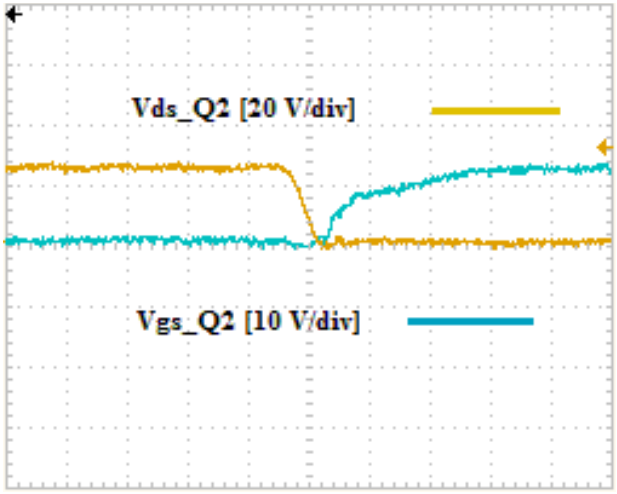


Figure 5.10: Experimental results of the gate-to-source voltages of the MOSFETs.

Figure 5.11 shows the zoom-in snapshots of the gate-to-source and drain-to-source voltages for *Q1* and *Q2* during turn-on transition to observe the ZVS turn-on condition of the MOSFETs. For both *Q1* and *Q2*, the drain-to-source voltages reach zero before the turn-on commands of *Vgs-Q1* and *Vgs-Q2* are applied to the MOSFETs. This fact verifies the ZVS operation of the MOSFETs.



(a)



(b)

Figure 5.11: ZVS turn-on operation of the MOSFETs: a) ZVS turn-on of *Q1*, b) ZVS turn-on of *Q2*.

According to the simulation and analytical results presented in the previous chapters, the resonant inductor currents are equal. This observation is confirmed in the experimental results of the resonant inductor currents shown in Figure 5.12. In the experimental setup, the dual series-resonant circuits are not identical. The mismatch in the values of the components (L_{r1} vs. L_{r2} and C_{r1} vs. C_{r2}), causes the experimental results of the resonant inductor currents not to be completely equal. However, it is noticed that the mismatches between the resonant components is very small and negligible. Figure 5.13 shows the zoom-in snapshots of the encircled areas (i.e., Area 1 and Area 2) of the resonant inductor currents shown in Figure 5.12, illustrating the variance in the resonant inductor currents. It is observed that the differences in the resonant inductor currents are very small and negligible. While the variance in the resonant inductor currents depends on the degree of mismatch, it can be concluded that within the design tolerance limits of the resonant components, the variation in the characteristics of the series-resonant circuits would not have significant effects on the operation of the converter.

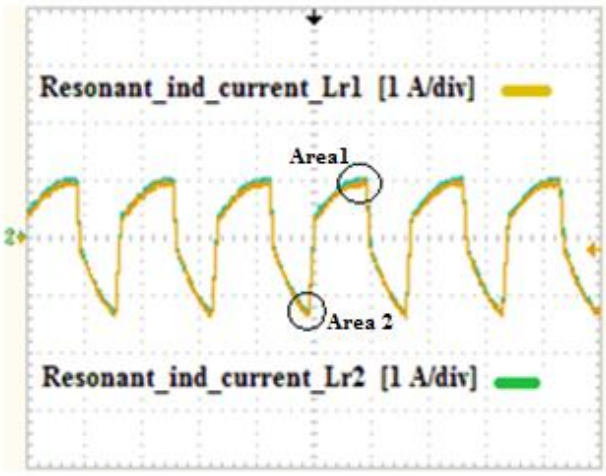


Figure 5.12: Experimental results of the resonant inductor currents.

(a) (b)

Figure 5.13: Effect of the mismatches between resonant components: a) Area 1 in Figure 5.12, b) Area 2 in Figure 5.12.

The results of the resonant capacitor voltages are shown in Figure 5.14. The small spikes on the resonant capacitor voltages are due to the switching actions. Finally, Figure 5.15 shows the PLECS and experimental results of the output voltage.

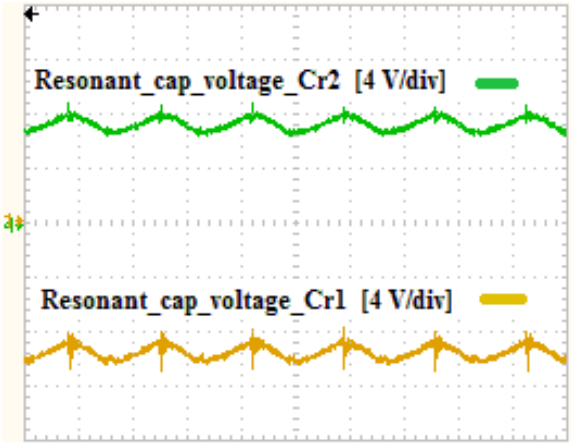


Figure 5.14: Experimental results of the resonant capacitor voltages.

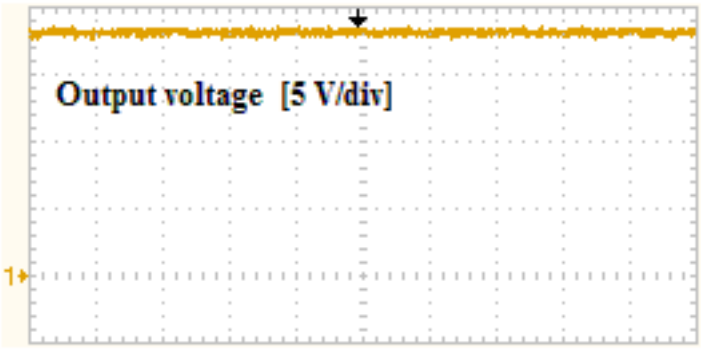


Figure 5.15: Experimental results of the output voltage.

The DC voltage conversion ratio of the converter is examined over a wide range of duty ratio and switching frequency and Figure 5.16 shows the experimental results of the voltage conversion ratio. The switching frequency of the PWM signals is set to four different values (i.e., 160 kHz, 240 kHz, 480 kHz, and 640 kHz, similar to the conditions simulated in Fig. 4.9) in by changing the time period of the 8-bit PWM block using the APIs in the PSoC Creator and keeping the clock frequency fixed at 24 MHz. For each value of the switching frequencies, the duty ratio of the PWM switching signal is varied between D=0.2 and D=0.8.

The experimentally measured voltage conversion ratio of the prototype is very close to the PLECS and modelling results shown in Figure 4.9. The DC voltage conversion ratio of the converter varies with respect to the duty ratio and the switching frequency of the PWM switching signal. Higher values of conversion ratio are achievable by reducing the switching frequency and increasing the duty ratio of the PWM switching signal. It is worth noting that the turns ratio of the transformer of the experimental prototype is N=1. A higher value of turns ratio would provide higher output voltage.

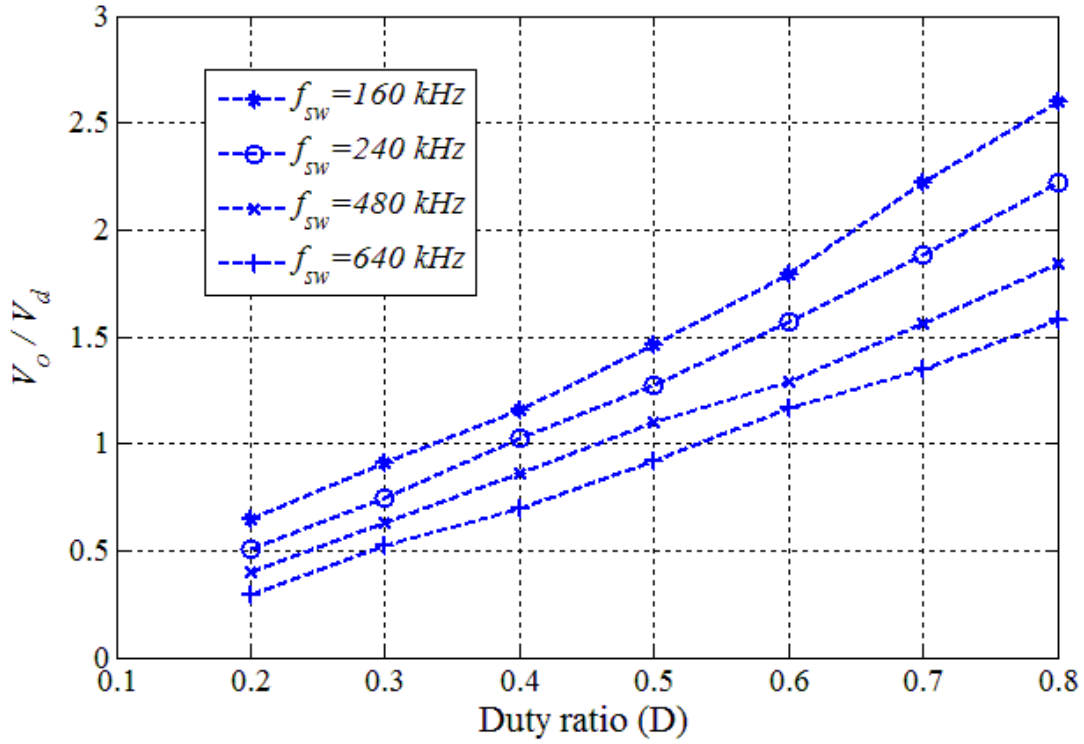


Figure 5.16: Experimental results of voltage transfer ratio versus duty ratio for different switching frequencies (V_d=10 V, R_o=30 Ω).

Table 5.2 lists the experimental results, modeling analytical results, and PLECS simulation results for six different case studies in accordance to the comparisons given in Table 4.1 in Chapter 4. It is demonstrated that the experimental results are in good agreement with the analytical and PLECS results. It is observed that the simulation results from PLECS are closer to the experimental results than the analytical results. This fact is expected due to the approximations made in the implementation of the extended describing function. In general, the simulation, experimental, and analytical results show the same trend, and the discrepancies in the results are within ± 13%.

Table 5.2: Comparison between PLECS simulation, analytical modeling, and experimental results

	$I_{1FLr1} = I_{1FLr1}$ [A]			V_{Cr1} [V]			V_{Cr2} [V]			V_o [V]		
	PLECS Results	Analytical Results	Experimental Results	PLECS Results	Analytical Results	Experimental Results	PLECS Results	Analytical Results	Experimental Results	PLECS Results	Analytical Results	Experimental Results
Case study I f_{sw}=240 kHz, D=0.3, R_o=30 Ω	0.43	0.46	0.47	-2.72	-2.76	-2.95	6.14	5.83	6.05	8.84	8.60	8.82
Case study II f_{sw}=240 kHz, D=0.6, R_o=30 Ω	0.90	0.82	0.94	-10.5	-10.8	-10.30	7.40	7.50	7.35	17.9	18.3	17.1
Case study III f_{sw}=320 kHz, D=0.6, R_o=30 Ω	0.82	0.79	0.89	-9.45	-10.6	-9.80	6.81	7.54	6.97	16.2	18.2	16.1
Case study IV f_{sw}=480 kHz, D=0.6, R_o=30 Ω	0.71	0.70	0.81	-7.86	-8.90	-8.13	5.86	6.40	6.05	13.7	15.3	13.7
Case study V f_{sw}=240 kHz, D=0.4, R_o=30 Ω	0.58	0.61	0.54	-4.66	-4.58	-4.81	6.80	6.51	6.73	11.5	11.1	11.2
Case study VI f_{sw}=240 kHz, D=0.4, R_o=15 Ω	0.95	0.90	0.89	-3.88	-3.46	-3.85	5.33	4.83	4.98	9.21	8.30	8.53

The performance of the circuit is compared with the traditional single series-resonant circuit. The topology of the single series-resonant converter can be realized by removing one of the shunt jumpers (either P1 or P2 in Figure 5.5) that is in series with the series-resonant circuits. Due to the balance operation of the series resonant circuits, removing P1 or P2 both result in identical single series-resonant converters. For this experiment, the shunt jumper P2 in series with the L_{r2} and C_{r2} is removed.

Figure 5.17 compares the output power transfer between the dual series-resonant resonant converter and the traditional single series-resonant converter. As expected, the continuous transfer of power to the output load in the dual series-resonant circuit converter, results in increased power transfer capability of the proposed converter over the whole range of duty ratio of the PWM switching signal. This figure shows that the power transferred by the dual series-resonant converter is 40%-60% higher compared to the single series-resonant converter. In addition, since the second series resonant circuit (L_{r2}-C_{r2}) takes only 5% of the PCB area, the power density of the dual series-resonant converter compared with the single series-resonant converter is improved.

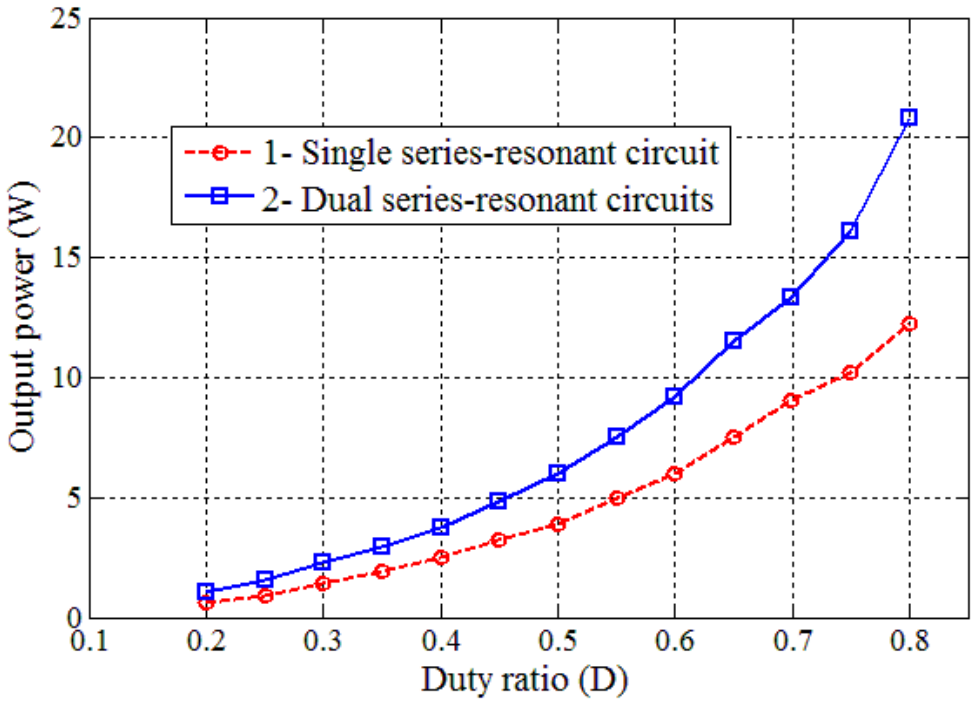


Figure 5.17: Experimental comparison of transferred power between two topologies: 1- proposed dual series-resonant circuits, 2- single series-resonant circuit.

In addition to the improvement in the power density of the converter, the manufacturing cost of the proposed dual series resonant converter is expected to be reduced. For the single series-resonant converter (red line in Figure 5.17) in order to achieve the same level of output power transfer as the dual series-resonant converter (blue line in Figure 5.17), a two-stage interleaved topology of the single series-resonant converter needs to be implemented which requires twice the number of passive and active components. However, the proposed dual series-resonant topology increases the output power transfer by adding a second series-resonant circuit and replacing the two transformers in the interleaved topology with a transformer that has two identical windings at its output.

The efficiency of the proposed dual series-resonant converter versus duty ratio at two different switching frequencies (i.e. 240 kHz and 400 kHz) is examined. Figure 5.18 shows the results of the comparison between the efficiencies of the proposed converter and the traditional single series-resonant converter. The improvement in the overall efficiency in the proposed dual series-resonant DC-DC converter over the whole range of duty cycle variation for both cases of switching frequencies is demonstrated. For the same value of inductor current, the proposed dual series-resonant converter generates higher voltage at the output compared with the single series-resonant circuit topology. Consequently, the output power of the dual series-resonant converter is higher for the same level of conduction losses. Hence, the efficiency of the proposed dual series-resonant DC-DC converter is improved.

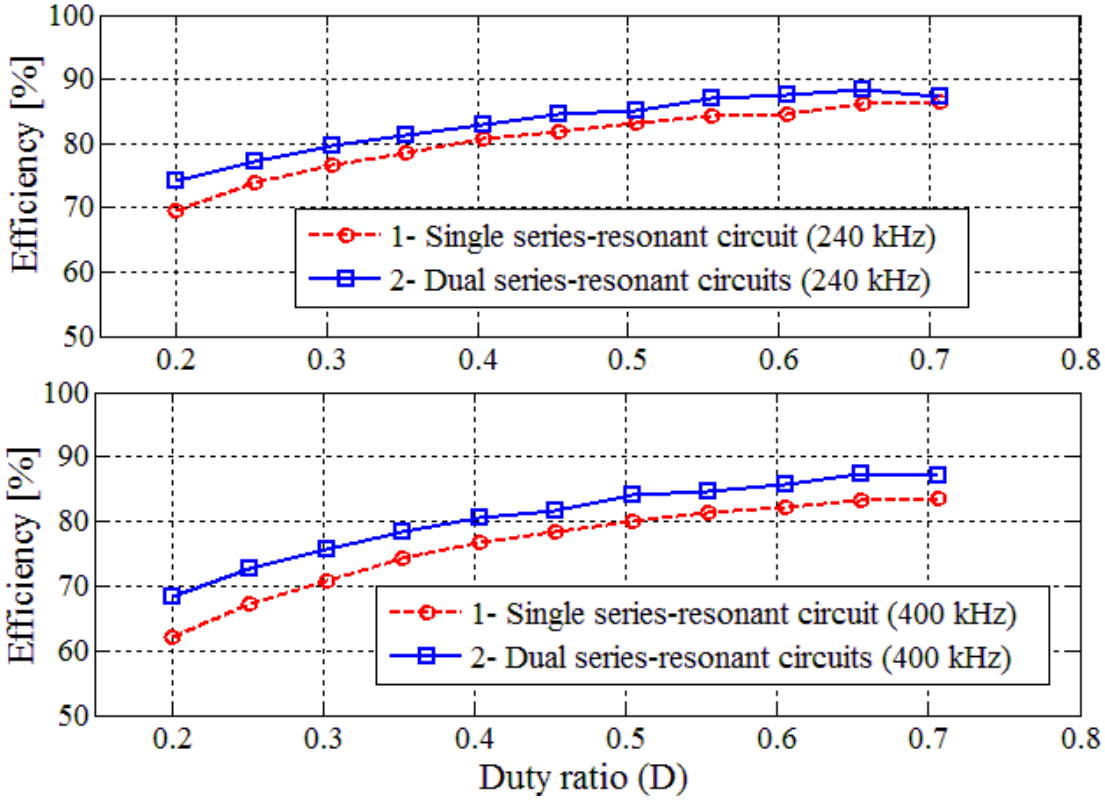


Figure 5.18: Experimental comparison of efficiencies between two topologies:

1- dual series-resonant circuits, 2- single series-resonant circuit.

5.3 Closed-Loop Operation

The objective of the closed-loop experiment is to demonstrate the regulation of the output voltage in the case of variation in the output load. For this purpose, the single-loop output-voltage feedback control scheme, which was developed in Chapter 4 based on the simplified model of the control-to-output transfer function, is implemented using PSoC 5LP. This closed loop control scheme updates the duty ratio of the PWM switching signals according to the operating condition of the converter and keeps the output voltage equal to the reference voltage.

5.3.1 Implementation of the Closed Loop System

For closed-loop operation of the proposed converter, two 8-bit successive approximation register (SAR) ADCs with 1 MHz external clock are added for implementation on PSoC 5LP to convert the analog signals (i.e., reference voltage and measured output voltage) to digital signals. Figure 5.19 shows the schematic configuration of the closed-loop control implementation in PSoC Creator environment. The output of the PWM block is a 5 V pulse, in which the duty ratio is updated in an infinite loop. The integral controller is implemented through the available APIs in the PSoC Creator and in C language.

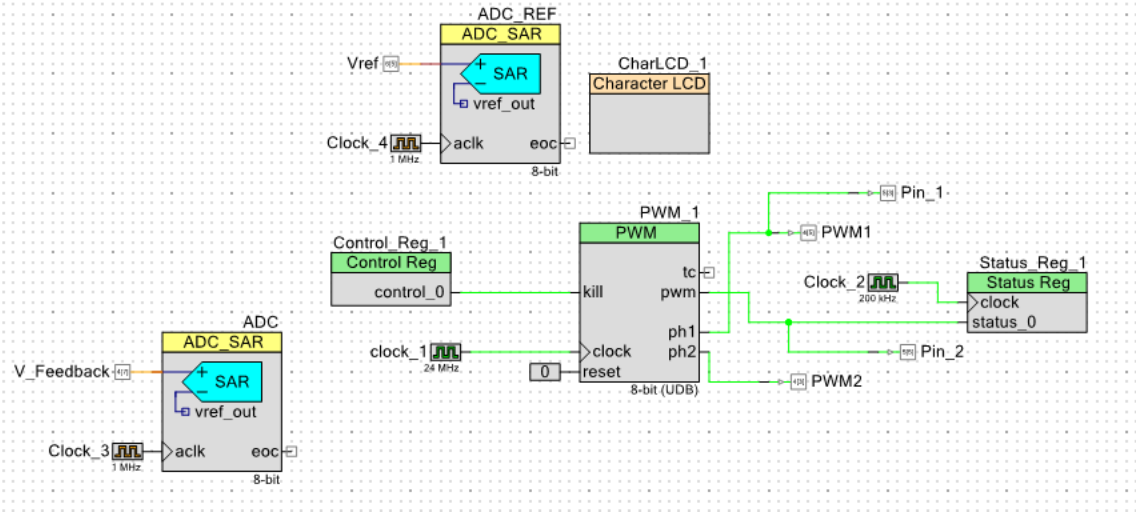


Figure 5.19: Schematic configuration of the PSoC Creator for the closed-loop experiment.

5.3.2 Closed-Loop Operation - Experimental Results

Figure 5.20 and Figure 5.21 show the simulation and experimental results of the state-plane trajectory of the state-space variables (i.e., i_{Lr} and v_{Cr}), respectively, when the output load is subjected to 50% change. Since the operation of the two resonant circuits is identical, Figure 5.20 represents the state-plane trajectory of both resonant circuits. It is observed that the simulation and experimental results follow the same trajectory pattern when *Q1* and *Q2* are conducting. Figure 5.22 and Figure 5.23 show the associated experimental results of v_o, i_{Lr} and v_{Cr} under the same variation in the output load. It is observed that the output voltage remains constant when the output load varies. A small ringing is observed in the capacitor voltage during the transition in currents between the two MOSFETs when the anti-parallel diodes (D_{Q1} and D_{Q2}) are conducting. This explains why during these modes the trajectories are not clearly detectible in the experimental plots of the state-plane trajectory.

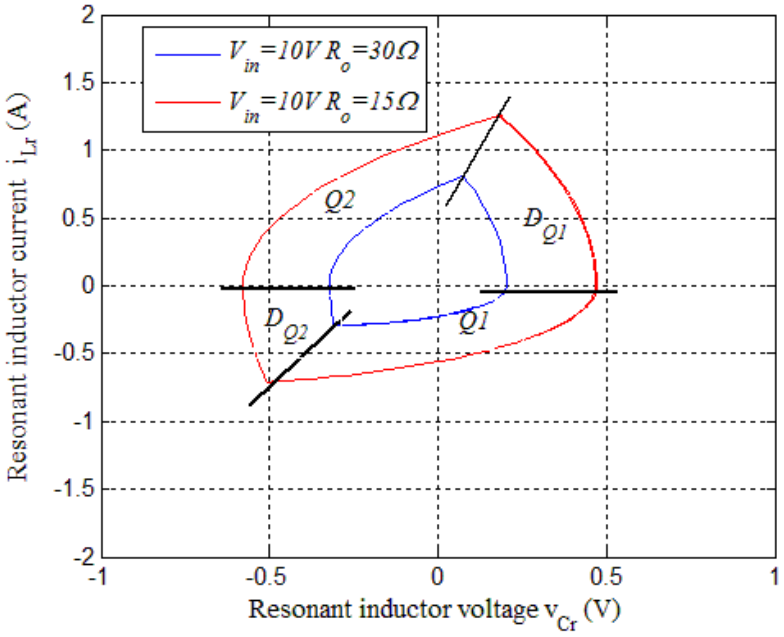


Figure 5.20: Simulation results of the state-plane trajectory for sudden change in the output load from R_o=30Ω to R_o =15Ω.

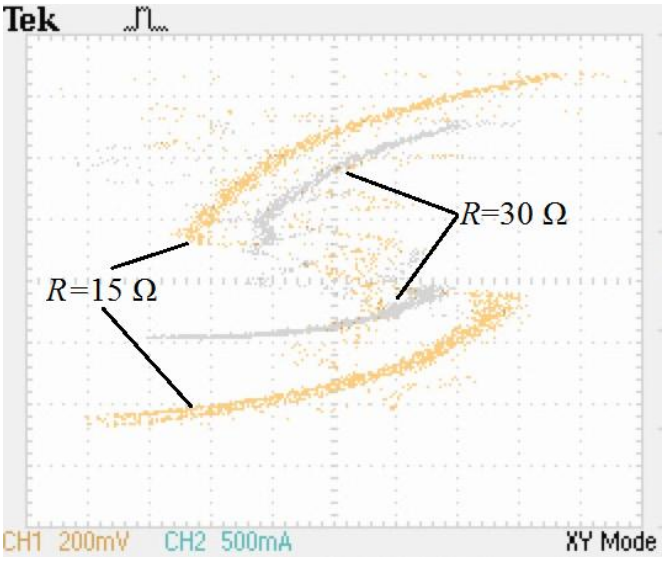


Figure 5.21: Experimental results of the state-plane trajectory for sudden change in the output load from R_o=30Ω to R_o =15Ω.

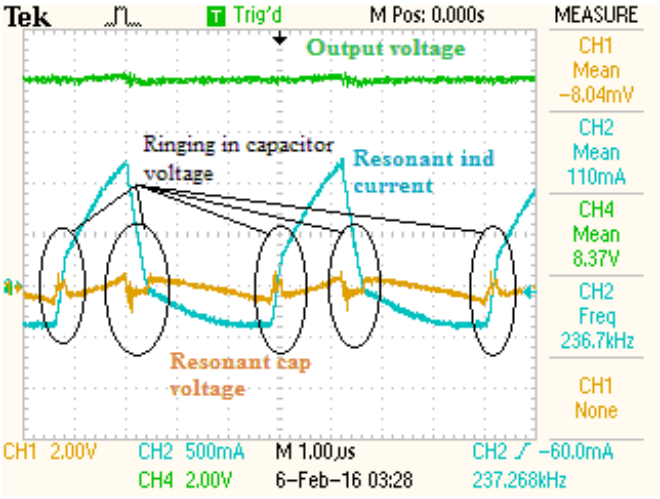


Figure 5.22: Experimental results of v_o, i_{Lr} and v_{Cr} - R_o= 30Ω.

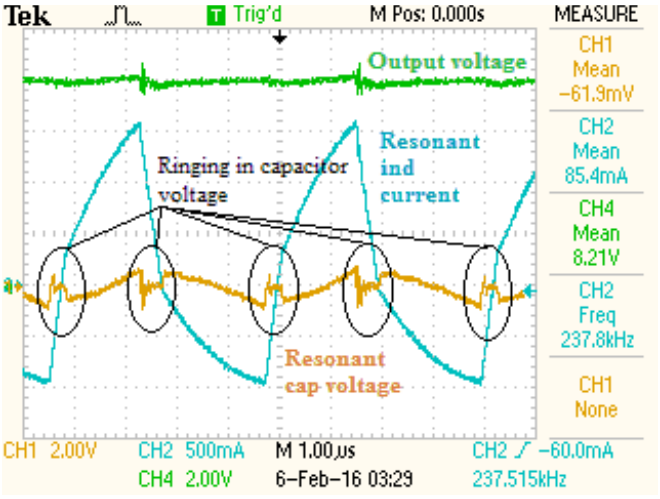


Figure 5.23: Experimental results of v_o, i_{Lr} and v_{Cr} - R_o= 15Ω.

The effect of the integral gain on the recovery of the output voltage in the case of a sudden change in the output load is investigated experimentally. The results are shown in Figure 5.24 and 5.25 for two scenarios of increase and decrease in the output load and for different values of integral gain. It can be seen from figures that increasing the value of the integral gain does not affect the percentage of the overshoots or undershoots; however, it

does affect the settling time of the output voltage. It is realized that by increasing the integral gain, the undershoot (for the scenario of increase in the output load) and the overshoot (for the scenario of decrease in the output load) of the output voltage remain unaffected; however, the settling time of the voltage reduces for both scenarios and the output voltage recovery to the reference voltage becomes faster. It is observed in Figure 5.25 (c) that the response of the system exhibits underdamped behavior for step change in output load from R_o=15 Ω to R_o=30 Ω.

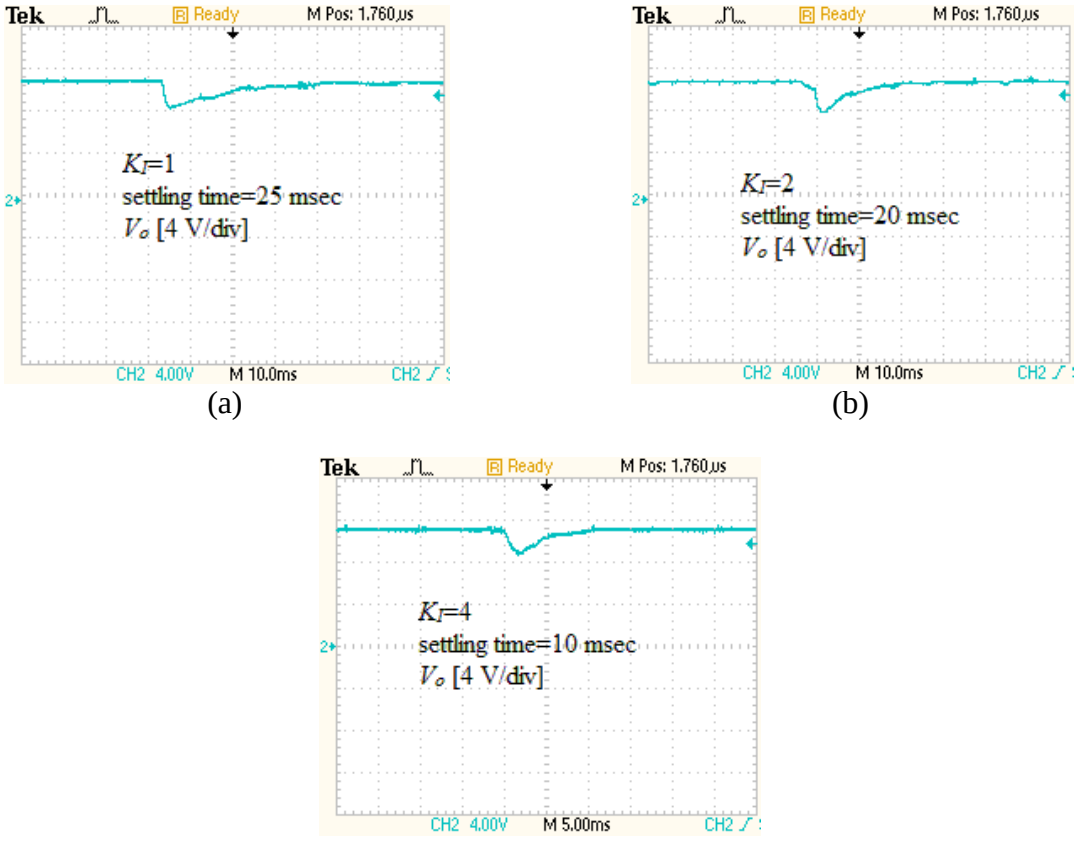


Figure 5.24: Effect of the integral gain on the voltage recovery characteristics of the converter for step change in the output load from R_o=30 Ω to R_o=15 Ω.

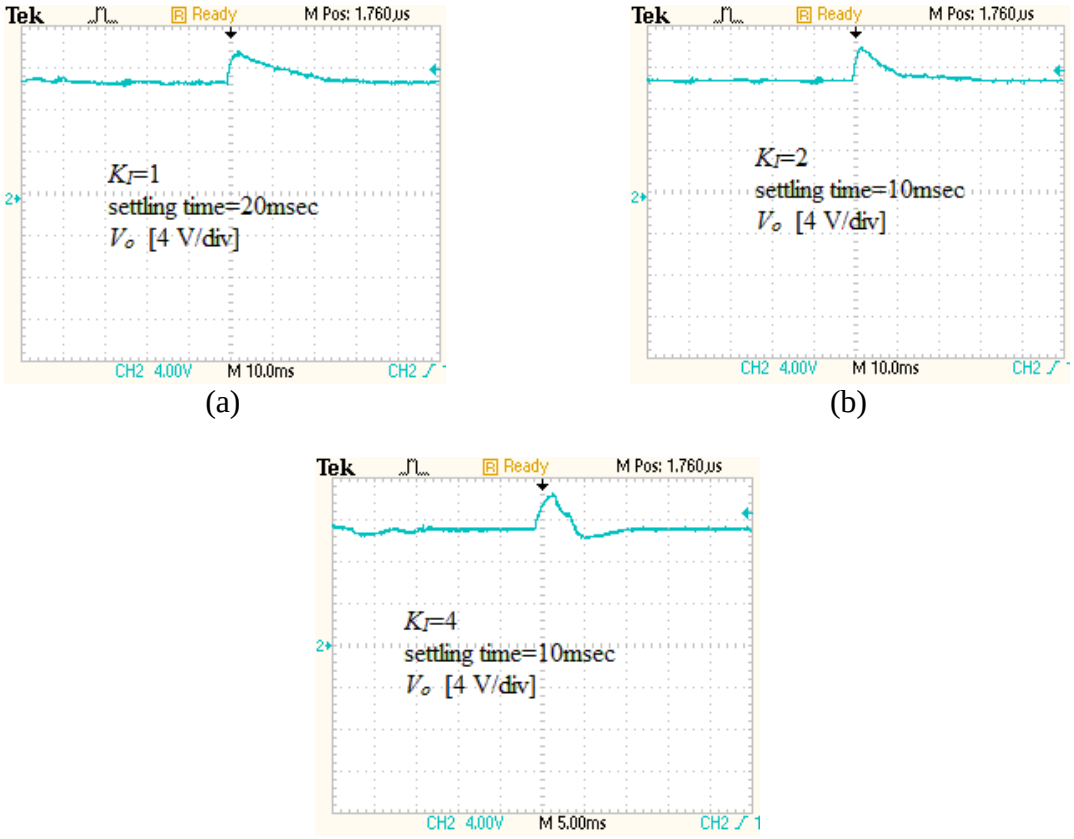
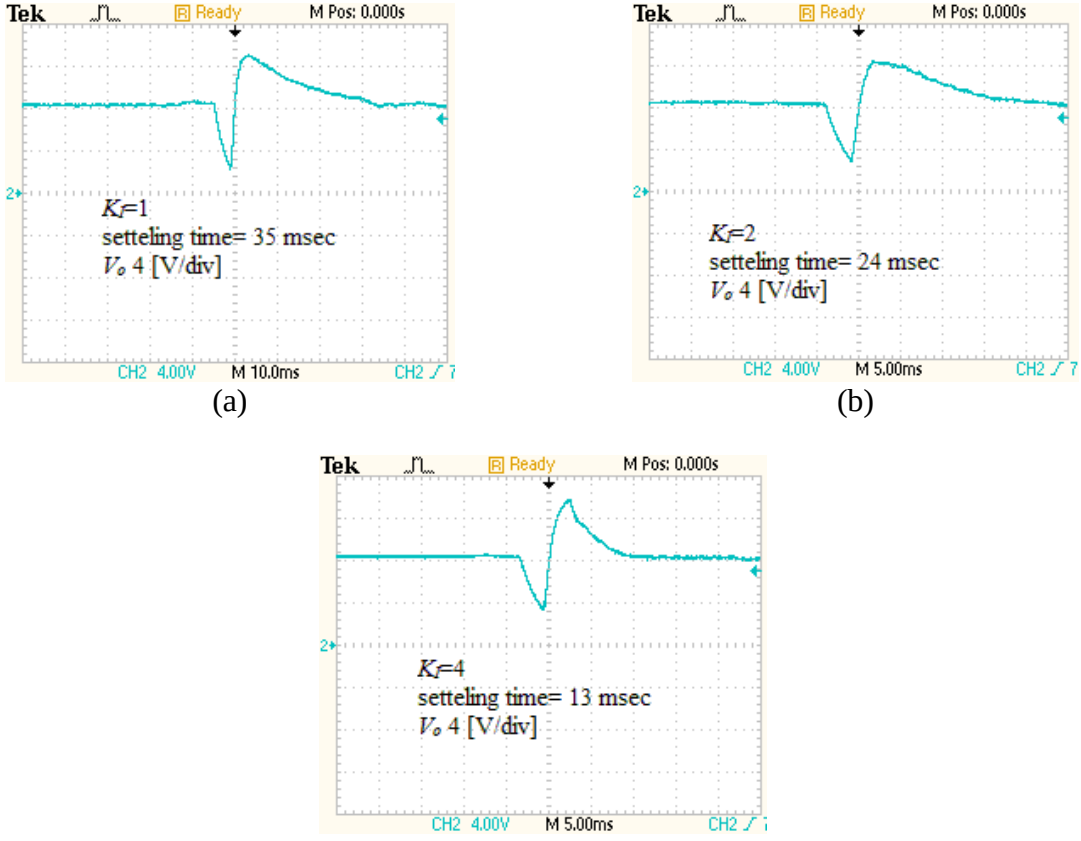


Figure 5.25: Effect of the integral gain on the voltage recovery characteristics of the converter for step change in the output load from R_o=15 Ω to R_o=30 Ω.

Figures 5.26 and 5.27 show the effects of the integral gain when the input voltage is subjected to a step change for two scenarios of increase (from V_d=7 V to V_d =10 V) and decrease (from V_d = 10 V to V_d =7 V) in the input voltage, respectively. This step change in the input voltage is done through a single-pole double-throw switch (SPDT). In both scenarios of increase and decrease in the input voltage, the control scheme regulates the output voltage and restores it to the reference voltage (V_{ref}=8 V). The undershoots in Figure 5.26 are due to performance of the SPDT switch. During the transition between

V_d=7 V to V_d =10 V, the input voltage initially reaches 0 V and then to 10 V. The momentary no-voltage condition on the input voltage results in the observed undershoots in Figure 5.26. However, for the scenario of decrease in the input voltage in Figure 5.27, the effect of the momentary no-voltage condition due to the operation of the SPDT switch is not significant and the observed undershoots are due to the decrease in the input voltage form V_d=10 V to V_d=7 V and as the value of integral gain increase to K_I=4, the response of the system becomes underdamped.



(a) (b)

(c)

Figure 5.26: Effect of the integral gain on the voltage recovery characteristics of the converter for step change in the input voltage from V_d=7 V to V_d=10 V.

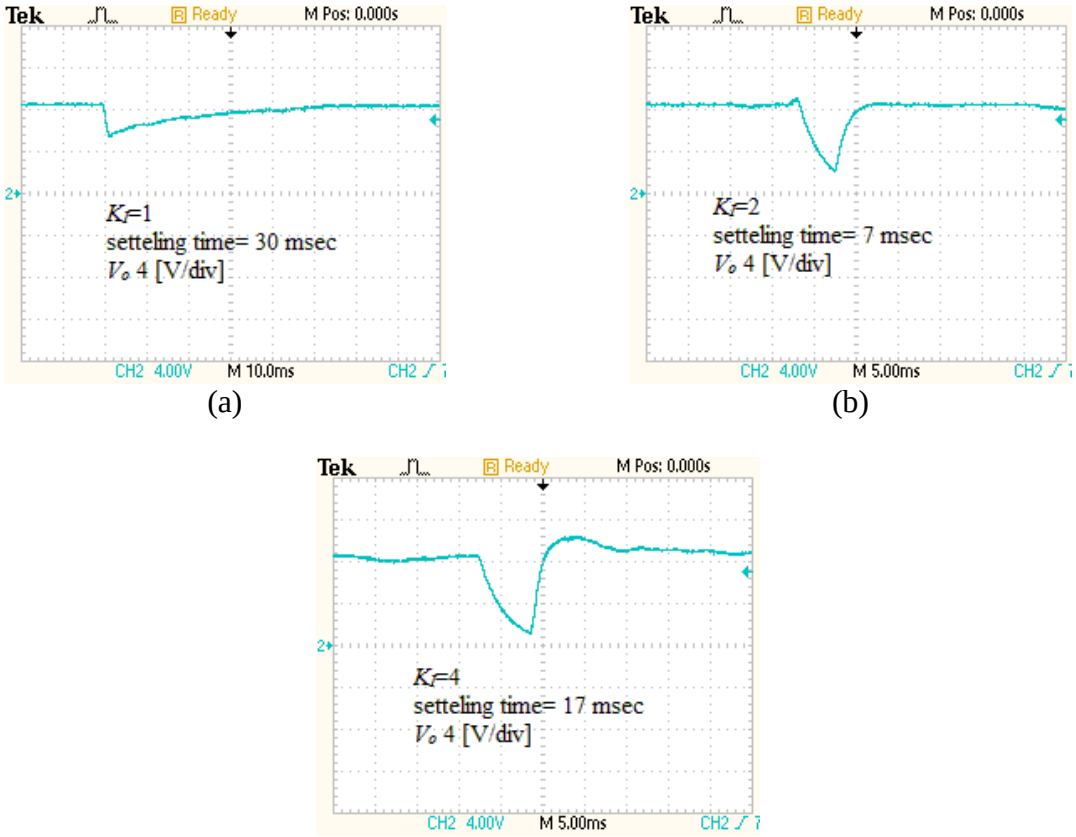


Figure 5.27: Effect of the integral gain on the voltage recovery characteristics of the converter for step change in the input voltage from V_d=10 V to V_d=7 V.

5.4 Summary

An experimental prototype of the proposed dual series-resonant DC-DC converter was implemented and tested in the laboratory and the experimental results were presented in this chapter. The main specifications of the chosen components were highlighted and the overall implementation of the experimental prototype in Altium Designer was presented. The operation of the converter was investigated experimentally in open-loop and closed-

loop operating conditions. The results of the open-loop operation demonstrate that the output voltage of the proposed converter can be changed with two degrees of freedom, which are the duty ratio of the PWM switching signal and the switching frequency. In addition, the converter is able to operate in both step-down and step-up regions. Soft switching operation of the converter was realized and the improvement in the output power transfer and the efficiency of the converter was demonstrated. The steady state experimental results of the output voltage, resonant inductor currents, and resonant capacitor voltages of the converter confirmed the PLECS simulation results and the extended describing function analytical modeling results discussed in Chapter 4. The performance of the closed-loop operation of the proposed converter was examined under different loading conditions and it was demonstrated that the designed single-loop voltage-feedback method was effective in regulating the output voltage of the converter under disturbances.

Chapter 6

Design of the Dual Series-Resonant DC-DC Converter

The experimental prototype of the dual series resonant DC-DC converter was constructed as a proof of concept to demonstrate the functionality of the proposed converter. An analytical model of the converter using the extended describing function methodology was then developed in Chapter 4 to characterize the steady state and small signal behaviour of the converter. Experimental results obtained from a 40 W, 10V laboratory prototype of the converter confirmed the results of the analytical model and simulation. This chapter therefore aims at using the analytical model of the converter to develop a step-by-step procedure to design the converter in order to meet the design requirements.

The selection of the components of the converter must fulfill the design requirement, which is established by the application of the converter. The preliminary information from any specific application is essential as the basis of the design procedure. This routine is taken into consideration in this chapter in order to propose a design procedure for the proposed converter. The proposed design procedure can be employed to customize the proposed DC-DC converter for any specific applications.

6.1 Design Considerations

The boundary of various parameters in the circuit should be taken into consideration to develop the design procedure of the converter as follows:

- *Input voltage range* ($V_{d-\min} - V_{d-\max}$): For applications that require the converter to regulate the output voltage and maintain a constant output voltage in the case of variations in the input voltage, the range of variation of input voltage is an important parameter and should be considered.
- *Switching frequency range* ($f_{sw-\min} - f_{sw-\max}$): Various platforms can be utilized to generate gate signals of the switching devices to drive the switching components. Simple PWM chips, microcontrollers, FPGA, and DSP boards are among these platforms. The range of frequency of the generated pulse is different for each of these platforms. Besides, the selection of the switching devices (i.e., IGBT, MOSFET, eGaN, SiC etc.) plays a crucial role in deciding the desired switching frequency range.

- *Output voltage range* ($V_{o-\min} - V_{o-\max}$): As described in previous chapters, the developed control scheme is able to track the reference voltage. Therefore, for applications that require a controllable DC output voltage, the range of variation of the output voltage should be taken into consideration.
- *Maximum output power* ($P_{o-\max}$): The maximum output power of the converter indicates the maximum current of the components of the converters such as diodes, MOSFETs, inductors, capacitors, and high frequency transformer. The converter should operate properly from no-load condition to full-load condition with maximum allowable current.
- *Maximum value of duty ratio* ($D_{\max}$): The maximum duty ratio of the PWM switching signal of switch *Q2* is important. According to (5.1), it determines the maximum voltage across the switching devices and the steady state voltage of the clamping capacitor.
- *Turns ratio of the Transformer* (*N*): The turns ratio of the transformer determines the output voltage level of the converter and it exhibits a nonlinear relationship with the output voltage in steady state (4.64). For this reason, it should be dealt with as an independent parameter.

6.2 Design Procedures

- ***Current Rating of the Components on the Secondary Side of the Transformer***

The maximum current on the secondary side of the transformer occurs at the full-load condition, which corresponds to a minimum value the of load resistor (R_{min}). The

minimum value of the load resistor is determined by the maximum output power ($P_{o\text{-}max}$) and the minimum output voltage ($V_{o\text{-}min}$) as follows:

$$R_{\min} = \frac{V_{o-\min}^2}{P_{o-\max}} \tag{6.1}$$

Considering only the fundamental components of the AC signals in the steady state condition of the resonant inductor current in (4.53) and (4.54), the RMS value of the resonant inductor current at full load is calculated as follows:

$$I_{Lr-\max} = \frac{\pi V_{o-\max}}{2R_{\min}\sqrt{1-\cos(2\pi D_{\max})}} \tag{6.2}$$

Equation (6.2) establishes the current ratings of the components on the secondary side of the transformer, i.e. L_{r1}, L_{r2}, C_{r1}, C_{r2} and the secondary coils of the transformer (i.e. N_{s1} and N_{s2}). Since the resonant inductor currents are equal and both are conducted through either *D1* or *D2*, the maximum current rating of the rectifying diodes (*D1* and *D2*) is twice the maximum current for the series resonant components.

- ***Sizing of the Series Resonant Components* (L_{r1}, L_{r2}, C_{r1}, and C_{r2})**

For balanced operation of the converter, the two series resonant circuits should be identical (i.e., L_{r1}=L_{r2}, and C_{r1}=C_{r2}). Considering the first component in the output voltage equation (4.64) and by using (4.78), the following equation is obtained.

$$V_o = \frac{2R_o\left|V_o\angle\theta - \frac{NV_d}{1-D}\right|}{\pi^2\left(F\Omega_r L_r + 1/F\Omega_r C_r\right)}(1-\cos 2\pi D) = \frac{4R_o\left|V_o\angle\theta - \frac{NV_d}{1-D}\right|Ff_r C_r}{\pi\left(F^2+1\right)}(1-\cos 2\pi D) \tag{6.3}$$

From (6.3), assuming the least value for switching frequency (F=2) and the mean value for the cosine term, the minimum value for the resonant capacitors is calculated for the minimum switching frequency (i.e., F=2) as follows:

$$C_{r-\min} = \frac{5V_{o-\min}\pi}{8R_{\min} f_{sw-\min}\left|V_{o-\max}\angle\theta - \frac{NV_{d-\min}}{1-D_{\max}}\right|} \tag{6.4}$$

As discussed in Chapter 3, in order to guarantee the CCM operation of the converter, the switching frequency should be more than twice the resonant frequency ($F \geq 2$). Following that argument and knowing the switching frequency range, the following conditions can be developed for the resonant inductors:

$$f_{sw-\min} > \frac{1}{\pi\sqrt{L_{r\_\min}C_{r\_\min}}} \tag{6.5}$$

$$L_{r-\min} = \frac{1}{\pi^2 C_{r-\min} f_{sw-\min}^2} \tag{6.6}$$

Equations (6.4)-(6.6) can be used to determine suitable values for the resonant inductors and capacitors.

It should be pointed out that the upper limit for the values of resonant inductors and resonant capacitors are set by the value of the resonant frequency of the magnetizing inductance of the transformer and the clamping capacitor. In order to isolate the resonance oscillations of the series resonant circuit from the resonance oscillations generated from the clamping capacitor and magnetizing inductance of the transformer, it is essential to ensure that the resonant frequency between the clamping capacitor and magnetizing

inductance (ω_m) is less than the resonant frequency of the series resonant circuit (ω_r). As a rule of thumb, the minimum value of ω_r should be greater than $10\omega_m$. Therefore, the upper limit for both L_r and C_r is chosen in conjunction with L_m and C_c as follows:

$$100L_rC_r < L_mC_c \tag{6.7}$$

Equation (6.7) suggests a parallel procedure for selecting L_r, C_r, L_m, and C_c.

- ***Clamping Capacitor (C_c)***

The voltage rating of the clamping capacitor depends on the input voltage and the duty ratio of the PWM switching signal (4.52). The selection of the clamping capacitor should be based on the maximum possible voltage of the clamping capacitor, which occurs at D_{max} and $V_{d\text{-}max}$ as follows:

$$V_{Cc} = \frac{D_{\max}}{1-D_{\max}} V_{d-\max} \tag{6.8}$$

The size of the clamping capacitor needs to be calculated in conjunction with the size of the magnetizing inductance of the transformer, as discussed below.

- ***Transformer***

The voltage of the secondary coils of the transformer is dependent on the duty ratio of the PWM switching signal and the input voltage. The RMS value of the fundamental component of the voltage on the secondary side of the transformer is calculated using given equations in (4.8)-(4.11) as follows:

$$V_{\text{sec}} = \frac{NV_d\sqrt{1-\cos(2\pi D)}}{\pi(1-D)} \tag{6.9}$$

Therefore, the maximum RMS voltage of each of the secondary coils at full load is calculated as follows:

$$V_{\text{sec}-\max} = 4.44\frac{NV_{d-\max}}{\pi} \tag{6.10}$$

From the knowledge of maximum resonant inductor currents and the maximum voltage of the secondary coils of the transformer, the power rating of the transformer can be calculated as follows:

$$P_{Tr} = 2V_{\text{sec}-\max}I_{Lr-\max} \tag{6.11}$$

The transformer needs to exhibit suitable performance at this power across the range of switching frequency ($f_{sw\text{-}min} - f_{sw\text{-}max}$).

The size of the magnetizing inductance of the transformer can be estimated in conjunction with the size of the clamping capacitor from the simplified small signal model of control-to-output transfer function stated in (4.99). The polynomial denominator of the control-to-output transfer function is used here to develop a constraint for L_m and C_c to be used along with (6.7) to select suitable values for L_m and C_c. As discussed in section 4.4.3, the step response of the control-to-output transfer function yields the output voltage. This step response of the control-to-output transfer function in the frequency domain can be expanded as follows:

$$v_o(s)=\frac{1}{s}(1-D)\frac{\hat{v}_o(s)}{\hat{d}(s)}=\frac{1-D}{s}\frac{K'_d}{\left(s+\frac{1}{R_oC_o}\right)\left(s^2+2\zeta(1-D)\Omega_m s+(1-D)^2\Omega_m^2\right)}= \\ \frac{K_1}{s}+\frac{K_2}{\left(s+1/R_oC_o\right)}+\frac{K_3 s+K_4}{\left(s^2+2\zeta(1-D)\omega_m s+(1-D)^2\omega_m^2\right)} \tag{6.12}$$

where,

$$K'_d=\frac{NV_d\left(B'_1a_1-A'_1b_1\right)}{2F\Omega_r L_r L_m C_c C_o} \tag{6.13}$$

$$K_1=K'_d\frac{R_oC_oL_mC_c}{1-D} \tag{6.14}$$

$$K_2=\frac{-K'_d(1-D)R_oC_o}{(1-D)^2\Omega_m^2+\left(\frac{1}{R_oC_o}\right)^2-\frac{2\zeta(1-D)\Omega m}{R_oC_o}} \tag{6.15}$$

$$K_3=\frac{K'_d}{(1-D)\Omega_m^2}\left(\frac{2\zeta(1-D)\Omega_m-\frac{1}{R_oC_o}}{(1-D)^2\Omega_m^2+\left(\frac{1}{R_oC_o}\right)^2-\frac{2\zeta(1-D)\Omega_m}{R_oC_o}}\right) \tag{6.16}$$

$$K_4=K'_d(1-D)\left(\frac{4\zeta^2-\frac{2\zeta}{(1-D)\Omega_m R_oC_o}-1}{(1-D)^2\Omega_m^2+\left(\frac{1}{R_oC_o}\right)^2-\frac{2\zeta(1-D)\Omega_m}{R_oC_o}}\right) \tag{6.17}$$

Equation (6.14) provides an alternative relation for the output voltage of the converter. The response of the system in the time domain is expressed as

$$v_o(t) = K_1 + K_2 e^{-t/RC_o} + K_3 e^{-\zeta(1-D)\omega_m t}\cos\left(t(1-D)\omega_m\sqrt{1-\zeta^2}\right) + \frac{K_4 - \zeta(1-D)\omega_m}{(1-D)\omega_m\sqrt{1-\zeta^2}} e^{-\zeta(1-D)\omega_m t}\sin\left(t(1-D)\omega_m\sqrt{1-\zeta^2}\right) \quad (6.18)$$

$$v_o(t) = K_1 + K_2 e^{-t/RC_o} + \frac{e^{-\zeta(1-D)\omega_m t}\sqrt{(K_4 - \zeta(1-D)\omega_m)^2 + K_3^2(1-D)^2\omega_m^2(1-\zeta^2)}}{(1-D)\omega_m\sqrt{1-\zeta^2}} \times \sin\left(t(1-D)\omega_m\sqrt{1-\zeta^2} + tg^{-1}\left(\frac{K_3(1-D)\omega_m\sqrt{1-\zeta^2}}{K_4 - \zeta(1-D)\omega_m}\right)\right) \quad (6.19)$$

Equation (6.19) shows that the output voltage consists of a steady state value, a second order response, and an exponential decaying response. These responses are shown in Figure 6.1. The settling times of the second order term and the exponential decaying term, assuming 0.7% tolerance band around the steady state value, are calculated as follows:

$$T_\zeta = \frac{-1}{\zeta(1-D_{\max})\omega_m} Ln\left(0.007\frac{K_1\sqrt{1-\zeta^2}}{\sqrt{(K_4 - \zeta(1-D_{\max})\omega_m)^2 + K_3^2(1-D_{\max})^2\omega_m^2(1-\zeta^2)}}\right) \quad (6.20)$$

$$T_{RC} = 5R_oC_o \quad (6.21)$$

where, T_ζ is the settling time of the second order term and T_{RC} is the settling time of the exponential term.

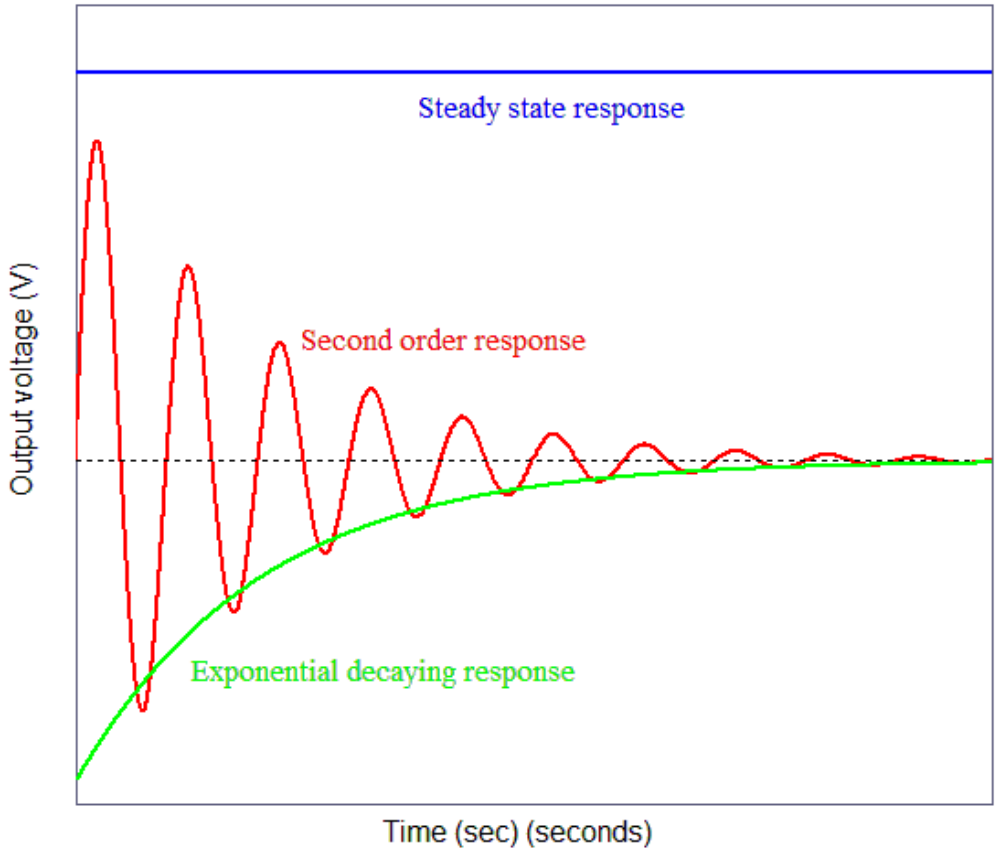


Figure 6.1: The steady state response, the second order response, and the exponential decaying response in the output voltage.

From Figure 6.1, it is observed that the initial fluctuations associated with the second order response are effectively mitigated since the initial value of the exponential decaying part (K_2) is a negative value with respect to the steady state value (K_1) in (6.19). Figure (6.2)

and Figure (6.3) show the variations of T_ζ versus L_m and C_c, respectively. It is observed that high values of L_m and C_c increase the settling time of the second order system.

As a rule of thumb, the following assumption can be considered in selecting L_m and C_c:

$$\zeta=0.1 \tag{6.22}$$

$$10\ L_r < L_m < 100\ L_r \tag{6.23}$$

$$10\ C_r < C_c < 100\ C_r \tag{6.24}$$

These assumptions take the worst case of elongated settling time into consideration and satisfy (6.7).

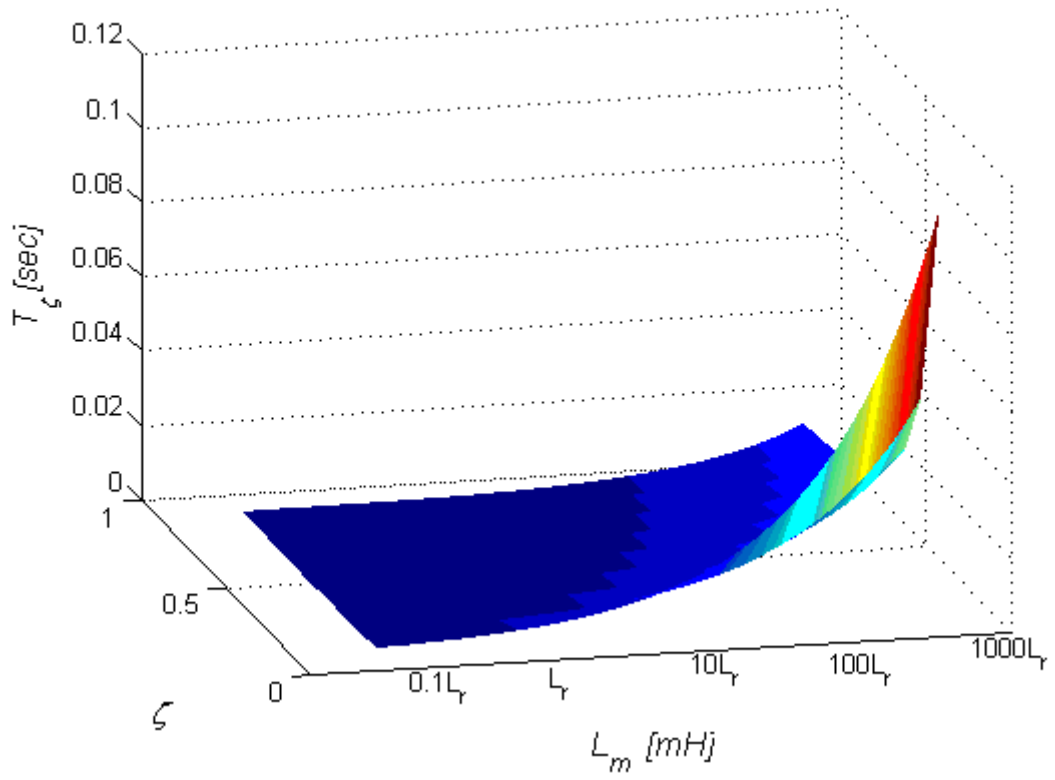


Figure 6.2: Settling time versus the size of magnetizing inductance and damping ratio.

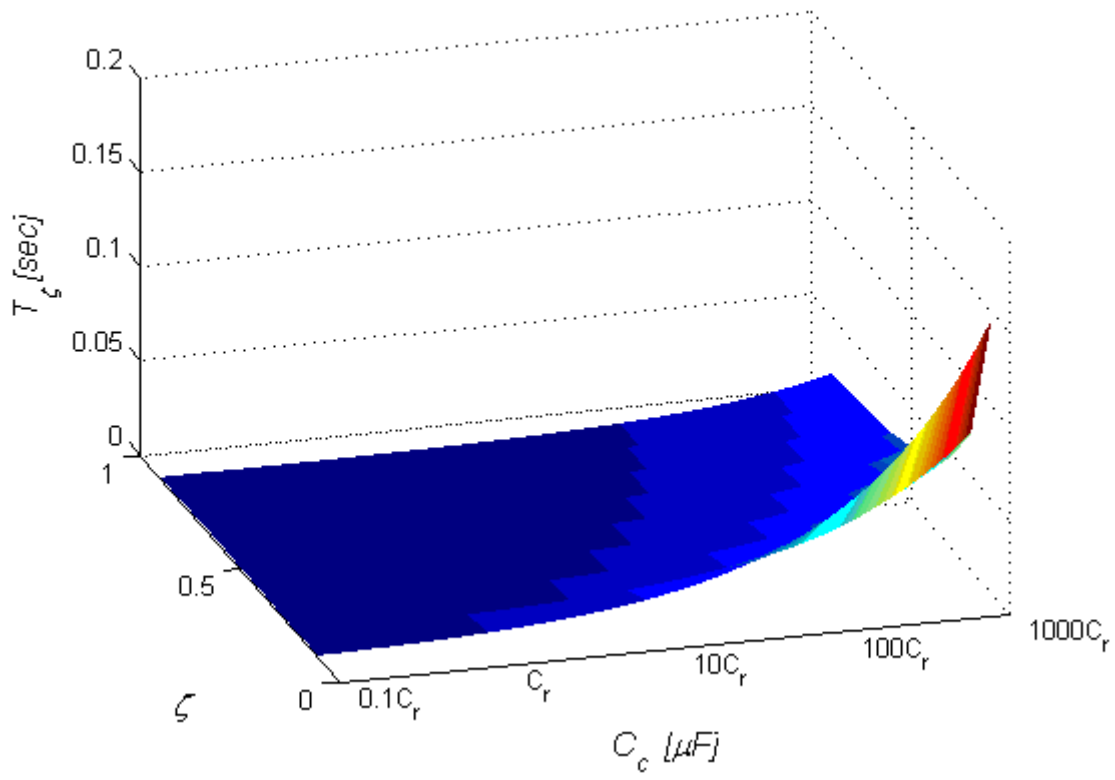


Figure 6.3: Settling time versus the size of clamping capacitor and damping ratio.

- ***Output Capacitor (C_o)***

The output capacitor is suggested to be larger than the clamping capacitor. The upper limit of the output capacitor can be calculated using the derived equations in (6.20) and (6.21) for the settling times. If the value of the output capacitor is selected to ensure $T_{RC} = T_\zeta$, then the fluctuations on the output voltage can be effectively mitigated. The maximum value for the output capacitor is obtained from (6.20) and (6.21) as follows:

$$C_{o-\max} = \frac{-Ln\left(0.007 \dfrac{K_1\sqrt{1-\zeta^2}}{\sqrt{(K_4-\zeta(1-D_{\max})\omega_m)^2 + K_3^2(1-D_{\max})^2\omega_m^2(1-\zeta^2)}}\right)}{5R_{\min}\zeta(1-D_{\max})\omega_m} \tag{6.25}$$

- ***Semiconductor Switches***

The semiconductor switches must operate properly in the required range of switching frequency between ($f_{sw\text{-}min}$ – $f_{sw\text{-}max}$). The maximum voltage and current of the switches at full load conditions are determined as follows:

$$V_{sw-\max} = \frac{V_{d-\max}}{1-D_{\max}} \tag{6.26}$$

$$I_{sw-\max} = I_{Lm-\max} + 2NI_{Lr-\max} = \frac{NV_{o-\max}}{R_{\min}(1-D_{\max})} + \frac{N\pi V_{o-\max}}{R_{\min}\sqrt{1-\cos(2\pi D_{\max})}} \tag{6.27}$$

A. Bootstrap Circuit of the Driver

The bootstrap circuit is an efficient and popular method to drive half bridge switches. Figure (6.4) shows the simplified circuitry of a half bridge gate driver. This circuit consists of a low side driver to drive the bottom switch (*Q2*) with respect to ground and the high side driver to drive the top switch (*Q1*) with respect to the switch node (V_S). A buffer (B) drives each gate. These buffer circuitries are integrated inside most of commercial driver ICs. However, the bootstrap diode (D_{Boot}) and the bootstrap capacitor (C_{Boot}) need to be selected according to the design requirement and switches.

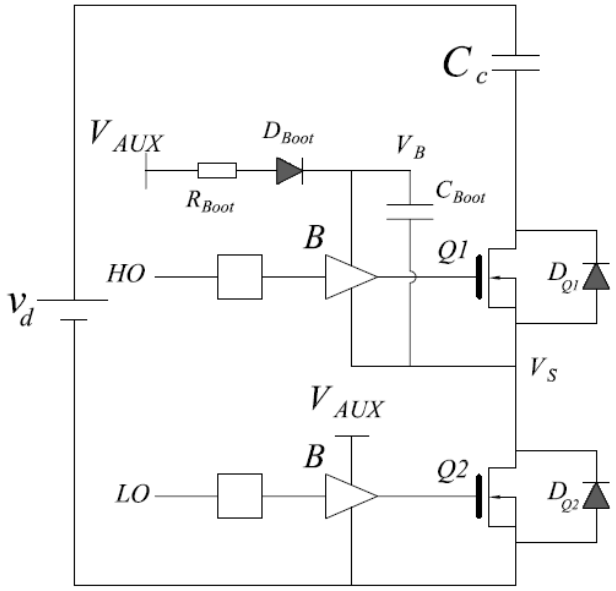


Figure 6.4. Bootstrap drive circuit.

The bootstrap capacitor charges when *Q2* is turned on and *Q1* is off through V_{AUX}, bootstrap diode, and bootstrap resistor (R_{Boot}) as shown in Figure 6.5. This provides a fixed voltage between V_S and V_B. When *Q1* is turned on and *Q2* is off, the bootstrap diode blocks the discharge current of the bootstrap capacitor and the gate signal of *Q1* can be generated with respect to V_S. The voltage of the capacitor when it is charged is calculated as follow [84]:

$$V_B = V_{AUX} - V_{Diode} - V_{GS-\min} \tag{6.28}$$

where, V_{AUX} is the auxiliary power of the chip, V_{Diode} is the forward voltage drop across the bootstrap diode, and $V_{GS\text{-}min}$ is the minimum gate-to-source voltage of the selected switch.

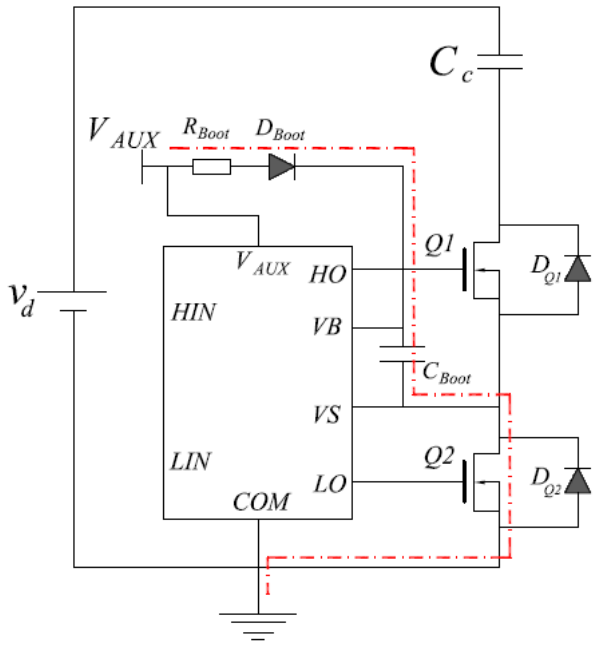


Figure 6.5. Charging of the bootstrap capacitor when *Q2* is turned on.

The size of the bootstrap capacitor can be calculated as follow [85]:

$$C_{Boot} > \frac{2\left(2Q_g + \frac{(1-D_{\max})}{f_{sw-\max}}\left(I_{QBS} + I_{LK} + I_{GSS}\right) + Q_{LS}\right)}{V_{Boot}} \tag{6.29}$$

where, I_{QBS} is the bootstrap circuit quiescent current; I_{LK} is the bootstrap circuit leakage current; I_{GSS} is the gate-to-source forward leakage current; Q_g is the total gate charge of the switch; and Q_{LS} is the total charge required by the internal level shifter of the gate driver which can be considered 5 *nC* for chips up to 600V [85]. Q_g and I_{GSS} can be obtained from the datasheet of the switch and I_{QBS} and I_{LK} are listed in the datasheet of the driver chip.

It should be mentioned that in (6.29), the leakage currents of the bootstrap capacitor and bootstrap diode are neglected since they are relatively low with respect to I_{QBS}, I_{LK}, and I_{GSS}. The bootstrap diode needs to block the rail voltage when the top switch is on and it should have fast recovery time. The bootstrap resistor should not be more than 5Ω to 10Ω in order to keep the time constant of charging and discharging of the bootstrap capacitor small enough for proper operation of the bootstrap circuit [84]. The driver IC should properly operate up to $V_{sw\text{-max}}$.

6.3 Design Example

The design procedure described in the previous section for the dual series-resonant DC-DC converter is followed with a design example. The procedures outlined below can be used for various applications with different design requirement. This example considers the design of a 100 W, 50 V – 80 V dual series-resonant DC-DC converter with the design requirements listed in Table 6.1.

Table 6.1: Design requirements.

Design requirement	***Value***
Output voltage range	50 V – 80 V
Maximum output power	100 W
Input voltage range	50 V – 120 V
Switching frequency range	100 kHz – 500 kHz
Maximum duty ratio	0.7
Transformer turns ratio	1

The minimum value of the load resistor can be calculated according to (6.1) as follows:

$$R_{\min} = \frac{V_{o-\min}^2}{P_{o-\max}} = \frac{50^2}{100} = 25\Omega \tag{6.30}$$

Next step is to calculate the maximum inductor resonant current according to (6.2).

$$I_{Lr-\max} = \frac{\pi V_{o-\max}}{2R_{\min}\sqrt{1-\cos\left(2\pi D_{\max}\right)}} = \frac{\pi 80}{50\sqrt{1-\cos(1.4\pi)}} = 4.4A \tag{6.31}$$

The resonant inductors and resonant capacitors must have current rating more than maximum inductor resonant current and the current rating for the output rectifying diodes must be at least twice this number.

The minimum value of the resonant capacitor voltage can be calculated using (6.4):

$$C_{r-\min} = \frac{5V_{o-\min}\pi}{8R_{\min} f_{sw-\min}\left|V_{o-\max}\angle\theta - \frac{NV_{d-\min}}{1-D_{\max}}\right|} = \frac{5\times 50\pi}{8\times 25\times 10^5 \times \left|80\angle(0.6\pi) - \frac{50}{0.3}\right|} = 0.2\mu F \tag{6.32}$$

The voltage rating for the clamping capacitor can be calculated as follows:

$$V_{Cc} = \frac{D_{\max}V_{d-\max}}{1-D_{\max}} = \frac{0.7\times 120}{0.3} = 280\ V \tag{6.32}$$

The given relation in (6.11) returns the maximum power of the high frequency transformer.

$$P_{Tr} = 2V_{\sec-\max}I_{Lr-\max} = 2\times 4.44\times\frac{120}{\pi}\times 4.4 = 1.4\ \ kVA \tag{6.33}$$

The minimum value of the resonant inductor can be calculated as follows:

$$L_{r-\min} = \frac{1}{\pi^2 C_{r-\min} f_{sw-\min}^2} = \frac{1}{\pi^2 \times 0.2 \times 10^{-6} \times (10^5)^2} = 50\ \mu F \tag{6.34}$$

By knowing the minimum values of the resonant components, the suitable range for the size of the clamping capacitor and the magnetizing inductor of the transformer can be realized using (6.23) and (6.24).

Assuming ζ=0.1, the output capacitor of the converter can be calculated according (6.25) as follows:

$$C_{o-\max} = \frac{-Ln\left(0.007 \dfrac{K_1\sqrt{1-\zeta^2}}{\sqrt{(K_4 - \zeta(1-D_{\max})\omega_m)^2 + K_3^2(1-D_{\max})^2\omega_m^2(1-\zeta^2)}}\right)}{5R_{\min}\zeta(1-D_{\max})\omega_m} = 74\ \mu F \tag{6.35}$$

The minimum current rating of the MOSFET switches can be calculated using (6.27):

$$I_{sw-\max} = \frac{NV_{o-\max}}{R_{\min}(1-D_{\max})} + \frac{N\pi V_{o-\max}}{R_{\min}\sqrt{1-\cos(2\pi D_{\max})}} = 19.45\ A \tag{6.27}$$

Table 6.2 lists the values of the parameters that need to be chosen for this design example.

Table 6.2: Components value and ratings for the design example.

Component	***Value***
$I_{Lr-\max}$	4.4 A
$I_{D-\max}$	8.8 A
$L_{r-\min}$	50 μH
$C_{r-\min}$	0.2 μF
L_m	530 μH - 5300 μH
C_c	2 μF - 20 μF
$V_{Cc-\max}$	280 V
P_{Tr}	1.4 kW
C_o	74 μF
$I_{sw-\max}$	19.45 A

6.4 Summary

In this chapter, the developed steady state and small signal models of the converter, presented in Chapter 4, were used to develop a systematic and parametric approach to size the components of the converter according to specified design requirements. A complete design procedure was developed and a design example was given to illustrate the design procedure. The step-by-step procedure can be used to design the dual series-resonant DC-DC converter with design specifications according to the application of the converter.

Chapter 7

Conclusion and Future Work

DC/DC power converter is an important component in applications such as renewable energy systems, switched mode power supplies, DC motor drives, DC distribution power systems, portable electronic devices, telecommunication systems, and home appliances. The extensive employment of DC-DC power converters in different industries always demands improvements in efficiency, power density, controlling systems, manufacturing cost, reliability, and stability of the converter. A novel topology of DC-DC converter was proposed and investigated in this thesis. Compared with the traditional interleaving technique to improve power transfer capability of the converter, the proposed dual series-

resonant topology provides significant improvement regarding the power density of the converter, efficiency of power conversion, simplicity of switching and control scheme, and reduced number of the switching components.

7.1 Conclusion

The high frequency requirement for compact and miniaturized conversion platforms demands soft switching operation with the help of resonant passive components for the switching semiconductors in the converter. The principles of operation of the basic topologies of resonant converters were presented in Chapter 2. The advantages and limitations of each topology were discussed. It was observed that the discontinues transfer of power to the output load is one of the common problems in resonant DC-DC converters. The traditional solution of interleaving identical stages results in increase in the size, weight, and complexity of the control scheme because of the doubling the number of switching components.

To address these problems, a novel topology of the DC-DC converter was proposed and simulated in PLECS software to investigate its feasibility and functionality. The proposed DC-DC converter employs two series-resonant circuits to increase the power transfer capability of the converter. The second added series-resonant circuit provides an identical path to supply the load current. As a result, the output load and the output capacitors are always supplied by at least one of the series-resonant circuits, leading to an improved power transfer capability.

The proposed topology was analyzed using the extended describing function approach. Steady state operating relationships and small signal models were developed to characterize the converter. It was demonstrated that the proposed converter provides two degrees of freedom to control the output voltage (i.e., duty ratio of the PWM switching signal and the switching frequency). Based on the small signal models, a single-loop voltage-feedback control method was developed to control the output voltage of the converter with respect to its reference voltage. The control method is based on the duty ratio of the PWM switching signal, which is easier to implement compared with a variable switching frequency control scheme.

An experimental 10 V, 40 W laboratory prototype of the proposed converter topology was built and tested to validate its steady state and transient operation and features. The improvement in the output power transfer capability and the overall efficiency of the proposed topology was experimentally demonstrated.

Finally, a design procedure was developed that can be used to customize the design of the converter for different levels of power, voltage, and switching frequency.

7.2 Contributions of the Research

The specific contributions of the research are presented in four categories based on the chapters of the thesis as follows:

1. Investigation and Study of the Soft Switching Methods and Resonant DC-DC Power Converters (Chapter 2)

Different methods and topologies that are used to achieve soft switching features were discussed in this chapter. The unique principles and features of the basic topologies of soft switching converters were categorized based on their topological differences. The switch networks for each of the discussed basic topologies were presented and the key aspects and characterizations of each of the topologies were discussed. From the investigation of the recent proposed topologies, their features and limitations were highlighted. The investigation focused on factors such as efficiency, power transfer ratio, complexity of the topology, control scheme, and number of components, which impacts manufacturing cost. The detailed discussion and investigation provided a context for the proposed topology developed in Chapter 3. In addition, the investigation resulted in the publication of three technical papers on multiple-loop control strategy [86]; the use of design of experiment methodology [87]; and EMI noise in a 2-stage interleaved topology of a boost converter [88].

2. The Dual Series-Resonant DC-DC Converter and Analysis (Chapter 3 and Chapter 4)

The proposed topology of the dual series resonant DC-DC converter was presented in Chapter 3. The operational principles of the converter and its features were described qualitatively, and PLECS software was used to simulate the converter to investigate its feasibility and functionality under different operating conditions. It was discovered that the

operation of the dual series-resonant converter involves six different operational modes. Equivalent circuits for each mode was derived and discussed in the time domain. Following the discussions over the operation of the converter, the soft switching operation of the MOSFETs and the output diodes were examined. It was demonstrated that the MOSFETs on the primary side of the transformer operates under ZVS condition, and the output diodes operates under ZCS conditions. In addition, it was demonstrated that continuous and uninterrupted current is supplied to the load throughout the operation of the converter. The necessity of operation in the continuous current mode (CCM) was discussed and it was shown that operation in the discontinuous current mode (DCM) results in more switching losses, as the turn-on of one of the MOSFETs occurs under hard switching condition. The boundary for CCM operation was established as the low threshold of the switching frequency when the switching frequency is twice the resonant frequency of the resonant circuits. The presentation in this chapter provides a detailed characterization of the proposed converter for a complete understanding of the features of the new converter. In Chapter 4, the extended describing function approach was used as the analytical tool to model the proposed converter. The approach allowed the thorough investigation of the proposed dual series-resonant converter in the most general form. This includes the state-space equations governing all six modes of operation, the large signal analysis, and small signal analysis. The results of the large signal analysis led to a full characterization of the proposed converter in the steady state condition. The challenge of obtaining simple steady state expressions from nonlinear sets of equations was resolved by making suitable assumptions and approximations. The result was a steady state voltage

conversion relationship expressed as a function of the parameters of the converter, duty ratio, and switching frequency of the converter. The results of the voltage conversion ratio of the converter from the derived steady state model were compared with the PLECS simulation results to authenticate the modeling procedure in the steady state domain. The state-plane trajectories of the resonant inductor currents and resonant capacitor voltages were presented to provide insights into the operation of the converter.

Transfer functions relating the output voltage of the converter to each of the converter input signals (i.e., input voltage-to-output, duty ratio-to-output, frequency-to-output, and output current-to-output transfer functions) were derived from the small signal analysis of the converter. The resulting transfer functions were investigated to provide qualitative insight into the effects of the converter parameters on the transient behavior and to design a control scheme to regulate the output voltage with respect to a reference voltage. The derived transfer functions were parameterized based on the values of gain, and location of zeros and poles. The duty ratio-to-output (i.e., control-to-output) transfer function was found the most suitable one for the control scheme. This transfer function was simplified by removing non-significant zeros and poles from the expressions, thereby reducing its order from seven to three. In order to validate the resulting 3^{rd} order transfer function, the step response of the reduced-order system was compared with PLECS simulation results. The results were in good agreement; therefore, the reduced order transfer function was used to develop a single-loop voltage-feedback control scheme with an integral controller to regulate the output voltage of the converter. The behavior and stability of the closed-loop system were investigated using the root locus plot and the suitable range for the

integral gain of the controller was calculated. Simulation results demonstrated the effectiveness of the designed control scheme to recover the output voltage of the converter in the case of any changes in the inputs of the converter.

The results of the research in Chapters 3 and 4 were presented at the *41st IEEE Industrial Electronics Society* conference in Japan [89].

3. Experimental Prototype (Chapter 5)

The detail procedures for constructing a 10 V, 40 W experimental prototype of the proposed dual series-resonant circuit DC-DC converter were presented in Chapter 5. The specifications of the selected components such as switching devices, driving circuitry, voltage transducer, planar transformer, and controller platform were discussed. The overall wiring diagram of the prototype was presented. A customized PCB layout of the converter was designed in Altium Designer. Experimental verifications were performed in two phases.

First, the open-loop operation and characteristics of the converter were verified by comparing the experimental results with the results from PLECS simulation and analytical models. This comparison showed good agreement between the experimental, simulation, and analytical modeling results. The soft switching operation of the converter was confirmed experimentally and the voltage conversion ratio as functions of duty ratio and switching frequency were experimentally confirmed. The improvements in the output power transfer capability and the overall efficiency of the proposed dual series-resonant converter were experimentally confirmed by comparing the results with the results

obtained from traditional single series-resonant topology. Finally, the effects of possible mismatches between the values of the series-resonant circuits were investigated experimentally.

In the second phase, the closed-loop operation of the converter was investigated and the experimental results were found to agree favorably with the results from simulation and analytical models. The proposed control scheme was implemented on the PSoC 5LP platform and the effect of the controller gain to recover the output voltage of the converter was examined. The closed-loop experiments confirmed the effectiveness of the designed control scheme to regulate the output voltage of the converter.

Parts of the work on the proposed converter presented in Chapters 3 and 4 augmented by experimental results from Chapter 5 were published in *IEEE Transaction on Power Electronics* [90]. The results of the small signal analysis, closed loop operation, and transient behavior of the converter are presented in a second manuscript, which is under review for publication in *IEEE Transactions on Power Electronics* [91].

4. Design Procedure (Chapter 6)

A procedure for using the developed analytical models to design the proposed converter is presented in Chapter 6. Several design considerations based on the range of input voltage, switching frequency, output voltage, as well as the maximum power of the converter, maximum duty ratio of the PWM switching signals, and turns ratio of the planar transformer were discussed. A complete parametric approach that leads to the determination of the required values and sizes of the converter components for given

specifications was presented. A design example for a 50 V-80 V, 100 W dual series-resonant circuits was given to illustrate the use of the design procedure to customize the converter for given requirements and application.

To the best of the author's knowledge, the research presented in this thesis is a pioneering work on dual series-resonant DC-DC converters. It is expected that the proposed converter will generate further research activities in the power electronics research community.

7.3 Future Work

While the thesis presents a comprehensive characterization of the topology to demonstrate its feasibility, effectiveness, and improvement in performance, there are a number of issues that require further investigation in order to extend the range of applications of the converter. Some of these are discussed below.

- *Conducted EMI emission*: The proposed converter operates under soft switching criteria for MOSFETs and output diodes; however, due to the implemented PWM operation of the MOSFETs, the switching transitions occur at finite *dv/dt* and *di/dt* for MOSFETs. This can cause non-zero emission for differential and common mode noises. Future work on the converter could investigate the propagation of these EMI interferences. The investigation would involve the development of analytical models and implementation of a higher power experimental converter to study the noise propagation.
- *Reducing the size of the high frequency transformer:* The operation of the proposed topology is such that during the intervals when one of the secondary windings of

the transformer is supplying the load current, the current in the other secondary winding circulates in the resonant *LC* circuit connected to that winding. This fact decreases the utilization of the power of the high frequency transformer. Improvement in the utilization of the transformer power can be investigated through two possible approaches. First, by disconnecting the resonant circuit from the winding that does not participate in supplying the load current. In other words, if the series resonant circuits of L_{r1}-C_{r1} and L_{r2}-C_{r2} at the beginning of *Mode VI* and *Mode III*, respectively, are disconnected with a switch, then the current in the corresponding secondary winding (i.e., *ns1* and *ns2*, respectively) will be zero and the full power of the transformer can be utilized through the other winding (i.e., *ns2* and *ns1*, respectively) to supply the load current. Since the resonant inductor currents at the beginning of *Mode III* and *Mode VI* are zero, this solution can be explored to increase the utilization of the transformer power in the converter. Second, an energy recovery scheme could be implemented to recover the energy in the winding that does not involve transferring of the load current to the output load.

- *Operation for medium and high voltage application*: The proposed converter is a suitable solution for low voltage applications. Since the voltage drop across each MOSFET is a function of the duty ratio and input voltage, the single stage of the proposed topology with MOSFETs cannot be used for medium and high voltage application; instead, the operation with other types of semiconductor switches, which can be connected in series for high voltage and power applications needs to

be investigated as one possible solution. Another solution can be a modular topology based on the proposed dual series-resonant converter.

Appendix A

Effect of Approximations in the Extended Describing Function

The state-space equations in (4.28)-(4.34) contain an infinite number of Fourier components. The 7^{th} order resultant state-space matrices in (4.71)-(4.73) are obtained by considering only the fundamental component of the state-space equations. By taking the other components (i.e., n=2, 3, …) into consideration, the size of the state-space matrices increases. For example, if in addition to the first component, the second component of the state-space equations is taken into consideration, the resultant state-space matrices will be of the 11^{th} order. The state-space matrices for the 11^{th} order system are as follows:

$$A=\begin{bmatrix}
0 & 0 & F\Omega_r & 0 & -\frac{1}{L_r} & 0 & 0 & 0 & 0 & \frac{-Nb_1}{L_r} & \frac{-B_1'}{2L_r} \\
0 & 0 & 0 & 2F\Omega_r & 0 & -\frac{1}{L_r} & 0 & 0 & 0 & \frac{-Nb_2}{L_r} & \frac{-B_2'}{2L_r} \\
-F\Omega_r & 0 & 0 & 0 & 0 & 0 & -\frac{1}{L_r} & 0 & 0 & \frac{-Na_1}{L_r} & \frac{-A_1'}{2L_r} \\
0 & -2F\Omega_r & 0 & 0 & 0 & 0 & 0 & -\frac{1}{L_r} & 0 & \frac{-Na_2}{L_r} & \frac{-A_2'}{2L_r} \\
\frac{1}{C_r} & 0 & 0 & 0 & 0 & 0 & F\Omega_r & 0 & 0 & 0 & 0 \\
0 & \frac{1}{C_r} & 0 & 0 & 0 & 0 & 0 & 2F\Omega_r & 0 & 0 & 0 \\
0 & 0 & \frac{1}{C_r} & 0 & -F\Omega_r & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & \frac{1}{C_r} & 0 & -2F\Omega_r & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{(1-D)}{L_m} & 0 \\
\frac{Nb_1}{C_c} & \frac{Nb_2}{C_c} & \frac{Na_1}{C_c} & \frac{Na_2}{C_c} & 0 & 0 & 0 & 0 & \frac{-(1-D)}{C_c} & 0 & 0 \\
\frac{B_1'}{2C_o} & \frac{B_2'}{2C_o} & \frac{A_1'}{2C_o} & \frac{A_2'}{2C_o} & 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{R_oC_o}
\end{bmatrix} \quad \text{(A.1)}$$

$$B=\begin{bmatrix} \frac{Nb_1}{L_r} & 0 & FI_{1nCLr} & 0 \\ \frac{Nb_2}{L_r} & 0 & 2FI_{2nCLr} & 0 \\ \frac{Na_1}{L_r} & 0 & -FI_{1nSLr} & 0 \\ \frac{Na_2}{L_r} & 0 & -2FI_{2nSLr} & 0 \\ 0 & 0 & FV_{1nCCr} & 0 \\ 0 & 0 & 2FV_{2nCCr} & 0 \\ 0 & 0 & -FV_{1nSCr} & 0 \\ 0 & 0 & -2FV_{2nSCr} & 0 \\ \frac{D}{L_m} & \frac{V_d}{(1-D)L_m} & 0 & 0 \\ 0 & \frac{I_{Lm}}{C_c} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{C_o} \end{bmatrix} \quad \text{(A.2)}$$

$$C=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \quad \text{(A.3)}$$

Figure A.1 shows the bode diagram of the compensated 7th order and 11th order control-to-output systems. It can be noticed that the effect of the second harmonic component is to change the behavior of the system at higher frequencies while the behavior of the system at low frequencies remains unchanged.

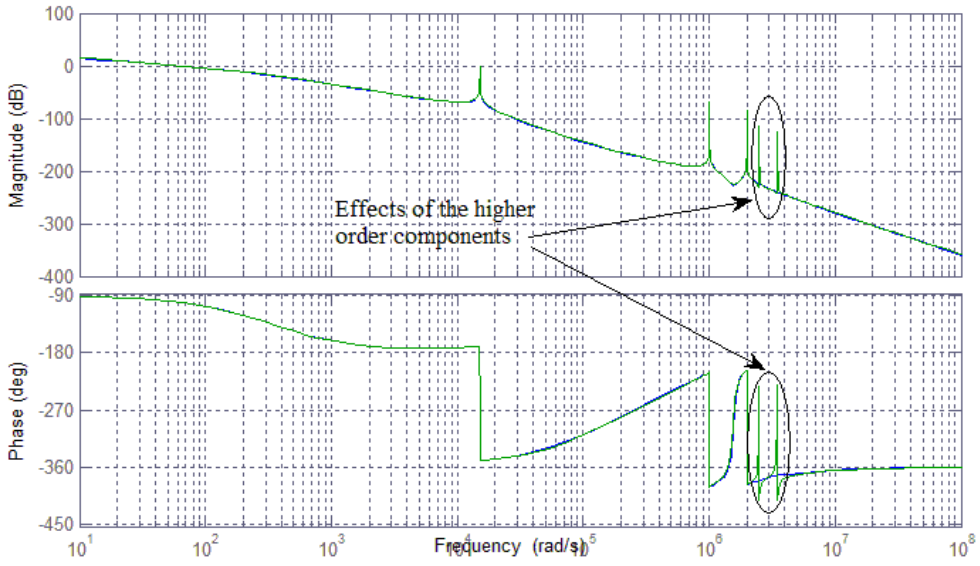


Figure A.1: Effect of the second harmonic component of the state-space variables on the small signal model of the compensated control-to-output system (K_I=1).

By considering the Fourier components from n=2 to n=m in the state-space equations in (4.28)-(4.34), the transfer functions in Table 4.2 are updated as follows:

$$T_{new}(s)=T_{n=1}(s)\times\prod_{p=2}^{m}\frac{\left(\left(s^2+2\zeta_{p1}(pF-1)\Omega_r+(pF-1)^2\Omega_r^2\right)\left(s^2+2\zeta_{p2}(pF+1)\Omega_r+(pF+1)^2\Omega_r^2\right)\right)}{\left(\left(s^2+(pF-1)^2\Omega_r^2\right)\left(s^2+(pF+1)^2\Omega_r^2\right)\right)} \quad \text{(A.4)}$$

In (A.4), $T_{new}(s)$ is the resultant transfer function when the higher order components are considered, $T_{n=1}(s)$ can be any of the transfer functions in Table 4.2, and ζ_{p1} and ζ_{p2} are the damping factors for the obtained high frequency zeros. In (A.4), the damping ratios of the higher order zeros are significantly small. This signifies that the imaginary parts of the

higher order zeros are significantly greater than the real parts. As an example, for m=2, the new damping ratio of the zeros associated with m=2 are as follows:

$$\zeta_{p1} = 0.0103$$

$$\zeta_{p2} = 0.0063$$

It can be assumed that the higher order zeros are purely imaginary, and therefore, the higher order zeros and poles cancel each other out.

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